GENERAL THEORY FOR PINCHED OPERATION OF THE JUNCTION-GATE FET*

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Abstract—A device oriented model is developed to describe the operation of the junction-gate field-effect transistor (FET) beyond pinch-off. The model is derived on the basis of a generalized structure with an arbitrary channel doping profile. It provides a qualitative and quantitative description of the current conduction mechanism, and is applicable over the entire dynamic range of device operation. Current conduction mechanisms in the vicinity of the source and the drain are examined separately. It is shown that the saturation of carrier drift velocities at high electric fields results in formation of a drain space-charge region of finite length. An approximate solution of the two-dimensional Poisson's equation is developed to describe the potential distribution within this region. A significant result of the device model is the prediction of a finite drain resistance in pinched operation, which shows a strong dependence on the device operation point.

Résumé—Un modèle orienté à un dispositif est développé pour décrire l'opération du transistor à effet de champ (FET) et à porte de jonction au delà du pinching. Le modèle est dérivé sur la base d'une structure généralisée ayant un profil de dose de canal arbitraire. Il fournit une description qualitative et quantitative du mécanisme de conduction et est applicable à l'ensemble de la gamme d'opérations du dispositif.
Les mécanismes de conduction de courant aux environs de la source et du drain sont examinés séparément. On démontre que la saturation des vitesses d'apport de porteurs aux champs électriques élevés résulte en la formation d'une région de charge d'espace de drain de longueur limitée. Une solution approximative de l'équation de Poisson à deux dimensions est développée pour décrire la distribution de potentiel dans la région. Un des résultats les plus significatifs du modèle est la prédiction d'une résistance de drain limitée dans l'opération pinçée, démontrant une forte dépendance sur le point opérationnel du dispositif.


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INTRODUCTION

The behavior of the junction-gate field-effect transistor (FET) at values of the drain potential less than the pinch-off voltage can be accurately described by means of a first-order "gradual-channel" approximation. This model was originally developed by Shockley\(^{(1)}\) for a uniformly-doped channel structure, and later expanded to devices with arbitrary impurity distribution.\(^{(2)}\)

The gradual-channel model is based on the assumption that the electric field gradients within the depleted channel region are normal to the direction of current flow. For operation with drain-to-gate voltage in excess of the device pinch-off voltage ("pinched-mode" operation), this model is no longer valid, particularly in the vicinity of the drain terminal. It is commonly accepted practice to describe device behavior beyond pinch-off by an arbitrary extrapolation of its V-I characteristics outside of their region of validity. This assumes complete independence of the output characteristics on the source-drain voltage, as well as zero source-drain conductance in the pinched mode. Therefore, the model fails to offer a physically acceptable description of the current conduction mechanism through the FET channel for device operation beyond pinch-off.

The exact determination of the FET characteristics for pinched operation requires the solution of the two-dimensional Poisson's equation under extremely complex boundary conditions. Grosvalet and Jvko\(^{(3)}\) have shown that, under certain idealized assumptions, it is possible to obtain a computer solution to this equation over the entire channel region by an iterative numerical approximation technique. However, their solution fails to give a physical insight to phenomena responsible for device operation. In addition, it is not readily applicable to practical problems of device design and characterization since its results and predictions cannot be expressed in a closed form.

In his original paper,\(^{(1)}\) Shockley suggested the possible use of a two-region model to describe the current conduction mechanism in pinched operation. This approach permits the separation of the FET channel into two regions in the direction of current flow, and allows the independent examination of conduction phenomena in the vicinity of the source and the drain terminals. An approximate solution for the potential and the electric field distribution over the entire channel is next obtained by matching the solutions in each of these regions at a predetermined interface within the channel, normal to the direction of current flow.

Various mathematical methods of joining these solutions have been discussed by Shockley,\(^{(1)}\) by Puk and Smolčič,\(^{(4)}\) and more recently by Wu and Saha.\(^{(5)}\) These models share two common features:

(a) Matching of the solutions in the two regions of the device is accomplished by a curve-fitting procedure, in terms of two adjustable parameters whose values are chosen to obtain the best match.

(b) The resulting device model is a mathematical one, and does not offer a physical description of the current conduction mechanism through the pinched channel region near the drain.

The aim of this paper is to develop a device-oriented physical model for the junction-gate FET which avoids the shortcomings of these mathematical models. The resulting model provides a working description of the V-I characteristics and a.c. parameters in pinched operation, in terms of the device geometry, the doping profile, and the electrical properties of the semiconductor material.

The characteristics of the FET beyond pinch-off are analyzed by treating the device channel as made up of two separate regions along the direction of current flow. In Region I, in the vicinity of the source, the gradual-channel approximation is used, and the depletion layer profile estimated from a solution of the one-dimensional Poisson's equation. In Region II, near the drain, the two-dimensional Poisson's equation is solved to determine the potential distribution. The boundary values for the solution of Poisson's equation within Region I and II are chosen to require the continuity of the potential distribution across the interface separating them.

It is shown that the current flow is constrained in Region II to a narrow conductive filament (residual channel) along the longitudinal axis of symmetry of the metallurgical channel. For practical device geometries, the saturation of carrier drift velocity at high electric field strength is found to be the dominant factor in determining the dimensions of this region. Consequently, in
the development of the model, it is assumed that the interface between the two regions of the channel is determined by the onset of carrier drift velocity saturation.\(^{9,10}\) The validity of this assumption, as well as other possible conduction mechanisms that may contribute to the total drain current in pinched-mode operation, is examined closely prior to the development of the model.

In the following analysis, an \(n\)-channel FET structure with parallel gate regions and an arbitrary channel impurity profile is considered. It is assumed that the gate regions are heavily doped, so that the gate-channel depletion layer spreads predominantly into the channel. Each of the gate regions is assumed to be independently biased with respect to the source. The structural diagram and the channel depletion layer profile for such an FET in pinched operation are shown schematically in Fig. 1. Since most commercially available units voltage, \(V_p\), the drain end of the channel is totally depleted of mobile carriers. Since the drain current, \(I_d\), is finite, this results in a physically unrealizable situation, requiring current conduction through a region of the channel that is totally devoid of mobile carriers.

A number of mechanisms may be postulated to explain current flow through a totally depleted channel section. These are as follows:

(a) Avalanche multiplication of carriers within the depleted channel section (Region II). The onset of this mechanism should result in a sharp increase of the noise level associated with the drain current in pinched-mode operation; this is not observed in practice. Furthermore, electric field strengths encountered within the drain space-charge layer (see Fig. 4) are typically well below those values at which avalanche multiplication effects become significant.

![Fig. 1. Schematic description of the FET channel depletion layer profile in pinched operation.](image)

are made of silicon, the numerical examples are confined to this material.

CURRENT CONDUCTION IN PINCHED OPERATION

Extrapolation of the gradual-channel model beyond pinch-off implies that, for a drain-gate potential \(V_{dl}\) in excess of the device pinch-off voltage, \(V_p\), the drain end of the channel is totally depleted of mobile carriers. Since the drain current, \(I_d\), is finite, this results in a physically unrealizable situation, requiring current conduction through a region of the channel that is totally devoid of mobile carriers.

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(b) Gate-channel junction breakdown, resulting in lateral carrier flow from gate to the drain. This can only occur when the reverse breakdown voltage of the gate-drain junction is exceeded. This voltage is typically far in excess of the pinch-off voltage, \(V_p\). In addition, breakdown of this type would result in a sudden decrease of gate impedance accompanied by an abrupt increase of gate
current. In physical FET structures, no such effects are observed at the onset of pinched operation.

(c) Thermal generation of carriers within the channel depletion layer. This is due to the presence of deep lying centers in the depletion layer. The magnitude of this current is on the order of the reverse current of a p-n junction diode of comparable dimensions. Thus it cannot account for a significant fraction of the observed drain current.

As indicated by the above discussion, none of the possible conduction mechanisms which may describe the current flow through a depleted layer can account for the observed behavior and magnitude of the drain current in pinched operation. Therefore, it is postulated that the channel is not totally depleted; instead, an effective residual channel filament of thickness $\delta$, remains through the drain space-charge region (Region II). Since carrier concentrations and drift velocities are at all times finite in physical device structures, the width of this channel opening has to be finite for non-zero drain current. In the analysis, the transition between the two regions of the channel is assumed to be abrupt for mathematical compactness.

The formation of a space charge region, Region II, at the drain end of the channel can be inferred from the extrapolation of the gradual channel model to the point of pinch-off. However, the first order model cannot explain the finite length, $L_2$, of this region, and its dependence on the drain potential in excess of the pinch-off voltage. In order to do so, it is necessary to consider a combination of the two following effects:

(i) Failure of the gradual-channel model in the vicinity of the drain, for $V_{sd} \approx V_s$.

The gradual-channel model is derived on the assumption that the longitudinal electric field gradients within the channel depletion layer are negligible compared to the transverse gradients. Consequently, the potential distribution, $V(x, y)$, within the depletion layer can be approximated from the solution of the Poisson's equation in one dimension:

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = -\frac{\varepsilon N(x, y)}{\varepsilon},$$

(1)

Where

- $q$ = electronic charge
- $N(x, y)$ = donor impurity concentration in the n-type channel
- $\varepsilon$ = permittivity of the material.

Defining the range of validity of the gradual-channel model as that region of the channel where:

$$\left| \frac{\partial^2 V}{\partial x^2} \right| \leq \frac{1}{2} \frac{\partial^2 V}{\partial y^2}$$

(2)

one can show that the model is valid only for that region of the channel where:

$$W(x) = W_1(x) + W_2(x) \geq A \left( \frac{I_0}{2 \varepsilon V_s} \right)^{2/3}$$

(3)

$W_1(x) = $ height of the undepleted channel
$A = $ vertical distance between the gates
$I_0 = $ saturation value of the drain current at a given gate bias
$(V_{st} = V_{ds})$
$\rho = $ average channel resistivity
$V_s = $ pinch-off voltage with $V_{sy} = V_{ds}$ and $V_x = V_{ds}$
$x = $ depth of the channel, measured perpendicular to the $x$ and $y$ axes.

As indicated by equation (3), the undepleted channel height, $W_1$, cannot go zero for any finite drain current without violating the gradual channel approximation.

(ii) Saturation of carrier drift velocity

As indicated by the experimental data of Fig. 2(b-d), carrier drift velocity $v$ in silicon does not increase indefinitely with the increasing electric field, but saturates at a maximum value of $v_0$, as a result of lattice scattering. The rapid saturation of the carrier velocity allows one to define a critical field $E_0$, depending on the charge carrier type, above which velocity saturation becomes dominant. For non-degenerate materials, $E_0$ and $v_0$ are independent of the impurity doping, and depend only on the type of charged carrier.

Defining $E_0$ as the value of the electric field at which $v$ attains 95 per cent of its saturation value, results in the following values of $v_0$ and $E_0$ in
For typical silicon planar FET structures, one observes that
\[
\delta / W_m > 1,
\]
thus indicating that the carrier velocity saturation is the dominant effect in determining the interface between the two regions of the channel in pinched operation. Consequently, for the following analysis, only the velocity-limiting phenomenon is considered as the dominant effect in determining the dimensions of Region II. Similarly, the interface between the two regions of the channel is marked by the onset of velocity saturation, i.e.,
\[
E = E_0 / 1.75.
\]

DEVICE MODEL IN PINCHED OPERATION

A schematic diagram of the channel depletion layer profile for an n-channel FET in pinched-mode operation is shown in Fig. 1. The p-type gate regions are assumed to be doped more heavily than the channel. The net donor concentration, \( N \) in the channel is assumed to vary in the transverse direction only, i.e.,
\[
N = N(y).
\]

The two gate sections are assumed to be parallel, and independently biased at gate-source potentials of \( V_{gs1} \) and \( V_{gs2} \), respectively.

As indicated in Fig. 1, the non-uniform channel doping profile, \( N(y) \), as well as the dissimilar gate bias voltages \( V_{gs1} \) and \( V_{gs2} \) cause the channel depletion layer profile associated with each gate section to be different. Thus, the physical device structure exhibits a lack of symmetry along the transverse direction. However, following the procedure outlined in Appendix I, one can define an effective plane of symmetry through the channel, labelled as \( \delta - \delta' \). The location of this plane is independent of the source-drain potential \( V_d \) in pinched operation, and is uniquely defined for a given choice of \( N(y) \), \( V_{gs1} \) and \( V_{gs2} \). The component
of the electric field normal to the \( K-K' \) plane is zero along the entire length of the channel; therefore, there is no net transfer of mobile charge across this plane. Consequently, one can separate the two-gate FET structure shown in Fig. 1 into two single-gate FETs about the \( K-K' \) plane, and consider each half of the device separately.

Figure 3 shows a schematic diagram of the depletion layer profile within the active channel region about the effective symmetry plane. The coordinate axes and the device dimensions to be used in the following analysis are also defined in this figure.

![Diagram of depletion layer profile](image)

**Fig. 3.** Depletion profile within the active channel in pinched operation, sectioned about the effective axis of symmetry.

In Region I, of length \( L_1 \), current conduction is described by the gradual-channel model. The channel depletion layer profile, \( h(x) \), can be determined by an approximate solution of the one-dimensional Poisson equation within the channel-depletion layer. A detailed analysis of current flow in this region has been carried out by Bockman and Richman for a generalized impurity distribution, \( N(y) \), and will not be repeated here.

The generalized expression for the drain current can be written as shown in equation (4). In dealing with the one-dimensional impurity distribution, i.e., \( N(x, y) = N(y) \), it is convenient to introduce a short-hand notation for the mathematical operation of integration as follows:

\[
\bar{N}(y) \equiv \int N(y) \, dy
\]

and

\[
\bar{N}(y) \equiv [N(y)].
\]

Similarly, a definite integral can be expressed as

\[
\int_{a}^{b} N(y) \, dy = \bar{N}(b) - \bar{N}(a).
\]

In terms of this notation, \( N_d(x) \) is given by

\[
N_d(x) = \frac{1}{W(x)} [\bar{N}(a) - \bar{N}(b)].
\]

As a result of the ohmic drop along the undepleted channel, \( W(x) \) is a monotonically decreasing function of \( x \). Since the current, \( I_0 \), is continuous through the channel, the carrier drift velocity, \( v(x) \), is forced to increase monotonically as a function of \( x \) in order to sustain the drain current. Ultimately, \( v(x) \) saturates, at which point the channel height attains its lower limit, \( \delta_0 \), corresponding to \( v(x) = v_0 \), as defined earlier in equation (3).

Formation of the residual channel of thickness \( \delta_0 \) as a result of velocity saturation marks the...
interface between the two regions of the model, since the conduction through the channel is no longer ohmic. For typical impurity profiles observed in practical device structures, and for device geometries having channel length-to-width ratios \( L_L / w \) in excess of 5, it can be shown that:

\[
\delta_0 \ll w. \tag{12}
\]

Therefore, from equation (11):

\[
N(x)= \frac{1}{\delta_0}[N(x)-\delta_0 \cdot N(x-\delta_0)] \simeq N(x). \tag{13}
\]

Thus,

\[
\delta_0 \simeq \frac{L_L}{qN(x)\nu_0\lambda}. \tag{14}
\]

The channel-gate potential, \( V_{OG} \), needed to extend the depletion layer a distance of \( (a-\delta_0) \) into the channel, and hence cause velocity saturation, can be related to the device pinch-off voltage, \( V_p \), as:

\[
V_{GO} = V_p - \left( \frac{q}{\epsilon} \right) \delta_0 \cdot N(a), \tag{15}
\]

where \( \epsilon \) is the permittivity of the semiconductor material. For a generalized doping profile \( N(y) \), \( V_p \) can be expressed as:

\[
V_p = \left( \frac{q}{\epsilon} \right) \left[ N(a) - N(0) - a\overline{N(a)} \right]. \tag{16}
\]

As indicated by equation (15), due to the finite value of \( \delta_0 \), pinched mode operation sets in at a value of the drain-gate potential somewhat lower than \( V_p \). However, for practical device geometries, \( \delta_0 \ll a \), therefore:

\[
V_{GO} \simeq V_p. \tag{17}
\]

The drain potential in excess of the value needed for velocity saturation, \( V_{DR} \), is defined as:

\[
V_{DR} = V_D + V_D - V_{GO} = V_D + V_D - V_p. \tag{18}
\]

This excess drain potential results in the formation of Region II in the vicinity of the drain, where the current flow is non-ohmic and is confined to an effective residual channel of thickness \( L_L \) along the \( K' \) plane. As will be shown later, the strong longitudinal field gradients in this region cause the free carrier concentration within the residual channel to deviate from its thermal equilibrium value of \( N(e) \), in a manner similar to that discussed by Junod and Grosvenor.\(^{19}\)

In Region II, the potential distribution must be determined through the solution of the two-dimensional Poisson's equation with appropriate boundary conditions. For mathematical compactness, the coordinate axes are moved to the interface between the two regions of the device, as shown in Fig. 1. This is accomplished by defining a new independent variable \( x' \), where:

\[
x' = x - L_L. \tag{19}
\]

The potential distribution in this region must satisfy:

\[
\nabla^2 V(x', y) = \frac{\partial^2 V}{\partial x'^2} + \frac{\partial^2 V}{\partial y^2} = -\frac{qN(x)}{\epsilon} \tag{20}
\]

for:

\[
0 < x' < L_L \quad \text{and} \quad 0 < y < (a-d) = a. \tag{21}
\]

To ensure a continuous transition between regions I and II, we invoke the following four boundary conditions:

1. \( V(x', 0) = -V_p \).
2. \( \frac{\partial V}{\partial y}(x', a) = -E_p(x', a) = 0. \)
3. \( V(0, y) = V_{SG} = (q/\epsilon)\overline{N(a)} - \overline{N(0,y)}. \)
4. \( V(0, y) = V_{GO} = -V_p. \)

Boundary condition 1 treats the metallurgical channel-gate junction as an equipotential plane, which is valid for a \( p^+ \) gate. Condition 2 is an outcome of the effective channel symmetry about \( y = a \) (the \( K-K' \) plane). Condition 3 requires the continuity of the electric field within the conducting channel. Condition 4 ensures the continuity of the potential across the entire Region I-Region II interface. The potential distribution on the right-hand side of equation (25) is that given along the \( x = L_L \) boundary of Region I by the gradual-channel approximation.\(^{13}\)

As shown in Appendix II, the above boundary conditions are not sufficient to determine an exact solution of equation (20). However, by using a
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A self-consistent approach, it is possible to obtain the approximate solution:

\[ V(x', y) = -V_0 + \frac{q\bar{a}}{\pi} \frac{N(y) - N(0) - yN(a)}{\frac{\pi}{2a} \sinh \frac{\pi x'}{2a}} + \frac{2E_0 a}{\pi} \frac{\pi y}{2a} \sin \frac{\pi x'}{2a} \]. \hspace{1cm} (26)

Along the center line of the channel, this reduces to:

\[ V(x', a) \approx V_0 - V_0 + \frac{2aE_0}{\pi} \sinh \left( \frac{\pi x'}{2a} \right) \]. \hspace{1cm} (27)

From equation (27), the dependence of the length of the pinch region on the drain potential may be determined as:

\[ L_2 = \frac{2a}{\pi} \sinh^{-1} \left( \frac{V_{ds}}{2E_0 a} \right). \hspace{1cm} (28) \]

Assuming that an abrupt boundary exists between the residual channel and the depletion layer, and that the carrier concentration within the residual channel in the direction of the current flow is uniform, the excess free carrier concentration within the conducting filament of Region II can be approximated from (27), by solving the Poisson's equation along the centerline of the channel, for \( 0 < x' < L_2 \):

\[ \frac{n - N(a)}{N(a)} = \frac{\pi E_0}{2qaN(a)} \sinh \left( \frac{\pi x'}{2a} \right), \hspace{1cm} (29) \]

where \( n \) is the actual value of the free carrier concentration.

Since \( I_d \) is continuous throughout the channel and the carrier saturation velocity \( v_o \) is fixed, the increase of free carrier concentration as predicted by equation (29) results in a monotonic decrease of the residual channel opening, \( \delta \), as a function of \( x' \), as given below:

\[ \delta(x') = \delta_0 \left[ 1 + \frac{\pi E_0}{2qaN(a)} \sinh \left( \frac{\pi x'}{2a} \right) \right]. \hspace{1cm} (30) \]

Note that, since at all times \( \delta \geq \delta(x') \) for \( x' \geq 0 \), the basic assumptions used in obtaining the approximate solution of equation (26) are not affected by finite deviations from charge neutrality within the residual channel. However, the deviation of \( n \) from \( N(y) \) may cause the potential along the centerline of the channel to be slightly higher than that predicted by equation (27) by an amount \( \Delta V \), where

\[ \Delta V \approx \frac{q\bar{a}^2}{2a} [n - N(a)]. \hspace{1cm} (31) \]

Due to small dimensions of \( \delta \), this corrective term may be neglected.

At this point, it is instructive to examine the electric-field and the potential distribution predicted by the model, by means of a numerical example. We shall consider the case of a symmetrical n-channel silicon FET with a uniformly doped channel, with the following device parameters:

- \( N(y) = N_D = 10^{18} \text{ cm}^{-3} \) (5Ω-cm channel resistivity)
- \( a = 3 \mu m \)
- \( L = 25 \mu m \)
- \( E_0 = 20 \text{ kV/cm} \)
- \( V_p = qN_D \bar{a}^2/2a = 6.75 \text{ V} \)

Keeping the drain voltage, \( V_d \), constant at 20 V, consider the case of two separate values of the gate bias, namely \( V_g = 0 \) and 5.5 V, respectively.

For \( V_g = 0 \), one calculates the following values:

- \( V_{ds} = 13.25 \text{ V} \)
- \( \delta_0/a = 0.036 \)
- \( L_1 = 21.3 \mu m \)
- \( L_2 = 3.7 \mu m \)

For \( V_g = 5.5 \text{ V} \):

- \( V_{ds} = 18.75 \text{ V} \)
- \( \delta_0/a = 0.001 \)
- \( L_1 = 20.5 \mu m \)
- \( L_2 = 4.5 \mu m \)

Note that the \( \delta_0 \ll a \), an assumption is well satisfied for both cases.

Figure 4 shows the electric field and the potential along the centerline of the channel (\( y = a \)) for \( V_g = 0 \). The predicted form of the equipotential contours through the body of the channel for zero gate bias condition is shown in Fig. 5. Note that, as a result of the boundary conditions used in the solution of the two-dimensional Poisson equation in the pinched region, the potential distribution across the \( x = L_1 \) plane is continuous. In sketching the equipotential contours of Fig. 5, it is assumed that there are a sufficient number of bound charges.
Fig. 4. Potential and the electric field in the conducting channel, for operation beyond pinch-off. (Values correspond to the numerical example in the text, with $V_g = 0$.)

Fig. 5. Equipotential contours within the channel for pinched operation. (Values correspond to the numerical example in the text, with $V_g = 0$.)
beyond the active drain region on which the electric field lines can terminate. These bound charges are provided by the extension of the depletion contour beyond the active channel region, as shown schematically in Fig. 1.

In terms of the device dimensions and properties discussed in the numerical example of this section, a graphical description of the variation of the free carrier concentration along the residual channel, as predicted by equation (20) is shown in Fig. 6 for the condition where \( V_D = 0 \). Using mode operation can be obtained as:

\[
I_d = \frac{2q^2 \mu_e}{\epsilon L_1} \int_{-a}^{0} y N(y)[N(a) - \overline{N}(y)] \, dy \tag{32}
\]

Since \( \overline{N} \) \( \equiv \) \( a \), equation (28) can be written as:

\[
I_d = \frac{2q^2 \mu_e}{\epsilon L_1} \int_{0}^{a} y N(y)[N(a) - \overline{N}(y)] \, dy \tag{33}
\]

The only parameter in (33) showing an explicit dependence on \( V_D \) is \( L_1 \). Therefore, differentiating equation (33) with respect to \( V_D \), with \( V_D = \) constant, we have:

\[
\frac{\partial I_d}{\partial V_d} = \frac{I_d}{L_1} \frac{\partial \overline{N}}{\partial V_d} \tag{34}
\]

Differentiating equation (33) with respect to \( V_D \), with \( V_D = \) constant, we have:

\[
\frac{\partial I_d}{\partial V_d} = -\frac{I_d}{L_1} \frac{\partial L_2}{\partial V_d} \tag{35}
\]

Realizing that \( L_1 + L_2 = L_1 \) and \( L_1 \gg L_2 \), equation (34) reduces to

\[
\frac{\partial I_d}{\partial V_d} \simeq \frac{I_d}{L_1} \frac{\partial L_2}{\partial V_d} \tag{36}
\]

\[\]
Evaluating
\[ V = \frac{2 \left( \frac{\delta I_d}{\delta V_d} \right) \left( \frac{\delta E}{\delta V_d} \right)}{\left( \frac{\delta E}{\delta V_d} \right)^2 - \left( \frac{\delta I_d}{\delta V_d} \right)^2}, \]
from equation (28):
\[ r_d \approx \frac{L_1 E_0}{I_a} \left[ 1 + \frac{V_{d0} a}{2 E_0} \right]^{1/2}. \] (37)

Even though \( r_d \) appears to be independent of \( V_f \), it should be remembered that the influence of the gate bias is included implicitly, through \( I_a \) and \( V_{d0} \). As indicated by the definition (18), for relatively large values of drain bias, \( V_{d0} \) shows a weak dependence on \( V_d \). Therefore, equation (37) implies that for any particular value of drain potential, the drain current resistance product, \( I_a r_d \), is relatively constant.

For operation of the device in the vicinity of pinch-off, i.e., \( V_{d0} = V_f \), the first term in (37) is dominant, and the dynamic drain resistance can be expressed as
\[ r_d \approx \frac{L_1 E_0}{I_a}. \] (38)

It should be noted that equation (38) may be used as an alternate means of determining \( E_0 \), from measured values of \( I_a \) and \( r_d \) at the point of pinch-off. The values of \( E_0 \) calculated in this manner are in very close agreement with those determined from the data of Fig. 2.

As the value of \( V_{d0} \) is increased, the second term in equation (37) becomes dominant very rapidly, so that
\[ r_d \approx \frac{\pi L_1 V_{d0}}{2 a d_a} \sim \frac{1}{a}. \] (39)

As indicated by equation (39), the incremental drain resistance is proportional to the excess drain voltage for operation well into the pinched-mode.

It is interesting to examine the temperature dependence of the \( I_d r_d \) product for operation within the pinched region. Differentiating equation (39) with respect to temperature \( T \),
\[ \frac{\delta}{\delta T} \left( I_d r_d \right) = \frac{\pi L_1 \delta V_{d0}}{2 a} \frac{\delta T}{T}. \] (40)

But:
\[ \frac{\delta V_{d0}}{\delta T} = \frac{\delta}{\delta T} \left( V_d + V_{f0} - V_{d0} \right) \approx -\frac{\delta V_d}{\delta T}. \] (41)

The temperature coefficient of the pinch-off voltage \( V_{f0} \) is the same as that of the built-in junction potential and is of the order of \((-2) \text{ mV} / \text{°C}) \) for silicon. Therefore, equation (40) can be re-written as:
\[ \frac{\delta}{\delta T} \left( I_d r_d \right) = \frac{\pi L_1}{a} \frac{\delta V_d}{\delta T} \text{ mV} / \text{°C}. \] (42)

For most commercially available devices, the right-hand side of equation (42) is in the range of 10–100 mV per °C. However, the \( I_d r_d \) product beyond pinch-off [as predicted by equation (39)] is very large (typically in the 100–400 V range). Consequently, this product is relatively insensitive to temperature changes, even though its individual terms are not.

From equations (39) and (42), the percentage variation of the \( I_d r_d \) product is:
\[ \frac{\delta \left( I_d r_d \right)}{I_d r_d} \approx 0.2 \frac{\delta V_d}{V_{d0}} \%	ext{°C}, \] (43)
where \( V_{d0} \) is expressed in volts.

(b) Transconductance, \( g_m \)

The device transconductance, \( g_m \), is defined as:
\[ g_m = -\left( \frac{\delta I_d}{\delta V_d} \right)_{V_f \text{ constant}}. \] (44)

Using the expression for \( I_d \) as given by equation (33):
\[ g_m = -\frac{\delta I_d}{\delta V_d} = \frac{I_d}{L_1} \left( \frac{\delta I_d}{\delta V_d} \right)_{V_f = \text{constant}} \] (45)
where \( g_m \) is the transconductance obtained by direct extrapolation of the gradual-channel model for operation beyond pinch-off, and is given as:
\[ g_m = \frac{\mu a}{L_1} \{ N(x0) - N(x0) \}. \] (46)

* This ignores the dependence of low-field mobility on the impurity concentration.
However:
\[
\frac{\partial I_2}{\partial V_s} = \frac{\partial I_2}{\partial V_g} \quad \text{and} \quad L_1 \approx L_1.
\] (47)

Thus, equation (45) can be approximated as:
\[
\bar{g}_m = g_m + g_d
\] (48)

where \(g_d\) is the incremental channel conductance in the pinched-mode operation, as defined by equation (37).

As indicated by equation (48), the model predicts that the device transconductance \(g_m\) in pinched-mode operation is greater than that predicted by the gradual-channel model by an amount equal to the drain conductance, \(g_d\). For practical device structures, typical values of \(g_m\) and \(g_d\) are of the order of 3 m\(\Omega\) and 50 \(\mu\)\(\Omega\) respectively. Therefore, the predicted increase of \(g_m\) over \(g_m^0\) is of the order of a few per cent.

(c) Transit time

In terms of a direct extrapolation of the gradual-channel model for pinched operation, the transit time \(\tau_0\) for the intrinsic device at the point of pinch-off can be expressed as:
\[
\tau_0 = \frac{L_1^2}{\mu_d} Q(h_0),
\] (49)

where \(Q(h_0)\) is a monotonically increasing function of \(h_0\) expressed as:
\[
Q(h_0) = \frac{\int_{h_0}^{a} y N(y) \left( N(a) - N(y) \right)^2 dy}{\int_{h_0}^{a} y N(y) \left( N(a) - N(y) \right) dy}.
\] (50)

In terms of the physical model for pinched operation developed in the previous section, the transit time \(\tau\) associated with the intrinsic device may be expressed as:
\[
\tau = \tau_1 + \tau_2 = \frac{L_1^2}{\mu_d} Q(h_0) + \frac{L_2}{v_o},
\] (51)

where \(\tau_1\) and \(\tau_2\) are respectively the transit times through Regions (I) and (II) of the channel in pinched operation. Since \(L_1 \gg L_2\):
\[
\tau = \tau_0 - \frac{L_2}{2v_o} \left[ \frac{2r_0 - \frac{L_1}{r_0}}{r_0} \right].
\] (52)

However:
\[
\tau_0 \gg \frac{L_1}{2v_o}.
\] (53)

Thus, an approximate expression for the transit time in the pinched-mode of operation is:
\[
\tau = \tau_0 \left( 1 - \frac{L_2}{L_1} \right) \quad \text{for} \quad L_2 \ll L_1.
\] (54)

Using the values of device parameters discussed in connection with the numerical example of the previous section with \(V_d = 3V_p\) and \(V_s = 0\), the result given by equation (54) indicates that an improvement of \(\approx 20\) per cent can be obtained in \(\tau\) over \(\tau_0\).

EXPERIMENTAL RESULTS AND DISCUSSIONS

In order to verify the results predicted by the physical model, several commercially available silicon planar FETs of varying geometries and impurity doping profiles were used as test units. In all cases, the device geometries chosen satisfied the \(L_1/a \geq 5\) condition. The values of the carrier saturation velocity, \(v_o\), and the critical field, \(E_o\), were computed from the independent experimental data of Fig. 2. (16-8)

For purposes of device design and application, the most significant result of the model for pinched operation is the presence of a finite drain resistance which can be readily related to the device parameters as well as to the choice of the operating point. Furthermore, the model predicts that the drain "current-resistance product," \(I_dR_d\), will be relatively constant, and independent of temperature for a given value of the drain potential beyond pinch-off.

Since these properties of the device show the most marked difference in device characteristics above and beyond those suggested by the gradual-channel model, they were chosen as the key parameters to be measured to verify the range of validity of the model. Detailed measurements of other device parameters are described in Ref. 9.

Experimental results are presented here for some typical test devices, whose properties are...
Table 1. Properties of test units

<table>
<thead>
<tr>
<th>Device type</th>
<th>2N2499</th>
<th>2N3458</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>p-channel</td>
<td>n-channel</td>
</tr>
<tr>
<td>Gate geometry</td>
<td>double diff.</td>
<td>epitaxial</td>
</tr>
<tr>
<td>Channel length, L</td>
<td>12 μm</td>
<td>8 μm</td>
</tr>
<tr>
<td>Vπ</td>
<td>3.8 V</td>
<td>2.5 V</td>
</tr>
<tr>
<td>a</td>
<td>1.2 μm</td>
<td>0.7 μm</td>
</tr>
<tr>
<td>r0</td>
<td>6 x 10^9 cm/sec</td>
<td>10^10 cm/sec</td>
</tr>
<tr>
<td>Kp</td>
<td>30 kV/cm</td>
<td>20 kV/cm</td>
</tr>
</tbody>
</table>

listed in Table 1. Figure 7 gives a graphical comparison of the measured and the calculated values of the incremental drain resistance, r_d, as a function of excess drain potential in pinched operation with zero applied gate bias for each of the test devices. The theoretical values of r_d are calculated from the device geometry and properties listed in Table 1 and from equation (37) of the text. The predicted and measured values of r_d are shown in Fig. 8 as a function of I_d with constant drain bias beyond pinch-off, i.e., for

---

Fig. 7. Measured and calculated values of the dynamic drain resistance, r_d, in pinched operation.

Fig. 8. Measured and predicted values of I_d and r_d in pinched operation, for constant V_d.
$V_{ir} = V_i + V_g - V_p = \text{constant}$. Here, the theoretical curve is that given by equation (39), since $V_{ir} > V_g$. Note that this curve shows close agreement to the measured data in both trend as well as in actual numerical values.

Figure 9 shows the measured temperature dependence of the $I_d$ product for operation in the pinch-off mode with zero applied gate bias. As indicated by the observed results, both $I_d$ and $V_g$ vary over a wide range of values as a function of

\[ \text{(a)} \]

\[ \text{(b)} \]

**Fig. 9.** Temperature dependence of device parameters beyond pinch-off.
temperature; however their product remains relatively unchanged. This is in excellent agreement with the results predicted by equation (4).

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REFERENCES


APPENDIX I

Determination of the effective axis of symmetry

Asymmetry of the channel depletion layer profile in pinched operation comes about as a result of one or more of the following causes:

(a) Different bias voltages $V_{n1}$ and $V_{p1}$ applied to gates 1 and 2.

(b) Non-uniform (asymmetric) channel doping profile.

When either or both of these asymmetry conditions are present, the location of the effective plane of symmetry, the $K-K'$ axis of Fig. 1, can be uniquely defined for a given set of gate bias voltages and doping profile.

Let the respective channel depletion layer thicknesses $h_1(x)$ and $h_2(x)$ within Region 1 be related to the gate channel reverse bias, $V_{th}(x)$, at any point along the channel as given below:

$$h_1(x) = d_1(V_{th1})$$  \hspace{1cm} (A.1)

$$h_2(x) = d_2(V_{th2})$$  \hspace{1cm} (A.2)

The gate-channel voltages $V_{th1}$ and $V_{th2}$ for the respective sections of the device can be expressed as

$$V_{th1} = V_{th1} + V_{th2(x)}$$  \hspace{1cm} (A.3)

$$V_{th2} = V_{th2} + V_{th2(x)}$$  \hspace{1cm} (A.4)

where $V_{th}(x)$ is the potential within the conducting channel at a distance $x$ from the source, for $0 \leq x \leq L_1$.

The functions $d_1$ and $d_2$ are monotonically increasing functions of $V_{th1}$ and $V_{th2}$, respectively. It will be assumed that the residual channel openings, $d_1$ and $d_2$, in Region II are small compared to the respective metallurgical channel widths, i.e.,

$$d_1 \ll d_2$$

$$d_2 \ll d_2$$

Setting $V_{th1}$ and $V_{th2}$ as the respective pinch-off voltages of the two single-gate devices, one can state:

$$V_{th1} = V_{th1} + V_{th1}$$  \hspace{1cm} (A.5)

$$V_{th2} = V_{th2} + V_{th2}$$  \hspace{1cm} (A.6)

where $V_{th}$ is the potential within the conducting channel at $x = L_1$, i.e.,

$$V_{th1} = V_{th1}(L_1)$$  \hspace{1cm} (A.7)

Considering the depletion layer thickness at $x = L_1$:

$$h_1(L_1) + h_2(L_1) = A - (d_1 + d_2) \approx A$$  \hspace{1cm} (A.8)

In terms of equations (A.1) and (A.2) the result of (A.8) can be expressed as:

$$a_1 + a_2 = d_1(V_{th1} + V_{th2}) + d_2(V_{th2} + V_{th1}) = A$$  \hspace{1cm} (A.9)

For a given channel and gate impurity profile, the functions $d_1$ and $d_2$ relating the depletion layer thickness across the junction to the applied potential are uniquely defined. $V_{th1}$, $V_{th2}$ and the total channel width $A$ are readily measurable quantities. Therefore, the only remaining unknown, $V_{th1}$, can be determined from the solution of equation (A.9) thereby uniquely defining the $K-K'$ axis of symmetry.

Except for the case of a uniformly doped channel, the functions $d_1$ and $d_2$ cannot be expressed in a convenient closed form, but are best described graphically. Therefore, in most applications a graphical, rather than analytical, solution of (A.9) may be preferable.

APPENDIX II

An approximate solution of Poisson's equation in the pinched region

Figure 3 shows a schematic description of the coordinate axes to be used in obtaining an approximate solution of the Poisson equation within the depletion layer of Region II. In order to ensure a continuous transition from Region I to Region II of the channel, the boundary conditions of equations (22) through (23) must be satisfied.
Let the general solution of equation (20) be of the form
\[ V(x', y) = V_1(x', y) + V_2(x', y), \tag{A.10} \]
over the range
\[ 0 < x' < L_2, \]
\[ 0 < y < (a - \delta) \equiv a. \]

The two components of the solution are to be chosen such that:
\[ \nabla^2 V_1(x', y) = 0, \tag{A.11} \]
\[ \nabla^2 V_2(x', y) = -\frac{qN(y)}{\epsilon}. \tag{A.12} \]

The function \( V_1(x', y) \) represents the solution of Laplace's equation within the space-charge region of Region II, and is chosen to have the following functional form:
\[ V_1(x', y) = \sum_{n=1}^\infty A_n \sin(n\pi x') \sinh(n\pi a'). \tag{A.13} \]

The boundary conditions to be satisfied by \( V_1(x', y) \) are:
1. \( V_1(x', 0) = 0 \)
2. \( V_1(0, y) = 0 \)
3. \( \frac{\partial V_1}{\partial y}(x', a) = 0 \)
4. \( \frac{\partial V_1}{\partial x'}(0, a) = -E_o. \tag{A.14} \)

The first two boundary conditions are satisfied by the functional choice of \( V_1 \). The third boundary condition, in conjunction with equation (A.11) requires that:
\[ \alpha_n = \beta_n = \frac{(2n-1)\pi}{2a}. \tag{A.15} \]

The fourth boundary condition is not sufficient to determine uniquely the unknown coefficient, \( A_n \), of equation (A.13) since this condition only states that:
\[ \sum_{n=1}^\infty A_n (2n-1)^2 = \frac{2aE_o}{\epsilon}. \tag{A.16} \]

This discrepancy occurs because of the fact that we have made no restrictions on the potential distribution at the drain, i.e., along the \( (x' = L_2) \) plane. If this potential distribution is known, then the coefficients \( A_n \) of equation (A.13) can be uniquely defined as:
\[ A_n = \frac{F_n}{\sinh \left( \frac{(2n-1)\pi L_2}{2} \right)}, \tag{A.17} \]

where \( F_n \) is the coefficient of the \( n^{th} \) term in the Fourier series expansion of the potential along the \( x' = L_2 \) plane.

For a physically meaningful solution, the coefficients \( A_n \) must tend to zero very rapidly as \( n \) increases. If this were not true, the hyperbolic sine terms of \( V_1 \) as given by equation (A.13) would lead to extremely high potentials and electric fields in the vicinity of the drain, resulting in an avalanche breakdown in the channel near the drain contact. Since \( V_1(L_2, y) \) is unknown, it is assumed to be of such a form as to make \( A_n \) vanishingly small for \( n \neq 1 \). This is a valid self-consistent approximation of the exact shape of the drain contact in terms what similar to the form of resulting electric potentials near the vicinity of the drain (see Fig. 4). Consequently, only the first term of the series given by (A.15) is retained, and the approximate expression for \( V_1(x', y) \) becomes
\[ V_1(x', y) \approx \frac{2aE_o}{\pi} \sin \frac{\pi y}{2a} \sinh \frac{\pi x'}{2a}. \tag{A.18} \]

Let the particular solution, \( V_2(x', y) \) be described by a general expression of the form:
\[ V_2 = \sum_{k=1}^\infty C_k(x')^k + \sum_{l=0}^\infty D_l(y)^l + h(y). \tag{A.19} \]

where \( h(y) \) is an arbitrary function of \( y \).

The boundary conditions to be satisfied by \( V_2(x', y) \) are:
1. \( V_2(x', 0) = -V_i \)
2. \( \frac{\partial V_2}{\partial y}(x', a) = -E_o(x', a) = 0 \)
3. \( \frac{\partial V_2}{\partial x'}(0, y) = 0 \)
4. \( V_2(0, y) = -V_i + (q\epsilon [\bar{N}(y) - \bar{N}(0)] - yN(0)) \tag{A.20} \)

The form of equation (A.19) which satisfies the boundary conditions of (A.20) as well as equation (A.12) is the one where:
\[ C_k = 0 \quad k = 1, 2, 3, \ldots, \tag{A.21} \]
\[ D_l = 0 \quad l = 3, 4, 5, \ldots, \tag{A.22} \]
\[ D_0 = -V_i, \tag{A.23} \]
\[ D_l = (-2)l(q\epsilon [\bar{N}(a) - \bar{N}(0)]), \tag{A.24} \]
PINCHED OPERATION OF THE JUNCTION-GATE FET

Therefore, the total approximate solution becomes:

\[ V(x', y) = V_1 + V_2 = -V_1 + \frac{(q/e)[N(y)]}{N(0) - yN(0)} \]

\[ \frac{2E_D}{a} \frac{\pi y}{2a} \sin \frac{\pi y}{2a} \]

Note that, due to the form of \( \phi(y) \) as given in equation (A.25), the coefficient \( D_1 \) cancels out of (A.19). Combining the terms given above, the particular solution, \( V_p(x', y) \), can be expressed as:

\[ V_p(x', y) = V_2(y) = -V_1 + \frac{(q/e)[N(y)]}{N(0) - yN(0)} \]

\[ \times \frac{2E_D}{a} \frac{\pi y}{2a} \sin \frac{\pi y}{2a} \]

which is the result stated in equation (26) of the text.