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Polarization Induced 2DEG in AlGaN/GaN HEMTs: On the origin, DC and transient characterization

A dissertation submitted in partial satisfaction of the requirements for the degree of

Doctor of Philosophy
in
Electrical and Computer Engineering

by

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Nani

Dedicated to the honest ones

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Publications and Presentations

1. **R. Vetury**, N.Q.Zhang, S.Keller, U.K.Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs", accepted for publication in *IEEE Transactions on Electron Devices* (Special Issue on GaN Electronics, Sep 2001)

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3. K. Krishnamurthy, **R. Vetury,** S. Keller, M.J.W. Rodwell, S.I. Long, U.K. Mishra**, "**Broadband GaAs MESFET and GaN HEMT resistive feedback power amplifiers", IEEE Journal of Solid-State Circuits, vol.35, (no.9), (GaAs IC Symposium. 21st Annual. Technical Digest 1999, Monterey, CA, USA, 17-20 Oct. 1999.) IEEE, Sept. 2000. p.1285-92.

4. **R.Vetury**, I.P. Smorchkova, C.R. Elsass, B. Heying, S. Keller, and U.K. Mishra, "Polarization induced 2DEG in MBE grown AlGaN/GaN HFETs: On the origin, DC and RF characterization", Materials Research Society Spring 2000 Meeting, San Francisco, CA, April 24-28, 2000.

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Polarization Induced Charge in AlGaN/GaN Heterostructure Field Effect Transistors: On the origin, DC and transient characterization

Abstract

The performance of devices using conventional semiconductors such as Si and GaAs is rapidly approaching the limit set by intrinsic material parameters. The increasing demand for higher power at higher frequencies has led to the development of microwave power devices in wide band gap material systems such as GaN and SiC. In this work, the impact of polarization induced charge on the performance of AlGaN/GaN HFETs is studied.

The spontaneous and piezoelectric polarization constants of the III-V nitrides are relatively large. Due to this, there exist strong polarization induced electric fields in an AlGaN/GaN heterostructure used in HFETs. The presence of these polarization fields leads to the formation of surface states in such heterostructures.

Measurement of surface potential using floating Schottky gates are presented. These provided the first direct measurement of the effect of these surface states. By using floating Schottky gates as potential probes, the lateral extent of gate depletion in high voltage HFETs was measured. The lateral extent of the gate depletion region was found to be inconsistent with the donor density, thus suggesting the presence of negative surface charge.

It has been observed experimentally that there exists a large 2DEG sheet density in an undoped AlGaN/GaN heterostructure. By means of electrostatic arguments, it is shown that in such undoped AlGaN/GaN heterostructures, the presence of positive surface charge is necessary to induce the formation of these 2DEG. It is shown that the these positive charges arise from positively charged donor like states on the surface that are the source of electrons in the 2DEG. By measuring the dependence of 2DEG carrier density on the thickness of the AlGaN layer, a surface donor energy level was extracted.

Historically, the output power from AlGaN/GaN HFETs as measured at microwave frequencies of interest (4-18 GHz) has been lower than the expected output power calculated from DC I-V measurements. This problem has been variously referred to as dispersion, current compression and current slump in the literature. It is shown the cause of current collapse is the consequence of the creation of a second virtual gate located between the gate and drain. Accumulation of negative charge on the surface results in a reverse biased virtual gate. It is proposed that the charging up of the surface is caused by positive donor states accepting electrons and becoming charge neutral. The time constant of the surface traps was measured to be in the order of seconds. It is shown that these effects can be decreased to a very large extent by passivating the surface of the device with a layer of silicon nitride dielectric, thus proving that the surface states are responsible for the current collapse.

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5. Conclusions and future work

Chapter 1

Introduction to Current Collapse in GaN HEMTs

1.1 Introduction

High speed semiconductor devices are the essential component of telecommunication systems, as they can handle analog and digital signals at high frequencies and high bit rates. In applications such as amplifiers in transmitting stations for cellular and satellite communication and radar applications for the military, there is a increasing demand for devices that are capable of delivering high power output at frequencies in the range of 2-20 GHz and above.

In the frequency range of interest, silicon devices are inherently limited by material parameters such as inversion layer mobility and saturation velocity. Silicon technology has matured to the extent that intrinsic material parameters limit the performance of devices. Further improvements in the speed of silicon based devices are based on decreasing gate lengths to nanoscale dimensions through the development of better lithographic tools and from using heterostructures such as Si-Ge alloys.

The ability to realize faster and more powerful devices by exploiting the material properties of the III-V semiconductors has been one of the principal motivations for development of three terminal devices in III-V semiconductors. The most widely used III-V high speed device has been the field effect transistor. This is a voltage controlled device. The control electrode is capacitively coupled to the active region of the device, the channel, and the charge carriers are separated by an insulator, wide band gap layer or a depletion region.

It has traditionally been very difficult to grow a good quality oxide layer on the surface of the III-V semiconductors. This has rendered a MOSFET-like structure impossible (although there have been several research efforts in this

direction, such devices are yet to be commercially available). A p-n junction can be used as the gate as in the Junction Field Effect Transistor JFET, or the depletion region of a Schottky metal contact as in the Metal Semiconductor Field Effect Transistor (MESFET). The development of advanced exitaxial growth techniques such as Metal-Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE) has enabled the growth of heterostructure FETs. This has resulted in the most popular member of the FET family, the Heterostructure Field Effect Transistor (HFET). The main advantages of the HFET arise from being able to confine the carriers in a two dimensional well created in a high mobility narrow band layer by placing a wide band gap layer on top. By placing the donor atoms in the wide band gap layer, the carriers are separated from the dopant atoms, thus increasing carrier mobility in the channel, especially at low temperatures. In addition to this, the Schottky barrier of the gate metal on the wide band gap layer is usually larger than the Schottky barrier on the narrow band gap channel layer, allowing a larger gate voltage swing and decreasing electron injection from the gate metal.

However, the use of III-V semiconductors and their heterostructures comes at a price. States within the forbidden energy gap, called deep levels or trap states are created at free surfaces and at the hetero-interfaces. During the growth process, certain impurity atoms are unintentionally incorporated in the bulk of the crystal and give rise to trap states. Sometimes impurities that introduce deep levels are used to create semi-insulating layers by pinning the Fermi-level at mid-gap.

The system of electrons in the deep levels interacts with the system of electrons in the conduction and valence bands through the process of recombination and generation. Since the rate of these processes is dependent on the energy available (in thermal or optical form) to overcome the energetic barrier

between a deep state and the two bands, the transient response of the electron population in the deep levels differs from the transient response of the electrons in the conduction and valence bands. This gives rise to several anomalies in the electrical behavior of III-V FETs.

In this chapter, the current status of HEMT research in the GaN material system is summarized. Current collapse, the main obstacle to the progress of GaN HEMT technology today, is introduced. Current collapse is caused by trapping effects. To provide perspective on trapping effects in III-V FETs, trap-induced anomalies observed in existing III-V FETs are described.

1.2 What makes a good power HEMT ?

Simply put, a good power device is that which allows to switch as large current as possible, on and off across as large a load resistance as possible, to obtain the maximum output power across this load resistance. This means we want to maximize the current available from the device and the voltage swing it can sustain, as shown in **fig 1.1**. To maximize current, the sheet carrier density of electrons and their velocity must be maximized. In GaN, because of the large values of the access resistances, the maximum drain current is not velocity limited but field limited hence the $n_s.\mu$ product is more important than the $n_s.v_{max}$ product. As will be seen in chapter 3, the 2DEG density is a consequence of the strong polarization field present in the GaN system. The strength of the polarization field is proportional to the Al mole fraction. This means that in order to increase the sheet density, AlGaN layers of high Al mole fraction must be grown. These high Al% AlGaN layers must be of high structural quality and the AlGaN/GaN interface must be smooth and ordered to prevent degradation in mobility of the 2DEG.

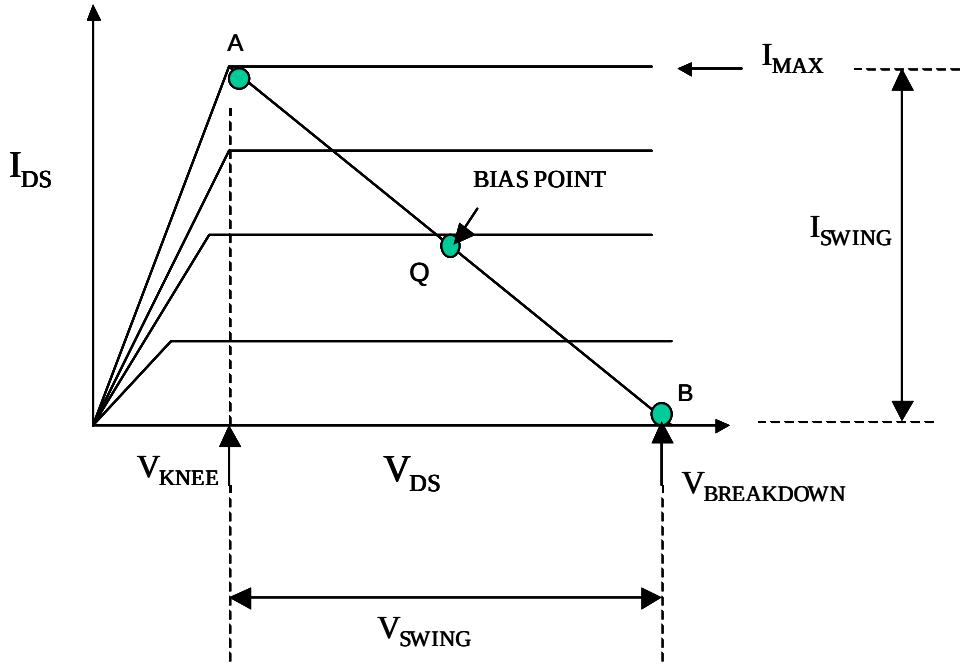


Fig 1.1 Obtaining power from a device

Maximize I_{MAX}	→	Maximize n_s, μ
Maximize n_s	→	Maximize P_{SP}, P_{PE} Maximize Al mole fraction without strain relaxation
Maximize f_τ	→	Minimize effective gate length, Minimize L_g and gate length extension
Maximize μ	→	Minimize dislocations, smooth interface

Fig 1.2 Key parameters to be optimized

The voltage swing sustained is the difference between the knee voltage and the breakdown voltage. A low knee voltage is obtained when the access resistances and the metal contact resistances are minimized. The access resistance is lowered by the same strategy as that needed to obtain high current densities, i.e. maximizing the $n_s.\mu$ product. Ohmic contact metallization schemes as described in **[65]** were used to obtain minimum contact resistances. However improved ohmic contact schemes were not pursued in this work. The strategy followed to obtain maximum breakdown voltages was merely to make the gate drain separation adequately large, i.e. equal to 1 micron. This distance resulted in DC breakdown voltages of the order of 80V. Since the breakdown voltage was not the primary limiting factor in obtaining increased microwave power, this work does not focus on the improvement of breakdown voltage. The key optimizations are summarized in **fig 1.2.**

1.3 Review of current status of GaN HEMTs

At the start of this work, the power performance of GaN HEMTs was already much improved from its embryonic stage in 1995, when the first GaN based FETs were demonstrated by Khan **[64]**. An output power of 2.6-3.3 W/mm at 8-18GHz **[65]** had been demonstrated at UCSB and were the highest demonstrated CW output power densities at these frequency from a solid state device. However, despite these impressive power results, the physics and technology of these devices was far from well understood. The origin of charge in the AlGaN/GaN heterostructure was unclear. Current collapse was the biggest obstacle to obtaining reproducible power performance and it represented an unsolved problem. The link between the nature of the free AlGaN surface to device characteristics was not recognized. The very large breakdown voltages observed and their dependence on gate drain separation was not well understood.

1.3.1 Non-Idealities in GaN HEMTs.

The main non-ideality of interest in GaN HEMTs has been variously referred to as current collapse, dispersion, DC/RF dispersion, and current slump. This is the most important problem that impacts GaN FET technology for high power applications. Current collapse is essentially the observation that the measured output power from the device at microwave frequencies of interest such as 4-18 GHz, is considerably smaller than that expected based on the equation,

$$P = 1/8 * I_{DS,MAX} * (V_{BREAKDOWN}-V_{KNEE})$$

where the values of $I_{DS,MAX}$ and V_{KNEE} are based on the values measured at DC.

This is illustrated in **fig 1.3** which shows the measured DC and pulsed I-V characteristics, typical of a GaN HEMT that exhibits current collapse. The DC curves are measured using a Tektronix curve tracer. The pulsed measurements are made using the pulsed mode of the Tektronix curve tracer where the sequence of drain and gate biases is as shown in **fig 1.4**. As can be seen from **fig 1.3**, there is a considerable reduction in the drain current, together with an increase in knee voltage, when measured under pulsed conditions. In chapter 4, these observations will be explained. Current collapse is caused by the presence of deep levels or traps located in the device structure. Deep levels are called traps because they are not in dynamic equilibrium with the system of electrons in the conduction and valence bands. The charge state of these deep levels does not respond to the high frequency signals applied to the device hence electrons can get “trapped” in them. The presence of traps in other material systems such as GaAs and InP has been well documented in the literature. The non-idealities in FET operation resulting from the presence of deep traps are many: these are summarised in the section below. Note that essentially all trap related anomalies are a result of charge storage in the trap states. These trap-related anomalies can be broadly classified as

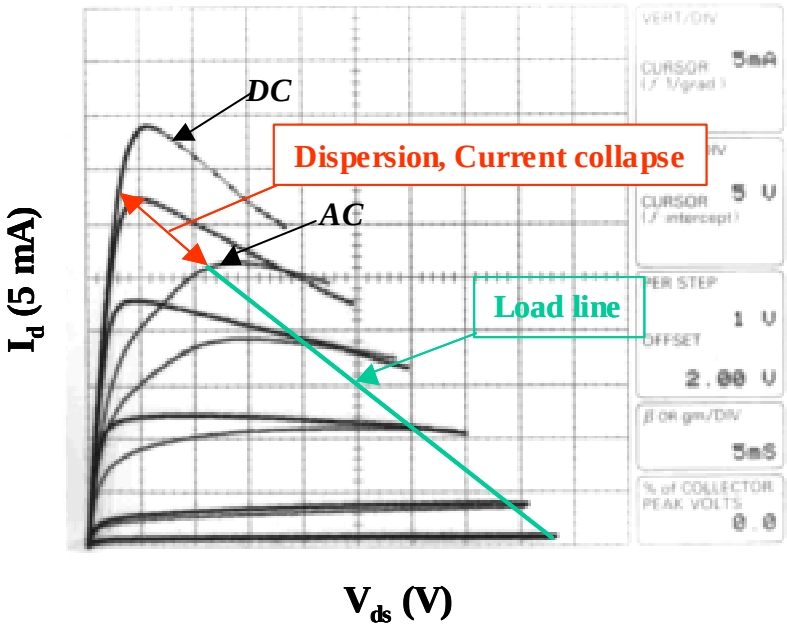


Fig 1.3 Typical DC and Pulsed I-V characteristics of a GaN HEMT

After Wu et.al. IEICE Transactions on Electronics, vol.E82-C, (no.11), Inst. Electron. Inf. & Commun. Eng, Nov. 1999. p.1895-905

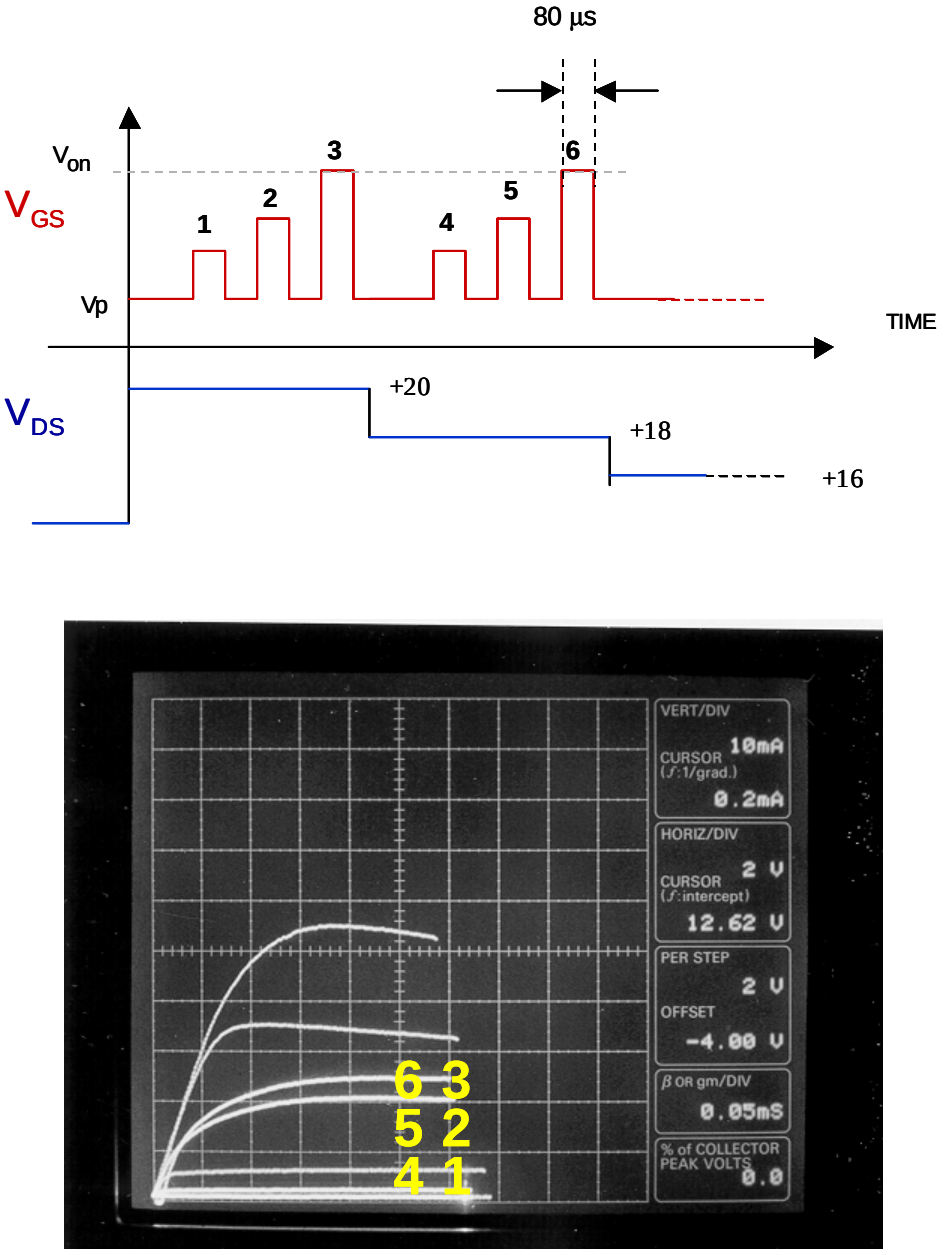


Fig 1.4 Sequence of pulses used to obtain the pulsed I-V curves

small signal high frequency effects, such as transconductance and output conductance dispersion and long term, slow time constant effects which are usually referred as degradation.

The focus of this dissertation is to identify the origin of current collapse, and suggest the means of eliminating current collapse.

The problem of current compression in GaN is unusual in that it is not purely a small signal effect, but its time scale affects device operation in the microwave range of frequencies. In the next section, trap-related anomalies in existing III-V FET technologies are summarised.

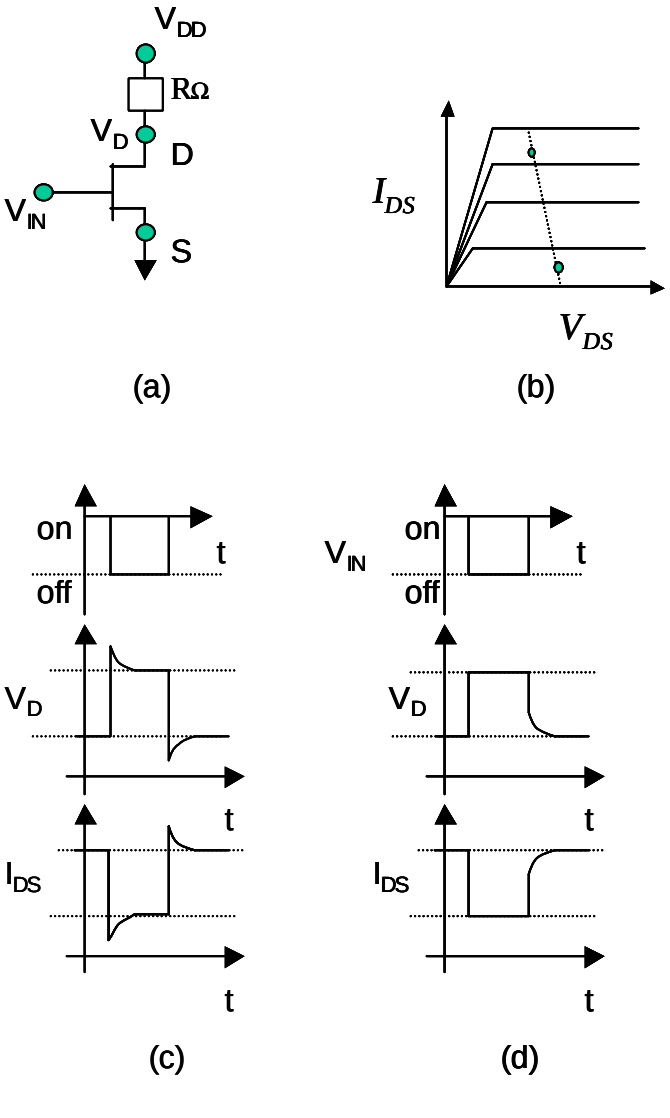
1.4 Trap-related small signal anomalies in III-V FETs

1.4.1 Gate Lag

The term gate lag is used to describe the slow transient response of the drain current when the gate voltage is changed abruptly. This is a serious problem in both analog and digital GaAs IC's [1,2] and is attributed to both surface state effects as well as substrate deep trap effects [3,4,5]. Surface passivation techniques [33,34,1,6] as well as buried p channels [5,7] have been used to reduce gate lag effect.

Figure 1.5(a) shows the measurement schematic used to measure gate lag. **Fig 1.5(b)** shows the movement of the device on the I-V plane. The FET is biased in common source mode and the gate voltage is pulsed from the pinch-off (or a negative value) to a varying final values. A low value of the drain load resistor is usually chosen to keep the drain voltage variation small and avoid any effects caused by variation in substrate trap densities due to drain voltage variation. **Fig 1.5(c)** and **fig 1.5(d)** show the sequence of input pulses and output responses. If the drain current is larger than its steady state when the gate is pulsed ON, this is referred to as overshoot, as shown in **fig 1.5(c).** In **fig 1.5(d)** the drain current

Fig 1.5 Schematic of gate lag measurement.



slowly increases to its steady state value when the gate is pulsed ON: this is referred to as lag.

Gate lag effects have long been attributed to the surface rather than the substrate and bulk effects. Horio [8] showed that although the surface trapping effects are more important, substrate traps can cause gate lag when the gate is strongly reverse biased beyond pinch-off (|Vgs|>|Vp|), [9] as is the case during RF overdrive in power FETs. The nature of the surface traps, i.e. whether electron-trap-like or hole-trap-like has been shown to play a crucial role in gate lag effects [8,10]. *Surface traps can be classified as electron traps or hole traps depending on whether the trap state achieves equilibrium with the system of electrons in the conduction band or valence band*. In a dynamic situation, the quasi fermi level for electron traps is fixed by the drain potential while hole trap quasi fermi level are tied to the gate potential. Surface hole traps lead to more significant gate lag effects than surface electron traps [8]. Near pinch-off conditions, the conduction is determined more by the channel under the gate; close to open channel, the effect of access regions is stronger. Hence the bias dependence is a pointer to the spatial origin of traps causing gate lag. Gate lag effects have been reported on GaAs FETs passivated with low-temperature grown GaAs insulator layers on the surface [11]. Drain current overshoot instead of lag, as shown in **fig 1.5(c)** has been observed in AlGaAs/GaAs HEMTs and is attributed to DX centers in AlGaAs located spatially under the gate [12]. Huang [13] demonstrated that the gate lag effect and two terminal gate drain breakdown breakdown voltage are correlated in a wide single recessed AlGaA/InGaAs psuedomorphic HEMT structure, showing that while negatively charged surface states reduce the electric field peaking at the gate edge, they also cause increased gate lag. It has been shown that by adopting a double recessed structure, the surface states are further removed from the active channel, thus reducing gate lag

effects, while still increasing breakdown voltage, experimentally and by simulation in GaAs MESFETs [4] and GaAs p-HEMTs [13]. In MBE-grown InAlAs/InGaAs/InAlAs HEMTs on InP substrates, gate lag effects that increase at positive gate bias were observed [32]. This kind of bias dependence is similar to that observed in GaAs MESFETs [33,34].

1.4.2 Drain Lag

The term drain lag is used to describe the transient in the drain current when the drain voltage is pulsed in the following manner – a) from an initial value V_{D1} to a final value V_{D2} and b) from an initial value V_{D1} to a final value , held at V_{D2} for a fixed duration and brought back to V_{D1} . The gate voltage is held constant in both cases. Depending on the values of V_{D1} and V_{D2}, the initial drain current is either larger or smaller than the steady state value. **Fig 1.6** shows the locus on the I-V plane during a drain lag measurement. Drain lag has been observed in GaAs MESFETs [14] and AlGaAs/InGaAs p-HEMTs [15] and in AlInAs/InGaAs/InP HFETs [16].

GaAs devices are usually fabricated on semi-insulating substrates which provide good isolation between devices in IC's and minimize parasitic capacitances. However, the semi-insulating nature of the substrate is achieved by impurity compensation by deep levels which can give rise to transient effects. Although the surface trapping effects cause transient effects in drain currents, even devices with single and double gate recesses and passivated surfaces have exhibited drain current transients. For this reason, drain lag effects are commonly also attributed to the substrate trapping effects.

In LEC-grown GaAs, the semi-insulating substrate contains a deep donor (EL2) and shallow acceptor (Carbon) with the concentration of the deep donor

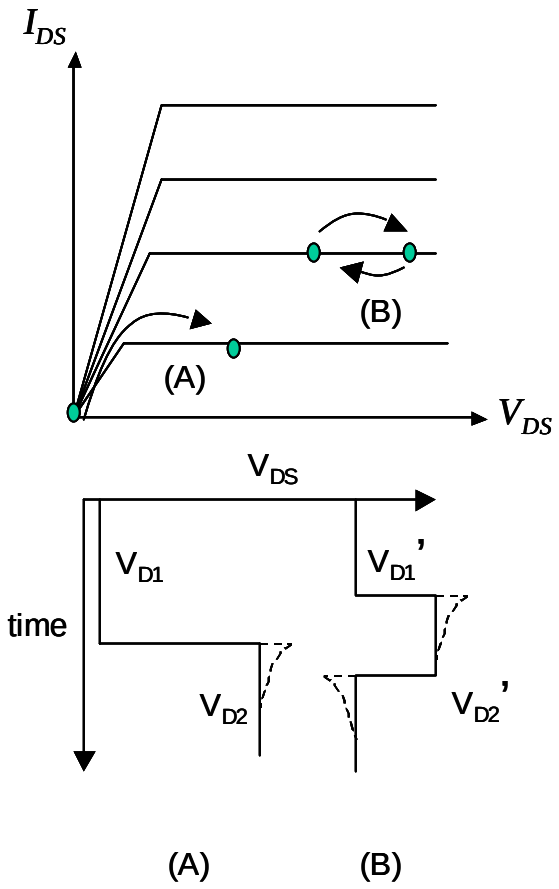


Fig 1.6. Schematic of drain lag measurement. The dotted lines show typical drain current transients.

much larger than that of the shallow acceptor [17,19]. Horio [14] has shown that when the drain bias is pulsed to a larger value a space charge layer is formed at the substrate-active layer interface. As the deep donor level captures electrons, a back gate is formed that constricts the channel, reducing the drain current. Because the compensation ratio given by $N_{deep\ donor}/N_{shallow\ acceptor}$ is usually kept constant, the concentration of empty available deep donor levels ($\sim N_{deep\ donor} - N_{shallow\ acceptor}$) is dependent on the concentration of native shallow acceptors. Hence the concentration of the native shallow level is the important parameter in deciding the magnitude of the drain lag effect. The rate limiting step in the drain lag effect has been found to be the capture and emission rate of electrons by the deep donors [18]. Kunihiro [15] developed a large signal equivalent circuit model including the effect of substrate traps in AlGaAs/InGaAs p-HEMTs.

1.4.3 **Frequency Dispersion – Transconductance**

The variation of small signal output transconductance g_m, with frequency has been observed in GaAs MESFETs [20], AlGaAs/InGaAs p-HEMTs [21] and AlInAs/InGaAs/InP HEMTs [22]. In AlInAs/InGaAs/InP HEMTs [22] the dispersion is primarily between 100Hz and 1MHz and in AlGaAs/InGaAs p-HEMTs [21,12] it occurs mainly in the range 100Hz-100kHz and in GaAs MESFETs in the range 10Hz-100kHz [20]. So far in the literature, g_m dispersion has not been reported to extend into the GHz frequency range in FETs in any material system.

In GaAs MESFETs, g_m dispersion is primarily attributed to surface states located in the gate-drain access region. One reason is that g_m dispersion has not been observed in FATFET structures in MESFETs where the metallurgical gate length is a very large fraction of the source to drain separation [24]. In such a

device the contribution of the access regions to the total resistance between source and drain is very small, thus any dispersive effect due to access resistance becomes too small to measure.

A theoretical study by Zhao [30, 45] on GaAs MESFETs reported that both surface traps and substrate traps cause negative g_m dispersion. It was shown that the peak frequency in transconductance spectrum $dg_m(f)/df$ vs f, frequency, is equal to the characteristic frequency of the surface state responsible for the peak. Hence temperature dependence of the g_m dispersion should reveal the energy level of the deep trap. Gate leakage current was considered to be the source of electrons needed to charge the surface states [20]. Since this current increases at negative V_{gs}, the magnitude of dispersion is expected to increase at V_{gs} close to pinch-off. Hence, it was hypothesized in [20] that the contributions of substrate and surface traps can be separated by observing the effect of gate bias on the dispersion. Golio [23] observed that in sub-micron GaAs MESFETs, the magnitude of g_m dispersion was larger for Vgs values close to open channel conditions. However, this was interpreted as indicating that under these bias conditions, traps closer to the device surface were important and no discussion of the supply of electrons necessary to fill the surface states was made.

Ladbrooke [24] developed a model to explain g_m dispersion in terms of the variation of the total resistance between source and drain, shown in **fig 1.7**. The total resistance between source and drain is composed of the resistance under the gate and the contribution of the access regions. The resistance of the source-drain and gate-drain access regions depends on the surface depletion depth which depends on the density of occupied states as shown in **fig 1.7.** In the linear region, the transconductance depends on the total resistance between source and drain. The charge transfer mechanism to the surface states was invoked to be thermionic

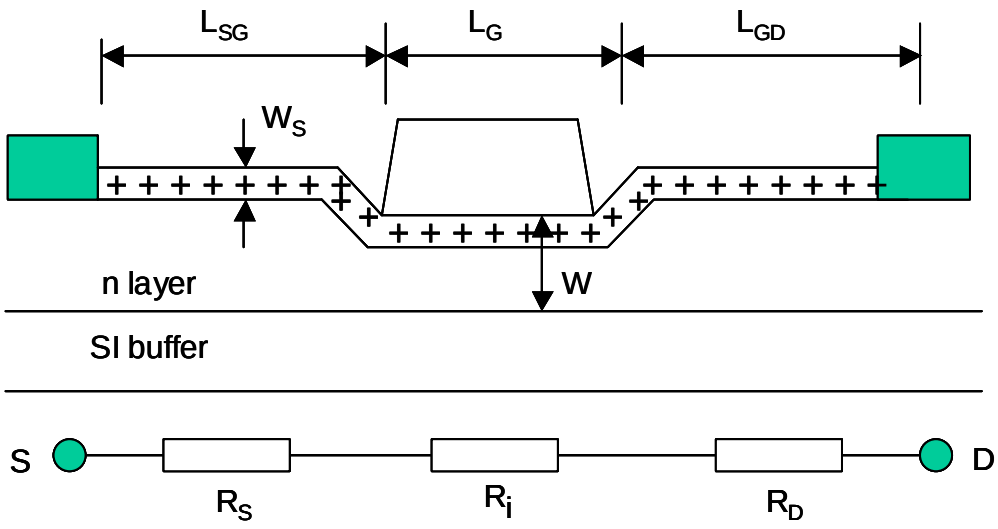


Fig 1.7. Modelling the effect of surface states in the access regions on transconductance dispersion. The access regions L_{SG} and L_{GD} contribute resistances R_S and R_D. In the linear region the transconductance depends on the total resistance between source and drain. Hence the surface depletion depth W_S in the access regions affects the transconductance.

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field emission from the gate edge singularity [25]. In [24] the compression in g_m for an unpassivated device was ~ 20% which was found to be reduced to ~ 15% after passivation after measurement and in properly pre-passivated devices, the extent g_m compression was found to be as low as 2.5%.

Balakrishnan [46] reported that a temperature dependent surface leakage current in passivated GaAs MESFETs was the origin of the reported [20] temperature dependence of the transconductance dispersion. It was also observed in [46] that the most important parameter in determining the extent of g_m dispersion is the density of surface states. Recently, capacitive DLTS measurements on GaAs MESFETs of large gate periphery showed the presence of two hole like traps at 0.65eV and 0.88eV below the conduction band [47]. These levels agree well with the energy levels of As_{Ga}^{+} (0.65eV below E_C) and As_{Ga}^{++} (0.90eV below E_C), which are held to be responsible for Fermi level pinning at the GaAs surface [63]. In the reverse pulse in a DLTS measurement, deep traps in the GaAs layer (such as EL2) emit electrons, while electrons are captured by the surface states The capacitance C is measured at times t_1 and t_2 after the application of the reverse pulse and the DLTS signal is given by $C(t_1)$-$C(t_2)$. By changing the time t_1 while keeping t_2/t_1 constant, the position of the peak in the DLTS signal is shifted in temperature. The peak height of the hole-trap like signals increased with temperature while the peak height of the signal due to the EL2 level is only bias dependent and temperature independent. The surface trap occupancy is dependent on the thermionic current from the gate edge which increases with temperature. Hence the hole-trap signal increases with temperature. This argument is used to conclude that the traps observed in [47] are surface traps.

When g_m dispersion is caused by traps in the wide-band gap barrier layer under the gate, the g_m is larger at RF frequencies than at low frequency (positive dispersion). This is because the traps in the barrier layer have relatively long time

constants (in the range of ms to s) and hence at microwave frequencies can be considered “frozen”. Hence all of the gate voltage modulation is reflected as a change in the channel charge that results in a change in output current. At sufficiently low frequencies when the deep traps under the gate respond to the gate voltage, part of the gate voltage is reflected in a change in trapped charge density that does not contribute to current. In HEMTs, where both the surface traps and traps in the wide band gap layer under the gate contribute to dispersive effects, both positive and negative dispersion can be observed in the same device. This kind of g_m dispersion has been observed in InAlAs/InGaAs MODFETs [26,22] where the deep electron traps are located in the InAlAs layer [27].

Kruppa [22] showed that in AlInAs/InGaAs/InP HEMTs both positive and negative g_m dispersions were present depending on the bias point. The extent of negative dispersion was smaller at more positive gate voltages, a trend opposite to that reported in [23]. In [22], gate leakage current is assumed to supply the electrons needed to charge the surface states, and since this current is larger at more negative gate voltages, the g_m compression is larger when V_{gs} is closer to pinch-off. Positive g_m dispersion is attributed to electron traps in the InAlAs donor layer. **Fig 1.8** shows the mechanism of positive dispersion proposed in [22]. At low frequencies the gate voltage modulates the electron traps in the InAlAs layer and the carrier density in the channel. At high frequency, the traps in the InAlAs layer do not respond and hence all the change in gate voltage is reflected in a change in the channel electron density. Hence g_m increases at high frequency.

Ng [28] found that in InAlAs/InGaAs HEMTs mainly negative dispersion was observed, which increased in magnitude as the gate voltage was more negative. Unlike in GaAs MESFETs, g_m dispersion with a similar trend was observed in FATFETs. As the extent of dispersion was found to vary with the In

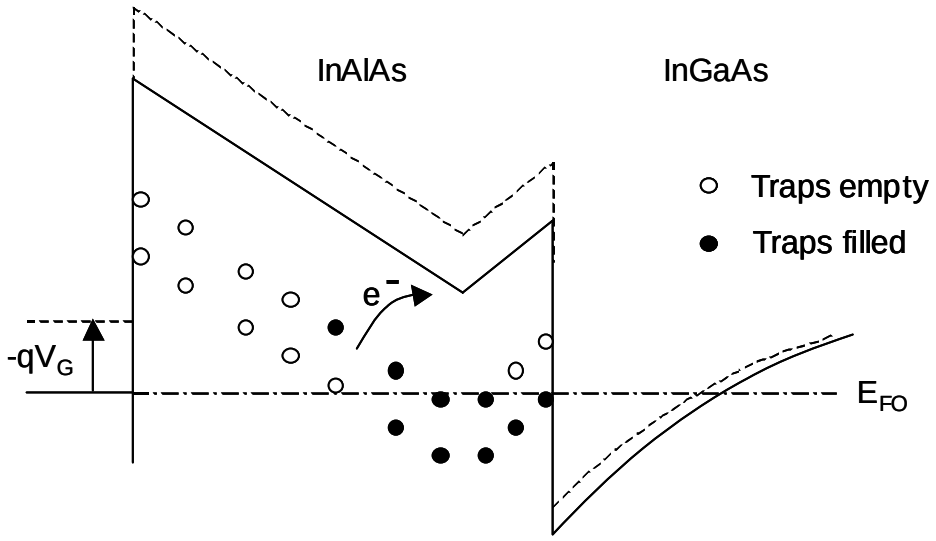

Fig 1.8. Mechanism of positive transconductance dispersion arising due to deep levels in the barrier layer. At low frequencies, part of the gate voltage modulates the traps in the wide band gap layer: at high frequency these are not modulated hence the modulation efficiency of the gate and the output transconductance increases.

After Kruppa et. al. IEEE Trans. ED 44(5), p687, 1997.

concentration in the channel, this dispersion was attributed to traps in the donor InAlAs layer/InAlAs/$In_xGa_{1-x}As$ interface located under the gate and not from the access regions.

Conflicting data has been presented in the literature regarding the g_m dispersion characteristics of AlGaAs/GaAs HEMTs. Chan [21] reported negative dispersion characteristics in the frequency range 100Hz-100kHz for unpassivated AlGaAs/GaAs and InGaP/GaAs HEMTs. Current collapse at low temperatures associated with a DX center caused by the Al present in AlGaAs layer, is absent for the InGaP/GaAs HEMTs. However the presence of another deeper trap in both the AlGaAs layer and non-Al-containing InGaP layers has been invoked to explain the negative g_m dispersion characteristics and no mention of contribution from surface traps was made. These findings are opposite to those of Canali et.al. [12,29] who tested AlGaAs/GaAs HEMTs passivated with SiN surface dielectric layer. Positive dispersion in the 100Hz-10MHz range was observed and attributed to DX centers in the AlGaAs layer.

Note that in all works in the literature on g_m compression, the experiments are conducted at small signal conditions, such that the amplitudes of V_{ds} and V_{gs} are typically less than 200mV.

1.4.4 **Frequency Dispersion – Output resistance**

Several researchers have measured output resistance dispersion in GaAs MESFETs. Golio [23] observed that output resistance decreases from the dc value by as much as 60%, depending on the bias conditions over the frequency range 20Hz-100kHz. The dispersion was found to be maximum for V_{ds} values in the saturation region and V_{gs} values close to open channel. This bias dependence was used to support the argument that the dispersion is caused by surface traps. This is because in the velocity saturated regime, only changes in charge density caused

by changes in the surface depletion region affect the current. Ng [28] measured the R_{ds} dispersion in InAlAs/InGaAs HEMTs and found that negative and positive dispersion occurred in the same device depending on the Vds bias. The magnitude of dispersion was found to be smaller than in GaAs MESFETs and AlGaAs/GaAs HEMTs and directly correlated with the trap density in the InAlAs layer. Traps in the InAlAs layer were hence indicated as the source of dispersion although no attempt was made to understand the reason for positive and negative dispersion characteristics. Ohno [31] reported dispersion in AlGaAs/GaAs HEMTs. The presence of a partially depleted floating p-type buffer layer in between the channel and the semi-insulating substrate suppressed the magnitude of output resistance dispersion arising from deep traps in the substrate [31]. In [31] it is reported that output resistance decreases with frequency while Canali report either an increase or decrease in output resistance, depending on the V_{ds} bias in AlGaAs/GaAs HEMTs [12]. In the literature, output resistance dispersion is used to show the existence of traps in the device structure. However, no correlation has been made between the bias dependence, the nature of the dispersion (positive or negative) and the spatial location of traps causing output resistance dispersion. The physics and mechanism of output resistance dispersion does not appear to be well understood. In all reported works, output resistance dispersion vanishes above 1MHz.

1.4.5 **Bias dependent and photo-sensitive drain current collapse at low temperatures**

Because of the spatial separation of dopant atoms from charge carriers, 2DEG mobility is enhanced considerably at low temperatures in AlGaAs/GaAs HEMTs. However when these HEMTs are cooled to 77K in the absence of illumination, the drain currents decrease: this is generally referred to as current

collapse[35]. This collapse is associated with DX centers in the AlGaAs donor layer [36]. It has also been observed to a lesser extent in $Al_{0.2}Ga_{0.8}$ As/InGaAs p-HEMTs [39,40].

The DX center is a deep donor level caused by a defect complex that occurs in doped $Al_xGa_{1-x}As$ [62]. Its optical and electrical properties are explained by invoking localized lattice relaxations using a configuration co-ordinate model. Its activation energy follows one of the indirect conduction bands in III-V structures. Once the composition of a ternary compound is at or near the crossover point between direct and indirect conduction bands, the DX center will start to affect the device electrical properties [44]. In $Al_xGa_{1-x}As$ this crossover occurs at x=0.37. For compositions well below the crossover point, the trap energy lies above the minimum of the conduction bands and no deep trapping effect is observed. At room temperature, Fermi-level pinning due to DX centers in AlGaAs/GaAs HEMTs has been shown to result in a decrease in dc transconductance and maximum current [42]. In AlGaAs/InGaAs pseudomorphic HEMTs, a large conduction band discontinuity can be obtained by using a small Al mole fraction ($x<0.2$) where DX centers are not created in the n-AlGaAs layers [43]. By using non Al containing alloys in the wide band gap donor layer, the low temperature collapse has been eliminated in GaInP/GaAs HEMTs on GaAs substrates [40] and GaInP/InP/GaInAs HEMTs on InP substrates [41].

It has been shown that the degree of current collapse, or variation of low field channel conductance strongly depends on the history of applied bias conditions, such as total drain voltage, gate voltage and their total applied time [37]. The detrapping process proceeds via thermal emission when the sample temperature is raised to above 140K [36] or can be optically induced [38]. Meneghesso [39] showed that in $Al_{0.2}Ga_{0.8}As$/InGaAs p-HEMTs the decrease of I_{DS} is caused by hot channel electrons getting trapped in the AlGaAs donor layer

mostly in the gate drain access region. Depending on bias conditions, a threshold voltage shift is also observed when hot electrons get trapped in the AlGaAs layer under the gate. Additional drain voltage stress causes recovery of the drain current due to holes generated by impact ionization recombining with the trapped electrons.

1.5 Failure Mechanisms and Degradation

It is noted from the preceding part of this chapter that in almost all works reported in the literature that attempt to relate the trapping location and physical origin of the deep trap to observed I-V characteristic, small signal experiments are usually conducted, with the exception of gate lag experiments where the gate voltage may be pulsed from pinch-off to open channel. In addition, the experiments are usually conducted in low field conditions i.e. small drain voltages. This is because it is indeed easier to interpret the results of such experiments and produce useful material models. Changes in device characteristics that occur during large signal and large drain bias operation are usually classified as degradation or failure. While attempts have been made to establish the connection between trap levels identified using small signal, low field experiments and observed large signal degradation, few direct correlations are reported in the literature. In this section, existing work in device degradation and correlations between small and large signal, non ideal behaviors are summarised.

In the early days of AlGaAs/GaAs HEMTs, degradation of gate metallization and an increase in source drain contact resistance was reported after accelerated lifetime tests [48]. These problems were mainly induced by thermally activated metal semiconductor interaction. Better manufacturing technology

appeared to have considerable reduced such failure modes especially in ohmic contacts. However under large signal conditions, several problems still persist in GaAs FET technology especially in GaAs p-HEMTs, devices where intrinsic transconductances are higher and therefore more susceptible to surface related problems. Recently Meneghesso [51] reported permanent degradation effects in AlGaAs/InGaAs PHEMTs with Al/Ti gates submitted to accelerated life tests. The degradation is ascribed to electron trap generation in the gate drain access region under high electric field conditions, resulting in a breakdown walkout phenomenon. Thermally activated interdiffusion of the Al/Ti gate occurred, resulting in a decrease of gate barrier height and increase in drain saturation current. Low frequency transconductance dispersion increased in magnitude and was reported to be the most relevant failure mode. Under high power RF operation, some problems associated with GaAs pHEMTs are gate lag [48], power drift [49] and power slump [50]. Huang [48] describes some of the degradation mechanisms common to GaAs pHEMTs, although it is noted that not all pHEMTs suffer from these degradations mechanisms.

1.5.1 **Breakdown walkout**

For power devices, breakdown voltage along with maximum drain current is the most important parameter. Avalanche breakdown is generally believed to be the mechanism of the gate drain breakdown. Wemple [54] showed that in a planar GaAs MESFET structure, breakdown voltage increased when the channel thickness was made smaller. This is purely a consequence of converting the electrostatic problem from two dimensions to one dimension and thus making electric field in the depletion region approximately linear. Surface passivation by SiN or SiO_2 dielectric was found to reduce the breakdown voltage in [54]. It was hypothesized that the passivant introduced positive charges that effectively

increased channel thickness by decreasing the surface depletion layer. It was also found that dc avalanche currents were substantially lower than pulsed values. David [55] found that recessed GaAs MESFET structures have better breakdown characteristics except under very pinched off conditions, in agreement with experimental observations [56]. Barton and Ladbrooke [57] showed that negative charge in surface states caused suppression of the electric field singularity at the drain edge of the gate resulting in an increase of breakdown voltage in GaAs MESFETs. The concentration of surface states could be enhanced by penetration of metal wave functions into the semiconductor, altering the band structure. The Franz-Keldysh effect allows for modifying the density of allowed states by the intense electric field at the drain edge of the gate. Mizuta [58] showed clearly that surface potential effects play a very strong role in reducing the electric field singularity at the gate edge. Experimental data was shown to be consistent with a surface pinning of 0.6-0.8 eV.

In AlGaAs/GaAs HEMTs breakdown walkout has been observed [59]. Breakdown walkout refers to the increase in breakdown voltage when the device is stressed under conditions close to pinch-off with the drain voltage gradually increased. After the stress, the breakdown voltage is found to be permanently increased, although the I_{DSS} g_m and R_S are not increased. Chou [60] showed that in passivated AlGaAs/InGaAs pHEMTs breakdown walkout depended strongly on the PECVD process conditions during passivation and were relatively insensitive to the starting wafer from different vendors. It was found in [60] that the breakdown walkout was accompanied by a decrease in gate current. Recently, a field plate configuration on SiO_2 passivated AlGaAs/GaAs HFETs was presented as a better method of suppressing the electric field singularity at the gate edge, than stored negative charge in surface traps. By using a metal field plate, which is

electrically shorted to the gate, breakdown voltage increased without the delay associated with the slow response of trapped charge. Hence increased microwave power output was obtained [61].

1.5.2 **Degradation – Power Drift**

Power drift is the change in output power from the device as a function of time under test. **Fig 1.9** shows power drift characteristic of a p-HEMT [48]. The device is over driven by 5dB (i.e input RF power is 5dB more than the 1dB compression point). Output power continuously decreases with time and recovers partially when RF drive is interrupted, as shown in **fig 1.9**. It was found that the recovery was thermally activated and complete recovery possible after 1 hour at 175 C. Note that since the gain of GaN HEMTs decreases continuously with input power, GaN FETs operated for maximum power output are usually overdriven by as much as 7dB. This will be discussed more in chapter 4. It was found in [48] that there was a correlation between drift in gate-lag (not gate lag per se) and power drift.

1.5.3 **Degradation – Power Slump**

Power slump refers to a gradual and steady drop in output power when a pHEMT is overdriven for hours [48]. The change in output power is associated with a change in dc characteristics such as drain current and breakdown voltage [50,53].Typically with storage time or thermal activation the slumped characteristics do not recover. Leoni [53] reported an increase in gate lag characteristics after power slump is induced by accelerated dc stress. After stress, gate overshoot (typical of traps under the gate) turns into gate lag (typical of surface traps) and conductance DLTS measurements show the presence of only hole-like traps after stress (the characteristic of hole-like traps is mentioned in

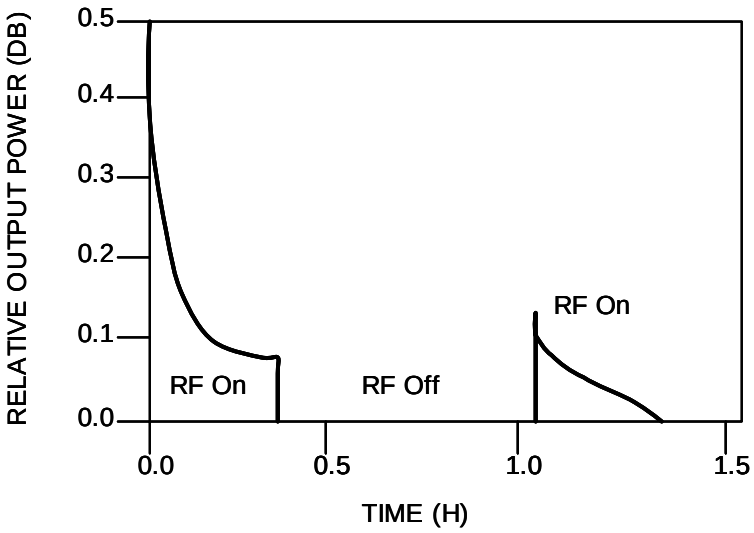

Fig 1.9. Typical power drift characteristics of a GaAs PHEMT under 5dB RF overdrive (RF power is increased 5dB beyond the 1dB gain compression point). After the RF drive is interrruputed, the output power recovers at least partially but undergoes a similar drift once the RF drive is re-applied.

After Hwang, Solid State Electron, 43, 1999, pp.1325-1331 .

section 1.2.3) with the same activation energy, as obtained before the stress. It is argued in [53] that the difference in gate lag characteristics is because of differences of surface recombination resulting from decreased hole concentration at the surface. After stress, the build up of negative charge in the passivant reduces the electric field in the high field region near the gate, reducing impact ionization rate. This leads to lower hole concentrations at the surface and increased rate of charge up of surface traps.

The distinction between power drift and power slump is the ability to recover the characteristics and the time scale of the test (hours instead of minutes). This suggests that the power slump is merely an advanced form of power drift i.e. temporary vs permanent degradation. The thermal activation energy of the recovery of pHEMTs suffering from power drift is reported to be 1.4eV [48] which is consistent with the reported energy of the K_0 center in amorphous hydrogenated silicon nitride [51]. The reported thermal activation energy of surface states in GaAs is 0.4eV [52]. This difference in activation energies, along with the very long time scales of the degradation experiment is used to support the argument that charge trapping in the silicon nitride dielectric layer is the cause of the long term degradation in GaAs pHEMTs. Since GaAs pHEMTs that do not suffer from such long term problems have been fabricated, developing a stable passivation technology is a technological problem that has been overcome. The lack of literature on stable passivation techniques suggests that commercial foundries have their individual recipes for overcoming such degradation, and that these recipes remain proprietary. It is interesting to note that GaN HEMTs suffer from power drift and power slump and usually HEMTs show the best output power when measured immediately after fabrication. Measured characteristics after storage times of a few months or more show a remarkable permanent decrease in output power and dc drain currents. Both passivated and

unpassivated devices display this degradation. However this data is not well documented. This is only mentioned briefly here as the long term degradation of GaN HEMTs is not the focus of this dissertation.

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Chapter 2
Sources of Non-idealities

2.1 Introduction

In the previous chapter, the status of GaN HEMT technology was reviewed. Current collapse, a trap related anomaly, was introduced as the dominant obstacle to obtaining high power output. To provide perspective, various trap related anomalies in III-V FETs were discussed. A first step toward eliminating trap related problems is to understand where traps exist in the device structure and what the sources of these traps are. In this chapter, the possible trapping locations in the device structure is discussed. The sources of these traps is also discussed. However, since the origin of traps and their densities are entirely related to the growth process of the device layers, which is not the focus of this dissertation, this discussion is restricted in scope and does not include a discussion of optimum MOCVD or MBE growth conditions needed to achieve lowered trap densities.

2.1.1 Outline of this chapter

First, the possible locations of traps is discussed. Then, progress of material quality resulting in the minimization of trap densities in the device structure is discussed. The discussion is restricted to the bulk of the structure, the contribution of the free AlGaN surface is discussed in a subsequent chapter. Deep level compensation as a method of obtaining semi-insulating material is reviewed. The origin of background electron concentration in unintentionally doped GaN due to shallow native donors such as oxygen and the compensation methods employed (incorporation of deep impurities, dislocations and dislocation mediated impurities) is discussed. The impact of dislocation density is separately studied by

comparison of the HEMT devices fabricated on laterally epitaxially overgrown (LEO) and non-LEO material. The development of high quality AlGaN layers necessary to obtain high power GaN HEMTs is briefly discussed. Data is presented that shows that while improving bulk material quality is essential to improving the output power of GaN HEMTs, another significant source of non-ideality remains to be eliminated.

2.1.2 **Possible location of traps**

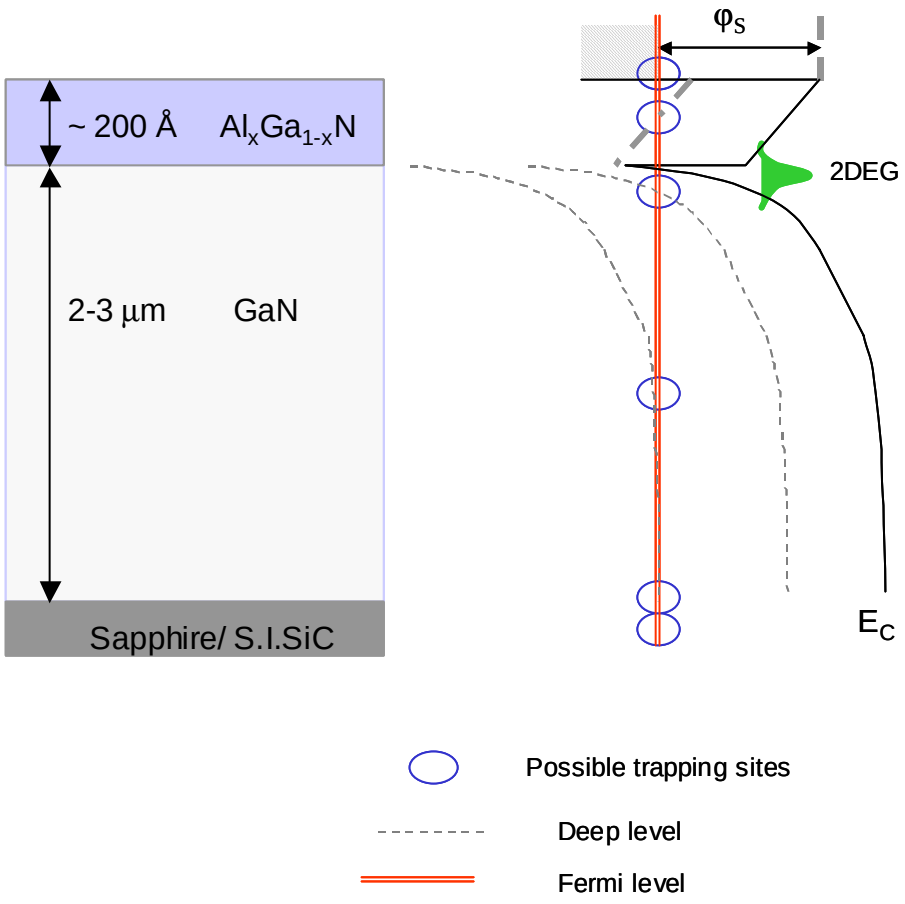
It is clear from a survey of existing literature that the traps causing non-idealities can be present in the semi-insulating substrate, the wide band gap barrier layer, the free surface of the wideband gap layer. In a typical GaN HEMT these locations translate to,

1) the semi-insulating substrate, (in the case of growth on SiC)
2) the interface between GaN and the substrate, either sapphire or SiC.
3) the GaN buffer layer
4) the AlGaN layer
5) the free surface of the AlGaN layer.

as shown in **fig 2.1**. It has been shown in the literature on FETs in GaAs and InP material systems that the traps are present in all the different locations corresponding to (1-5) above. Progress in material growth and devices layer structure design resulted in the suppression of trap densities and their effects on device performance.

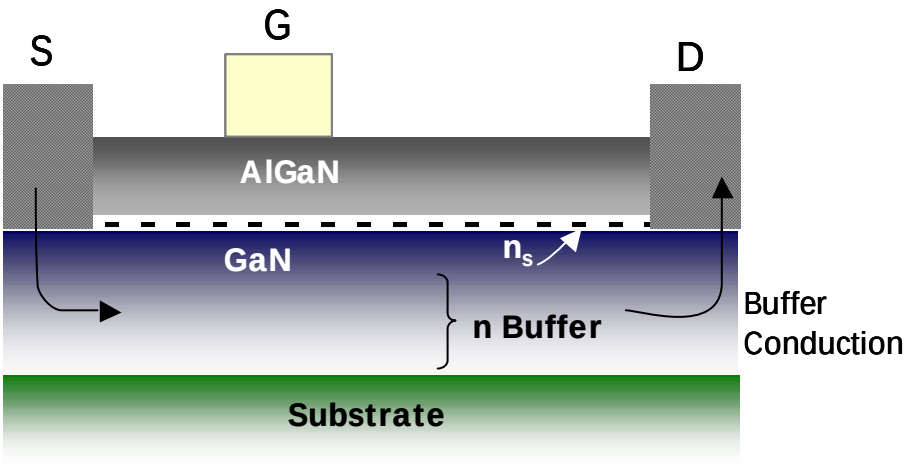
2.2 Traps in the GaN buffer layer

We first consider the GaN buffer layer. Why are there traps in this layer? Conduction between source and drain can occur through the 2DEG and also through a leakage path in the GaN buffer. For good pinch-off characteristics, the



1. S.I. Substrate
2. Substrate-GaN buffer interface
3. S.I. GaN buffer
4. AlGaN bulk
5. Free surface of AlGaN

Fig 2.1 Possible location of traps



HIGH RESISTIVITY BUFFER IS ACHIEVED THROUGH COMPENSATION → SOURCE OF TRAPS

For a 1 µm Thick Buffer

$$n_{Buffer} \sim 10^{16}\,cm^{-3} \times 10^{-4}cm = 10^{12}cm^{-2}$$

$$n_{Channel} \sim n_S \sim 10^{13}cm^{-2}$$

$$\frac{I_{Buffer}}{I_{Channel}} \sim 10\% \text{ (Unacceptable)}$$

Fig 2.2 Need for traps in the GaN buffer

leakage through the GaN buffer must be minimal or absent, as illustrated in **fig 2.2**. To obtain minimal leakage through the buffer layer the electron density in the buffer must be minimized, or the Fermi level must be close to the intrinsic level or midgap. The fermi level is close to midgap in material of very high purity. Obtaining material of such high purity that the carrier concentration is at intrinsic levels ($n=p=n_i$) is an extremely difficult technological problem. It is easier, technologically, to pin the Fermi level at midgap by adding deep impurities. This method of obtaining insulating material has been used in GaAs and InP material systems and is referred to as compensation. Using compensation, buffer leakage is eliminated; however compensation introduces traps in the buffer layer. Compensation is explained in the next section.

2.2.1 **Making a semi-insulating buffer - Compensation**

Consider a situation where as-grown material contains a density of native shallow donors, N_D. The native shallow donors are compensated by adding deep acceptors of density N_{AA}. The other case in which native shallow acceptors are compensated by added deep donors obeys similar reasoning. **Fig 2.3(a)** shows the electron density in the conduction band as a function of the deep acceptor concentration N_{AA}. The curves are drawn for different concentrations of N_D, the shallow donor, as a parameter. It is seen that for compensated material ($N_{AA}/N_D>1$) the electron density in the conduction band remains at a very low value, practically independent on the density of native shallow donors. **Fig 2.3(b)** shows the Fermi level in the same structure, drawn for different native donor densities. Observe that the Fermi level is close to the conduction band when the material is under-compensated ($N_{AA}/N_D <1$) and falls sharply to the deep acceptor level for compensated material ($N_{AA}/N_D >1$). In the simulations, the deep acceptor level is set to 600 meV above the valence band. **Fig 2.4** shows the ionization ratio

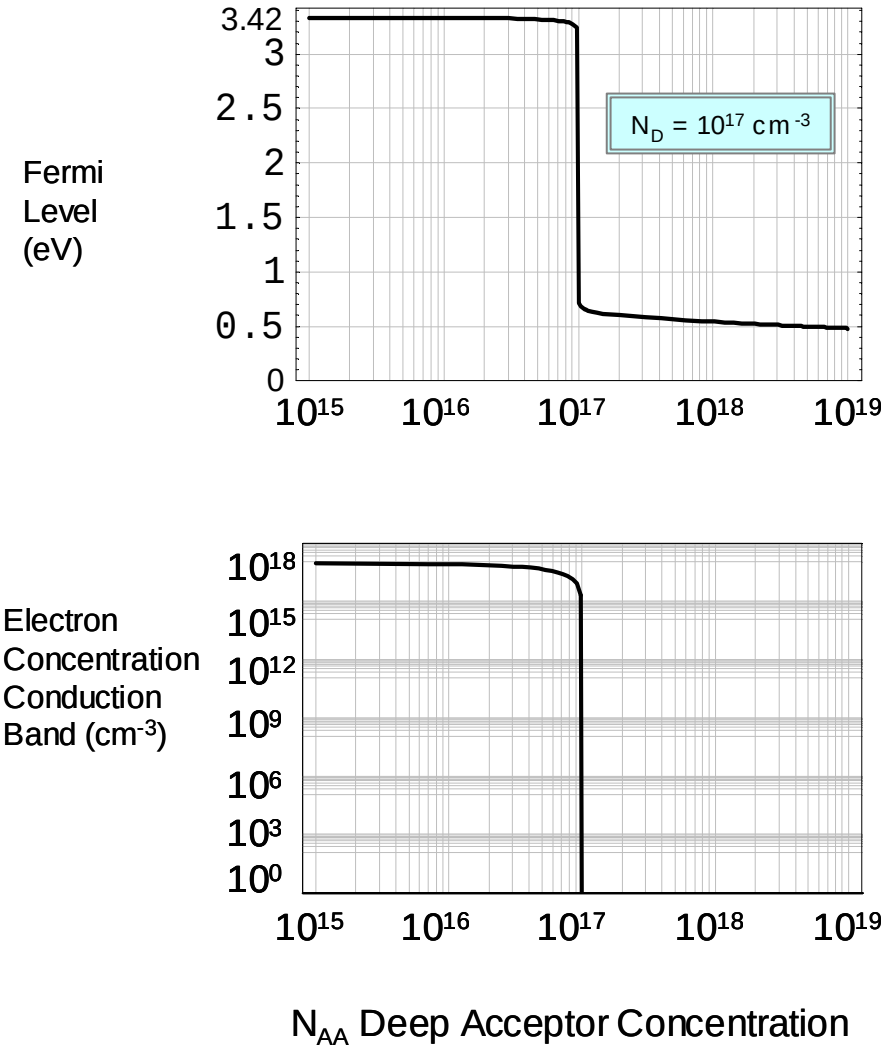
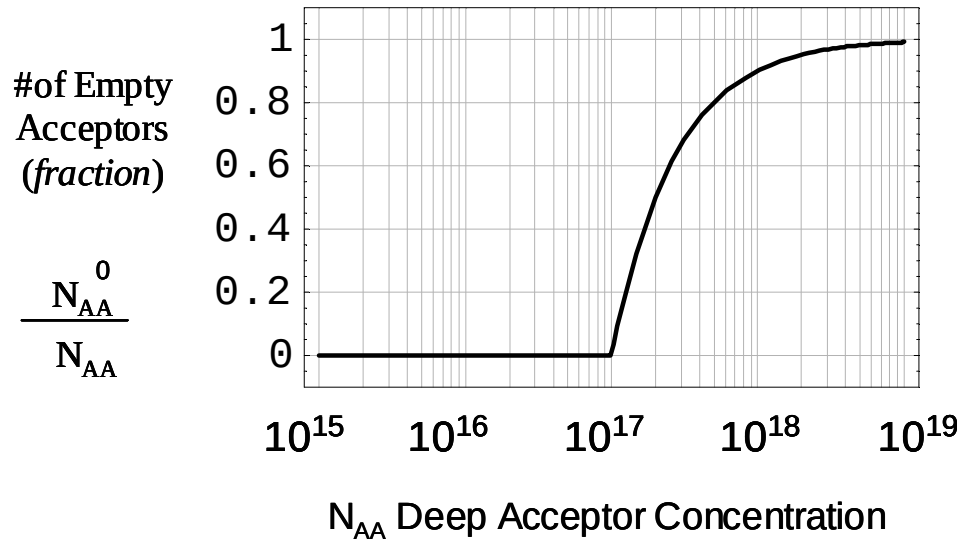


Fig 2.3(a) electron density in conduction band as a function of deep acceptor concentration.
(b) Fermi level for different acceptor concentration.



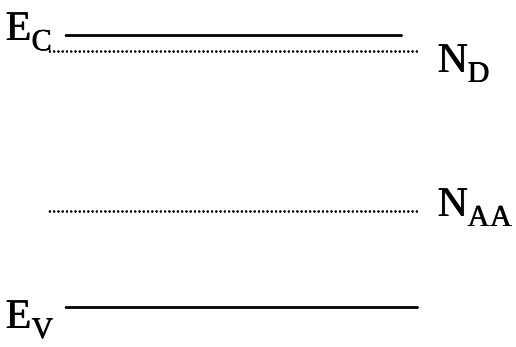


Fig 2.4 Ionization Ratio for different deep acceptor concentration

of the deep acceptors (defined as the ratio of full acceptors to the total acceptor density N_{AA}^{-} /N_{AA}) as a function of deep acceptor concentration N_{AA} for a particular N_D (N_D=10^{17} cm^{-3}). The ionization ratio of the deep acceptors decreases rapidly for compensation ratios >1, therefore the neutral or empty deep acceptor concentration is very large for compensation ratios >1. Note that the density of empty deep acceptors is the important parameter to consider for trapping effects in the bulk because this is the density of available sites for electron trapping. The density of empty deep acceptors needs to be minimized. Since the minimum compensation ratio to obtain a semi-insulating buffer is fixed by the native shallow donor concentration as seen from **fig 2.3(a)*, it follows that to minimize trapping effects of the deep traps in the buffer, the density of native shallow donors should be minimized*.

2.2.2 **Compensation in GaAs**

Single crystals of GaAs have been grown by many techniques utilizing melt and solution approaches, including horizontal Bridgman (HB) and vertical Bridgman (VB), gradient freeze, Czochralski, liquid encapsulated Czochralski (LEC), liquid encapsulated Kyropolous, float zone, horizontal and vertical zone melting. The Bridgman technique is dominant in terms of material quantity. However its application is mainly in optoelectronic substrates and the LEC growth technique is dominant in electronic applications [2]. Carbon is a shallow acceptor in GaAs produced by the LEC technique. The semi-insulating nature of GaAs is due to the balance between the concentrations of carbon, a shallow acceptor and the native defect EL2 which is a deep double donor. EL2 concentrations are found in semi-insulating GaAs grown under As-rich conditions at a concentration level of a few times 10^{16} cm^{-3}. The resistivity of GaAs grown by the LEC technique strongly depends on the melt stoichiometry: the material is

p-type if the As concentration is below 0.475 As atom fraction and semi-insulating otherwise. Under some growth conditions GaAs is weakly n-type: this is mainly due to the incorporation of oxygen and sulphur [49], present as impurities in the system. Chromium, which produces a deep acceptor level is used to obtain semi-insulating material in this case.

2.2.3 **Non-idealities resulting from compensation**

Horio [3] studied the effect of deep levels in the substrate on turn-on transients in GaAs MESFETs. He found that when deep donors such as EL2 (electron traps) are used to compensate the background conductivity due to shallow acceptors, then drain current overshoot occurs when the FET is suddenly turned on. In material where the background resistivity is due to shallow donors and deep acceptors such as Cr (hole traps) are used as compensation mechanisms, a lag is observed in the drain current transient when the FET is turned on. Lag occurs because the a part of the substrate close to the substrate buffer interface becomes negatively charged under deep pinch-off conditions. Overshoot occurs because a part of the substrate close to the substrate buffer interface becomes positively charged under deep pinch-off conditions.

2.3 **Compensation in GaN buffer layers**

2.3.1 **Origin of the background electron concentration in GaN films**

Under the conditions that are normally used to produce GaN single crystals of good structural quality on either sapphire or SiC by MBE or by MOCVD, the crystal obtained is always weakly n-type. The bulk of device development effort in UCSB has thus far been concentrated on the development

of GaN HEMTs on sapphire by MOCVD. *Why is GaN on sapphire by MOCVD weakly n-type and how is it made semi-insulating?*

GaN epitaxy on sapphire is always performed using a two step process [4]. First, a 15-25 nm thick GaN nucleation layer is deposited at temperatures between 500 and 700C to ensure complete wetting of the sapphire substrates before the temperature was raised to above 1000C for the growth of the main GaN layer. Keller [1] reported the optimum growth conditions of this nucleation layer to obtain the best structural, optical and electrical properties of the GaN epitaxial layer that followed. Structural properties of the epitaxial film are measured by X-ray, photoluminescence and AFM of the surface. A further measure of the crystal quality is the electron Hall mobility. The best n-type GaN films grown at UCSB demonstrated a Hall mobility of 820 cm^2/Vs. The background carrier concentration in this film was $4x10^{16}$ cm^{-3} and the thickness of the film was 4 μm [5]. In general, the electron mobility of the unintentionally doped layer increases when the carrier concentration is lower. A minimum film thickness of 3 μm was necessary to obtain good values of mobility and low background electron concentration, although thicker films resulted in only minor improvements.

2.3.2 **Impurities in GaN - Oxygen**

The background electron concentration in GaN films was attributed to nitrogen vacancies in the early days. Recently, oxygen, rather than nitrogen vacancy has been suggested as the major source of residual electrons [6,7]. The source of oxygen is impurities present in the NH_3 and metal-organic precursors used in MOCVD growth, the residual water vapor in MBE or MOCVD chambers, oxygen impurities leached from the quartz containment vessel often employed in N_2 plasma sources, and in the MOCVD reactor. Water and oxygen present as impurities in the metal-organic precursors and gases can enter the system through

leaks, or during wafer loading. The sapphire substrate (Al_2O_3) is another source, because water is formed during the pre-treatment of sapphire in hydrogen. The donor energy level of oxygen is reported at E_c-0.078eV by Chung [50] and Zolper [48] measured an activation energy of 29meV.

Experiments to identify the source of background native donors were carried out in UCSB, as reported by Keller [17]. The sources of background oxygen impurities are the precursors, trimethylgallium (TMGa), trimethylaluminium (TMAl) and ammonia (NH_3), water and air present during loading, and from the sapphire substrate. Since oxygen impurity from the precursors is inevitable, the problem is reduced to minimizing the contribution from the loading procedure and from pre-treatment of sapphire substrate. A series of variations were tested, which included a)baking the sapphire wafer inside the reactor and ex-situ, and b) flushing the system before growth for different times to flush out moisture introduced during loading and during the sapphire bake. The results of these experiments indicated that both the sapphire bake and the wafer loading contributed to the residual carrier concentration. The lowest background carrier concentrations were obtained by using ex-situ baked sapphire substrates and inserting a long flush time (~ 2 hours) after wafer loading. The lowest background electron concentration obtained was 2.2 x $10^{16}cm^{-3}$.

2.3.3 **Compensation mechanisms in n-type GaN -Incorporation of Carbon.**

The dominant unintentional impurity resulting in acceptor levels in GaN is generally held to be carbon. Carbon, when sitting on a nitrogen site (C_N) is a shallow acceptor: this configuration is energetically favored over incorporation in a Ga site according to theoretical calculations. C_N is generally assumed to be the dominant form of carbon impurity, although some calculations by Boguslawski [8] suggest that carbon is an amphoteric impurity in both GaN and AlN.

Intentional carbon doping is reported to produce n^+ GaN under certain conditions [15]. Carbon incorporation can also lead to self-compensation under certain conditions, as predicted in [8], due to the formation of C_N-C_{Ga} pairs. Carbon has been linked to the yellow luminescence in GaN by several researchers. [10-12]. Circumstantial evidence for this comes from the fact that there is little yellow PL in GaN grown by halide vapor phase epitaxy which employs carbon-free precursors (Ga, NH3 and HCL) [13-14]. It has been suggested that carbon assists in the formation of gallium vacancies which have been identified as the source of yellow luminescence in experiments comparing the results of photoluminescence and positron annihilation studies [9].

2.3.4 **Incorporation of Carbon in GaN - SIMS results**

A comprehensive study of the effect of various growth conditions on the incorporation of carbon and oxygen was carried out in UCSB by Parish and Keller [18]. They found that carbon was most affected by growth conditions. Carbon incorporation was found to decrease with temperature and ammonia flow. The reason for this is believed to be increased conversion of methyl groups to methane thus decrease the amount of carbon available. Carbon incorporation is also reduced by increasing the ammonia flow, which is believed to be due to two reasons, 1) greater hydrogen from the ammonia leads to increased conversion of the methyl groups to stable methane 2) the increased availability of nitrogen species reduces the likelihood of formation of nitrogen vacancies, which are the preferred carbon sites. Carbon incorporation increased with growth rate and Al content: this is believed to be due to the increased precursor concentration. Oxygen incorporation is believed to follow similar trends. However, since the concentration of oxygen is lower than carbon by an order of magnitude, the oxygen content was below the SIMS detection limit and oxygen incorporation

trends could not be established in GaN. In studies of the carrier gas used, carbon incorporation was lower when nitrogen was used as the carrier gas and oxygen incorporation was lower when hydrogen was used as the carrier gas.

2.3.5 **Compensating Impurities in GaN – Threading dislocations**

Because of the large lattice mismatch between GaN and sapphire substrates (14%) (lattice mismatch between GaN and SiC is 3.5%), a very large number of threading dislocations, (TD's), ($5x10^{8}$-$1x10^{11}$) exist in GaN films grown on sapphire substrates. The density of threading dislocations for GaN on SiC substrates is similar to sapphire.

In conventional III-V materials such as GaAs, a TD density higher than 10^{3}-10^{4} prevents operation or leads to extremely rapid degradation of optoelectronic devices [36]. While Nakamura has demonstrated extremely long lifetimes in GaN lasers on low dislocation material [35], LEDs and LASERs work in regular GaN layers with dislocation densities higher by six orders of magnitude than GaAs. In the past, this fact has led many researchers to speculate that these dislocations are not associated with electronic states within the band gap. However several theoretical predictions and experimental observations indicate that dislocations are associated with non radiative (NR) states within the band gap. Recently, [41], it has been argued that the large TD dislocation density does not cripple optoelectronic device operation in GaN for two reasons – 1) much shorter minority carrier diffusion lengths, 50-250nm in GaN [42,43], compared to 1μm in GaAs and 2) the immobility and fixed number of dislocations in GaN, compared to the movement and multiplication of extended defects in GaAs under operating conditions.

Early theoretical calculations by Elsner [44] indicated that pure edge TD showed no deep levels. Subsequent theoretical studies [40] indicated that gallium

vacancy-oxygen impurity (V_{Ga}-O_N) clusters are stably trapped at the dislocation core and these complexes can give rise to deep single and double acceptor levels. It was suggested that these deep acceptor were associated with the yellow level commonly observed in undoped and n-type GaN. Wright showed using density functional theory that edge dislocations have states in the band gap [38,39]. Cathodoluminescence studies indicate that TDs limit the efficiency of band edge luminescence [43] and may also contribute to the broad yellow luminescence [28]. Cathodoluminescence studies in combination with atomic force microscopy shows that TD's act as non-radiative recombination centers [42]. Because TD's manifest as deep levels, they can compensate the dominant background impurity, i.e. they act as electron traps in n-type GaN and hole traps in p-type GaN [31]. By using scanning capacitance microscopy in combination to local C-V studies of unintentionally doped n-type GaN, Hansen [37] showed that TD's were sites of negative charge accumulation. Depending on the charge state of the associated deep levels, the dislocation related traps can form a line of charge and hence affect the transport properties in GaN and in 2DEG.

The spacing of traps along the TD's is determined by the c-lattice constant of hexagonal GaN (5.1A). If there exists a trap site at every atomic plane, this leads to an equivalent trap density of $2x10^{17}cm^{-3}$ for a dislocation density of 10^{10} cm^{-2}. Leung [46] calculated the charge accumulation on TD related trapping sites as a function of the TD density and the background donor concentration and considered Coulomb interactions between TDs and dopants. It was found that for small doping densities all dopants are ionized and depleted by charge transfer to the dislocation defect sites. As dopant density increases, the dislocation sites become charged. The crossover is found to occur at a dopant concentration approximately equal to the volume concentration of dislocation related trap sites

i.e. a donor density of $2x10^{16}cm^{-3}$ for a dislocation density of 10^9 cm^{-2}. Thus dislocation density variation is a major parameter that influences the conductivity of undoped and doped GaN layers.

Keller [29] observed an inverse correlation between electron Hall mobility and dislocation density. The effect of dislocation density on electron mobility has been theoretically modeled by Look [45] and Weimann [24] and Ng[30]. The results of Weimann and Ng demonstrated that dislocation scattering must be included in mobility analysis when TD density is > 10^8cm^{-3}. Look rigorously calculated the scattering resulting from the potential due to vertical line charge within the framework of the Boltzmann transport equation. It was shown that dislocation related scattering is dominant below a certain electron concentration, while above that value of n, ionized-impurity scattering is more important. This explained the reason that mobility in some GaN epilayer samples displayed a maximum with respect to electron concentration.

2.3.6 **Development of semi-insulating films at UCSB**

Hence the strategy for growing a good buffer from the trap point of view was to a) minimize the concentration of unintentional donors (mainly oxygen) by optimum wafer loading and wafer preparation procedures b) adjust the incorporation of compensating acceptors (carbon, threading dislocations) by optimum choice of growth rate, growth temperature, growth pressure, and carrier gas so that the amount of added donors was just compensated. The dominant compensating acceptor in material grown at UCSB is believed to be a dislocation related defect. The density of states is unknown but it must exceed the background donor concentration of ~ $4x10^{16}$ cm^{-3}.

2.4 **Improvement of AlGaN layer**

From the trapping point of view, the presence of deep level impurities in the AlGaN needs to be minimized. Carbon and oxygen are the main impurities that can give rise to deep levels in the AlGaN. In AlGaN, isolated oxygen is believed to make a transition to a DX center in $Al_xGa_{1-x}N$ with increasing Al mole fraction [19-21] as the oxygen moves from a shallow donor in GaN to a deep trap in AlN**.** Carbon is believed to be an amphoteric impurity in AlGaN [8] but little is known about the role of carbon in AlGaN. A quick calculation shows that in a 200A thick AlGaN layer, the density of deep traps needed to compensate a sheet charge density of $1x10^{13}$ cm^{-2} is $5x10^{18}$ cm^{-3}. Impurity concentrations well below $5x10^{18}$ cm^{-3} are not expected to significantly impact current collapse.

The growth of AlGaN layers first concentrated on improvement of structural quality of the AlGaN. Initially, growth of AlGaN layers with mole fractions above 20% exhibited a grain like structure. Later work performed by Keller and workers at UCSB [22] showed that grain formation could be prevented by ensuring a high surface mobility of metal species. Under optimized conditions, coherently strained AlGaN layers could be grown up to 50% Al composition [51].

Under these optimal growth conditions for AlGaN, Parish and Keller [18] conducted a study of the incorporation of carbon and oxygen into the AlGaN layers. They found that both carbon and oxygen content increase with Al content. The incorporation trends of C and O in AlGaN are similar to the trends in GaN. The concentrations of carbon and oxygen are both higher in AlGaN, in the mid to high 10^{17} range. However, these concentrations are believed to be too low to cause significant current collapse. The growth parameters of the AlGaN were hence chosen so that 1) structural problems such as cracking and grain formation were minimized and 2) Impurity (C,O) incorporation was minimized.

2.5. **Impact of threading dislocation density on current collapse in GaN HEMTs**

In the optimizations discussed so far, the density of bulk traps due to unintentional impurities and point defects was minimized. However, as discussed earlier in section 2.3.5 there exists a very large density of threading dislocations (TD) in GaN layers grown on sapphire substrates. In order to verify if traps are associated with the dislocations, a comparison between the characteristics of HEMTs fabricated on GaN layers with high TD density and low TD was made. This experiment is described in the following sections.

Experimentally, the density of threading dislocations in GaN is reduced by the technique of lateral epitaxial overgrowth or LEO [32-34]. In this technique, the "seed" GaN layer grown on lattice mismatched substrate is partially masked by an amorphous layer of SiN or SiO_2. Regrowth occurs through openings in the masking layer such that existing TD's are prevented from propagating in the vertical direction by the masking layer. Laterally overgrown GaN on the masked areas is dislocation free since the threading dislocations do not propagate laterally. In this way areas with high TD density and low TD density can be located next to each other on the wafer as shown in **Fig 2.5**.

The main goal of data presented in this section is to determine whether TD related traps were the dominant source of current collapse. A comparison between the characteristics of HEMTs fabricated on regular high TD GaN and on LEO GaN on the same wafer is presented.

2.5.1 **Fabrication of HEMTs on LEO GaN**

A 2 micron thick GaN template was grown on sapphire substrate by MOCVD. A 2000A thick e-beam deposited SiO_2 mask layer was patterned in stripes 15 mm wide separated by 5 mm. After patterning selective epitaxial growth of GaN was initiated on the window regions of exposed GaN. Lateral overgrowth of GaN across the SiO2 mask occurred as shown in **Fig 2.5**. The LEO GaN was grown under conditions that typically resulted in a TD density below $10^6 cm^{-2}$ compared to 10^8-10^9 in standard GaN. At the time of this work, the coalescence of the wing regions was not optimized. Hence over most of the wafer, coalescence was left unfinished, leaving a very small gap between the wings. The device layer structure as shown in **Fig 2.6(a),** was then grown on this LEO template. The LEO material was unintentionally doped and n-type as grown, probably due to auto doping from the SiO_2 mask occurring during overgrowth. A 3 um thick insulating FET buffer layer was grown to separate the device layers from the underlying n-type material. HEMTs were fabricated on adjacent regions of LEO GaN and regular GaN such that a fair comparison could be made between the two regardless of the absolute quality of the devices obtained. **Fig 2.6(b)** shows the plan view of the wafer after device fabrication is complete showing the location of the HEMTs on regular GaN beside HEMTs on LEO GaN. **Fig 2.6(c)** compares AFM pictures of surface morphology of the AlGaN grown on regular GaN and LEO GaN, showing that concentration of dislocation mediated defects is much smaller on LEO GaN.

2.5.2 **Device Results on LEO and regular GaN**

Fabricated devices showed lower current densities than the normal range (700-800 mA/mm) for similar devices grown at that time. This was ascribed to the non-optimized growth of AlGaN and FET buffer layers under these conditions.

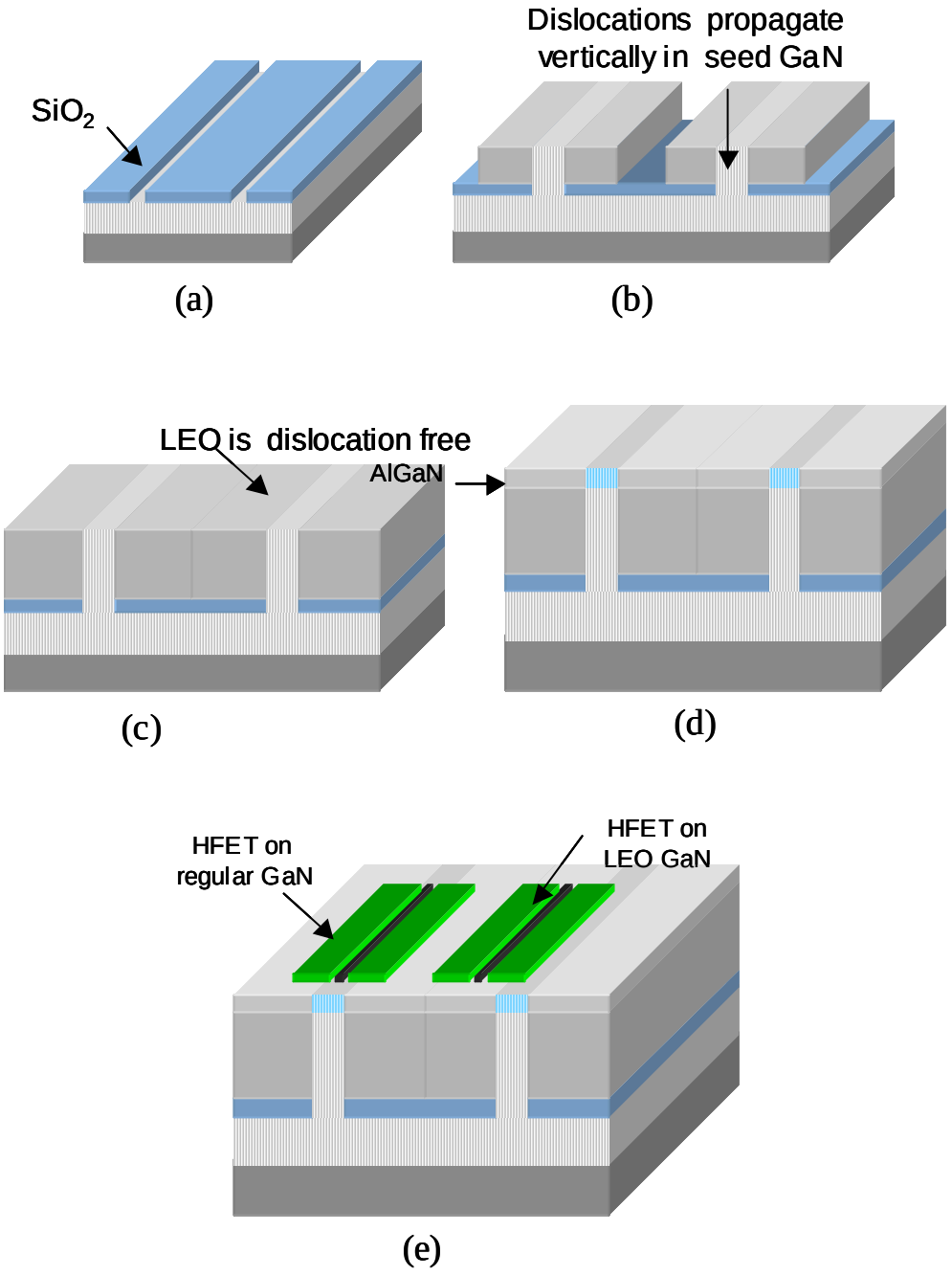


Fig 2.5 . LEO wafer growth process

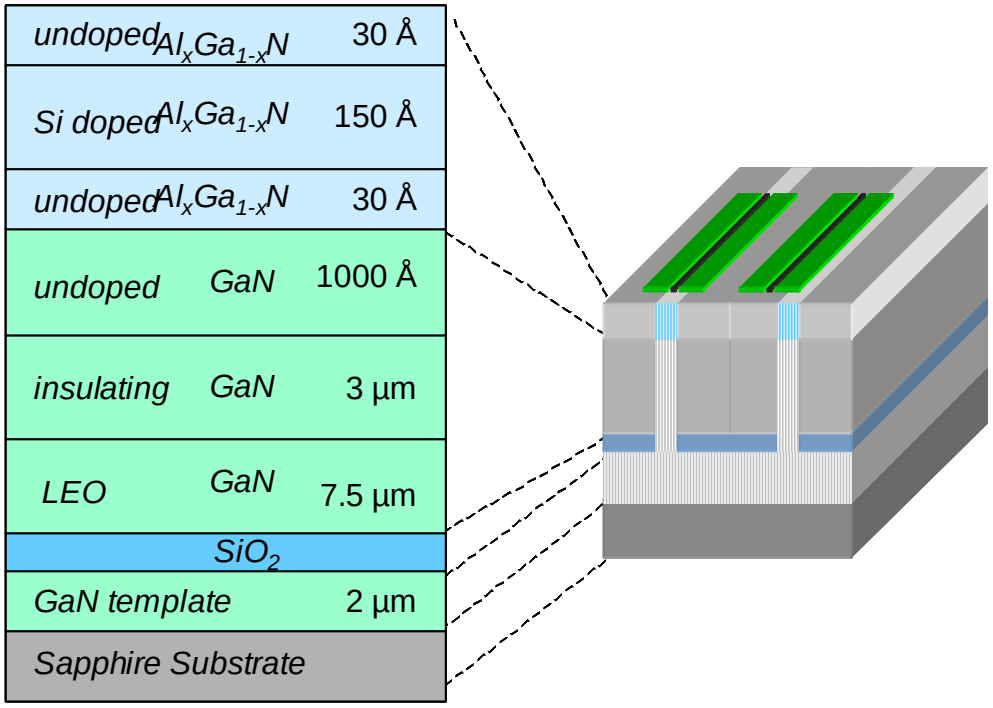


Fig 2.6 (a). LEO device layer structure

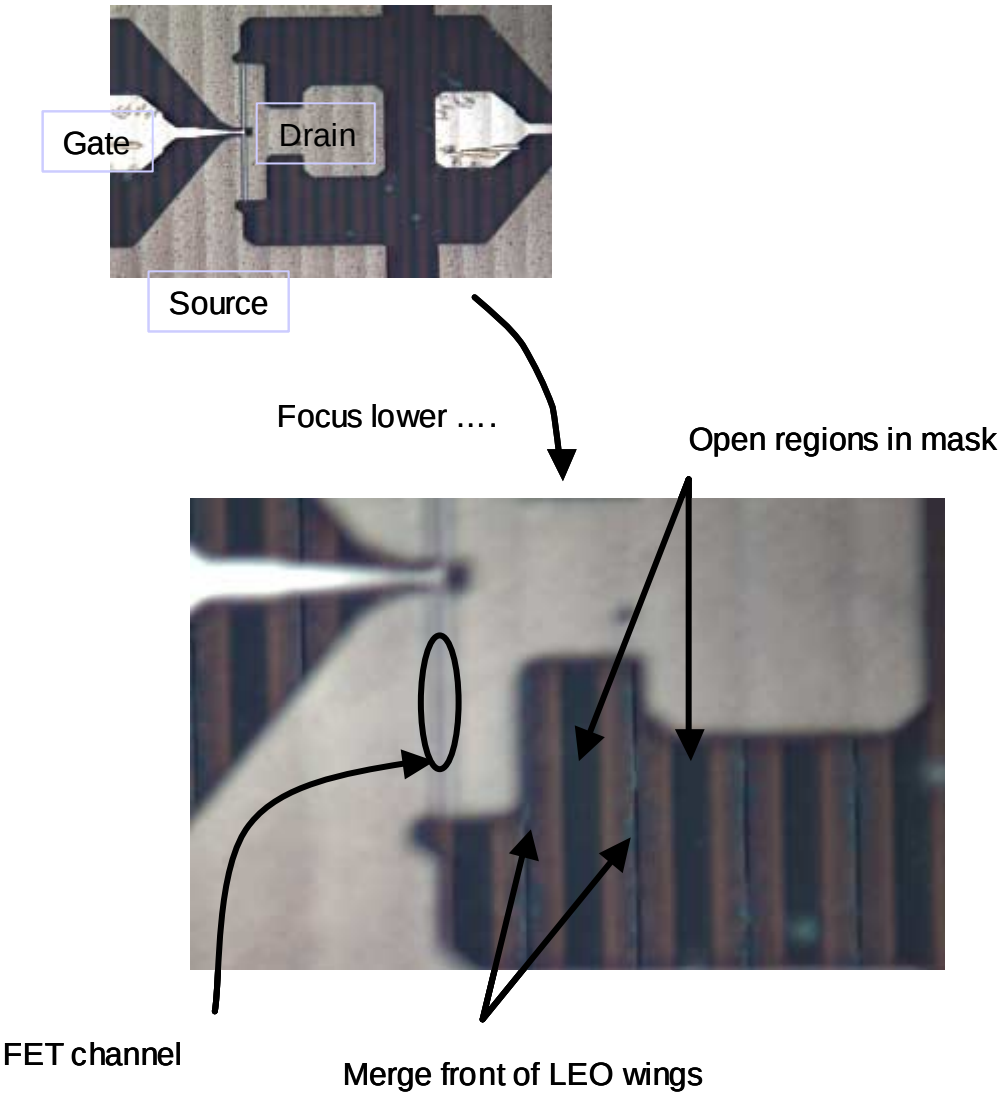


Fig 2.6 (b). Plan view of LEO device layout. This figure shows a device on LEO wing.

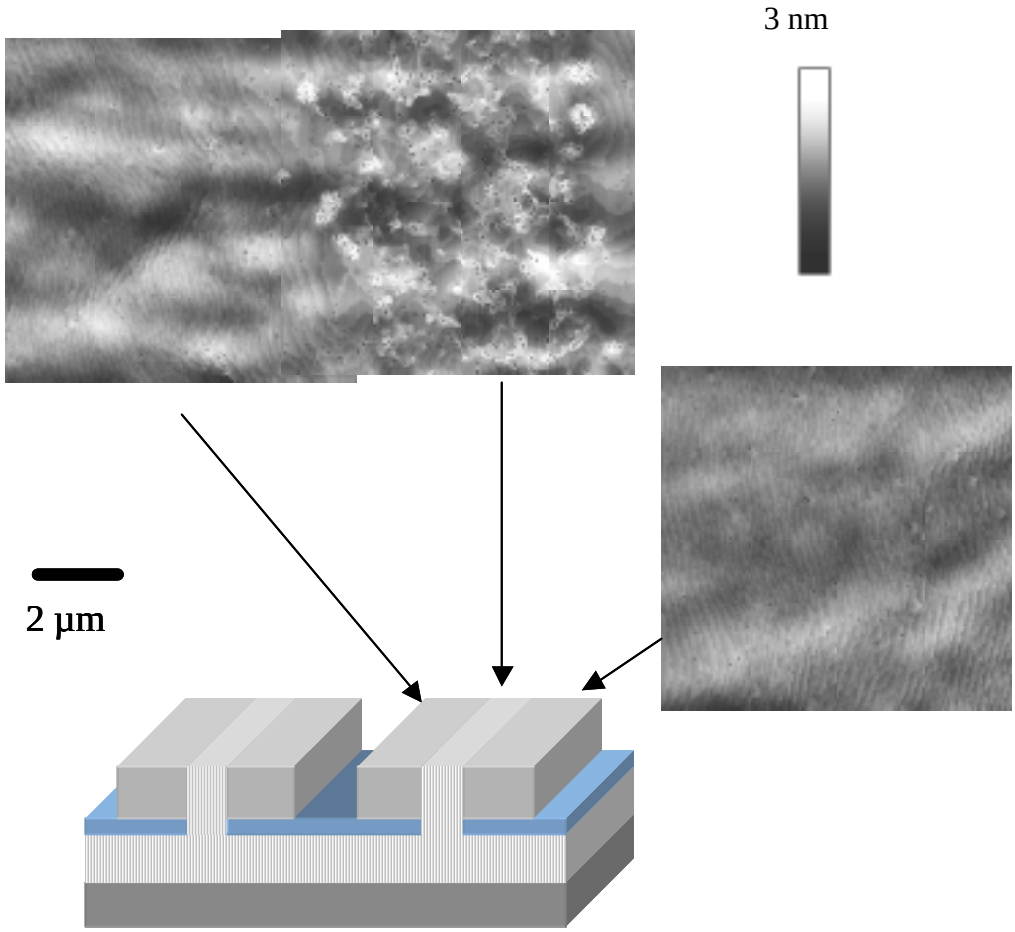


Fig 2.6(c) Dislocation mediated structural defects absent in $Al_{0.3}Ga_{0.7}N$ on LEO GaN

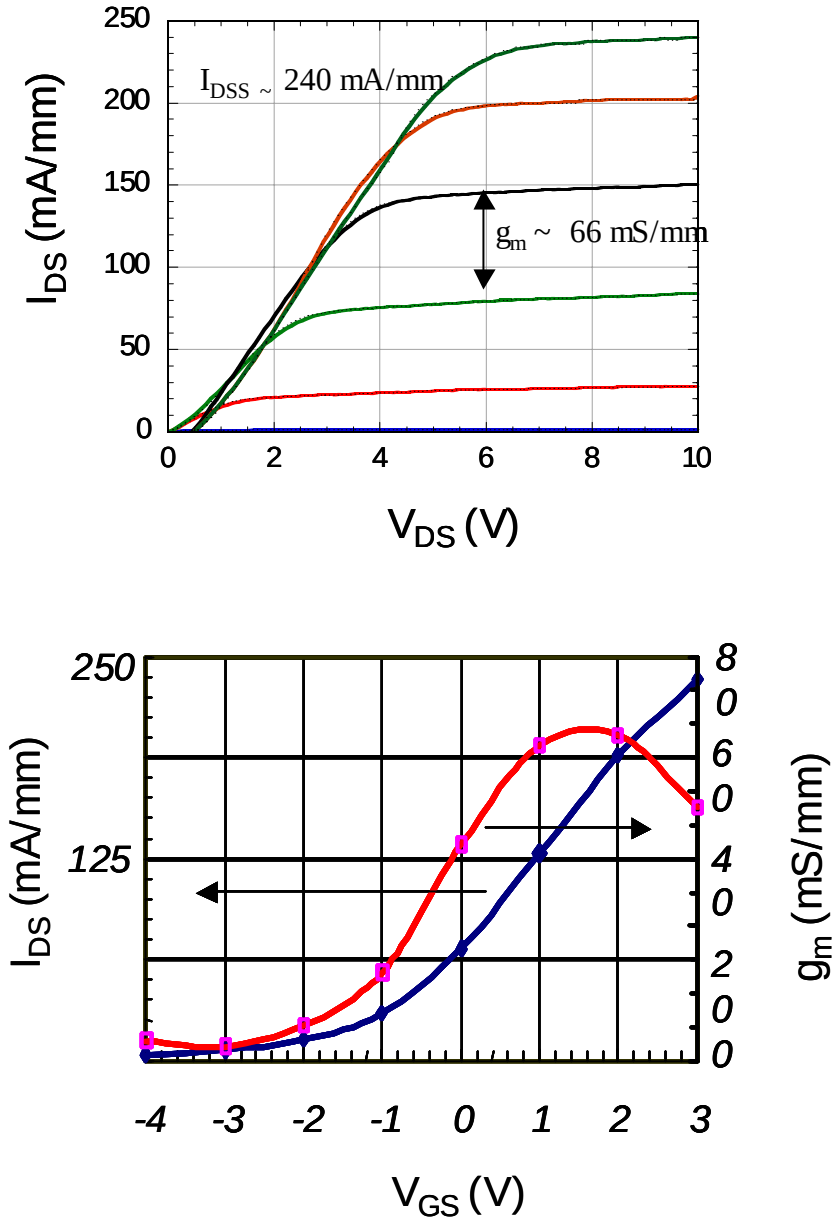


Fig 2.7. HFETs on LEO and regular GaN showed similar DC I.V. characteristics.
Typical max I_{DS} ~ 250 mS/mm, max g_m ~ 60 mS/mm.

Maximum current densities were 240mA/mm and transconductances were ~ 66 mS/mm. The I-V characteristics of the HEMTs on LEO GaN and on regular GaN were remarkably similar, as shown in **fig 2.7**.

As the LEO wings were not coalesced, contact pads suitable for microwave probing could not be laid out. However, pulsed I-V measurements using a Sony Tektronix Curve Tracer made using the DC test pads showed that both types of HEMTs suffered from significant current compression as shown in **Fig 2.8**. The extent of current compression was similar for both LEO HEMTs and regular HEMTs, thus indicating that dislocation related traps were not the dominant source of current collapse. Therefore the current collapse could either come from the highly compensated buffer layer, the AlGaN layer, or the AlGaN surface.

The gate diode characteristics of HEMTs on LEO GaN were much improved compared to HEMTs on regular GaN. HEMTs on LEO GaN consistently showed much lower (up to two orders of magnitude) lower leakage current. The forward and reverse characteristics are shown in **fig 2.9**. These results are in agreement with those of Kozodoy [36] who obtained reverse leakage current in p-n junctions on LEO material lower by three orders of magnitude than in p-n junctions on regular high TD density GaN and Parish [48] who obtained leakage currents lower by six to eight orders of magnitude in AlGaN based p-i-n UV solar photodetectors fabricated on LEO GaN. The impact of threading dislocation density in 2DEG on HEMT devices has not been well studied, mainly because of the difficulty of device fabrication on such non-planar material and in controlling unintentional Si doping arising from the SiN or SiO_2 mask material. Growing a FET structure in LEO material is harder to achieve than in regular GaN because the uncontrolled Si doping from the silicon nitride mask makes obtaining a semi-insulating layer difficult. In fact, so far there has

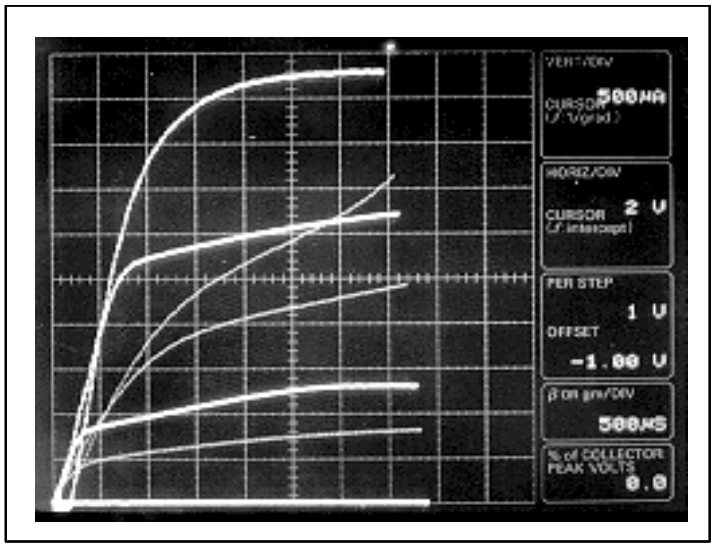


Fig 2.8. Pulsed measurement on HEMTs on LEO GaN showing significant current collapse. The bright lines are swept DC curves. The lighter lines are pulsed curves, with V_{gs} starting at pinch-off.

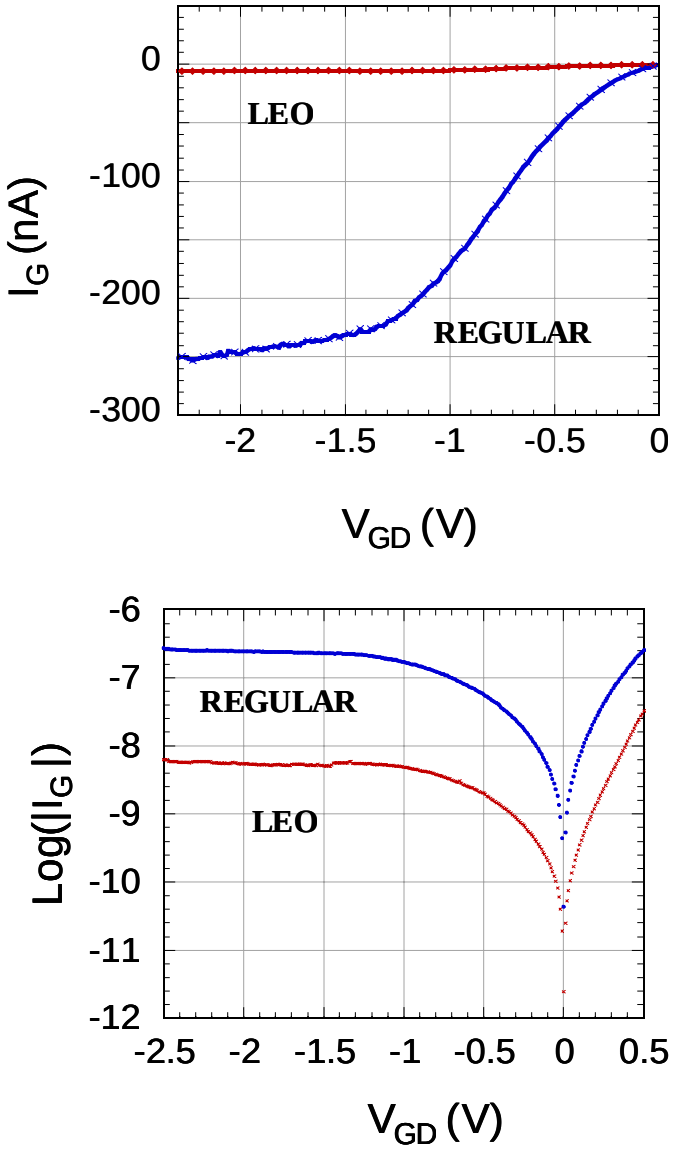


Fig 2.9. Reverse gate leakage of HFETs on LEO GaN is consistently lower than HFETs on regular GaN

been only one report of experimental data on the impact of reduced TD density on the properties of HEMT structures on GaN grown using LEO techniques [47].

2.6 **Conclusions**

The result of the improvement of the material quality and efforts aimed at minimizing the trap densities in the AlGaN and GaN layers can be seen in **fig 2.10**. The data shows the best power results obtained over the time period 1995-2000. As material quality improved, the average power results improved over this period. Significant improvements in material quality , such as the improvement in buffer quality and improvement of the AlGaN layer are indicated on the graph. The highest value shown in **fig 2.10** is obtained due to a further improvement in surface processing which is discussed in the next chapter. As can be seen from the data presented in this chapter, minimization of defect density in the buffer and the AlGaN did not eliminate the problem of current collapse. HEMTs on LEO material with significantly lower threading dislocation density (up to three orders of magnitude lower) still displayed significant current collapse. Despite the improvements in the quality of the semi-insulating GaN and the AlGaN layers, the performance of the FETs was still well below the maximum available from these devices. These facts indicated that the dominant source of current collapse remained to be eliminated. The only source of non-ideality left is the free surface of the AlGaN. In the next chapter, the nature of this free surface in GaN material system is discussed.

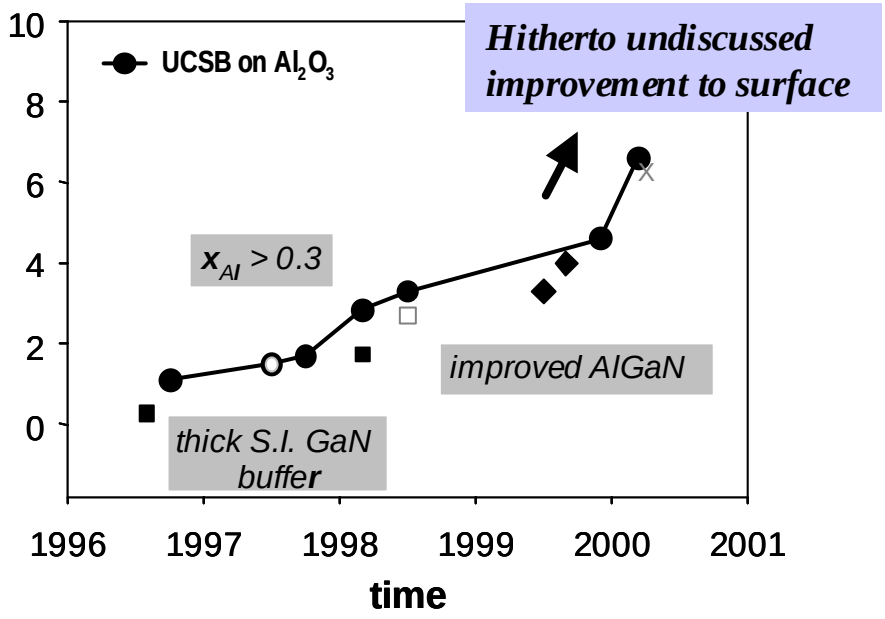


Fig 2.10 Best power data obtained over the period 1995-2000. Significant improvements are shown as they occurred in time. The arrow at the end shows the power result obtained as a result of improved surface processing technique.

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Chapter 3

The importance of the free AlGaN surface

3.1 Introduction

From the previous chapters, it is clear that despite improvements in bulk GaN and AlGaN material, there remained a dominant source of current collapse that was not clearly identified. The one variable that has not been investigated so far is the free surface of the device. Why is this free surface important? And how is it different from free surfaces in other III-V systems such as GaAs/AlGaAs? In this chapter, arguments are advanced to show that the free surface of the AlGaN is fundamentally different from conventional III-V materials and plays an extremely important role in determining the properties of the HEMT.

Measurements of surface potential using floating gates in GaN HEMTs are presented. These measurements indicate that the surface in GaN HEMTs can become negatively charged thus indicating that surface states exist in these devices. The presence of very large polarization fields in the GaN system is a fundamental difference between conventional III-V semiconductors and GaN. It is shown that the large polarization fields necessarily lead to the formation of charged surface states and that these charged surface states are critical to the origin of the 2DEG in the HEMT structure in GaN. The nature of the surface states in GaN HEMT structures is discussed.

3.2 Measurement of surface potential

3.2.1 Floating gate measurement technique

Fig 3.1 shows the device structure and layout. The AlGaN/GaN layers were grown by metal organic chemical vapor deposition (MOCVD) technique on sapphire substrate. Fabrication began with lithography to define source drain

regions and ohmic metal (Ti/Al/Ni/Au) deposition. a 2.5 μm semi-insulating GaN buffer layer. A 20 Å undoped $Al_{0.25}Ga_{0.75}N$ spacer layer was grown next, followed by a 150 Å thick Si doped donor layer. An undoped 30 Å cap layer completed the structure. The source drain contacts were annealed in a rapid thermal annealer at 850°C for 30 seconds. Gate lithography and deposition of Schottky metal gate (Ni/Au) followed this. Devices were isolated by etching mesas using Cl_2 reactive ion etching (RIE).

To obtain the potential distribution in between the gate and drain, floating Schottky gates were located between the gate (hereafter referred to as the active gate to distinguish it from the floating gate) and drain. The floating gates are defined at the same mask level as the active gate. L_1, the separation between the gate and floating gate and L_{FG}, the length of the floating gate, were variable parameters.

Fig 3.2 shows the measurement schematic. A variable reverse bias, (V_{GD}), is applied on the active gate, the drain is maintained at ground potential and the source is left floating. The active gate leakage current (I_G) and the voltage on the floating gate (V_{FG}) are monitored as V_{GD} is varied. The voltage on the floating gate is monitored using a high impedance voltage monitor whose input impedance is greater than 10^{12} Ω (Hewlett Packard 4145B Semiconductor Parameter Analyzer). This ensures that the measurement process itself does not affect the potential of the floating gate.

3.2.2 Observation of lateral extent of depletion region

Fig. 3.3(a) shows a typical trace obtained from the measurement. As seen, the potential of the floating gate exhibits two different regimes depending on the value of V_{GD}, the bias on the active gate. At a certain value of V_{GD} the potential on the floating gate makes the transition from regime to the other. We designate

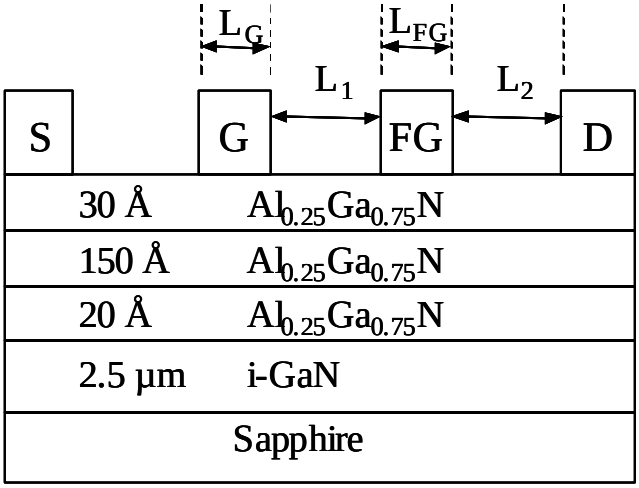


fig 3.1 Device structure and layout

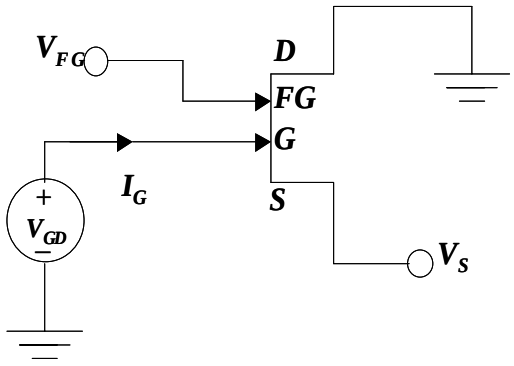


Fig 3.2 measurement schematic in floating gate measurement.

the active gate voltage where the transition occurs as V_T, the transition voltage. In regime 1, [$|V_{GD}| < |V_T|$], as $|V_{GD}|$ is increased, the potential of the floating gate remains at the drain potential (or ground): in regime 2, [$|V_{GD}| > |V_T|$], the potential of the floating gate increases almost linearly with increase in $|V_{GD}|$. In regime 2, the change in V_{FG} is a high (between 0.6 and 1) fraction of the change in V_{GD}. **Fig 3.3(b)** shows measurement traces from three different devices. These devices had different values of L_1 but the same L_{FG}. All three traces exhibit the same general behavior, and the transition voltage V_T increases with L_1. These observations are explained in the following way.

In regime 1, as the reverse bias on the active gate is increased, the depletion region extends laterally from the drain edge of the gate towards the drain. However the edge of the depletion region does not extend to the floating gate. The floating gate is electrically connected to the drain. The potential of the floating gate potential therefore remains at the drain potential, which is grounded.

In regime 2, the depletion region edge extends up to and beyond the floating gate. Here the floating gate is no longer electrically connected to the drain. The potential of the floating gate is now linked to the gate potential and is established by the potential drop across that section of the depletion region that exists between the gate and the floating gate, including the potential drop underneath the floating gate. The transition to regime 2 occurs when the edge of the depletion region extends beyond the floating gate: we denote the gate to drain potential at this point as the transition voltage, V_T.

3.2.3 Transition Voltage – V_T.

The magnitude of V_T is the voltage supported by a depletion region of length L_1. In order to establish that this drop underneath the floating gate did not significantly affect the measured transition voltage, V_T, devices with the same

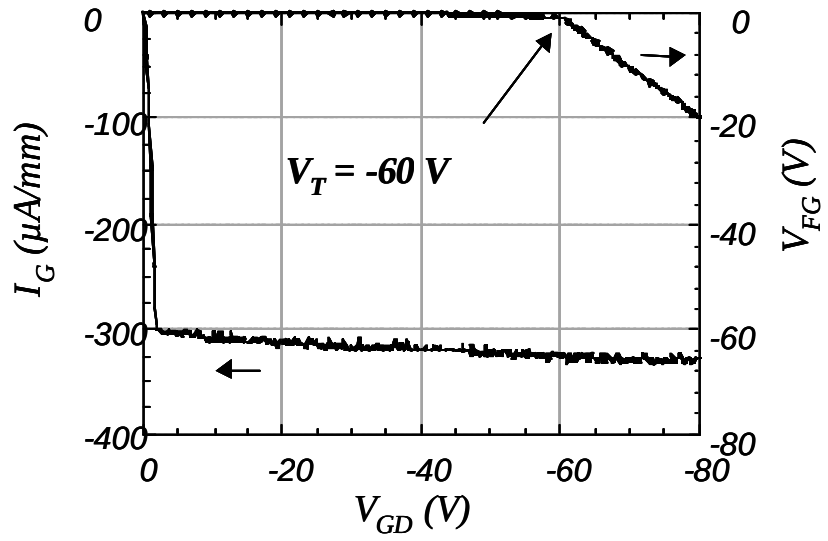


Fig 3.3 (a) a typical trace obtained from the measurement

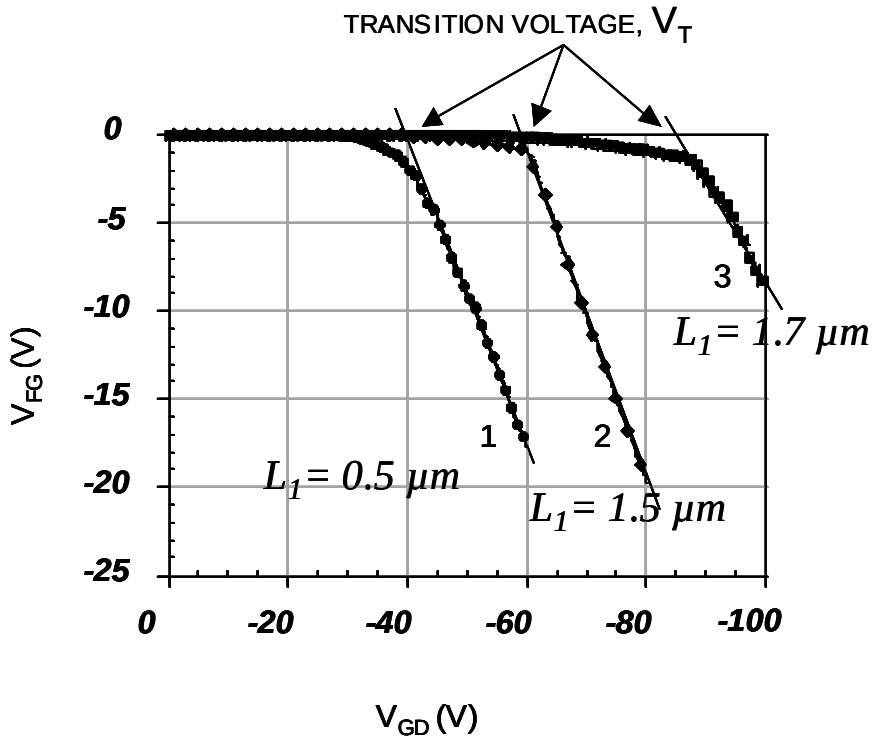


Fig 3.3 (b) Three different traces obtained from the measurement on three different devices with different values of L_1.

value of L_1 but different L_{FG} (1 to 6 μm) were built and tested. V_T was found to increase with L_{FG} (2-3 V increase in V_T per μm increase in L_{FG}). This dependence of V_T on L_{FG} is small compared to the magnitude of V_T. Hence, when L_{FG} is small i.e. 1 μm, the magnitude of V_T is assumed to be the voltage supported by a depletion region of length L_1. This conclusion is confirmed by three observations, a), V_T does not depend upon L_2, but only on L_1, b), V_T does not significantly depend on the value of L_{FG}, the length of the floating gate, and c), beyond V_T, the floating gate voltage rises almost linearly with V_{GD} because a large percentage of the additional voltage, i.e. V_{GD}-V_T, is now supported between the floating gate and the drain.

A plot of V_T, as a function of L_1, is shown in **Fig. 3.4(a).** Note that is equivalently a plot of the lateral extent of the depletion region as a function of gate to drain reverse bias. The lateral extent of the gate depletion region is very large and increases with the magnitude of the reverse bias on the gate. Hence the average electric field across the depletion region does not increase rapidly with increasing reverse bias. This explains why the breakdown voltage of these devices should increase with gate to drain spacing.

Off state breakdown was characterized by gate drain diode measurements. As shown in **Fig 3.4(b),** the breakdown voltage was found to increase with gate to drain spacing. The data in **Fig 3.4(b)** is for devices with no floating gates. The maximum breakdown voltage of 405 V was obtained at a gate to drain separation of ~7 microns.

3.2.4 Existence of surface states

The large extension of the depletion region that is observed in these AlGaN/GaN HFETs allows high reverse voltage to be supported without breakdown. For the depletion region to extend as observed, it is necessary that

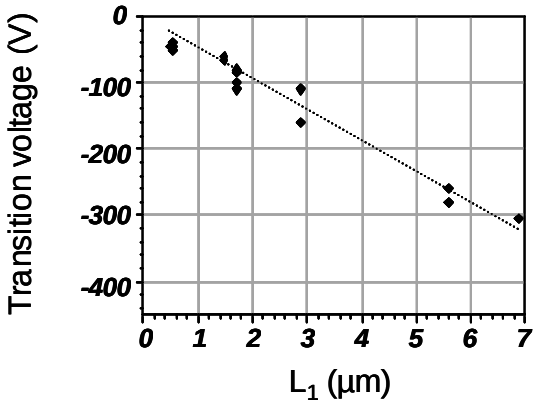


Fig. 3.4(a). A plot of the lateral extent of the depletion region as a function of gate to drain reverse bias. The dotted line shows an approximately linear dependence.

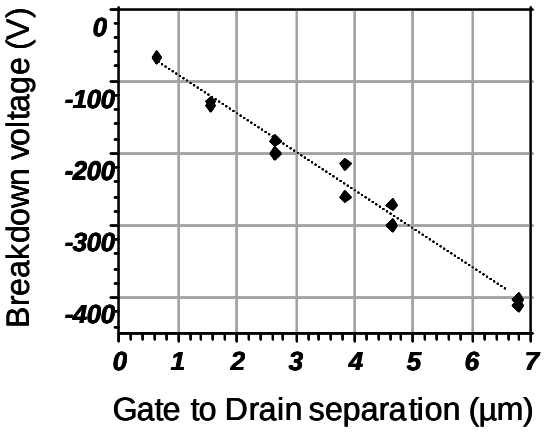


Fig. 3.4(b). A plot of the gate drain breakdown voltage dependence on the gate drain separation. The dotted line shows an approximately linear dependence

there must exist negative charge in between the gate and drain: this negative charge effectively subtracts from the positive ionized donor density. The negative charge can arise from negative surface charge in between the gate and drain or from a positive donor ion accepting an electron to become charge neutral. These experiments provided the first direct evidence that surface potential in between gate and drain was made negative when gate drain diode was strongly reverse biased. These observations naturally lead to the question of how such a surface negative potential might arise. It is proposed that there exist surface states in the AlGaN and that these states accept electrons, becoming negatively charged and hence a negative surface potential is measured. Before further evidence is presented that there exist surface states in AlGaN, surface states in III-V semiconductors are briefly discussed.

3.3 Surface states in semiconductors

3.3.1 The nature of the free surface: Surface states

The surface of a crystal interrupts the perfect periodicity of the crystal lattice. The layer of atoms at the surface has unterminated or “dangling” bonds. It is hence easy to imagine that at the surface of the crystal, the band structure can be modified and there can now be states in the otherwise forbidden energy gap. These states are localized and exist only at the crystal surface. There exist two kinds of these surface states, “intrinsic” states and defect related states.

3.3.2 Intrinsic surface states

The term “intrinsic” refers to the fact these states would exist in an ideally perfect surface. They correspond to solutions of Schrodingers equations with energy levels within the forbidden gap and to imaginary values of the wave vector **k**: the wave functions are evanescent waves which decay exponentially with

distance and hence exist only at the surface. These were first predicted by Tamm and Shockley **[1]** and are sometimes referred to as Tamm-Shockley states. The surface state wave functions are drawn from the valence and conduction band states of the crystal and so the densities of states in the valence and conductions bands are decreased close to the surface. Hence the surface of the crystal is electrically neutral only if the band of surface states is partly filled. The donor and acceptor like nature of the states is dependent on their origin. The states drawn from the conduction band are initially empty, they are capable of accepting electrons, hence they are acceptor-like. The states drawn from the valence band are initially full, they are capable of donating electrons and hence are donor-like. This is a reversal of the usual positions of donor and acceptor levels with respect to the band edges, since surface states close to the valence band are donor like and states closer to the conduction band are acceptor like. There can now be defined a surface neutral level ϕ_0 which is the level to which the surface states are filled when the surface is electrically neutral. States above ϕ_0 are acceptor-like and states below ϕ_0 are donor-like. Hence if states below ϕ_0 are empty, the surface has a net positive charge: if states above ϕ_0 are full, the surface has a net negative charge. **Fig 3.5** shows the band diagram at the surface showing the surface neutral level.

3.3.3 Extrinsic surface states

The second kind of surface state is referred to as “extrinsic” surface state. These states are caused by surface point defects or impurities at the surface, formed during crystal growth or in subsequent device fabrication processes such as metal evaporation. Spicer **[2]** proposed the “defect model” of surface states in III-V semiconductors to explain the observed pinning of the surface Fermi level in III-V semiconductors. In GaAs, several measurements on atomically clean [110]

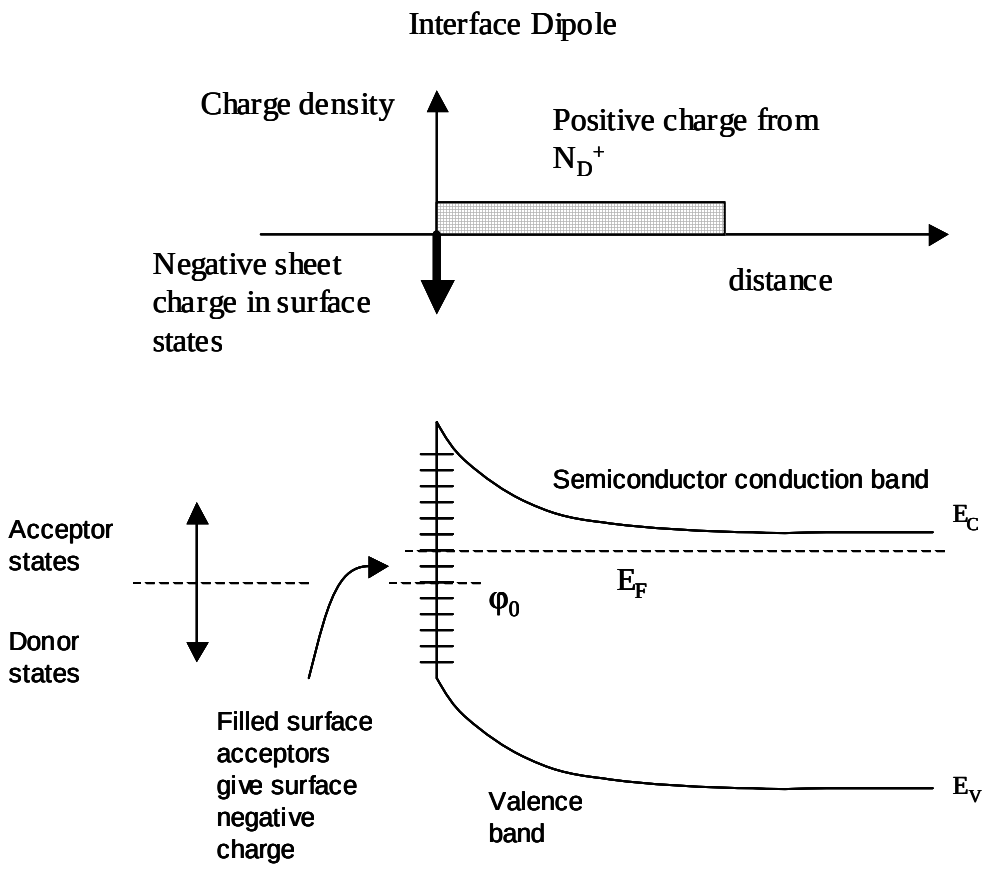


Fig 3.5. Band diagram at the surface showing the surface Tamm Shockley states in an n-type semiconductor and the neutral level φ_0.

surfaces showed that no intrinsic surface states exist **[3,4]**. This is thought to be because of surface relaxation, whereby the full As surface states and the empty Ga surface states move out of the gap, leaving no states in the gap. The absence of surface states in clean high quality [110] surfaces means that there should be no pinning of Fermi level at the surface due to intrinsic surface states. However, measurements made by photoelectron spectroscopy on *in situ* deposited metals on vacuum cleaved [110] surfaces indicated that Fermi level pinning occurred in both p and n type GaAs **[4]**. These observations were explained by Spicer [**2**] who postulated the creation of "*defect states*" at the surface. Such defect states are referred to as "*extrinsic"* surface states" and are described below.

. In Spicer's model of the GaAs surface, native defects such as vacancies and antisites are formed during the process of metal deposition and during the exposure of the surface to oxygen. Vacancies resulting from a missing cation, V_{Ga} were assigned as donors, and vacancies resulting from a missing anion, V_{As} were assigned as acceptors. It was suggested that the true defects are more likely to be antisites and complex defects rather than simple vacancies. Spicer's model is currently widely accepted in explaining the observed Fermi level pinning in III-V semiconductors. **Fig 3.6** shows the distribution of surface states in Si and three III-V (GaAs, GaSb, InP) compounds as proposed by Spicer **[2]**.

3.3.4 Ionicity of the semiconductor

What determines whether a given semiconductor will have surface states? This was studied by Kurtin **[5]**. It was proposed that there was a strikingly abrupt transition in the Fermi-level-stabilization property of compound semiconductors depending on the degree of ionicity of the bond between the constituent atoms. The difference in electro negativity, (ΔX), between the two component elements was used as a measure of the degree of ionicity of the bond. The Schottky barrier

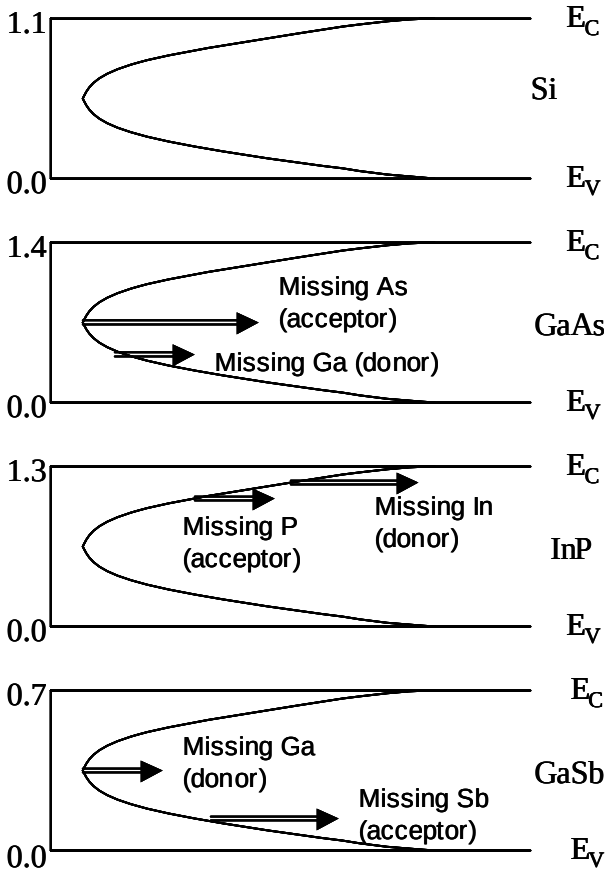


Fig 3.6 Spicer model of surface states in GaAs, InP, GaSb and Si

height of various metals on a semiconductor was plotted as a function of electro negativity of the metal. The slope S of a straight line fitted to the barrier data is inversely correlated to the extent of Fermi-level stabilization.

$$S = d\phi_B/d\phi_M$$

A value of S close to 1 indicates that the surface barrier is directly related to the metal work function, indicating an absence of surface states. A low value ($S<<1$) indicates that the surface barrier is very weakly dependent on the metal work function, or that surface pinning determines the barrier height. Kurtin plotted the index S as a function of the electro negativity difference, ΔX, for various compound semiconductors, He obtained a correlation between the electro negativity difference and the index S. It was found that for strongly ionic compounds, where $\Delta X > 0.4$, S was close to 1 and for more covalent compounds, where $\Delta X < 0.4$, the index S was closer to 0. For GaN, $\Delta X > 1$, and is hence seen to fall into the strongly ionic category , indicating that surface states should not be dominant in this material system. A subsequent study by Schluter **[6]** cast some doubt on the abrupt division of semiconductors into ionic and covalent, but it is generally held that the more ionic a crystal is, the less likely it is to have surface states.

It therefore appears that there must be some other factor that has not been taken into account in predicting the nature of the surface of the GaN crystal. ***This hitherto unconsidered factor is the existence of polarization induced fields in GaN/AlGaN hetero and homo structures.*** In the next section, it is shown that the presence of the polarization fields necessarily leads to the existence of positively charged donor-like surface states at the free surface of the AlGaN in an AlGaN/GaN heterostructure.

3.4 Polarization Fields in AlGaN/GaN

3.4.1 Spontaneous polarization

Spontaneous polarization refers to the built in polarization field present in an unstrained crystal. This electric field exists because the crystal lacks inversion symmetry and the bond between the two atoms is not purely covalent. This results in a displacement of the electron charge cloud towards one of the atoms in the bond. In the direction along which the crystal lacks inversion symmetry, the asymmetric electron cloud results in a net positive charge located at one face of the crystal and a net negative charge at the other face. The spontaneous polarization coefficient is the parameter that characterizes the strength of the spontaneous polarization electric field.

The electric field and charge sheet present in a Ga-face crystal of GaN and AlGaN grown on c-plane, purely due to spontaneous polarization is shown in **fig 3.7 Fig 3.8** shows the values of the spontaneous polarization coefficients in the GaN material system **[7]**.

3.4.2 Piezoelectric polarization

Piezoelectric polarization is the presence of a polarization field resulting from the distortion of the crystal lattice. Due to the differences in lattice constants of AlN and GaN, AlGaN layers grown pseudomorphically on GaN buffer layers are compressively strained as shown in **Fig 3.9(a)**. Due to the large values of the piezoelectric coefficients, this strain results in a charge sheet at the two faces of the AlGaN layer. **Fig 3.9(b)** shows the values of the piezoelectric coefficients in GaN and other III-Vs **[7]**. Note that the values of the polarization coefficients are significantly larger than those in GaAs and InP material systems. The electric field and charge sheet present purely due to piezoelectric polarization in an AlGaN/GaN heterostructure grown on c-plane sapphire, in Ga-face crystal is

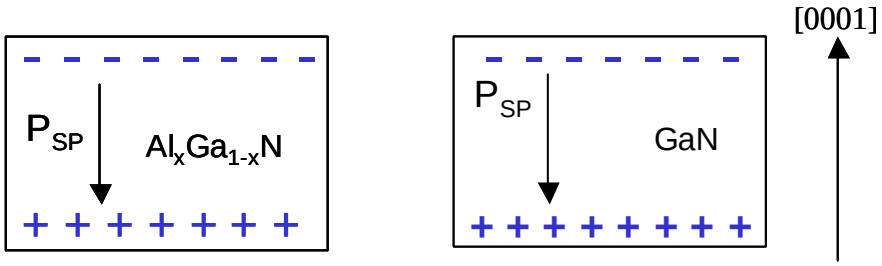


Fig 3.7 Electric field and charge sheet present due to spontaneous polarization only in GaN and AlGaN crystals grown on c-plane in a Ga-face crystal.

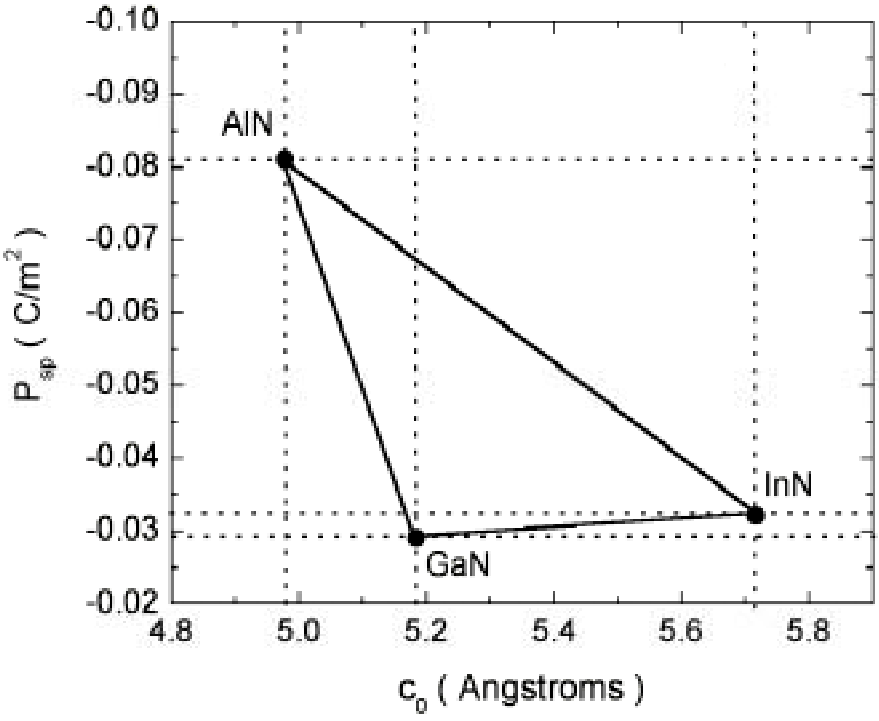


Fig 3.8 Spontaneous polarization coefficients in the GaN system.

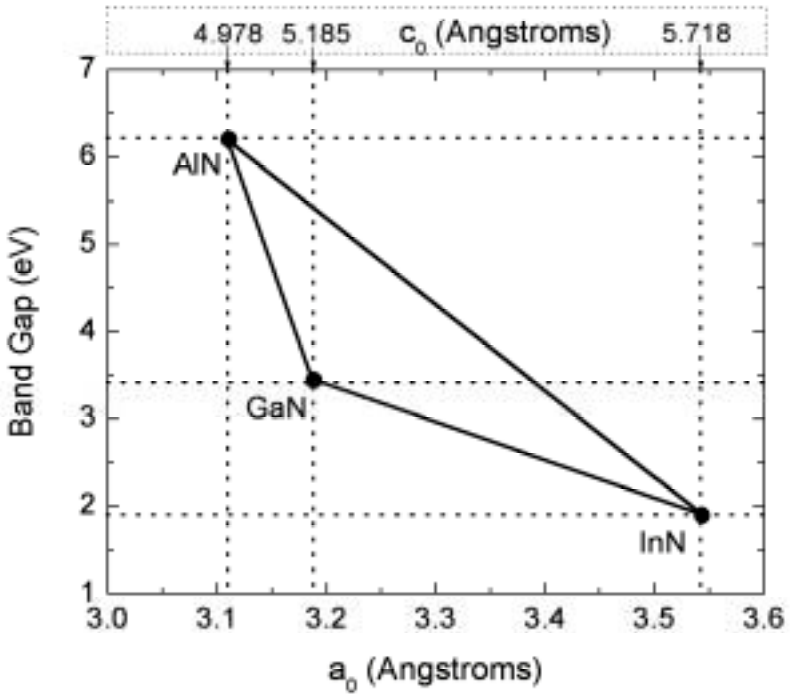
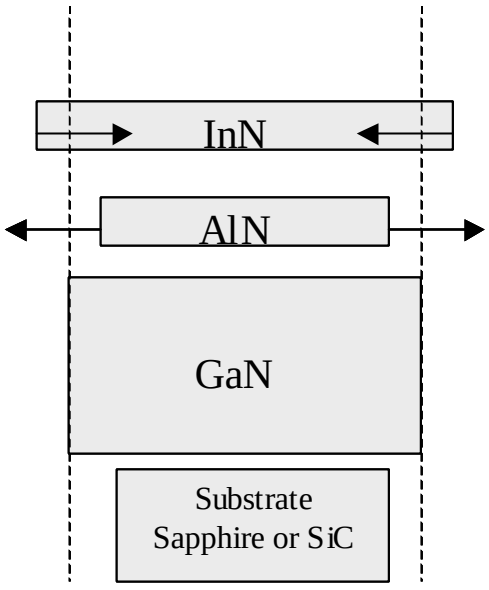


Fig 3.9 (a) Strain in an AlGaN/GaN structure



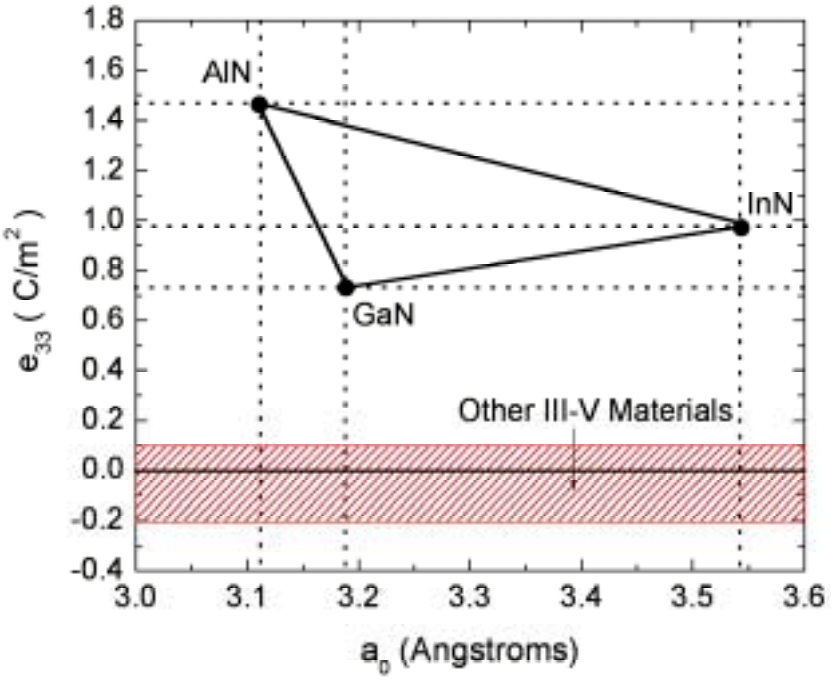


Fig 3.9(b) Piezoelectric polarization coefficents in the GaN system.

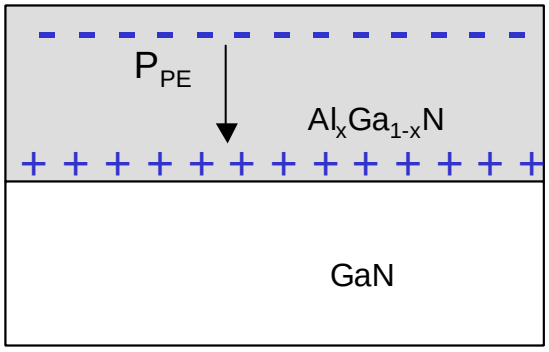


Fig 3.10 Electric field and charge sheets present due to piezoelectric polarization only in GaN and AlGaN crystals grown on c-plane in a Ga-face crystal

shown in **Fig 3.10.**

3.4.3 Orientation Dependence

The GaN crystal does not have inversion symmetry along the c-axis. Hence there exist two different crystals that can grown on c-plane sapphire **[8,9]**. These are referred to as N-face and Ga-face crystal, as shown in **Fig 3.11**. If N-face crystal is inverted, Ga-face crystal is obtained. ***It is important to realize that the crystal orientation, Ga-face or N-face, is a bulk property of the crystal and not a function of the surface termination***. In heterostructures grown on Ga-face crystal, the charge sheets caused by spontaneous and piezoelectric polarization add. In N-face the spontaneous and polarization charge sheets subtract from each other. GaN grown by MOCVD on sapphire and SiC substrate is Ga-face in UCSB-MOCVD reactors. MBE growths of device structures were performed on UCSB-MOCVD grown templates and hence all device structures used in this work were grown on Ga-face crystal.

3.5 Polarization Induced surface states as the source of charge in 2DEG

3.5.1 The importance of intentional doping to 2DEG density in AlGaN/GaN

Experimentally, it has been observed that

a) A 2DEG is formed in GaN in the lower AlGaN/GaN interface even when there is no intentional doping of the AlGaN layer.

b) When the AlGaN is intentionally doped, the charge density in the 2DEG is not proportional to the amount of dopant (Si, a shallow donor in GaN) introduced into the AlGaN layer.

Various workers have shown that the magnitude of sheet charge resulting from intentionally added dopants to increase the sheet charge is much smaller, typically less than 20%, than the sheet charge densities present in an undoped

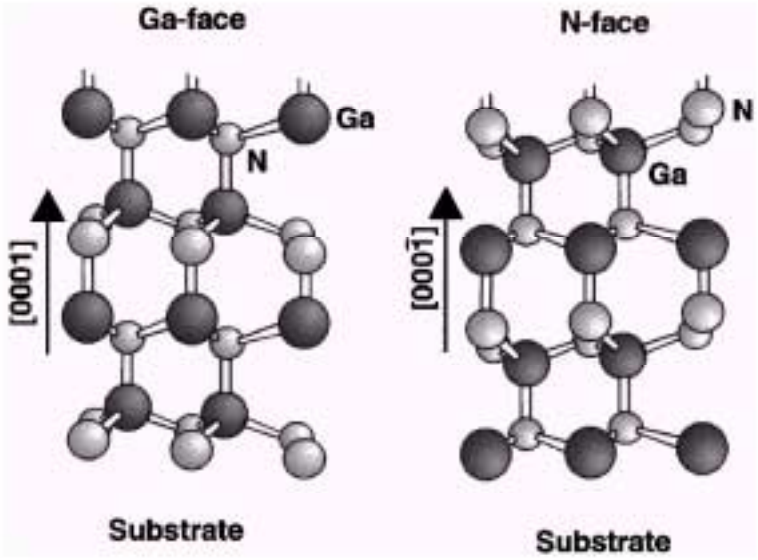


Fig 3.11 N-face and Ga-face crystal orientations.
(After Ambacher et. al. J. Appl. Phys. 1999)

AlGaN/GaN heterostructure. This is partly due to the magnitude of carrier densities present in an undoped structure and also due to the technological difficulty of introducing the requisite concentration of dopants into the AlGaN layer while maintaining the structural quality of the AlGaN. As an example, a 27% AlGaN heterostructure has a sheet density of $1x10^{13}$ cm^{-2} with a 200 A thick AlGaN layer. To obtain the same carrier density from intentional shallow dopants would require an impurity concentration of $5x10^{18}$ cm-3 in the AlGaN layer, a larger number than can currently be achieved.

In MOCVD growth, the dopant incorporation efficiency in AlGaN is not known. What is known, however, is the flux of silane (SiH_4) that flows into the reaction chamber. It has been found in our laboratories that under the conditions needed to grow device quality AlGaN layers, the sheet carrier concentration increases slightly with increasing flux of silane and then saturates i.e. any further increase of silane flux results in no further increase in channel charge, as shown in **fig 3.12**. The fraction of the total charge resulting from the Si doping is less than $4x10^{12}$ from a total of $15x10^{12}$, i.e. ~ 25%.

The evidence above suggests that dopants play only a secondary role in determining the sheet carrier concentration. The major cause of the formation of a 2DEG is the presence of polarization induced charge sheets in bottom and top surfaces of the AlGaN layer.

3.5.2 Consequence of the polarization dipole in the AlGaN

The influence of the polarization dipole on the band structure was first discussed by Ibbetson [10]. Consider what happens when a layer of strained AlGaN is grown psuedomorphically on a bulk Ga-face crystal. A polarization dipole, consisting of the sum of the spontaneous and piezoelectric dipoles, is set up as shown in **fig 3.13** The electric field inside the AlGaN crystal is dependent

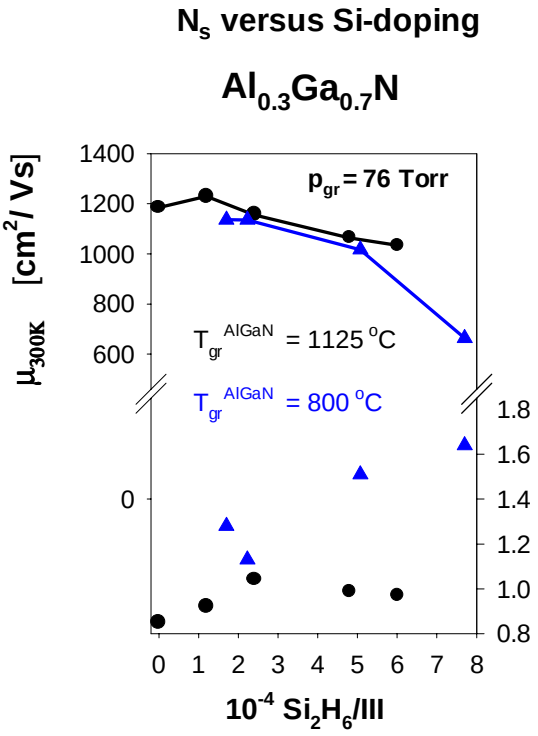


Fig. 3.12 Dependence of 2DEG sheet carrier concentration on Disilane flux in HEMTs by MOCVD

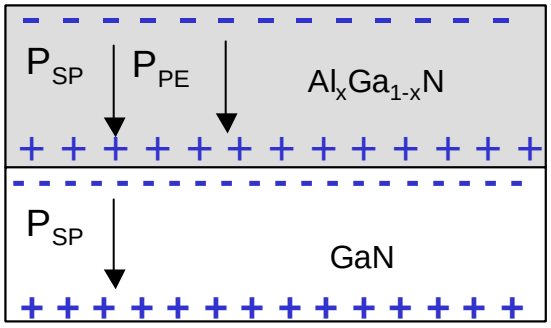


Fig 3.13 Combined piezoelectric and spontaneous polarization dipole in AlGaN/GaN crystals grown on c-plane in a Ga-face crystal

only on the sheet charges at the top and bottom faces. Since this field is constant, the energy of the crystal as reflected in the potential drop across the two faces of the crystal is continuously increasing with thickness of AlGaN. It is easy to imagine that beyond a certain thickness, which we will denote as critical thickness, it becomes energetically more favorable for the crystal to create some kind of compensating charge of opposite polarity to the polarization charge which would lower the electric field inside the AlGaN. ***Note that the configuration with the lowest energy would require the compensating charges to form closest to the polarization charge sheets i.e. a negative charge sheet (2DEG) at the lower AlGaN/GaN interface and a positive sheet charge on the top surface of the AlGaN layer***.

3.5.3 2DEG formation – ideal surface

Consider what happens when the surface is ideal, i.e. no surface defects are formed as a consequence of the polarization fields present in the AlGaN. In this case, as the thickness of the AlGaN is increased, there will come a point when the valence band approaches the Fermi level. Note also that the crystal is in equilibrium and hence a constant fermi level can be drawn across the AlGaN as shown. When the valence band approaches the Fermi level, an accumulation of holes occurs at the surface, and this positive charge sheet due to holes will prevent any further increase in surface potential with further growth of AlGaN. A negative 2DEG charge sheet of the same magnitude as the positive hole charge sheet is formed at AlGaN/GaN interface. Note that no 2DEG will form until the surface hole gas is created. The minimum thickness of AlGaN needed to induce formation of 2DEG is referred to as the critical thickness. In the case of an ideal surface, this critical thickness of AlGaN will depend on the band gap of the

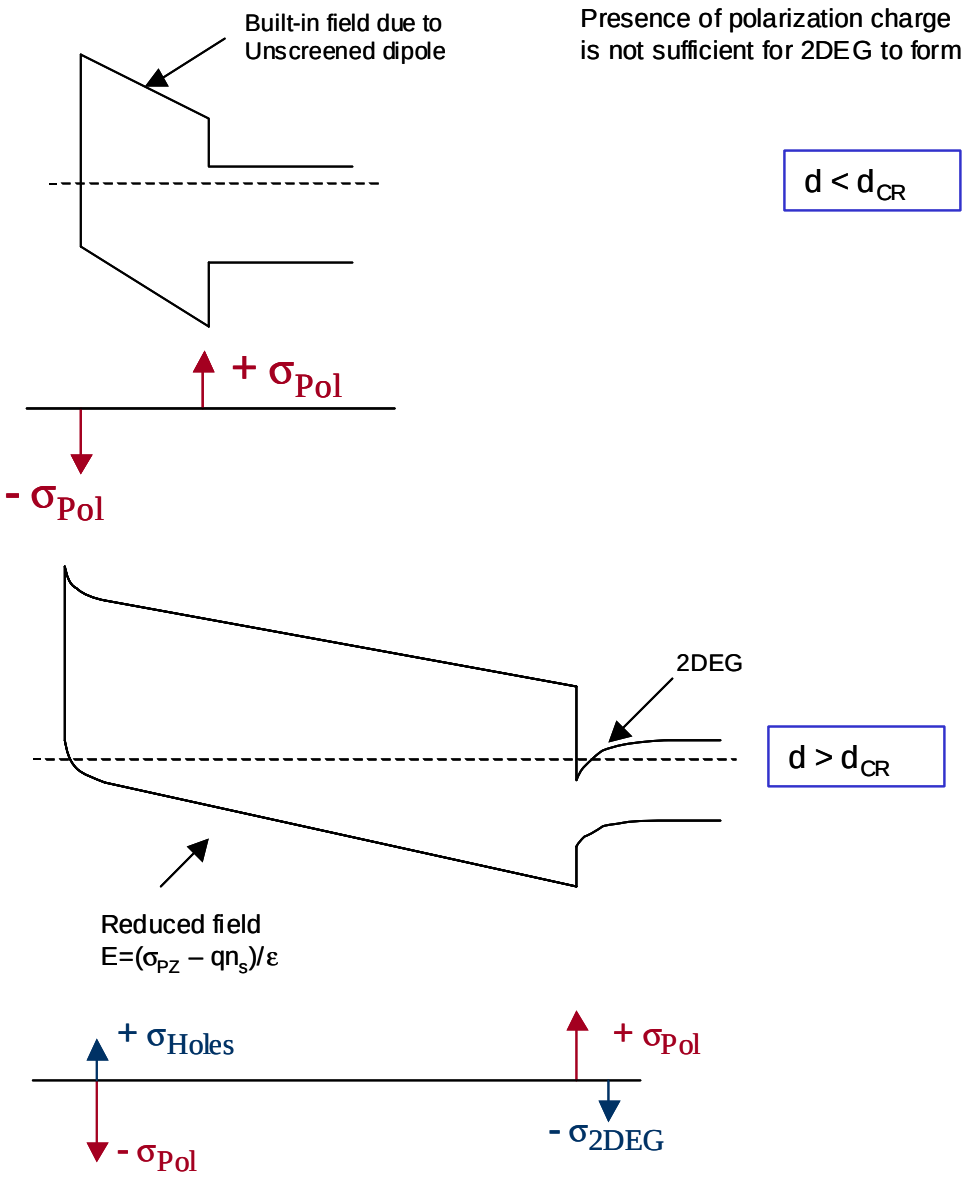


Fig 3.14 2DEG formation case of an ideal surface

AlGaN layer and the magnitude of the polarization dipole. This scenario is shown in **fig 3.14**.

3.5.4 2DEG formation – surface donors

Let us consider the case when the surface is non-ideal. Let us adopt the hypothesis that when the energy of the crystal has been raised above a certain point, due to the separation of the polarization charge sheets, a surface state is formed at the level indicated in **Fig 3.15** with a net positive charge. This positive surface state results in the formation of a negative 2DEG at the AlGaN/GaN interface. Since this energy level of the this surface state is dictated by the energy of formation of some physical defect such as a vacancy or some other surface defect, it is reasonable to assume that this level remains constant during further AlGaN growth. Note also that the crystal is in equilibrium and hence a constant fermi level can be drawn across the AlGaN as shown. Electrostatics leads to the relations between the sheet charge and the thickness of the AlGaN and the polarization sheet charge density and also d_{CR}, the critical thickness of AlGaN, as shown in **eqns 3.3-3.5**. This theory of surface state as the origin of the 2DEG in undoped structures was first proposed by Ibbetson [11].

3.5.5 2DEG density dependence on AlGaN thickness and Al mole fraction

As the thickness of AlGaN increases beyond the critical thickness, note that the pinning of the fermi level at the surface implies that the electric field across the AlGaN must decrease. This decrease is due to the increasing magnitude of the compensating sheet charges, the 2DEG and the positive surface charge. Note also that the relation (3) implies that, neglecting the correction due to the second term on the RHS, the 2DEG concentration is linear with the surface pinning level and follows an monotonic increasing behavior with thickness of

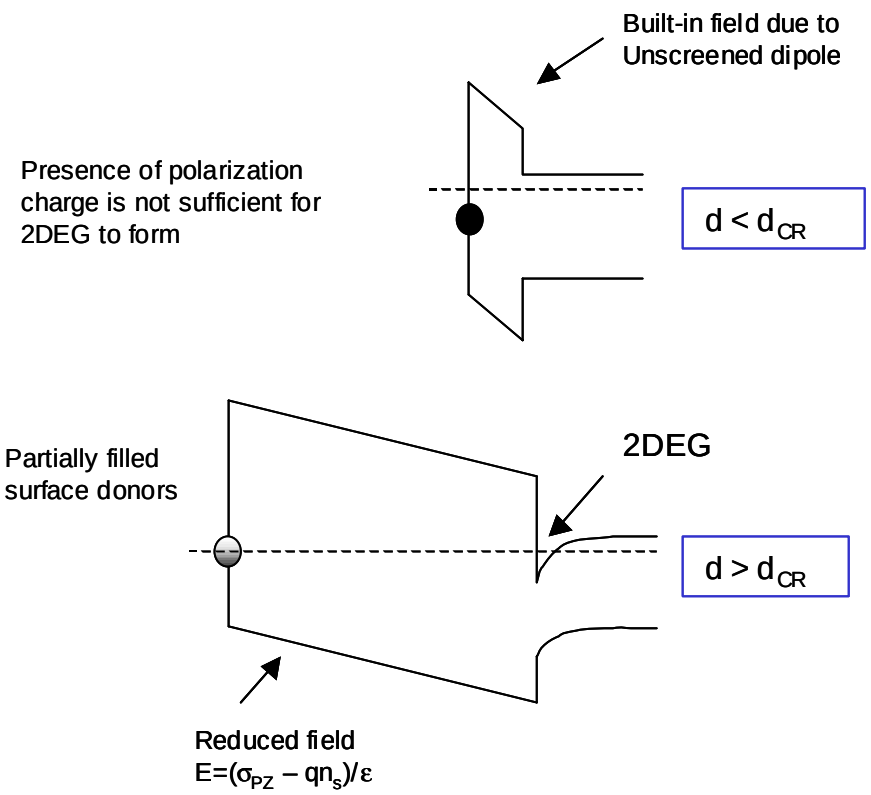


Fig 3.15 The surface donor model
After Ibbetson et.al. Appl. Phys. Lett. 77(2) 10 July 2000

AlGaN. **Fig 3.16** shows the simulated 2DEG charge densities as a function of both the surface pinning level and the AlGaN thickness.

Fig 3.17(a) shows the measured 2DEG concentration when only the thickness is varied.

$$q.n_s = \sigma_{Pol}.(1-d_{CR}/d) - \varepsilon.E_{fo}/d + N_d d/2 \qquad (3)$$

$$q.n_s = \sigma_{Pol}.(1-d_{CR}/d) \qquad (4)$$

$$d_{CR} = \varepsilon(q.\varphi_S - \Delta E_c)/\sigma_{Pol} \qquad (5)$$

From **eqns (3-5)** a fit to the data has been performed using a surface pinning level of 1.42 eV. The close agreement between theory and experiment indicates that the formation of surface states at a particular energy level after a certain critical thickness of AlGaN is a correct hypothesis [12,13]. **Fig 3.17(b)** shows the sheet charge densities in heterostructures in which the thickness of AlGaN has been kept constant and the Al mole fraction in the AlGaN layer is varied.. The data shows a good correlation between experiment and surface state hypothesis.

3.5.6 The meaning of critical thickness

Consider **Fig 3.18**(a), the band diagram resulting from the formation of sheet charges of opposite polarity to the polarization charge sheets. From the condition of charge neutrality it is obvious that the 2DEG concentration must equal the positive sheet charge on the surface. It is also clear that the energy of formation of this surface charge dictates the thickness of AlGaN that can be grown without the formation of a 2DEG. What happens when the growth of AlGaN continues beyond the point where this surface charge is created?

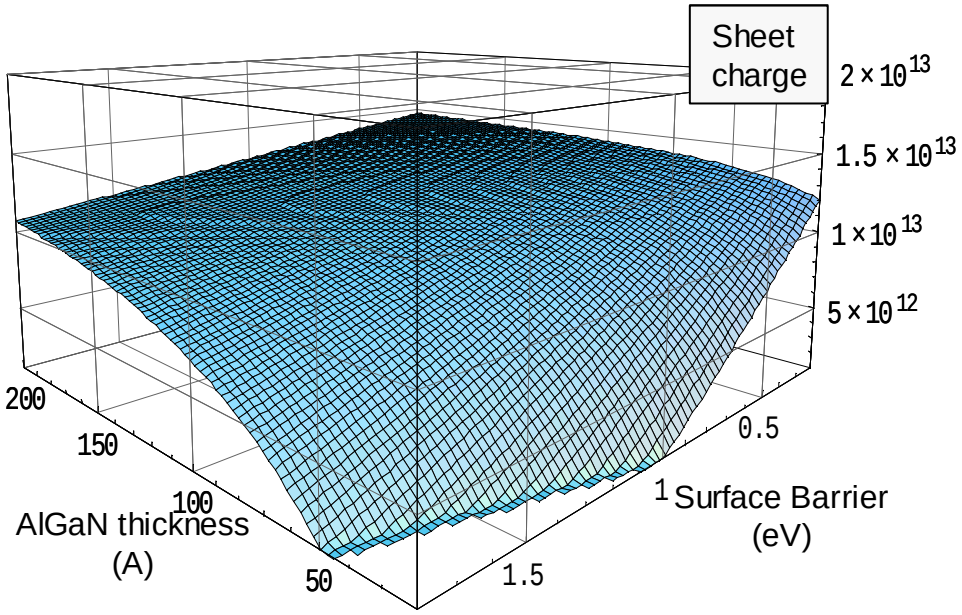


Fig. 3.16 Simulated dependence of 2DEG sheet density on AlGaN thickness and surface pinning level.

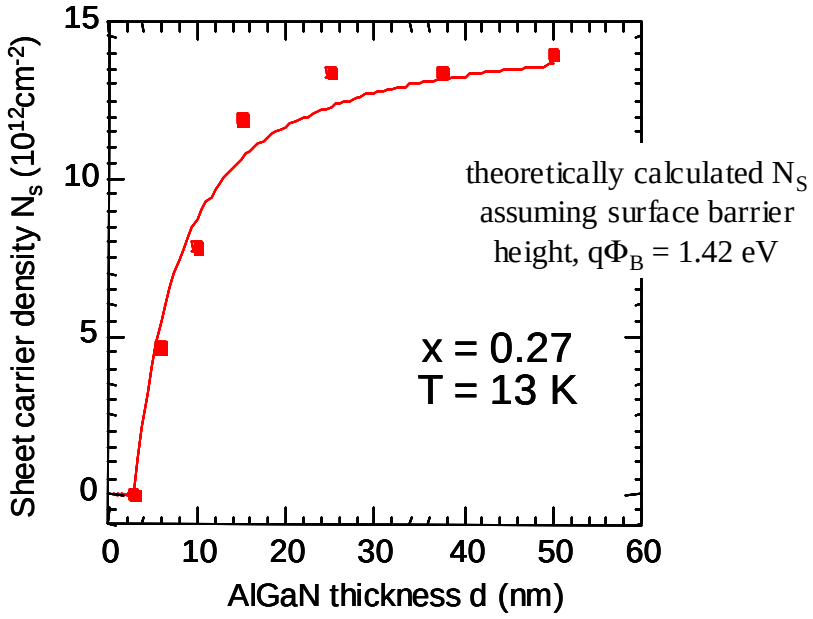


Fig. 3.17(a) Dependence of 2DEG sheet density on AlGaN thickness
After Smorchkova et.al. J. Appl. Phys. 86, pp.4520-6, 1999.

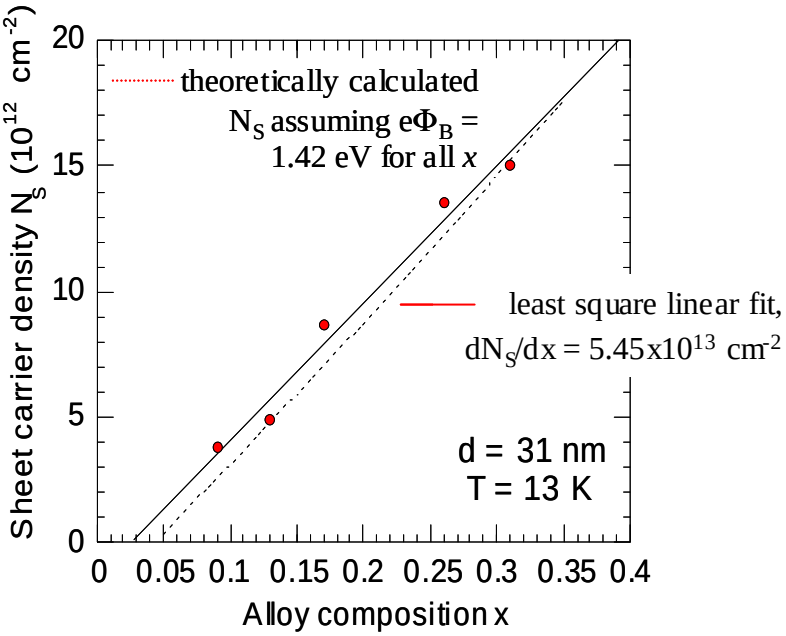


Fig. 3.17(b) Dependence of 2DEG sheet density on Al mole fraction
After Smorchkova et.al. J. Appl. Phys. 86, pp.4520-6, 1999.

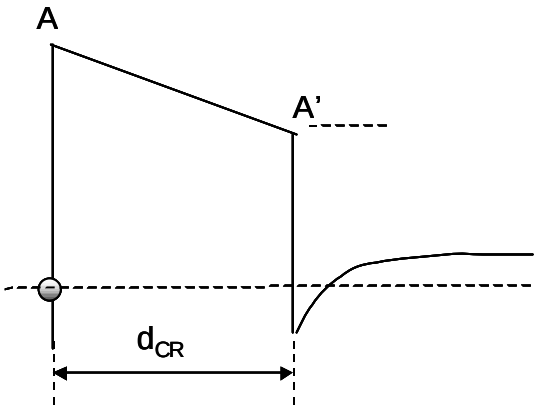
Does the surface state incorporate into the AlGaN and become a bulk state? Or does the surface state stay on each newly forming surface i.e. does it "ride" the surface?

It is clear from the energy of the crystal is lowest when the charge sheets that compensate the polarization charge sheets are closest to the polarization charge, because the energy of a dipole is lowest when the positive and negative charge sheets are closest to each other. Consider what happens if a surface state incorporated into the crystal and become a bulk state that was fully ionized with the positive ionized donor charge contributing to the negative 2DEG. The electric field contributions due to the two set of opposite charges, namely a) the two polarization charge sheets and b) the bulk donor charge and 2DEG, are shown in dashed lines and the resultant band diagram in solid line in **Fig 3.18**(b). Note that once past the incorporated donor, the electric field is the same as when there are no compensating charge sheets. *Hence an additional critical thickness later, surface states would form once more*. Also energy of formation of this surface state relates to the surface condition: incorporation of a surface state into a bulk state would require a different energy and may not be feasible. Hence it is likely that the surface states ride the surface.

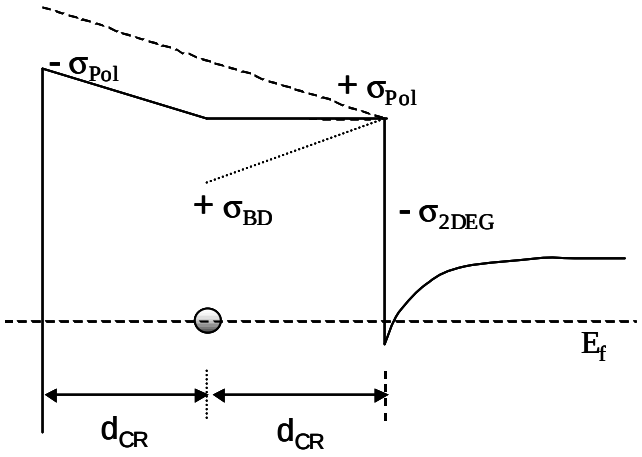
3.6 Nature of the free AlGaN surface in AlGaN/GaN heterostructures

3.6.1 Different possible surface configurations

From the evidence presented in this chapter, it is clear that the surface states must exist in the AlGaN layer in an AlGaN/GaN structure. However, all that can be inferred from electrostatic analysis and Hall measurements of 2DEG density is the density of net surface positive charge. This requirement of positive charge on the surface can be satisfied by a surface donor state at a particular energy level, a donor acceptor pair or a distribution of surface donor states, as



(a)



(b)

Fig. 3.18 Does the surface donor ride the surface?

shown in **Fig 3.19**. How can we distinguish between the different surface state possibilities? One way is through a measurement of Schottky barrier heights when metals of different work functions are deposited on the surface. Metal semiconductor interfaces and resulting barrier heights is briefly discussed in the next section.

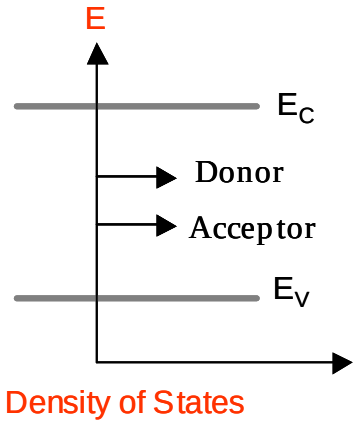
3.6.2 Metal Semiconductor Interfaces

The theory of metal semiconductor junctions was first discussed by Schottky **[1]**. The Schottky model is shown in **fig 3.20**. The difference in electro-chemical potential between the metal and semiconductor results in the creation of a dipole at the interface: the potential drop across this dipole is equal to the difference in chemical potentials between each side. Depending on whether the electrons in the semiconductor or metal have higher energy, transfer of electrons takes place from one side to the other. A dipole consists of a charge sheet in the metal and a region of opposite charge in the semiconductor. Hence in the case of an n-type semiconductor, either an accumulation of electrons or a depletion region containing fixed ionized impurities is formed on the semiconductor side. The resulting junction is shown in **fig 3.20**. In the case when the energy of electrons in the semiconductor is initially higher than the metal, there now exists a barrier for electron transfer from the semiconductor side to the metal. This kind of a junction is usually referred to as a Schottky contact. The height of the barrier seen from the semiconductor side is the difference in chemical potentials on either side, given by

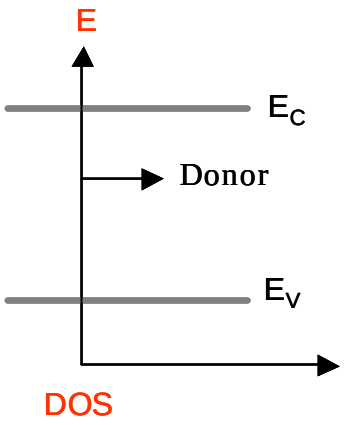
$$V_{Bi} = \phi_M - \phi_S,$$

The height of the barrier seen from the metal side is given by,

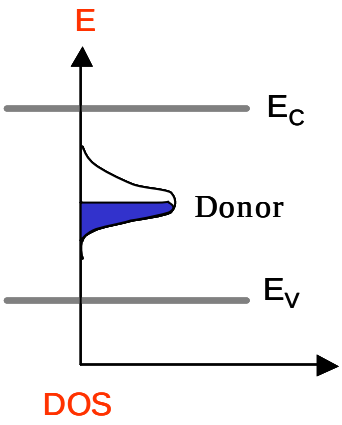
$$\phi_B = \phi_M - \chi_S,$$



(a)



(b)



(c)

Fig 3.19 Possible surface states giving rise to positive surface charge.

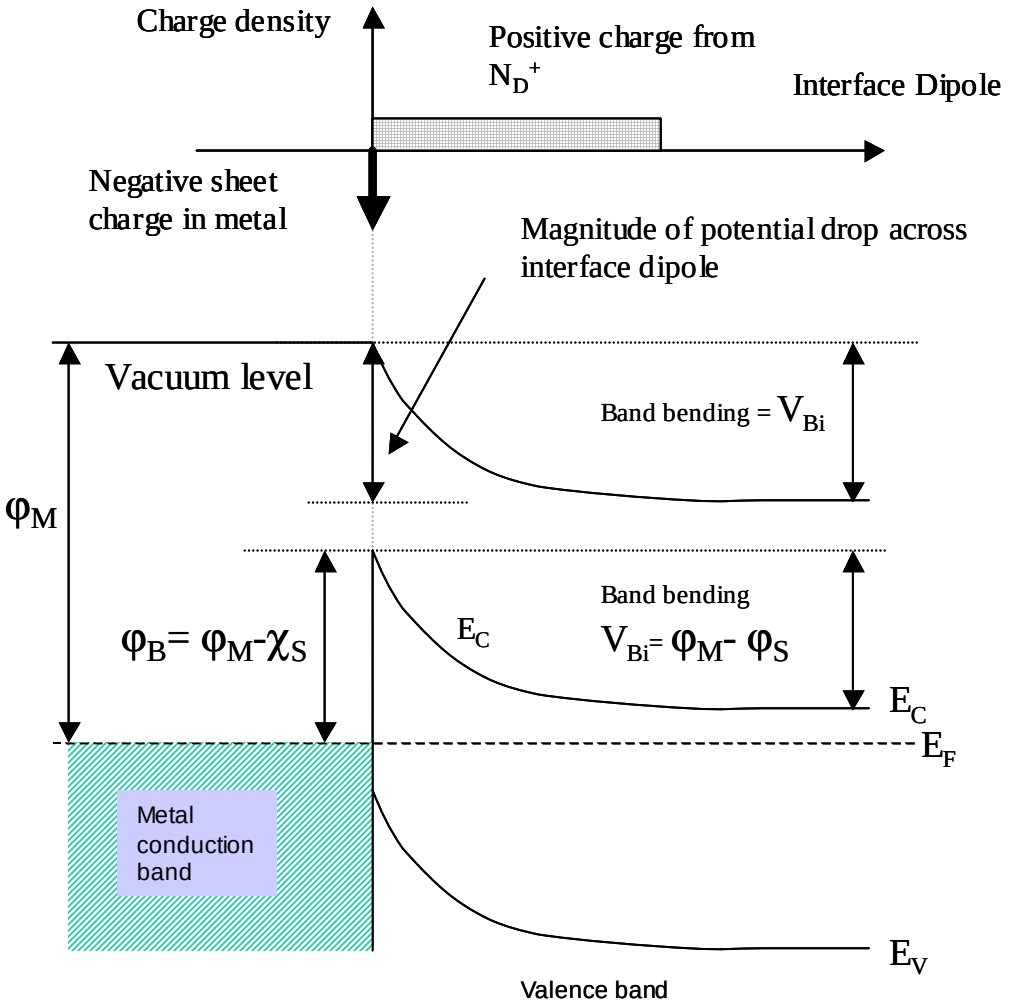


Fig 3.20 Schottky barrier between a metal and n-type semiconductor at zero bias. No surface states exist.

This value of barrier height is referred to as the Schottky limit or the Mott limit. It is obtained under the conditions of no surface charge. In any real semiconductor, there exists a finite density of states within the band gap, localized at the surface. These states can be charged and therefore can contribute to the dipole that accommodates the difference in chemical potential. Hence the charges in the surface states can screen the semiconductor bulk from the metal. In the limiting case of an infinite or sufficiently large number of surface states, the charge from surface states forms one half of the dipole needed to accommodate the difference in chemical potentials between the semiconductor and the metal, as shown in **fig 3.20**. In this case, the barrier to electron flow from the semiconductor to the metal is independent of the work function of the metal and is given by

$$\phi_{B=} E_G - \phi_O \qquad (2)$$

where ϕ_O is the chemical potential of the surface. The value of Schottky barrier in this case is referred to as the Bardeen limit **[14]** and a representation of the junction formed in this case is shown in **fig 3.21.** Note that the Bardeen limit is not dependent on whether a metal is deposited on the surface or not. Since a large density of surface states exist in the semiconductor always, the Fermi level at the surface is pinned at ϕ_O when the surface is left free.

3.6.3 Schottky barrier pinning

It is important to realize that the existence of a high density of surface states does not necessarily mean that the Schottky barrier height is pinned for all metals. Consider **fig 3.19(a) and 3.19(b)** which show two different kinds of surfaces. The surface in **fig 3.19(a)** has a donor acceptor pair at the surface. In the limit of large density of states at these two levels, the fermi level at the surface will always be pinned in between the two levels. This is because a these surface states can generate either a positive or negative charge of arbitrary magnitude to

accommodate any electrochemical difference between any metal and the semiconductor i.e. the magnitude of the dipole due to the surface states can be as large as necessary. Hence for metal of any work function the surface fermi level would remain pinned in between the surface donor and acceptor levels as shown in **fig 3.22 (a) and (b)**.

The surface in **fig 3.19 (b)** has a single surface donor level. There can only be positive charge arising from empty surface donors. Note that when a donor state is filled, i.e. the fermi level at the surface is above the donor level, it has no net charge and hence ceases to influence the electric field or the potential of the heterostructure. Hence, as shown in **fig 3.23(a),** if the metal work function were larger than the energy ($E_D + \chi$), in the case of a donor state at the surface, the measured Schottky barrier height would be pinned by the donor state. If the metal work function were smaller, as in **fig 3.23(b),** then the surface Fermi level would be free to rise above the surface donor level and the surface would not be pinned.

Preliminary measurements indicate that the surface fermi level is not pinned by a donor-acceptor pair, since the barrier height of Schottky diodes for a metal with a small work function such as Ti is smaller, by an estimated 0.2eV, than that measured on Pt diodes.

3.7 Conclusions

Measurements made using the floating gates as potential probes show that the surface potential of the device was made negative, when the gate drain diode is strongly reverse biased. This negative potential was shown to be inconsistent with the ionized donor density. These measurements of surface potential indicated that there had to exist some mechanism to allow negative charge to accumulate on the surface and raise the surface potential. In the second half of this chapter it has been shown that merely the existence of a polarization induced dipole is not

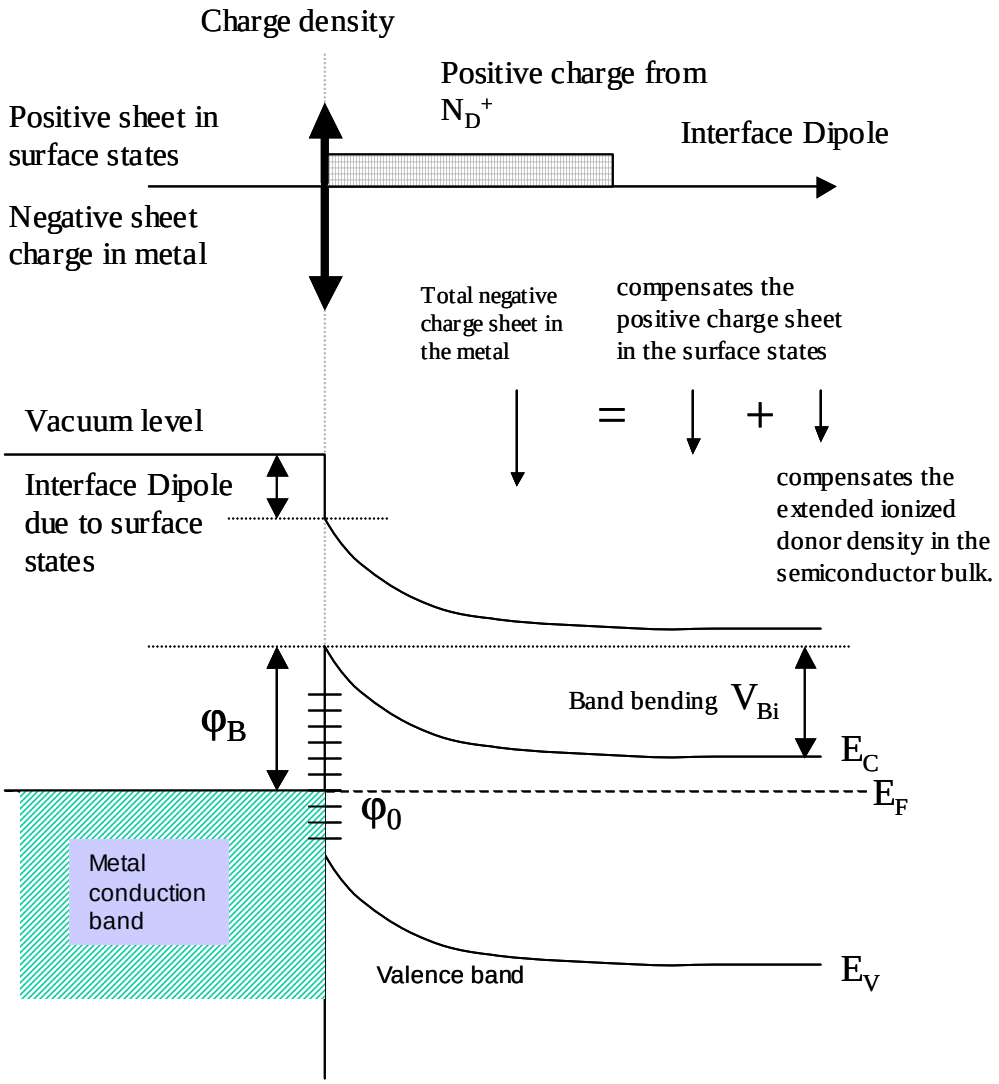


Fig 3.21 Schottky barrier between a metal and n-type semiconductor at zero bias with surface states.
A thin interfacial layer is usually assumed, but is not shown here for clarity.

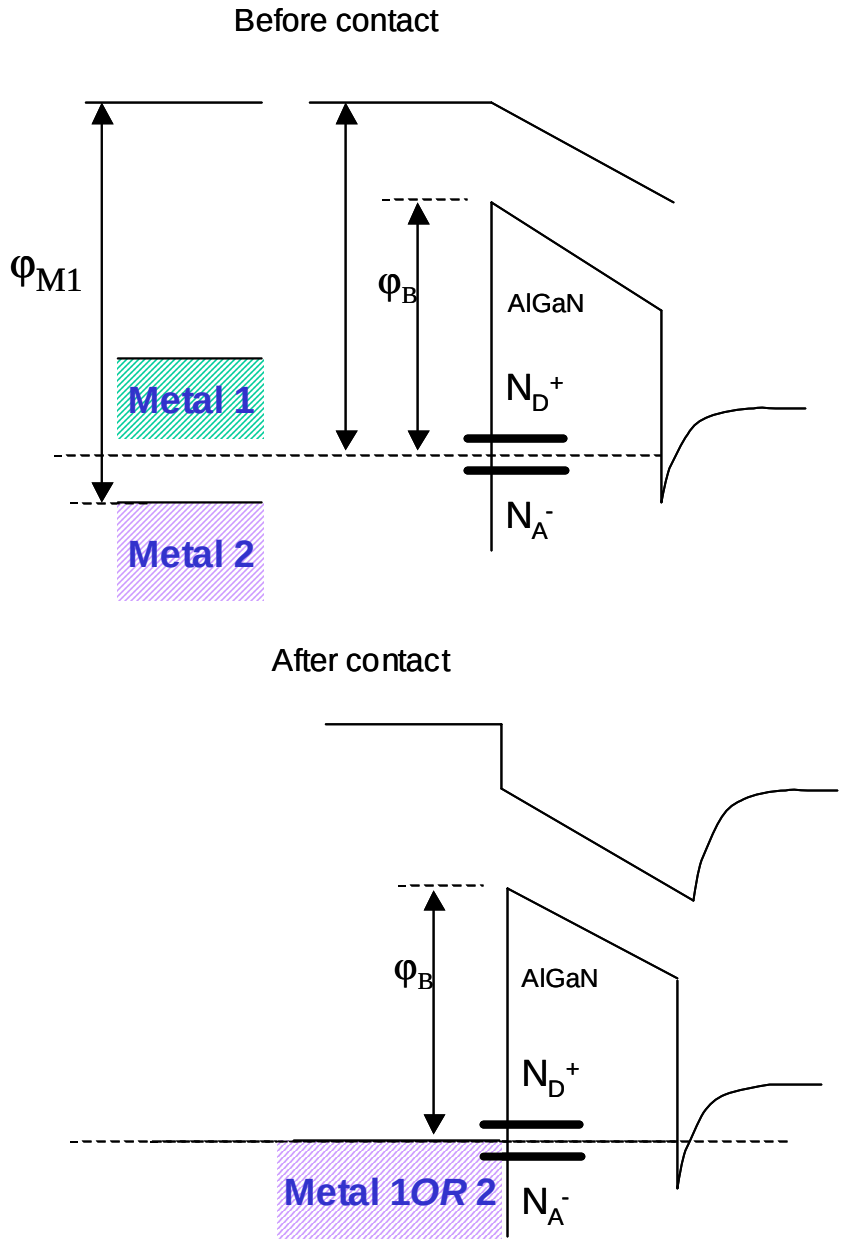


Fig 3.22 (a) Donor-Acceptor pair : $\varphi_{M1} > \chi + E_D$.
Surface is pinned in for both metals.

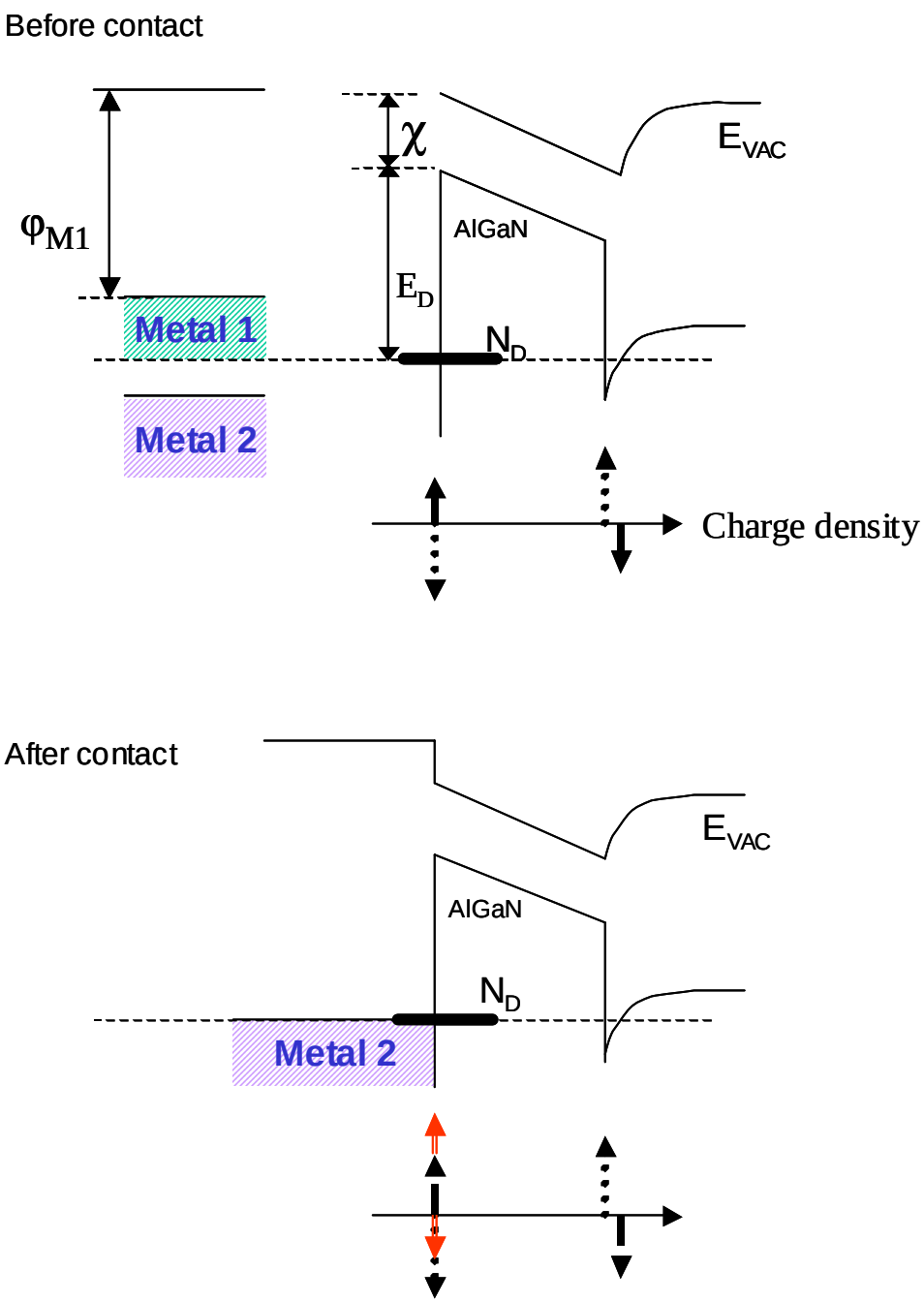


Fig 3.23 (a) Single donor level : $\varphi_{M1} > \chi + E_D$.
Surface is pinned in this case.

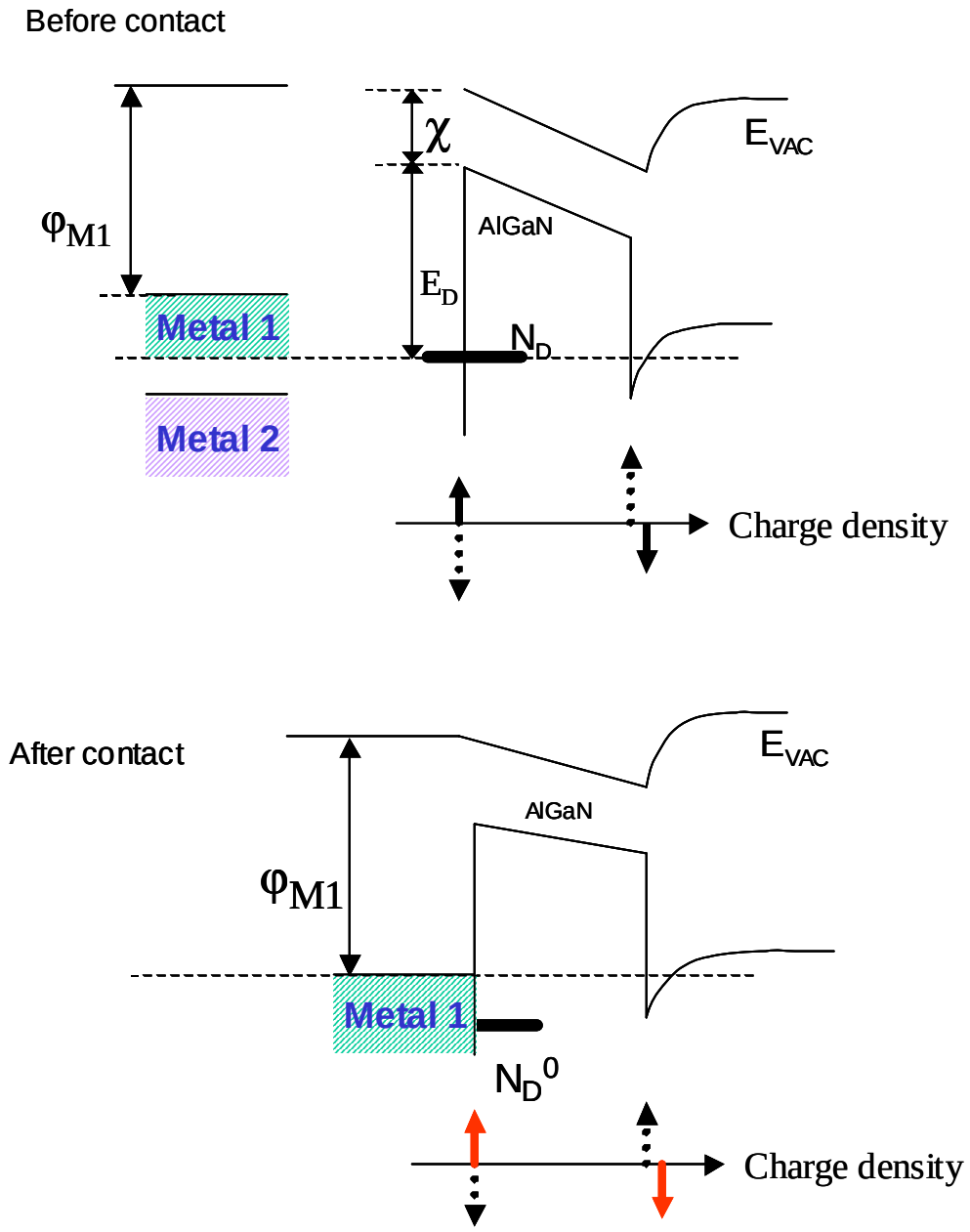


Fig 3.23 (b) Single donor level : $\varphi_{M1} < \chi + E_D$. Surface fermi level is not pinned in this case.

sufficient to form a 2DEG in the GaN channel of an AlGaN/GaN heterostructure. From charge neutrality conditions, there must exist a net positive sheet charge at the surface to balance the negative charge of the 2DEG. Such a sheet charge must come from positively charged donor-like states on the AlGaN surface. If such donor-like states exist on the surface, that carry a net positive charge when the device is in the as-grown state, then any electrons trapped by these states would give rise to a negative change in surface charge. This change in surface charge would make the surface potential negative, thus explaining the large negative surface potentials observed in the floating gate experiments. Now the question arises as to the time response of this trapped negative surface charge. This is the subject of the next chapter.

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Chapter 4

4.1 Current collapse in GaN HEMTs

The problem of current collapse has been variously referred to as dispersion, DC/RF dispersion, current slump and current collapse. This is the most important problem that impacts GaN FET technology for high power applications. In the previous chapters the development of high power GaN HEMTs was presented. Factors affecting the trap density in the bulk of the GaN and AlGaN layers were discussed. It was shown that minimization of bulk trap densities led to improved power performance of GaN HEMTs but did not completely eliminate the problem of current collapse. The presence of large polarization fields in a HEMT structure was shown to lead to the presence of a positive charge sheet at the surface of the AlGaN layer that was responsible for the existence of a 2DEG in the AlGaN/GaN interface. Measurements of 2DEG density dependence on AlGaN thickness and mole fraction in a HEMT structure showed that the Fermi level at the surface was pinned. Measurements of surface potential showed that the surface became negatively charged under large drain bias in the off-state. These observations could be explained by a postulating donor-like surface states on the AlGaN surface that accepted electrons to become negatively charged. In this chapter, the nature of current collapse is discussed.

4.1.1 Decrease of power at microwave frequencies.

As mentioned briefly in chapter 1, current collapse is essentially the observation that the measured output power from the device at microwave frequencies of interest such as 4-18GHz, is considerably smaller than that expected based on the equation,

$$P = 1/8 * I_{DS,MAX} * (V_{BREAKDOWN}-V_{KNEE}) \qquad (4.1)$$

where the values of $I_{DS,MAX}$ and V_{KNEE} are based on the values measured at DC using a Tektronix curve tracer or a HP 4145B Semiconductor Parameter Analyzer. To explain the lower output power at RF, $I_{DS,MAX}$ is supposed to be decreased and/or V_{KNEE} increased, from their DC values. Since this change in device parameters is expected to occur at some frequency between DC and the RF frequencies of measurement, the term DC/RF dispersion has been sometimes used to describe this phenomenon. **Fig 4.1** shows the nature of the problem.

In this chapter, the phenomenon of current collapse is explained using the concept of the virtual gate. First, the concept of the virtual gate is presented. Then measurements are presented that show that current collapse is a consequence of the formation of this virtual gate, located in the gate drain access region, under high power operation. It will be shown that surface passivation by SiN dramatically reduces the extent of current collapse. Transient measurements of the maximum drain current available from unpassivated devices made under dark and illuminated conditions are presented. A model is hence presented to explain the nature of current collapse as the consequence of surface states capturing electrons. It is shown that holes generated under above band gap illumination can forward bias the surface and neutralize the virtual gate, thus eliminating current collapse. Although the exact mechanisms by which the surface passivation reduces current collapse are unclear at this point (as will be discussed in chapter 5), it is shown in this chapter that surface passivation prevents current collapse by preventing the formation of the virtual gate.

4.1.2 Status of current research on trapping effects in GaN HEMTs

A brief review of existing literature on the current collapse is presented. An important point to be made here is the distinction between steady state and transient responses. As will be made clear in this chapter, since trapping effects in

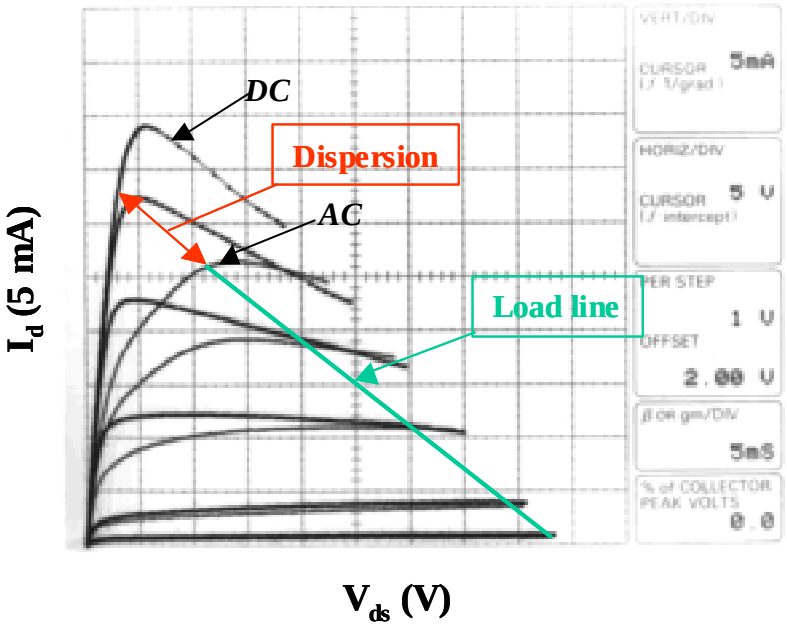


Fig 4.1 The nature of current collapse. The maximum power available from the device is given by

$$P = (\Delta V. \Delta I)/8.$$

Here ΔI is the maximum drain current available, $I_{DS,MAX}$ and ΔV is the voltage swing given by $V_{BREAKDOWN}$-V_{KNEE} .

A decrease in output power can result from the decrease of $I_{DS,MAX}$ and an increase in V_{KNEE} as shown above.

GaN HEMTs have time constants (in the order of minutes and longer) and are very strongly dependent on illumination conditions, it is important to ensure steady state conditions are reached before making frequency dependent measurements. Interpreting data taken during a transient response as a frequency dependence can be misleading.

The problem of current collapse leading to reduced microwave output was first reported by Wu **[1]** and was referred to as "dispersion". Drain current compression during large signal operation at microwave frequencies has been reported by Nguyen **[2]**. Current compression was observed even when the load impedance was zero. Since voltage swing is minimal under zero load impedance, it was concluded in **[2]** that the trapping of carriers takes place in the AlGaN barrier or the surface of the device and not the buffer. Gate drain conductance and capacitance dispersion was reported by Miller **[3]**. However these studies were conducted at small signal operation and did not reveal the physical location of the traps. Large signal current swing and small signal transconductance dispersion in the 10-100 kHz was reported by Kohn **[4]**. However, in these studies, no mention of transient response was made. The data was interpreted as evidence of the AlGaN layer behaving like a lossy dielectric and thus leading to an RC time constant as observed. Binari observed current collapse in GaN MESFETs under high drain voltage operation **[5,6]**. By varying the energy of incident illumination, it was concluded that the photoionization thresholds for these traps were at 1.8eV and 2.85eV respectively **[7]**. Because the studies were conducted in MESFET structures, the trapping location was assigned to the GaN S.I. buffer layer. Binari **[8]** also performed gate lag and drain lag measurements on GaN HEMTs and found that both drain lag and gate lag effects occurred. Hence it was concluded that traps existed in both the buffer (contributing to drain lag) and the AlGaN surface (contributing to gate lag). Pulsed measurements using pulse widths of 400

ns were performed on GaN MESFETs by Trassaert **[9]** and Binari **[10]**. Since the threshold voltage was found to be the same under DC and pulsed conditions, it was concluded that the traps were located in the surface. Drain current collapse under high voltage operation and the effect of illumination on drain current collapse was reported in **[11,12]**.

For high power operation, the most relevant parameter is the maximum current swing, however only Kohn **[3]** focused on the direct measurement of the large signal current swing as a function of frequency. The location of the traps responsible for current collapse remained ambiguous. An accepted physical model for current collapse did not exist. The link between the surface as the source of electrons and hence also the reason for current collapse was not recognized. By correlating the measurement of microwave power and the drain current swing as a function of frequency for both passivated and unpassivated devices, the data presented in this chapter conclusively demonstrates the importance of the surface traps to the problem of current collapse.

4.1.3 How can traps affect the device I-V characteristics?

In this section the concept of the virtual gate is presented. First, we ask the question, how can traps affect device I-V characteristics?

Traps can affect the device I-V characteristics by

1. Directly trapping electrons that would otherwise be part of the mobile channel electrons i.e. depleting the 2DEG density at the channel.
2. Trapping charge elsewhere, (not in the channel), thereby creating a potential barrier that impedes the flow of channel electrons.

Where can charge be trapped?

Charge can be trapped under the gate, on the surface in the gate drain access region, and in the insulating buffer. If charge trapping occurs under the

gate, then the pinch off voltage of the device should change correspondingly, as given by

$$\Delta V_P = q.\ \Delta n_s / C_{AlGaN} \qquad (4.2)$$

where C_{AlGaN} is the capacitance of the AlGaN layer and Δn_s is the change in 2DEG density. Since the pinch off voltage does not change commensurately with the change in maximum current as expected from equation 4.1, it is clear that current collapse is not caused by traps underneath the gate,

If channel electrons are trapped by traps in the GaN close to the heterointerface, or located at the heterointerface, then a surface treatment such as surface passivation through SiN deposition should not influence the trapping behavior. Since current collapse is affected by surface passivation, trapping of channel electrons is not the dominant cause of current collapse.

In the AlGaN/GaN heterostructure, as described in the previous chapters, there exists a net positive charge on the surface to compensate the negative sheet charge due to electrons in the channel. Neutralizing this surface positive charge sheet, by either the capture of electrons in trap states or the emission of holes is analogous to negatively charging up an imaginary metal gate on the surface and hence depleting the channel charge underneath and giving rise to a second barrier to electron flow along the channel. This imaginary metal gate will be referred to hence as the virtual gate.

4.2 Concept of the virtual gate

4.2.1 Virtual gate model

In this model, the external I-V characteristics now depend on the potential on the virtual gate V_{VG}. V_{VG} depends the spatial distribution of trapped charge along the gate drain access region. **Fig 4.2** shows the model of the device showing the virtual gate in series with the metal gate. Note that depletion of charge in the

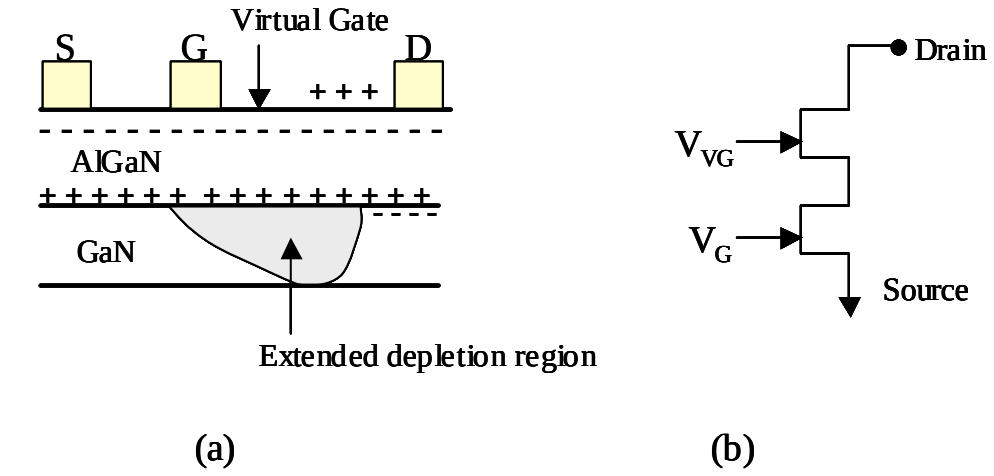


Fig 4.2 Model of device showing the location of the virtual gate.

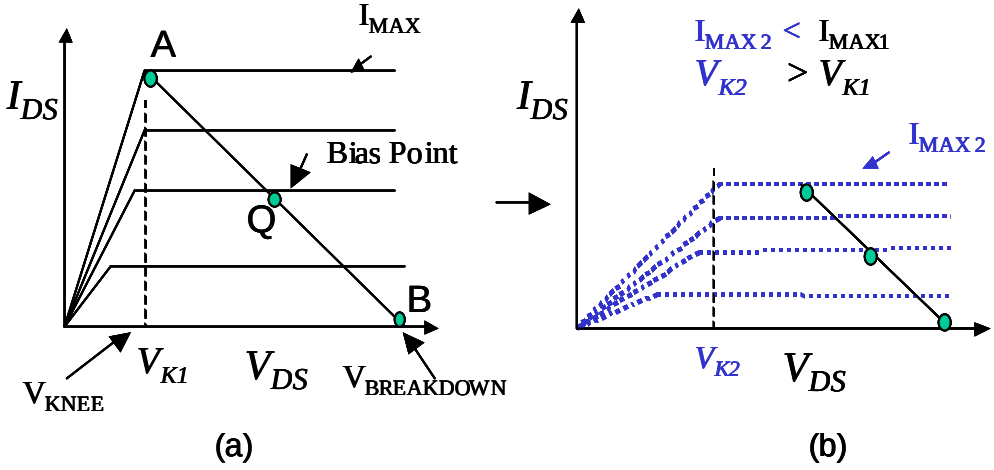


Fig 4.3 The consequence of a reverse biased virtual gate, the device I-V characteristic changes from (a) to (b).

access region is not equivalent to a simple increase in the value of the access resistance. Simply increasing the access resistance results in a voltage drop that causes the measured I-V characteristics to be stretched out horizontally on the voltage axis. *In the GaN HEMT the sheet resistance everywhere along the source-drain region is the same, unlike a recessed gate GaAs FET where the conductivity in the access region is substantially larger than under the gate. Hence any increase in resistance at any point in the source-drain region is effectively a gate in series*. An additional gate in series can limit the maximum current. A significant fraction of V_{DS} is dropped across this virtual gate, thus preventing the field at the source from increasing and the maximum current is now limited by reverse bias on the virtual gate. Hence the effect of the trapped surface charge is to change the measured I-V characteristic from **Fig 4.3(a) to Fig 4.3(b).**

Given that when the charge is trapped in the surface trap states, the device now looks like **Fig 4.3(b)** the questions relevant to device performance are –

Charge trapping

1. What causes the charge to be trapped?
2. What is the time constant associated with the charge trapping? Does the time constant depend on the bias stress (V_{ds}, V_{gs}) on the device?

Charge Detrapping

1. How does detrapping occur?
2. What is the time constant associated with the detrapping process?

4.2.2 Virtual Gate Potential, V_{VG}

The virtual gate potential V_{VG} is a measure of the total trapped charge in the device. By definition, V_{VG} has its zero value when the device structure is in the as-grown condition i.e. when the device has just come out of the growth chamber. In this condition the sheet charge anywhere in the channel is that which

is measured by Hall measurements. After fabrication of the device is complete, and before any bias is applied to the device, V_{VG} is again at this zero value, assuming that the surface of the device remains in the as-grown condition. Any applied bias on the device changes V_{VG}. In the device I-V plane, the potential on the virtual gate becomes increasingly reverse biased, as indicated in **Fig 4.4**. The general trend is that the virtual gate becomes reverse biased when the gate is biased toward pinch-off and the drain bias is increased. In any dynamic measurement such as a load pull power measurement, the current available at any point during the cycle is dependent on the instantaneous trap occupancy, or the instantaneous value of V_{VG} at that point. *It is also clear that ability of the metal gate to decrease current is never impaired since to decrease the current, the trap occupancy (or equivalently, the magnitude of the reverse bias on the virtual gate) must either remain unchanged or increase. It is the ability of the metal gate to increase the current that is impaired since that requires the trap occupancy to decrease (and the virtual gate to become less reverse biased).*

4.2.3 Time constants of interest

There exists an equilibrium trap occupancy and value of V_{VG} associated with every point on the I-V plane of the device. On the load line shown, V_{VG} is most positive for point A, denoted $V_{VG,A}$ and most negative for point B, denoted $V_{VG,B}$. A quiescent trap occupancy condition and value of $V_{VG,Q}$, is established as the result of the dc bias applied to the device. As the device moves from A to B through the load line the actual current measured at any point depends on the instantaneous trap occupancy. V_{VG} is a complex function of the spatial distribution of the total trapped charge. The trapping of electrons corresponds to making V_{VG} more negative and detrapping of electrons corresponds to making V_{VG} less negative. The time constant associated with the process of making V_{VG}

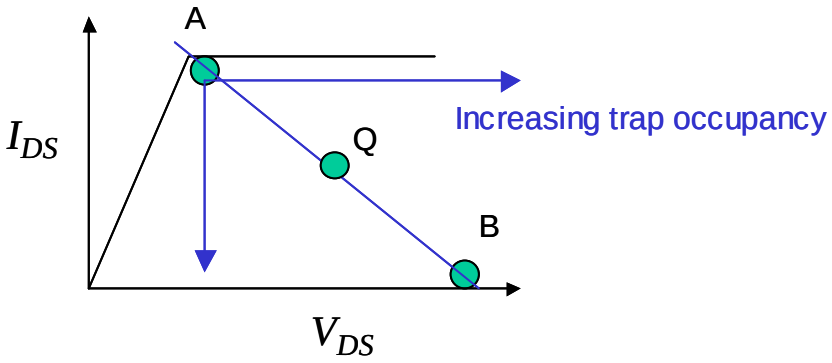


Fig 4.4 This shows the trend of increasing reverse bias or increasing trap occupancy on the I-V plane of the device. The arrows point in the direction of increasingly negative V_{VG}. On the load line, V_{VG} is most negative at point B and least negative at point A.

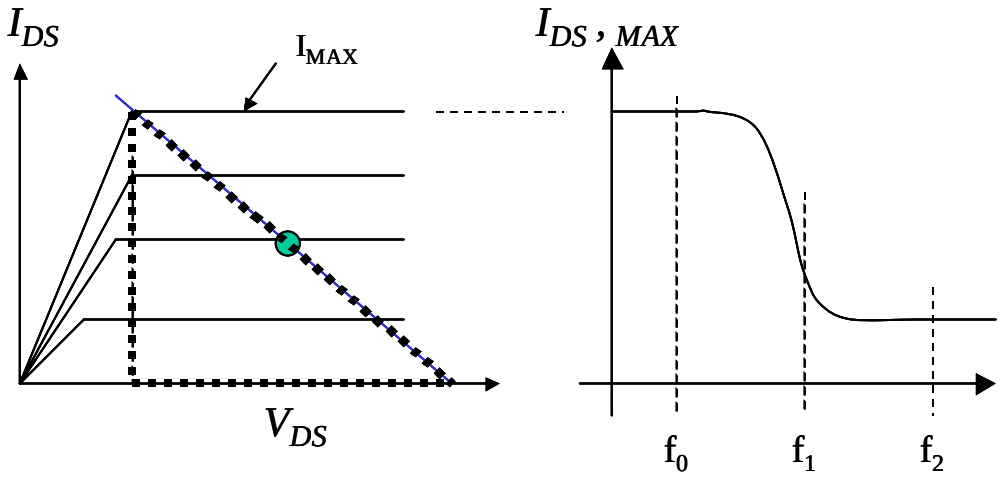


Fig 4.5. Expected plot of the maximum drain current as a function of frequency

less negative is denoted as T_{DETRAP} and that associated with making V_{VG} more negative is denoted as T_{TRAP}. The time constants T_{DETRAP} and T_{TRAP} depend not only on the emission and capture constants of the surface traps but also on the spatial location of the traps. The movement of charge on the surface depends on the surface mobility of the electrons which is a function of the electric field at that point. As already observed in chapter 3, the surface electric field depends on the distribution of trapped charge. Hence it is expected that the time constants T_{DETRAP} and T_{TRAP} are related to the emission and capture times of the traps in a complex manner. The time constants T_{DETRAP} and T_{TRAP} depend on the initial and final values of V_{VG} and hence are measurement dependent i.e. dependent on the initial position of the device in the I-V plane and the load line along which the device moves during the measurement.

Consider the ideal situation of **fig 4.3(a)** where the device is biased in class A (I_{DS},quiscent = $I_{MAX}/2$) and the device is driven with an input of sufficiently large amplitude to drive it to the limits of I_{DSS} and V_{MAX}, shown as points A and B on the load line. To go from the quiescent bias point (Q) to point A, the time taken is T/4, where T is the time period of the input signal. Let T_{DETRAP} denote the time it takes for the potential of the virtual gate V_{VG} to change from $V_{VG,Q}$ to $V_{VG,A}$. We only consider the detrapping time constant in this measurement since it is only the detrapping process that limits the maximum current. Clearly the maximum output current now depends on the relation between these three time constants. Now consider the two cases,

Case 1 : $T_{DETRAP} << T/4$

In this case, the trap occupancy exactly follows the input signal. Hence the available current is exactly as that measured from dc measurements since, as far as the traps are concerned, at each point the trap occupancy is the same as when the device is held at that point in a dc measurement.

Case 2 : T_{DETRAP} >> T/4

In this case the trap occupancy is not at equilibrium with the input signal. The maximum current available from the device depends on the steady state V_{VG} (or trap occupancy). What is the steady state V_{VG} in this case? In steady state the V_{VG} is that which is associated with the time average values of the current and voltage in the device.

In GaN HEMTs the measured power at microwave frequencies is smaller than that predicted from the DC values of maximum current. The measured power at microwave frequencies such as 4-8 GHz measured at UCSB and reported by several groups is lower than that obtained by inserting the values of I_{MAX} and ($V_{BREAKDOWN}$-V_{KNEE}) as measured using a curve tracer or a HP 4145B Parameter Analyzer into eq. 4.1. It was supposed therefore that there existed a frequency f_0 corresponding to which T/4 = T_{DETRAP}. Hence for input frequencies well above f_0, T_{DETRAP} >> T/4 and the maximum current is now given by the steady state value of V_{VG} and for input frequencies well below f_0, the maximum drain current is the same as is measured at dc. Hence it was expected that a plot of the maximum drain current as a function of frequency would look like as shown in **fig 4.5.** The problem remained of finding the frequency f_0. Note that this is essentially a measurement of the detrapping time constant. In order to find this frequency, a large signal measurement of the maximum drain current as a function of input frequency was set up.

4.2.4 Measurement of detrapping time constant.

Frequency response of maximum drain current

The experimental set up as shown in Fig 4.6 was used. The frequency response of the maximum drain current using a similar set up was reported by [4]. In the frequency range 0.1 mHz – 20MHz, a HP 3325 signal source was used to

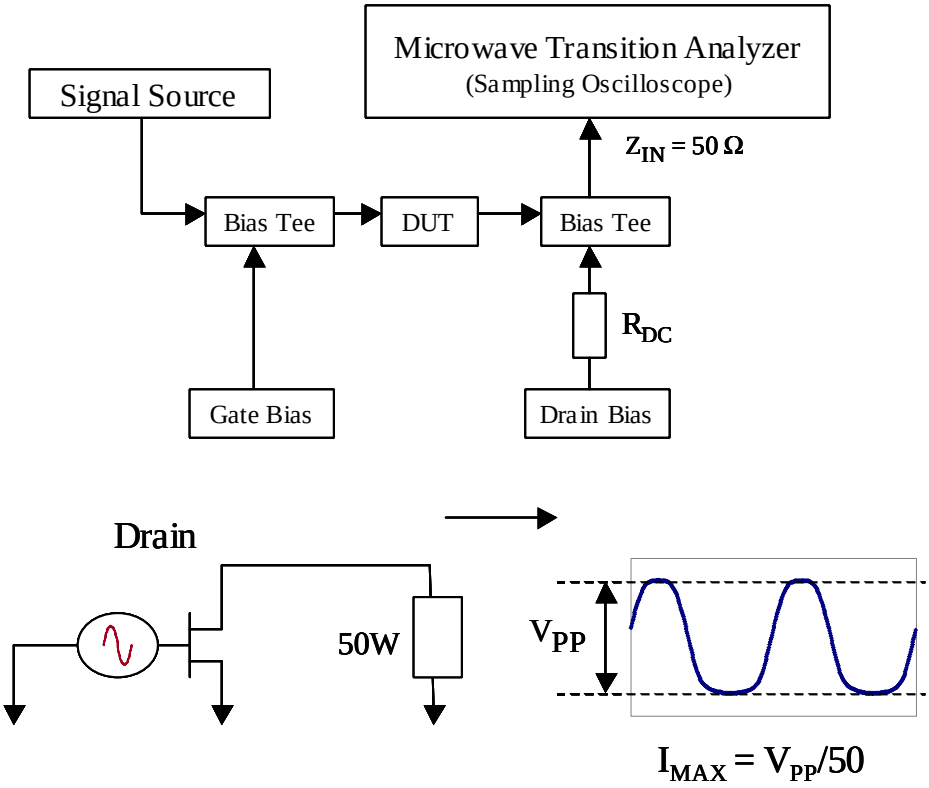


Fig 4.6. The experimental set up to measure frequency response of maximum drain currents.

supply both the gate DC bias and the sinusoid input drive signal. In the frequency range 20MHz – 2GHz, a Wiltron signal source was used to supply the input drive and DC gate bias was applied through a bias tee. In the frequency range 0.1mHz – 1MHz, the drain was connected to the bias supply through a 50 ohm load resistance. The voltage at the drain was monitored using a 500MHz HP 54510 digitizing oscilloscope. No bias tee was used. In the frequency range 100kHz - 2GHz the drain was connected to an HP 70825 Microwave Transition Analyzer (MTA). The drain bias was supplied through an external bias tee. The MTA provides an input impedance of 50 ohms over the entire frequency range of interest and was used as an load impedance and also as a high frequency oscilloscope to measure the AC waveform at the drain. No dc signal can be present at the input port of the MTA which meant that bias tees had to be used in order to use the MTA. Hence the low frequency limit of the external bias tees decided the frequency range over which the MTA could be used.

The measurement consisted of first applying the gate bias and the input gate RF signal. The drain bias was then applied and the output waveform at the drain recorded. The drain bias was applied for a short duration, typically 30 seconds, to prevent any long term degradation of the device due to heating effects. The input power to the device was increased until the output drain waveform displayed a truncated sine wave, thus indicating the saturation of the drain current in both the open channel and pinched off condition. This measurement was then repeated with the input frequency changed. In between two frequency points, the drain bias was turned off to prevent the degradation of the device. When the measurement was performed in this manner, the maximum drain current obtained from a device showed a decrease as frequency was increased apparently indicating that there existed a transition frequency f_0. However when the measurement was repeated starting at a different frequency a similar decrease was

obtained. It appeared that the a decrease with frequency was always observed but this depended more on the history of the measurement than the actual frequency of measurement. **Fig 4.7** shows two successive series of data points taken at increasing frequencies on the same device. The time interval between successive measurements is approximately one minute. Note that the peak current at the same frequency is lower for the second series**.** This behavior was observed for nearly all the devices studied. These observations suggested that the occupancy transient of the traps is what is really being measured in this measurement.

Note that there are two time constants of interest in this measurement, a trapping time (T_{TRAP}) in which the steady state trap occupancy corresponding to the quiescent bias condition of the measurement is established and a detrapping time (T_{DETRAP}) which determines the frequency response of the maximum drain current. When the trapping time constant is sufficiently long in comparison to the time needed to obtain a data point, care must be taken to ensure that the trap occupancy reaches its steady state value before measuring the frequency response of the maximum drain current. *Interpreting the data shown in Fig 4.7 as a frequency dependence of the maximum drain current is erroneous.*

By simply operating the device for a few minutes under large signal RF drive, the equilibrium trap occupancy was established. Fig 4.8 shows the maximum drain current as a function of frequency obtained after steady state was established. The device was biased in class AB, ($I_{DS,QUISCENT} = I_{MAX}/4$). As the input power increased, the device self biased up to the class A bias point. The gate bias was dynamically adjusted to obtain roughly a symmetric square wave at the output i.e. the time average value of the drain current was half the peak to peak value of drain current. It was found that under large signal overdrive the initial bias point did not matter, the device self biased up to the same point. The dc and ac load resistance was set to 50Ω to ensure that the device stayed on the same

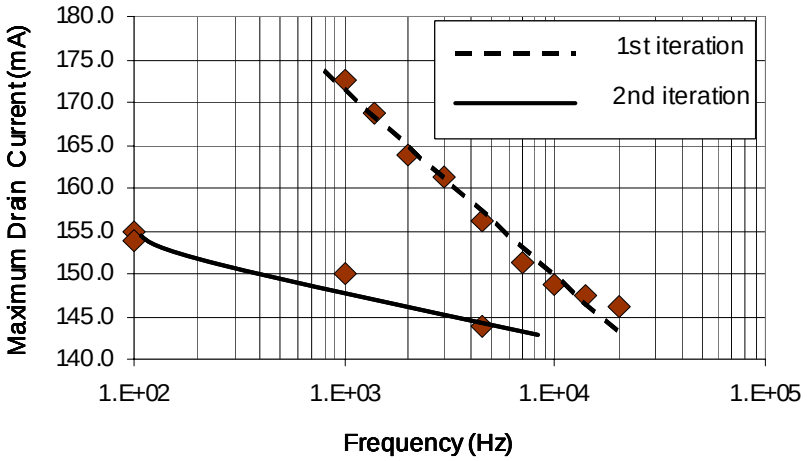


Fig 4.7 Two successive series of data points taken at increasing frequencies on the same device. The maximum current is lower for the second iteration, suggesting that what is being measured is a transient response, rather than a steady state frequency response.

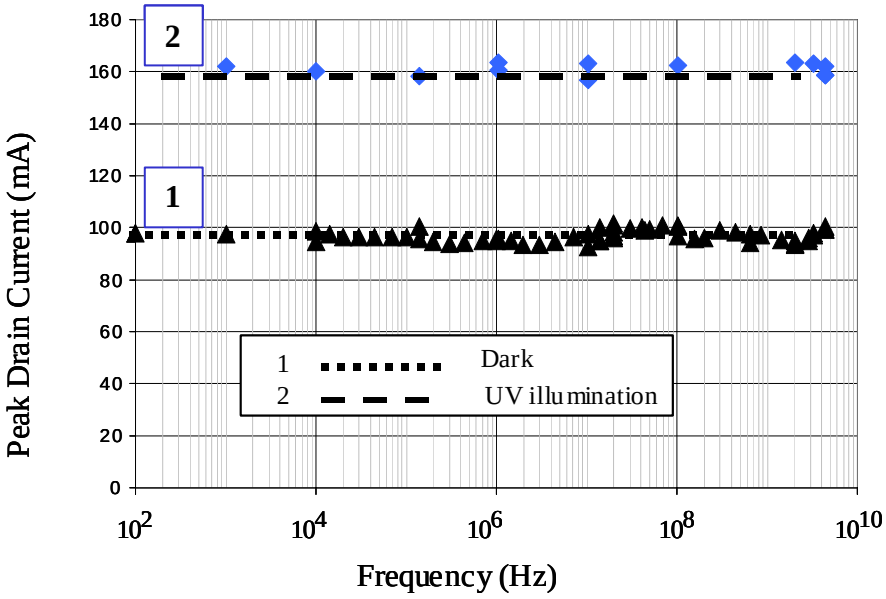


Fig 4.8 shows the maximum drain current as a function of frequency obtained after steady state was established. The device was biased in class AB, ($I_{DS,QUISCENT} = I_{MAX}/4$), V_{DD}=14V

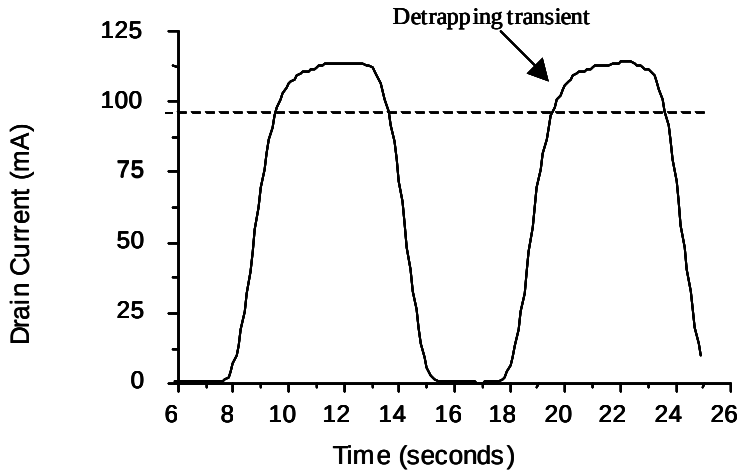


Fig 4.9 Output current waveform at 0.1Hz .The detrapping transient can be observed in the upper half of the drain current waveform. The detrapping time constant is on the order of seconds.

load line irrespective of any change in device characteristics. The maximum drain current remained approximately constant, independent of frequency from 10 kHz to 1 GHz. Note that the detrapping time in these devices is fairly long as compared with an input signal of even 10 kHz. Hence the maximum drain current is independent of frequency for frequencies greater than 10 kHz. The experiment was repeated with UV illumination from a HeCd laser incident on the device. It was found that the current was now restored to its maximum value. This observation is explained later in this chapter.

When the frequency of the input drive is lowered to below 0.1Hz the detrapping transient can be observed in the upper half of the drain current waveform shown in **Fig 4.9**. The detrapping time constant was hence observed to be on the order of seconds.

4.2.5 Measurement of trapping time constant

The measurements of the previous section showed that the detrapping time constant was on the order of seconds. In order to understand the nature of current collapse during a microwave power measurement, a different measurement schematic as described below was implemented.

The measurement schematic is as shown in **fig 4.10(a).** First, the gate signal is applied. This gate signal is chosen on the basis of the dc transfer characteristic and is of sufficiently large amplitude to drive the device hard into saturation. Then the drain bias is pulsed on. The voltage across the 50 ohm load, and hence the drain current, is measured. The envelope of the output waveform shows the decay of the maximum drain current due to the occupancy transient of the traps i.e. the formation transient of the virtual gate.

Measurement of trapping time constant tells us two things –

1. The time taken to trap electrons to create the virtual gate

2. The extent of current collapse, or the magnitude of the reverse bias on the virtual gate.

The extent of current collapse depends on the steady state value of V_{VG}. This potential depends on the bias point and the extent to which the device is overdriven beyond the linear gain regime. The aim of these measurements is to understand the nature of collapse when the device is operated as an amplifier and driven to saturation, hence these measurements were made under similar drive conditions. The sequence of bias applied to the device is shown in **fig 4.10(a).** Note that the time taken for the drain bias supply to reach its desired value is ~ 100ms. This is hence a limit of the measurement system on the smallest transient that can be measured. During this time, a virtual gate of ill-defined extent is formed, leading to an initial collapse of the drain. This means that the initial value of the peak current is lower than the true maximum current. To ensure that the initial maximum value is the same for all measurements, the experiment was repeated as follows. UV light from a white light source is incident on the device while both the gate and drain biases are applied. At this point the maximum drain current is available from the device. Then the UV light is cut off and the decay of the output waveform measured. This measurement sequence is shown in **fig 4.10(b).**

Dependence on drain bias.

By choosing different V_{DD}, the drain supply voltage, we can scan across the IV plane, as shown in **Fig 4.11** and observe the effect of drain bias on the creation and potential of the virtual gate. Note that the initial value of the maximum current is different at different drain biases. This is because of self heating. **Fig 4.12** shows the trapping transient in the dark at different drain biases obtained from an unpassivated device. The data is shown normalized to its initial ***maximum value. DC I-V measurements were taken after each data point and***

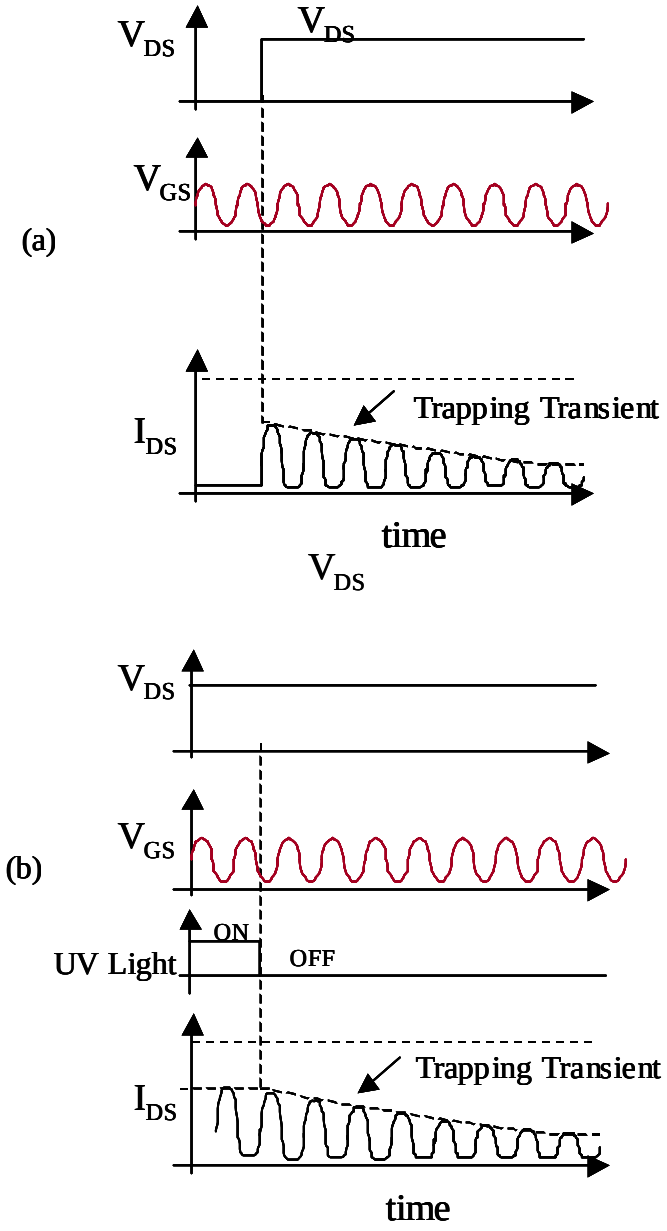


Fig 4.10 Measurement of trapping time constant, showing biasing sequence.

(a) shows the measurement in the dark and

(b) (b) shows the alternate measurement with UV illumination as the initial condition.

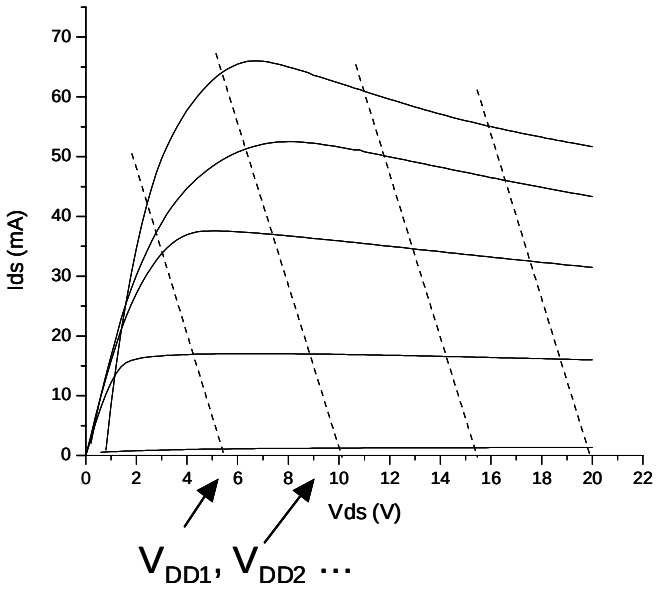


Fig 4.11 Scan across the IV plane by choosing different V_{DD}, the drain supply voltage, to observe the effect of drain bias on the creation and potential of the virtual gate.

showed that permanent degradation as a result of bias stress did not occur. The frequency of the input signal was 10 kHz, chosen so that the trapping time constants are much longer than the time period of the waveform and so the envelope can be easily measured. The trapping transients can be fit to a stretched exponential of the form below

$$I = I_0 + I_1 \, e^{-(t/\tau)\beta} \quad \textbf{(4.3)}$$

Here (I_0+I_1) is the maximum current $I_{DS,MAX}$ (when no virtual gate exists, or when t = 0), I_0 is the steady state current, I_1 indicates the extent of the current collapse, τ is the time constant associated with the trapping process and β the stretching parameter, tells us how much the decay deviates from the exponential. Values of β lie between 0 and 1, and a lower value of β tells us that the decay deviates more from the true exponential. In other words, a lower value of β, indicates that as the decay proceeds, the driving force that causes the decay decreases and hence the decay decreases. This kind of behavior indicates a very field dependent decay, since as the current collapses, the electric field that induces collapse decreases.

From **fig 4.12**, observe that for higher drain biases, I_1 increases, indicating that the extent of drain current collapse is larger for larger drain biases. The time constant τ is smaller for larger drain biases indicating that the decay proceeds faster at larger drain bias. The stretching parameter B also becomes smaller, indicating that the trapping transient is more non exponential and hence more field dependent.

Fig 4.13 shows a comparison of the normalized trapping transients on an unpassivated device obtained when UV light is incident on the device compared with trapping transients obtained in the dark. The trapping transients are fitted to the stretched exponentials of the form of equation (4.3). The decay curves

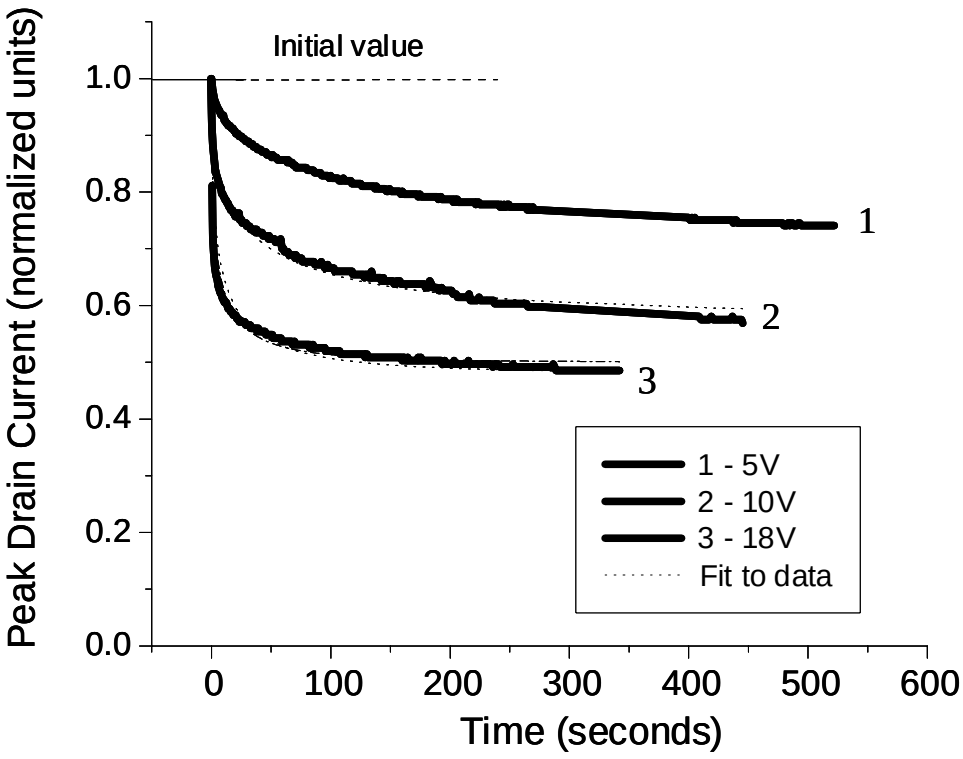


Fig 4.12 The trapping transient in the dark at different drain biases obtained from an unpassivated device.

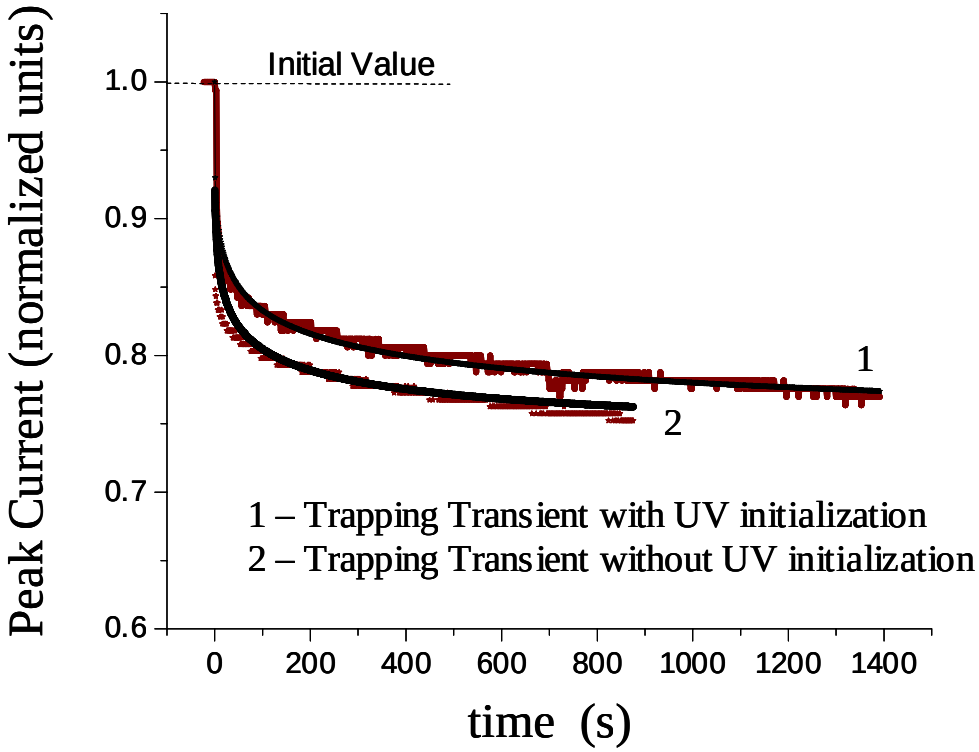


Fig 4.13. Comparision of the normalized trapping transients on an unpassivated device obtained when UV light is incident on the device with trapping transients obtained in the dark

obtained with UV illumination as the initial condition consistently have larger time constants than those obtained in the dark.

To see how the recovery of current depends on the wavelength of the incident light, low pass filters (i.e. transparent for wavelengths above a cut-off wavelength) were inserted between the UV light and the sample. First, the steady state collapsed current value was obtained under dark conditions. Then low pass filters of different cut-off wavelengths, in the order of decreasing wavelength (increasing energy) were inserted and the new steady state maximum current measured. A plot of the steady state maximum current with respect to filter cut-off in eV is shown in **fig 4.14**. The above observations are explained in the next section.

4.2.6 Mechanism of current collapse and recovery

1. When the wafer is in the as-grown condition, there exists net positive charge on the surface.

2. The formation of a virtual gate is due to a reduction in the amount of net positive charge on the surface. This can occur by trapping of electrons on the surface in donor like states. The parameter that now determines the drain current from the device is the potential on the virtual gate, referred to as V_{VG}.

3. How does current collapse occur in the dark? In the dark, when the bias is applied, the process of current collapse is simply a function of how quickly the reverse bias on the virtual gate increases. This is dependent on the supply of electrons to fill up the empty surface states. If these electrons come from the gate metal, then this supply is limited by the field at the gate that induces the leakage and the surface mobility of electrons.

4. The strong dependence of trapping transient on drain bias and its excellent fit to a stretched exponential indicates that the trapping process is strongly dependent

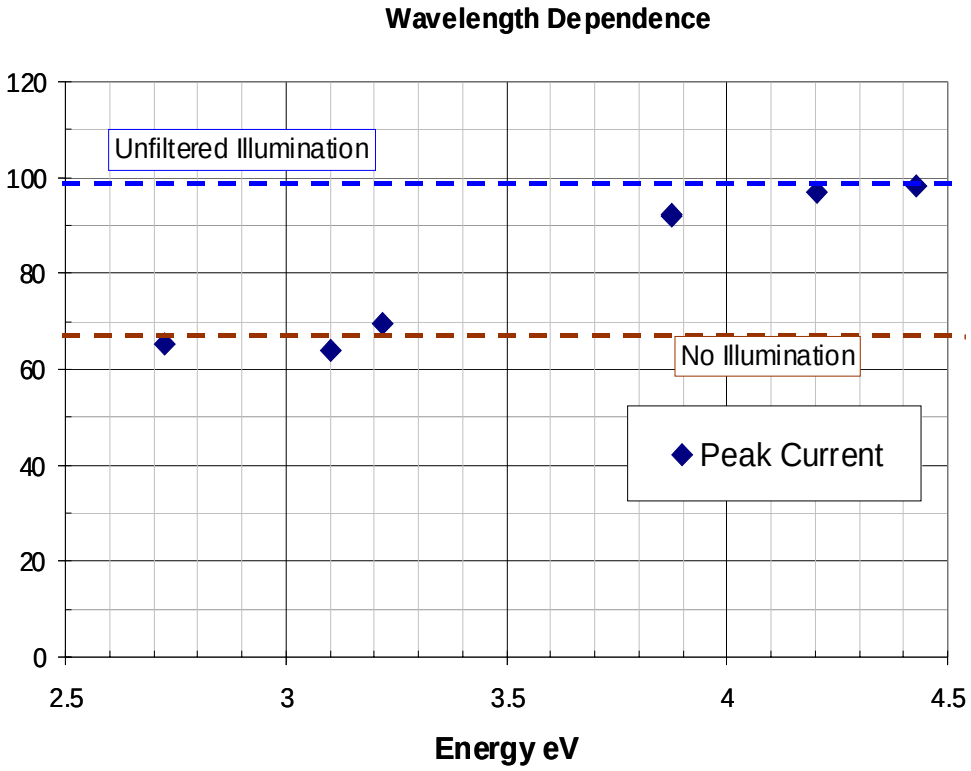


Fig 4.14 The steady state maximum current with respect to filter cut-off in eV. The frequency of measurement was 200 MHz. The measurement schematic is as shown in fig 4.10(b). The steady state current obtained when light is incident on the sample is shown.

on the electric field between the gate and the drain. As the trapping proceeds, the depletion region extends due to the formation of the virtual gate. When this happens, the electric field at the gate edge is reduced, reducing the surface leakage current and unoccupied surface states are located continuously further from the metal gate, hence reducing the rate at which the depletion region extends.

5. In order to restore the current to its value the net positive charge on the surface must be restored i.e. V_{VG} is forward biased, or the virtual gate is neutralized. This can be done as follows,

a) Electrons trapped in the surface states are removed. This can happen when the metal gate is forward biased with respect to the source and drain. However this method of current recovery is not a complete recovery, the extent to which the current recovers varies across devices and wafers.

b) Incident photons of energy greater than band gap induce the formation of electron hole pairs in the GaN channel. The holes are pulled to the surface by the electric field in the AlGaN . The accumulation of holes at the surface forward biases the surface, again eliminating the virtual gate. The process of virtual gate formation and its neutralization by incident photons is shown in **fig 4.15 and fig 4.16.**

c) Incident photons knock electrons out of the surface traps. However this is not a likely possibility. *Why?* It is necessary for above band gap UV light to be present to neutralize the virtual gate. The surface donor level reported in the literature is 1.42 eV [13] and 1.65 eV[14]. The data shown in **fig 4.14** clearly suggests that above band gap light is necessary, indicating that holes play a major role in the photon induced neutralization of the virtual gate.

6. How is the process of current collapse different when the initial condition is caused by the presence of incident photons? The electrical conditions (drain bias

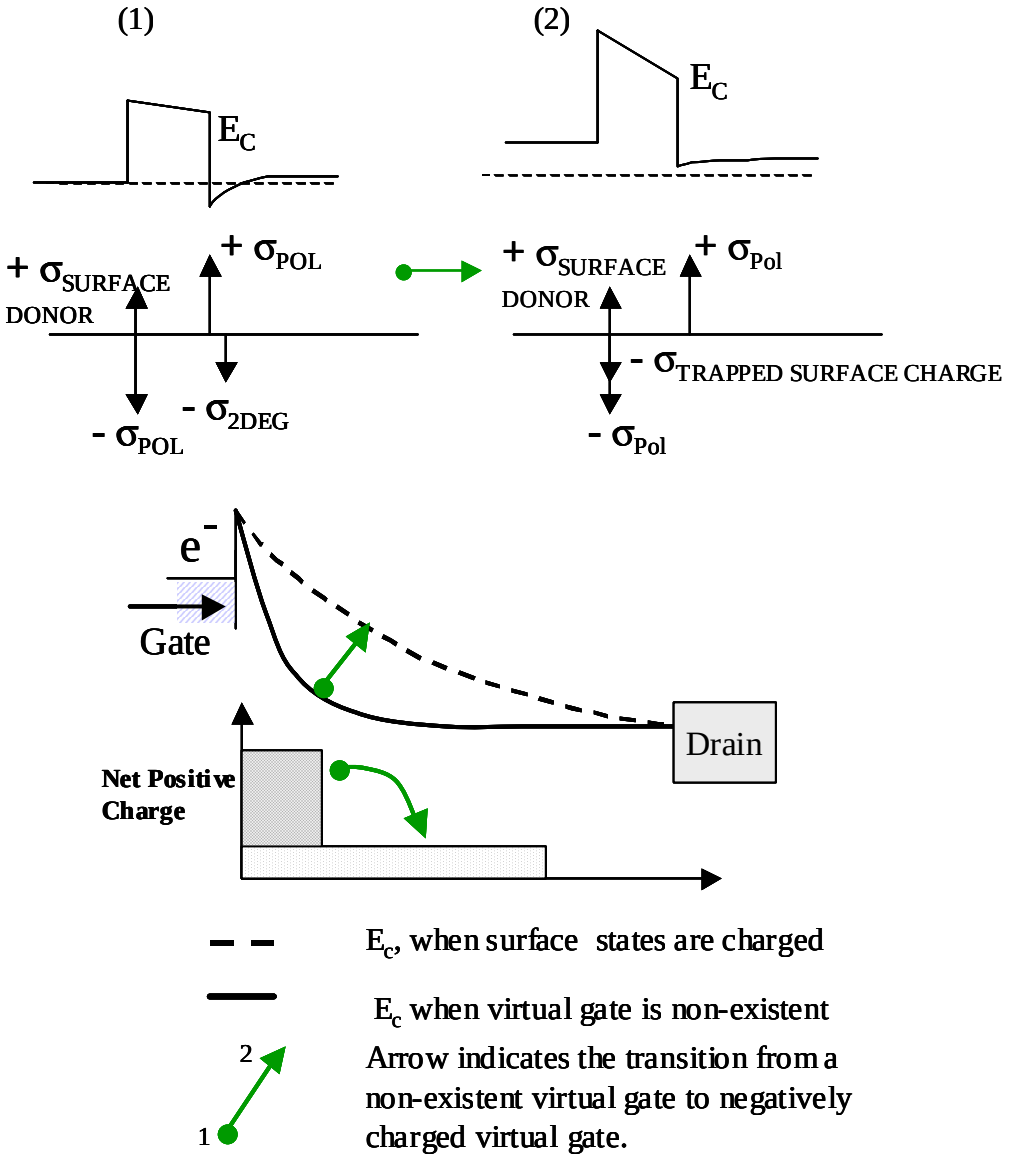


Fig 4.15. Band diagram of the AlGaN/GaN heterostructure showing the transition from a non-existent virtual gate to the a negatively charged virtual gate. The surface negative charge reduces the effective donor density leading to an extension of the depletion region as shown.

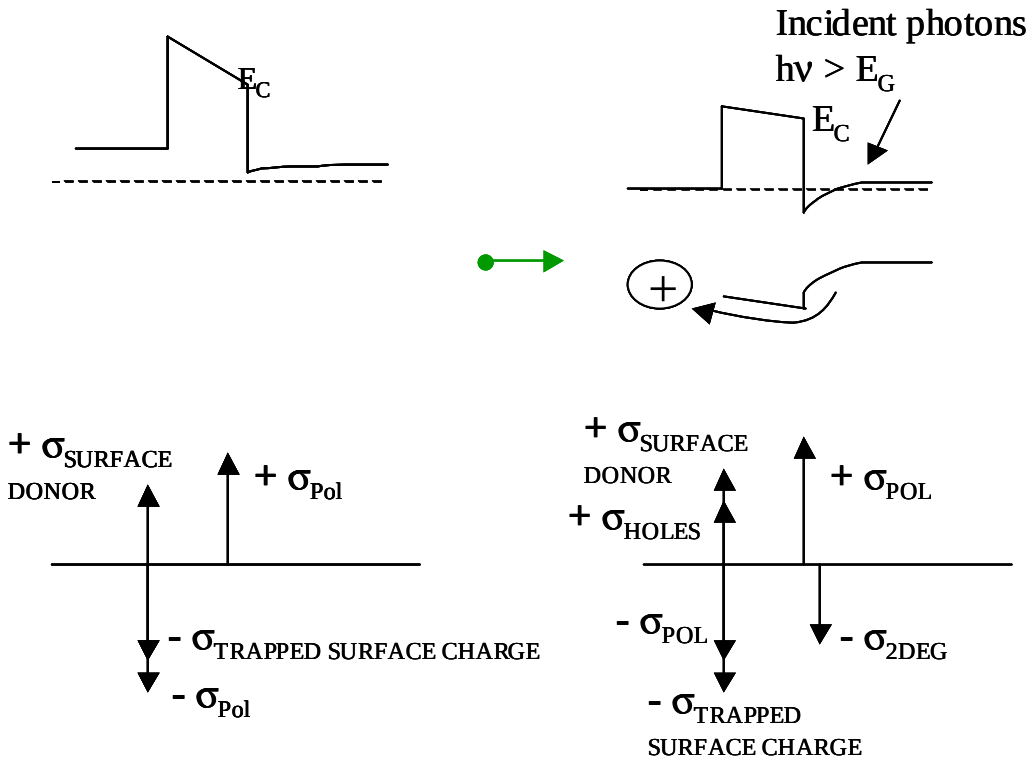


Fig 4.16. The effect of incident photons. Holes generated in the GaN channel are swept to the surface. The positive charge due to the holes neutralises the virtual gate.

voltages and drain voltage RF swing) that cause the formation of the virtual gate are always present. The difference from the situation in the dark is the presence of holes. The holes accumulated at the surface, very close to the gate are swept into the gate metal by the large electric field at the edge of the gate metal. This causes the virtual gate to reform very close to the metal gate. Now, there exist three processes that occur simultaneously and lead to the extension of the virtual gate.
a) Holes farther away from the metal gate, are driven by the electric field (caused by the drain gate bias) towards the metal gate. Note that the movement of these holes is limited by the small surface mobility of these holes.
b) Holes on the surface at any point, recombine with the electrons trapped in surface states. This causes some of the surface states to empty.
c) Electrons leaking from the gate metal, are driven by the field (caused by the drain gate bias) towards the drain. These electrons are trapped in the empty, available surface states. Note that the rate at which the electrons are trapped in the surface states (assuming that there exist empty surface states) is limited by the supply of electrons. If these electrons come from the gate metal, then this supply is limited by the field at the gate that induces the leakage and the surface mobility of these electrons.

Note that process 6(a) leads to the increase of the reverse bias on the virtual gate. Process 6(b) leaves the surface unchanged electrostatically. Process 6(c) leads to increase of the reverse bias on the virtual gate. However for process 6(c) to occur, surface states must be available (empty) for electrons to be trapped. This can occur only when holes recombine with the electrons in surface states, i.e. only after process 6(b) occurs. Due to this, the rate at which the virtual gate reforms is limited by the slower of the two processes, electron hole recombination, and electron trapping in empty surface states. Since e-h recombination is unique to the

experiment with UV initialization, the measurements indicate that e-h recombination is the rate limiting process.

4.3 Surface passivation

4.3.1 The effect of passivation by SiN

All the measurements described so far were made on unpassivated devices. Typical trapping transients obtained on passivated and unpassivated devices on the same wafer are compared in **fig 4.17**.

Observe that for the passivated device, the extent of current collapse at the same drain is much smaller than on unpassivated device. Although the amount of current collapse does increase slightly at higher drain biases the magnitude of collapse is very much smaller in the passivated device. Also, for passivated devices, there is very little difference between the trapping transients with the UV illumination as the initial condition and those measured in the dark.

Continuous wave (CW) load pull measurements at 6GHz on a passivated device is shown in **fig 4.18**. Typically passivated devices obtained output powers greater than 6W/mm compared to a typical value of 4W/mm on unpassivated devices. A similar effect on microwave power output after SiN passivation was reported by Green **[15].**

4.3.2 The mechanism of surface passivation

These results demonstrated that surface passivation prevented current collapse by preventing the formation of the virtual gate. However, the mechanism by which this occurs is not clear. Some possible mechanisms by which this occurs are listed below.

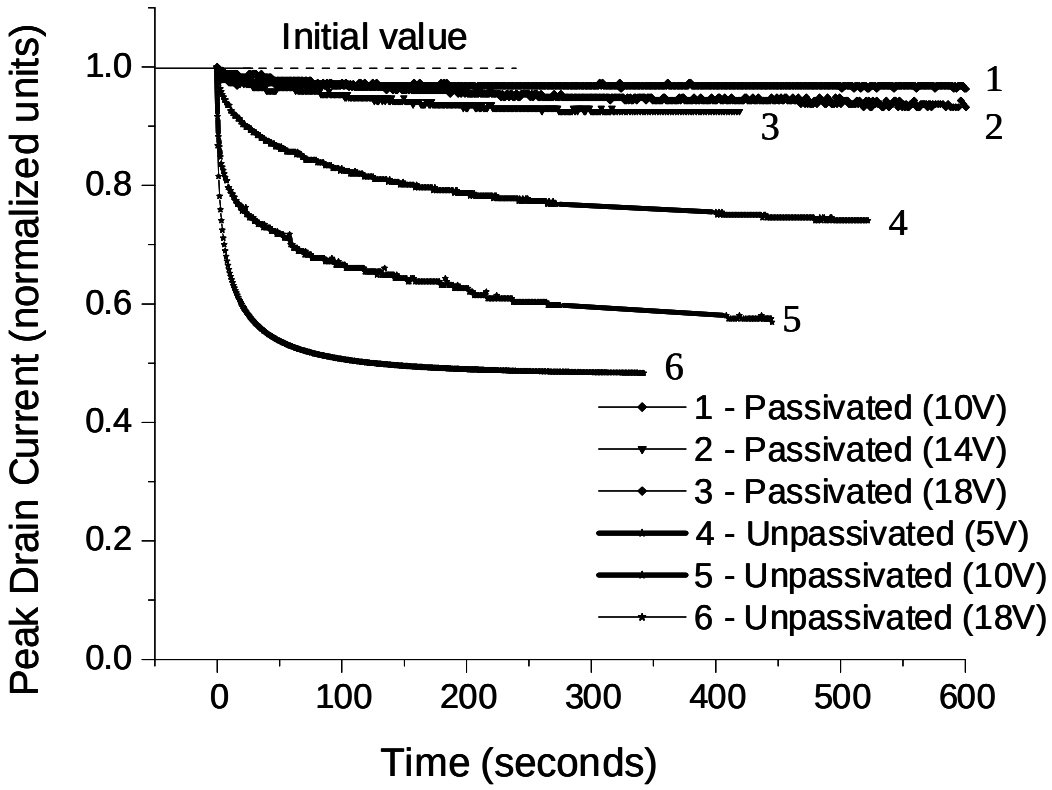


Fig 4.17 Comparision of trapping transients obtained on passivated and unpassivated devices on the same wafer. The extent of current collapse is much smaller on the passivated devices and its dependence on drain bias is also reduced.

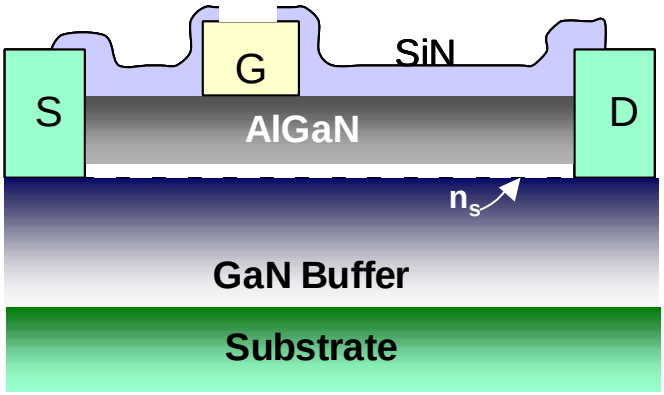
1. The passivant buries the surface donors and make them inaccessible to electrons leaking from the gate metal. Hence, trapping of the electrons leaking from the gate is prevented.

2. The process of depositing the passivant causes Si to incorporate as a shallow donor at the AlGaN surface in sufficiently large quantities to replace the surface donor.

3. In addition to making the surface states inaccessible to electrons leaking from the gate, the passivant or the process of depositing the passivant changes the energy level of the surface donor. This mechanism is likely since it is observed **[16,17]** that depositing the SiN passivant results in an increase of the 2DEG density. An increase of 2DEG density must mean that the electric field in the AlGaN layer must change as shown in **fig 4.19**, since the process of passivation cannot change the band diagram in the bulk of the GaN. This change of electric field implies that the surface pinning level is now smaller as shown in **Fig 4.19.**

4.3.3. Gain compression in GaN HEMTs

Despite the suppression of current collapse by passivation, the power performance of these devices is below optimum. Shown in **fig 4.20** is the power performance of a typical GaAs power HEMT **[9]**. Note that the gain is almost constant until the output power saturates. The maximum output power is obtained at approximately 2dB gain compression. This is compared to a typical unpassivated GaN HEMT (**fig 4.21 (a**)), a passivated HEMT adjacent to the unpassivated GaN HEMT (**fig 4.21 (b**)), and finally the same unpassivated HEMT with UV light incident on it, (**fig 4.21 (a**)). Note that the gain of the unpassivated GaN device continuously decreases and the maximum output power is obtained at nearly 10 dB compression. The passivated device has better output characteristics. The gain roll off starts at a higher input power than the unpassivated device but



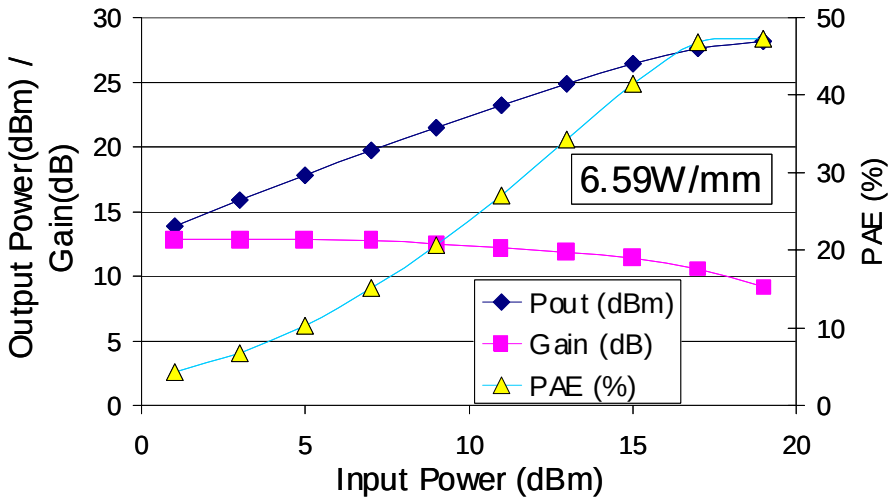


Fig 4.18 load pull measurements at 6 GHz on a passivated device. Typically, passivated devices obtained ~6W/mm output power and unpassivated devices obtained ~ 4W/mm.

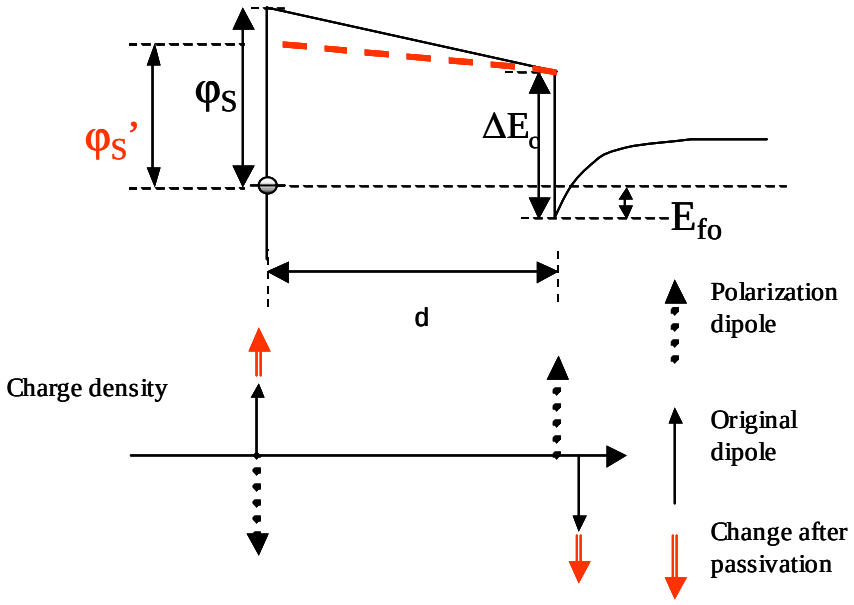


Fig 4.19 Effect of passivation on the surface pinning level.

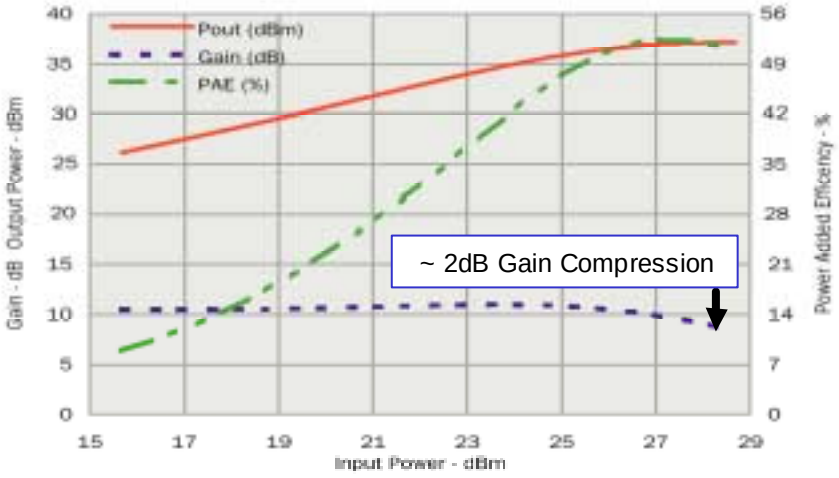


Fig 4.20 TriQuint Semiconductor Commercial Power GaAs HFET (TGF4260) Power Performance

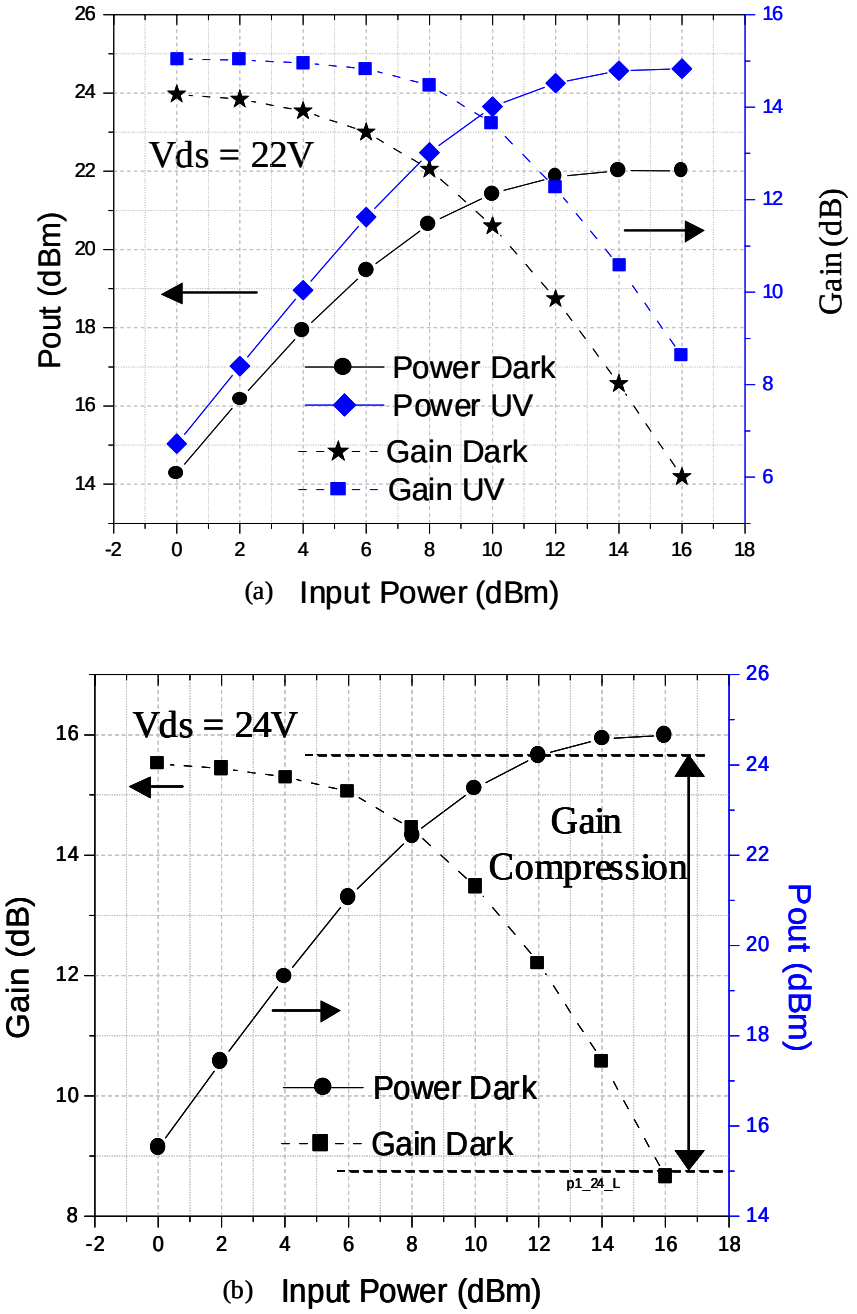


Fig 4.21(a) Unpassivated device. Dark and Illuminated Power Performance (b) Passivated device.Dark Power Performance

decreases in a similar fashion and the maximum output power is obtained at 7 dB gain compression. When UV light is incident on the unpassivated device, output power is higher, but the gain compression is still evident and maximum power is obtained at 7 dB compression. This gain compression remains a severe problem in the design of amplifiers using these devices and further work needs to be done to understand the reason for this behavior.

4.4 Conclusions

It was shown in this chapter that current collapse observed during a microwave power measurement is the consequence of the creation of a second virtual gate located between gate and drain. Accumulation of negative charge on the surface results in a reverse biased virtual gate. It is proposed that the charging up of the surface is caused by positive donor states accepting electrons and becoming charge neutral. The spatial extent and total negative charge stored in this second negative gate depends on the quiescent bias condition and magnitude of the RF swing on the device. The time constant of the surface traps was measured to be on the order of seconds. Great care should be taken when making parametric measurements on these devices since the initial conditions and the time to establish a steady state can impact the interpretation of measured data. It was shown that current collapse can be decreased to a very large extent by passivating the surface of the device with a layer of silicon nitride, thus proving that surface states are responsible for current collapse. Although further experiments are necessary to establish the mechanism by which passivation prevents current collapse, it is clear that the passivant prevents the formation of the virtual gate by preventing the positive sheet charge at the surface from being compensated.

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Chapter 5

Conclusions and Future Work

5.1 Conclusions

At the start of this work, the power performance of GaN HEMTs was already much improved from its embryonic stage in 1995, when the first GaN based FETs were demonstrated. An output power of 2.6-3.3 W/mm at 8-18GHz **[1]** had been demonstrated at UCSB and were the highest demonstrated CW output power densities at these frequency from a solid state device. However, despite these impressive power results, the physics and technology of these devices was far from well understood. The origin of charge in the AlGaN/GaN heterostructure was unclear. Current collapse was the biggest obstacle to obtaining reproducible power performance and it represented an unsolved problem. The link between the nature of the free AlGaN surface to device characteristics was not recognized. The very large breakdown voltages observed and their dependence on gate drain separation was not understood. The progress made in GaN HEMT research during the course of this work is summarized below.

5.1.1 Growth of Bulk GaN and AlGaN

Work performed by Keller **[2]** demonstrated that oxygen was the dominant impurity resulting in the n-type conductivity in unintentionally doped GaN films grown at UCSB by MOCVD. The development of proper pre-growth wafer and reactor preparation resulted in background electron concentrations as low as 10^{16} cm^{-3}. Better control of compensating mechanisms such as carbon and dislocation related deep levels was achieved through optimization of the growth conditions. SIMS investigations performed by Parrish and Keller **[3]** on the dependence of native and intentional impurity (C,H,O,Si) incorporation resulted in the development of semi-insulating films with lowered concentrations of trapping sites while still retaining good pinch-off characteristics. The dominant strategy employed in the S.I. buffer development was to reduce the concentration of

background donors and precisely control the density of compensating centers to just compensate the background impurities.

Optimization of the growth of AlGaN layers resulted in simultaneously improving the structural quality and minimizing the concentration of defects resulting in deep levels. Structural problems such as cracking and grain formation were minimized by Keller **[4]** for AlGaN layers with up to 50% Al. Optimization of impurity incorporation in such films of high structural quality were performed by Parrish and Keller **[3].** These improvements in growth conditions resulted in improvement of the output power density to 4.6W/mm. However, an uncontrolled variable in these experiments has always been the free AlGaN surface. Hence, the effect of the different growth conditions on the AlGaN might have influenced the surface trapping effects and hence the power results. A controlled separation of the contribution of bulk and surface trapping effects requires precise knowledge of the contribution from at least one source of current collapse. This is a subject of future work as discussed in section 5.2.2. However, the average output power from unpassivated devices increased from 2W/mm to 4W/mm **[5]** on account of the optimization of growth parameters.

5.1.2 Surface States - The importance of the free surface of the AlGaN

The presence of surface states was first suggested by measurements of surface potential between gate and drain using floating gates as potential probes **[6]**. The measurements showed that the surface became negatively charged under large gate drain biases in the off-state. The lateral extent of the gate depletion region was measured using floating gates. It was found that the depletion region extent was inconsistent with the ionized positive donor density in the AlGaN. This indicated that the ionized positive donor charge along gate to drain was compensated by negative charge. It was hypothesized that electrons

leaking from the gate metal were trapped by surface states, making the surface negatively charged, and extending the gate depletion region.

The large spontaneous and peizoelectric polarization coefficients of the GaN material system lead to the presence of a polarization dipole with charge at each face of the AlGaN layer in an AlGaN/GaN heterostructure. It was shown that in Ga-face crystal, the electric fields due to this polarization dipole raise the energy of the AlGaN surface in a HEMT structure and lead to the formation of positively charged donor-like states at the free AlGaN surface and a negative charge sheet (2DEG) at the AlGaN/GaN interface. The dipole formed by the positively charged surface states and the 2DEG compensates the polarization dipole and lowers the crystal energy. The 2DEG channel in the HEMT structure thus arises from electrons donated by the positive donor-like surface states. A model was developed based on Fermi level pinning at the surface due to a single donor level at E_{donor} below the AlGaN conduction band edge. The dependence of the 2DEG sheet charge density in an undoped HEMT structure on the AlGaN thickness and Al mole fraction was experimentally observed and found to be consistent with a surface pinning level of 1.42 eV below E_C for an $Al_{0.27}Ga_{0.73}N$/GaN structure grown by MBE. It was also observed that there existed a critical thickness of AlGaN that needed to be grown before the formation of 2DEG, as predicted by the model. This critical thickness decreases with increasing Al mole fraction and was found to be 30A for an $Al_{0.27}Ga_{0.73}N$/GaN structure. Further work needs to be done to determing the exact nature of the surface states as discussed in section 5.2.1.

5.1.3 Current collapse and surface passivation

Historically, it was observed that the power measured at frequencies such as 4-8 GHz was considerably lower than that predicted from DC I-V curves as

measured by a curve tracer or a HP 4145B Semiconductor Parameter Analyzer. The reduction in measured power was attributed to a reduction in maximum drain current together with an increase in knee voltage at microwave frequencies and was referred to as current collapse. This led to the commonly held view that there existed traps in the device that caused a decrease in the maximum current as a function of frequency. Based on the existing literature on g_m compression, this decrease in drain current as a frequency was supposed to occur at a characteristic frequency which depended on the energy level of the deep trap responsible for the current collapse. A measurement set up was built to test the frequency dependence of the maximum drain current over the frequency range DC-4GHz.

It was found that current collapse was the consequence of the slow charging of the surface, leading to the formation of a virtual gate, located in the gate drain access region. The output drain current depends on the potential of this virtual gate. Under input drive conditions similar to those in a microwave power measurement, the virtual gate charges up, leading to current collapse. In steady state and under large signal overdrive, the maximum current from the devices tested was found independent of frequency over the range 1 kHz to 4GHz and significantly collapsed (by upto 50% in some cases) from the DC values. The time constant of this virtual gate was hence measured to be on the order of seconds. It was found that the maximum drain current recovered when UV light is incident on the device. This recovery is attributed to the generation of holes in the GaN layer that are swept to the surface. These holes forward bias the surface, neutralizing the virtual gate and recovering the maximum current. By comparing unpassivated and unpassivated devices adjacent to each other on the same wafer, it was shown that current collapse was decreased to a very large extent by passivating the surface of the device with a layer of silicon nitride, thus proving that surface states are responsible for current collapse. Passivated devices on

sapphire typically obtained output powers of 6W/mm compared to 4W/mm obtained from unpassivated devices on the same device.

5.2. Future Work

5.2.1. The nature of the free AlGaN surface

It has been established in this work that the fermi level at the AlGaN surface is pinned and that there must exist positive charge at the surface that is responsible for the existence of the 2DEG in an AlGaN. However, more than one configuration of surface states can satisfy the above requirements as shown in **fig 3.19** Further work needs to be done to identify the exact configuration at the surface. Measurements of Schottky barrier height on AlGaN/GaN HEMT structures with different metals on the surface can distinguish between the different possible surface configurations. Preliminary measurements indicate that the surface fermi level is not pinned by a donor-acceptor pair, since the barrier height of Schottky diodes for a metal with a small work function such as Ti is smaller than that measured on Pt diodes. Photoresponse measurements yield more precise values of barrier heights and should be done to establish the nature of the surface. It is also possible that the growth conditions in the last monolayer of AlGaN growth and the ambient conditions during post-growth cool down influence the surface defect formation. It is known that the changing reactor conditions during the final layer of AlGaN growth and during the cool down affect the output power, as discussed below.

5.2.2 The influence of growth conditions on the free AlGaN surface

It is clear that trapping of electrons along the surface is the dominant cause of current collapse. While it is necessary for positive charge on the surface to exist to induce 2DEG formation it is not clear whether these surface traps must

necessarily charge up during high power operation. Changing the growth conditions in the last monolayer of AlGaN growth and the ambient conditions during post-growth cool down can influence the surface defect formation and change the current collapse behavior. It is possible that the different kinds of surface defects are formed depending on the growth conditions and the energy level and time constants of these surface defects are dependent on the growth conditions. This dependence needs to be investigated. Preliminary investigations showed that current collapse was significantly affected by final growth conditions and the cool down ambient. A series of wafers were grown in which only the AlGaN growth and termination was varied, while the substrate preparation and GaN buffer growth were the same. Although sheet carrier densities and mobilities were very similar for the various surface terminations, the unpassivated power results varied strongly. This indicates that the nature of the surface, and hence the current collapse is dependent on how the growth is terminated. Further work needs to be done to investigate the dependence of current collapse on a)AlGaN growth and cool down conditions b) surface preparation before passivation.

5.2.3 Polarization free structures

It is clear that the existence of the polarization dipole leads to the formation of surface states that give rise to the 2DEG. However, for a HEMT structure, what is needed is only a large conduction band discontinuity to confine the channel electrons. Because the lattice constant of InN is larger than that of GaN and that of AlN is smaller than that of GaN it is clear that adding In to AlGaN alloys reduces the strain in the AlInGaN layer and hence the magnitude of the piezoelectric polarization dipole. In fact adding more In than is necessary to match lattice constants results in a layer of smaller lattice constant than GaN and hence a polarization dipole that is opposite in sign to that present due to

spontaneous polarization in AlGaN/GaN. This piezoelectric dipole cancels the spontaneous polarization dipole. Because the spontaneous polarization coefficient of InN is very close to GaN adding In does not affect the spontaneous polarization significantly. Hence by adding the right amount of In to AlGaN an AlInGaN/GaN heterostructure layer can be grown that has zero net polarization dipole. This possibility is exciting because such a heterostructure may not have surface states and the 2DEG density can be controlled by the concentration of added dopant. Such a device may not suffer from current collapse and may not be so critically dependent on surface passivation.

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