UNIVERSITY of CALIFORNIA
Santa Barbara

# High voltage GaN HEMTs with low on-resistance for switching applications

A dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy
in
Electrical and Computer Engineering

by

Naiqian Zhang

Committee in charge:

Professor Umesh K. Mishra, Chair
Professor Steven P. DenBaars
Professor Evelyn L. Hu
Dr. Vivek Mehrotra

September 2002

The dissertation of Naiqian Zhang is approved.

---

Steven P. DenBaars

---

Evelyn L. Hu

---

Vivek Mehrotra

---

Umesh K. Mishra, Committee Chair

July 2002

High voltage GaN HEMTs with low on-resistance for switching application

## Acknowledgements

To study in UCSB and in the best compound semiconductor research environment was totally my luck. I am always indebted to my advisor, Prof. Umesh Mishra, for taking me into his group and bringing me into a new world of semiconductor. Not only have I learnt a lot of knowledge and methodology of research from him, but also he showed me how to be a nice man in my life. I must thank Prof. Steven DenBaars for his MOCVD lab and his leading group, and I still remember his help on my first public presentation in Japan. I am very grateful to Prof. Evelyn Hu for serving in my Ph.D. committee, for many useful suggestions about this dissertation. I cannot thank Dr. Vivek Mehrotra enough for his support in the switching measurement and his help on my understanding of power supplies.

I owe more gratitude to Brendan than I can express, for supplying me the cutting edge materials and so many valuable discussions on material growth technique. I also benefited greatly from Stacia, Sten and Yulia for their contribution of state of the art material. Special thanks go to Yifeng and Primit for their priceless help and guidance. During the five years, Ching-Hui and Rama taught me processing technique hand by hand; James Ibbetson, Prashant, Rob U., Peter Kozodoy, James Champlain, Lee, Gia gave me uncountable suggestions on my research; Rob C. and Likun have done sizable work in the development of GaN HEMT simulation; DJ's theoretical analysis helped me to understand the basics in

GaN HEMTs; and Dan diced numbers of samples for me. I appreciate everything they have done for me. Members of the Mishra-York groups provided a supportive, enjoyable environment to study in and I am grateful to all of them: Jae, Can, Huili, Ilan, Dario, Yingda, Yun, Haijiang, Tim, Yee-Kwang, Ariel, Jack, Matt, Jason, Amir, Siddharth, Michael and Paolo who set up computers for us despite many fights, Vicki, Pengcheng, Bruce, Pete, Troy, Hongtao, Jim, Nadia, Justin, Joe. Thank you all for your collaboration and your companionship. And thanks to all the friends I have met during my time at UCSB.

Thanks also go to Masika Henson, Cathy Fogarthy, Lee Baboolal and Valerie De Veyra for their administrative support and much more. And thanks to cleanroom management team – Jake Whaley, Bob Hill and Neil Baker and all cleanroom users for their help on processing development. I cannot forget help from other research teams: Sriram Chandrasekaran from Rockwell Science Center, Xiewen Wang and Prof. T.-P. Ma from Yale University, Prof. Dave Pulfrey from University of British Columbia and Prof. Tamotsu Hashizume from Hokkaido University.

Finally I attribute my success to my family. Thank my parents for their sacrifice to bring me up and to support me to pursue my dreams. Thank my sister to be my best friend and to take care of my parents when I am away from home. Thank my wife Xie Yuan for her endless love, encouragement and patience on me.

## Vita

| | |
|---|---|
| Oct. 12, 1973 | Born, Hanshou, Hunan, P.R. China. |
| Sept. 1990 – July 1995 | B.E. in Electronic Engineering, Department of Electronic Engineering, Tsinghua University, Beijing, P.R. China. |
| July 1995 – Sept. 1997 | Research Assistant, Tsinghua University, Beijing, P.R. China. |
| Sept. 1997 – July 2002 | Research Assistant, University of California, Santa Barbara. |
| July 2002 | Ph.D. in Electrical and Computer Engineering, University of California, Santa Barbara. |

## Publications


[1] **N.-Q. Zhang**, B. Moran, S. P. DenBaars, U. K. Mishra, X. W. Wang, and T. P. Ma, "Effects of surface traps on breakdown voltage and switching speed of GaN power switching HEMTs," presented at International Electron Devices Meeting 2001, Washington, DC, USA, December 2001.

[2] **N.-Q. Zhang**, B. Moran, S. P. DenBaars, U. K. Mishra, X. W. Wang, and T. P. Ma, "Kilovolts AlGaN/GaN HEMTs as switching devices," *phys. stat. sol. (a)*, vol. **188**, pp. 213-7, 2001.

[3] Y.-F. Wu, **N.-Q. Zhang**, J. Xu, and L. McCarthy, "Group III Nitride base FETs and HEMTs with reduced trapping and method of producing the same." U.S.: patent pending.

[4] L. Shen, S. Heikman, B. Moran, R. Coffie, **N.-Q. Zhang**, D. Buttari, I. P. Smorchkova, S. Keller, S. P. DenBaars, and U. K. Mishra, "AlGaN/AlN/GaN high-power microwave HEMT," *IEEE Electron Device Letters*, vol. **22**, pp. 457-9, 2001.

[5] H. Marchand, L. Zhao, **N. Zhang**, B. Moran, R. Coffie, U. K. Mishra, J. S. Speck, S. P. DenBaars, and J. A. Freitas, "Metalorganic chemical vapor

deposition of GaN on Si(111): Stress control and application to field-effect transistors," *Journal of Applied Physics*, vol. **89**, pp. 7846-51, 2001.

[6] S. Keller, Y.-F. Wu, G. Parish, **N. Zhang**, J. J. Xu, B. P. Keller, S. P. DenBaars, and U. K. Mishra, "Gallium nitride based high power heterojunction field effect transistors: process development and present status at UCSB," *IEEE Transactions on Electron Devices*, vol. **48**, pp. 552-59, 2001.

[7] **N.-Q. Zhang**, S. Keller, G. Parish, S. Heikman, S. P. DenBaars, and U. K. Mishra, "High breakdown GaN HEMT with overlapping gate structure," *IEEE Elect. Dev. Lett.*, vol. **21**, pp. 373-5, 2000.

[8] **N.-Q. Zhang**, J. P. Ibbetson, S. Keller, R. Vetury, S. P. DenBaars, and U. K. Mishra, "High voltage GaN HEMTs," presented at The 4th International Conference on Solid State Devices and Materials, Tokyo, Japan, 1999.

[9] Y.-F. Wu, D. Kapolnek, J. Ibbetson, **N.-Q. Zhang**, P. Parikh, B. P. Keller, and U. K. Mishra, "High Al-content AlGaN/GaN HEMTs on SiC substrates with very high power performance," presented at International Electron Devices Meeting 1999, Washington, DC, USA, 1999.

[10] S. Keller, G. Parish, P. T. Fini, S. Heikman, C.-H. Chen, **N. Zhang**, S. P. DenBaars, U. K. Mishra, and Y.-F. Wu, "Metalorganic chemical vapor deposition of high mobility AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. **86**, pp. 5850-7, 1999.

[11] H. Marchand, **N. Zhang**, L. Zhao, Y. Golan, G. Rosner, G. Girolami, P. T. Fini, J. P. Ibbetson, S. Keller, S. DenBaars, J. S. Speck, and U. K. Mishra, "Structural and optical properties of GaN laterally overgrown on Si(111) by metalorganic chemical vapor deposition using an AlN buffer layer," *MRS Internet Journal of Nitride Semiconductor Research*, vol. **Res. 4**, 1999.

[12] **N. Zhang** and B.-X. Gao, "Load regulation to expand the bandwidth of class E amplifier," presented at Asia Pacific Microwave Conference, Yokohama, Tokyo, Japan, 1998.

[13] **N. Zhang**, Y.-O. Yam, B.-X. Gao, and C.-W. Cheung, "A new type high frequency class E power amplifier," presented at Asia-Pacific Microwave Conference 97', Hong Kong, China, 1997.

[14] B. Gao, J. Zhao, **N. Zhang**, and R. Liu, "Simulation software for microwave integrated circuits and interconnections: Tsinghua microwave SPICE," *Journal of Tsinghua University*, vol. **36**, pp. 28-39, 1996.

## Abstract

**High voltage GaN HEMTs with low on-resistance for switching applications**

*by Naiqian Zhang*

Power electronics as a means to control electrical energy is showing increasing importance in refining and innovating the social infrastructure in the new century. To break through the material limits of Silicon and to realize the drastic performance improvement needed to meet the severe requirements in the future, wide bandgap semiconductors such as SiC and GaN have attracted much attention because of their superior physical prosperities. This dissertation focuses on high voltage AlGaN/GaN HEMTs for high speed, low loss switching applications.

AlGaN/GaN HEMTs were projected to have lower on-resistance and higher switching speed than SiC devices due to the high electron mobility of the 2-DEG. Theoretical analysis was conducted to quantitatively predict that the on-resistance of AlGaN HEMTs is 50 to 200 times lower than that of SiC FETs, depending on the Aluminum composition. Device simulation was also carried on in ATLAS to probe into the operation mechanism of GaN HEMTs and assist the high breakdown voltage devices design. In device fabrication, highly resistive GaN buffer is the least requirement for high voltage operation. For this reason, the leakage of the GaN buffer was reduced to 0.2 mA/mm from 50 mA/mm at the beginning of the work by applying AP/LP growth on SiC substrates. With reduced electric field peak at the gate edge, a $V_{BR}$ higher than 500 V was obtained on field-plated GaN HEMTs for the

first time. Further improvement was brought by low gate leakage from insulated-gate structure. 1300 V breakdown voltage together with 1.65 mΩ·cm$^2$ on-resistance was achieved on a device with 16 μm gate-drain distance and 100 Å $SiO_2$ underneath the gate.

To improve the switching speed, GaN MIS structures were investigated by photo-*CV* technique to search for the proper dielectrics for GaN HEMT passivation. Sputtered SiN was found to eliminate the current dispersion in GaN HEMTs and improved the CW output power density from 3.3 W/mm to 6.6 W/mm for microwave HEMTs at 6 GHz. Thus, SiN was applied to the gate dielectric of high voltage GaN HEMTs and reduced the dispersion, but it also increased the gate leakage and hence resulted in low breakdown voltage. To combine the advantage of passivation from SiN and low leakage from $SiO_2$, double-layer gate-dielectric structure was implemented in insulated-gate GaN HEMTs and displayed both low dispersion and over 1000 V breakdown voltage. Subsequent switching measurement revealed very short turn-on time of 3.5 ns and turn-off time of 7 ns for a large-scale device. Yield was the highest priority in the design and fabrication of large periphery GaN HEMTs. $V_{BR}$ of 600 V and total $R_{on}$ of 0.4 Ω were realized on a 38.4 mm device consisted of 64 small device units, which indicated a bright future of GaN HEMTs in the switching applications.

# *Table of Contents*

# CHAPTER 1

# Introduction

Power semiconductor devices play a crucial role in the regulation and distribution of power and energy in the world. By some estimates, more than 60 percent of all the power utilized in the United States flows through at least one power device [1]. The market for power discrete devices exceeds many billions of dollars while leveraging systems worth many orders of magnitude more in value. It is well recognized that the improvements in system performance in terms of efficiency, size, and weight are driven by enhancements made in semiconductor device characteristics. Power devices used in systems can be broadly classified into two categories: power rectifiers and power switches. Silicon has long been the dominant semiconductor of choice for high voltage power switching devices. However, silicon power devices are rapidly approaching the theoretical limits of performance. In order to minimize the power losses in silicon power MOSFET, there has been a concerted effort to reduce the on-resistance by increasing the device die area. In high-frequency applications, as the die size increases, the increase in the input capacitance produces

a corresponding increase in the switching losses that offsets the reduction in the conduction losses achieved by the decrease in the on-resistance. Thus, it is necessary to reduce the specific on-resistance (on-resistance per square centimeter) to keep the die size small for small input capacitance.

At the same time, wide bandgap semiconductors, particularly SiC and GaN, are attracting much attention because they offer several potential advantages over silicon devices in the areas of switching (faster with lower losses), operating temperature, and blocking voltage. Unique material properties such as wide bandgap, high electric breakdown field, and high saturated electron velocity give these materials their tremendous potential. Table 1-1 compares some key electronic properties of GaN to other major semiconductors [2].

**Table 1-1: Physical properties of different semiconductors for high-voltage devices**

| Material | Si | 4H-SiC | GaN | AlN | Diamond |
|---|---|---|---|---|---|
| $E_g$ (eV) | 1.1 | 3.26 | 3.39 | 6.1 | 5.45 |
| $n_i$ ($cm^{-3}$) | $1.5\times10^{10}$ | $8.2\times10^{-9}$ | $1.9\times10^{-10}$ | $\sim10^{-31}$ | $1.6\times10^{-27}$ |
| $\varepsilon_r$ | 11.8 | 10 | 9.0 | 8.4 | 5.5 |
| $\mu_n$ ($cm^2$/Vs) | 1350 | 700 | 900 | 1100 | 1900 |
| $E_c$ ($10^6$ V/cm) | 0.3 | 3 | 3.3 | 11.7 | 5.6 |
| $v_{sat}$ ($10^7$ cm/s) | 1.0 | 2.0 | 2.5 | 1.8 | 2.7 |
| $\Theta_K$ (W/cmK) | 1.5 | 4.5 | 1.3 | 2.5 | 20 |

The wide bandgap of SiC and GaN results in very low intrinsic carrier concentration that gives negligible junction leakage current up to 500 $^{o}$C. This allows high temperature operation without excessive leakage or thermal runaway and reduces cooling requirements. The high breakdown strength requires thinner drift layers for a given blocking voltage, as compared to silicon, thus reducing the specific on-resistance and storage of minority carriers. The associated switching loss is then reduced, which enables higher switching frequency of the devices and significantly reduces the size and weight of the magnetic components in power switches. Finally the high thermal conductivity of the materials drains out dissipated power, allowing ultra-high power operation.

Recently, these potentials are becoming reality because of significant progress in growth and process technology for SiC and GaN. SiC switches with blocking voltage of a few kilo-volts and devices operating at a forward current density of up to 1 KA cm$^{-2}$ have been demonstrated. On the other hand, microwave power GaN HEMTs are close to commercialization. The objective of this thesis is to explore the possibility of applying GaN HEMTs to high voltage, low loss switching applications.

## 1.1 Advantages of AlGaN/GaN HEMTs as switching devices

The important parameters to evaluate power switching-devices are breakdown voltage $V_{BR}$, on-resistance $R_{on}$ and voltage control ratio $V_{BR}/\Delta V_{control}$. Normally if low $R_{on}$ is desired, device doping-level should be increased. Since the

breakdown voltage is twice integration of the doping level along the depletion region, it drops at a square rate with the decrease of the on-resistance. Therefore, the power device figure of merit $V_{BR}^2/R_{on}$ should be used to compare devices with different $V_{BR}$ and $R_{on}$ rating. This "power device figure of merit" leads to the "power semiconductor figure of merit" when we compare semiconductors directly from the material property point of view. From the figures of merit of different wide bandgap semiconductors summarized in Table 1-2, the advantages of AlGaN/GaN over SiC are clearly illustrated [3]. The problem of lower thermal conductivity of GaN is largely mitigated by the SiC substrate that the GaN can be grown on.

**Table 1-2: Normalized figure of merit of wide bandgap semiconductors**

| Material | Si | 4H-SiC | GaN | AlN | Diamond |
|---|---|---|---|---|---|
| BM ($\varepsilon_r \mu E_c^3$) | 1 | 130 | 650 | 31700 | 4110 |
| BHM ($\mu E_c^2$) | 1 | 22.9 | 77.8 | 1100 | 470 |
| JM ($E_c v_{sat}/2\pi$) | 1 | 180 | 760 | 5120 | 2540 |
| KM $\Theta_K (v_{sat}/\varepsilon_r)^{1/2}$ | 1 | 4.61 | 1.6 | 21 | 32.1 |

* BM is the Baliga's figure of merit for power switching and BHM is for high frequency power switching. KM is Keyes's figure of merit considering thermal limitation. JM is Johnson's figure of merit for high frequency devices [5].

Most importantly, HEMTs can be fabricated on AlGaN/GaN material system to take advantage of the 2-DEG (two-Dimensional Electron Gas) at the hetero-junction. High mobility provided by the 2-DEG further reduces the on-resistance, together with the high channel density brought by the large band discontinuity and

the polarization field. A HEMT structure also leads to low input capacitance, because the 2-DEG can be generated without doping the AlGaN layer. High $\mu \cdot n_s$ product ($\mu$ = 1500 cm$^2$/V·s and $n_s = 2.15\times10^{13}$ cm$^{-2}$) has been achieved recently [4], offering the potential of very low on-resistance and high switching speed of GaN power HEMTs. On the contrary, device fabrication in SiC presents unique problems in spite of the rapid progress presented in SiC MOSFETs. The outstanding problems include (i) activation of p-type implants, (ii) formation of low resistance ohmic contact to p-type material, (iii) reduction of fixed charge and interface states of MOS interface, and (iv) obtaining acceptable electron mobility in the MOS inversion layer (50 ~ 100 cm$^2$/V·s at present). Another advantage of HEMTs is the simplicity of processing. Only three mask steps are required to fabricate a GaN HEMT, while at least six masks are necessary to process a SiC MOSFET or VJFET.

Based on vertical device structure with a uniform doping profile, the on resistance of a SiC MOSFET is represented as:

$$R_{on} = \frac{4V_{BR}^2}{\varepsilon_r \mu_n E_c^3}, \qquad (1.1)$$

where $\varepsilon_r$ is the dielectric constant, $\mu_n$ is the mobility and $E_c$ is the critical electric field. For the same breakdown voltage, $R_{on}$ of a SiC device could be lower by two orders of magnitude than that of Si. Analysis in chapter 3 will exhibit more than 50 times further reduction of the specific on-resistance by GaN HEMTs.

## 1.2 Applications of high voltage AlGaN/GaN switching HEMTs

Some of the prominent applications for power semiconductor devices are shown in Figure 1.1 [1]. The projected voltage and current ratings of GaN HEMTs are one to two thousand volts and tens of amperes, respectively. Due to the difficulty to make good ohmic contact to wide bandgap materials, it is unlikely that the GaN HEMTs will operate at very low voltage or low current. The application of GaN HEMTs should cover power supplies, motor control, factory automation, and part of automotive electronics. Figure 1.2 illustrates a motor drive application in which the power supply is used in the drive electronics to control the power section.

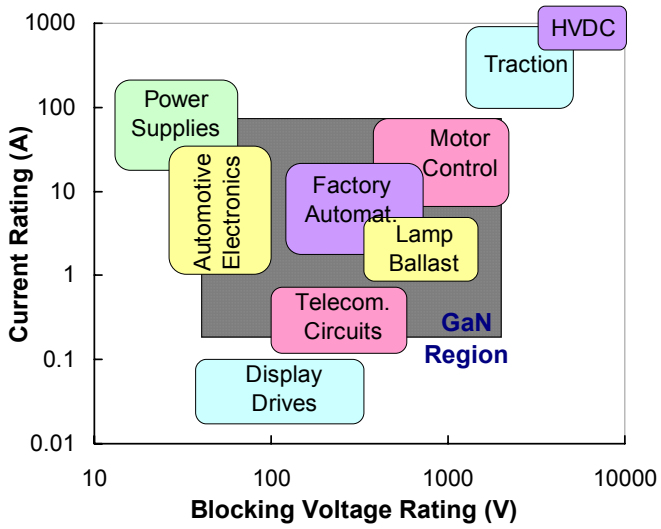



**Figure 1.1 Applications for GaN power switching HEMTs.**

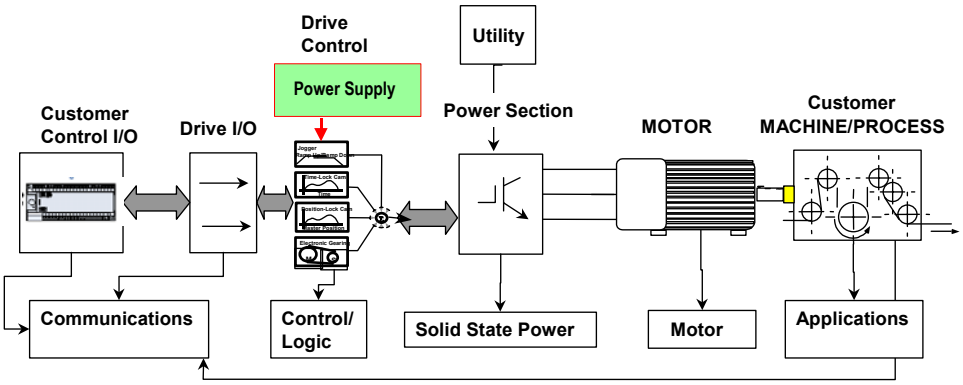



**Figure 1.2 Schematic illustrating the different components of a typical motor drive system. High performance power supply for drive electronics is an essential component that impacts the overall system.**

One of the major applications of AlGaN/GaN HEMTs is ultra compact, high efficiency power converters for megawatt power electronics. Power converters or supplies are an essential building block in a majority of military and commercial electrical hardware. In DC-link based topologies (Figure 1.3), the power section

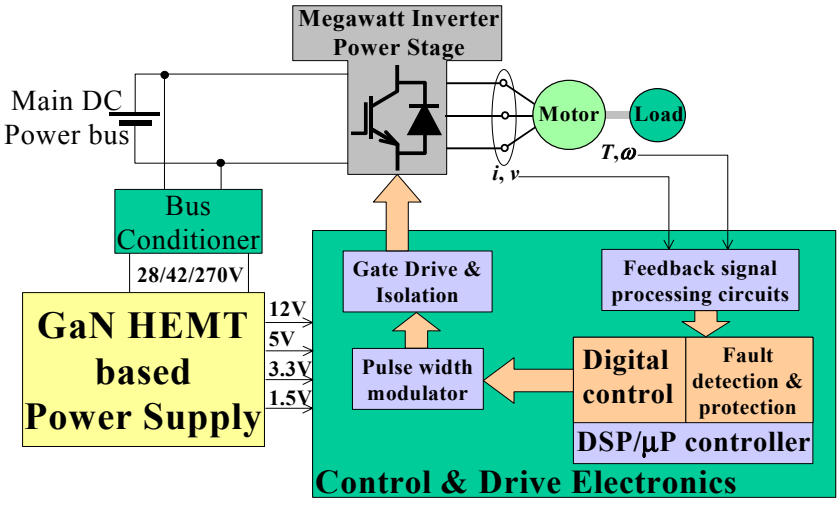



**Figure 1.3 Schematic block diagram of mega watt drive system. GaN power supply provides power to a variety of analog and digital loads.**

follows the DC filter section, and power converters are used to process and deliver power to a variety of digital and analog loads - including digital signal processors (DSP) and microprocessors, power integrated circuits, and sensors and actuators. These power converters typically range from a few watts to a few hundred watts and provide a well-regulated DC output (1.5 – 12V) from relatively unregulated dc input section (28 – 500 V). To minimize delay, electromagnetic noise, parasitics and losses associated with interconnects, and also to provide a well regulated output, these power converters must be in close proximity to the load they drive and are hence called point of load regulators. Power devices with voltage blocking capability in the range 100 – 1500 V, current carrying capability in the 1 – 10 A range, ultra low on-resistance and input/output capacitance, and temperature capability in excess of 250 °C will be required to develop high performance power converters for drive electronics for mega watt inverters.

State of the art power converters typically range in power density from about 20 to 50 W/in$^3$ with efficiencies in the range 80 – 85 %. As an example, a state of the art 100 W DC-DC converter with 48 V input and 1.5 V output for microprocessor and DSP based loads has an efficiency of about 85 % and a power density of 30 W/in$^3$ not including the heat sink. Majority of power loss occurs in the Silicon based power MOSFETs typically used in these power supplies for control electronics. As an example, power devices account for about 70 % of the total losses in a typical 100 W / 1.5 V output converter. Power devices also limit the maximum switching frequency owing to the large input capacitance of the device, which in turn

determines the size of the filter components - e.g. magnetics may occupy up to 60% of the converter volume. In addition, the Si power MOSFETs and the magnetic elements typically limit the temperature capability of these converters to about 80 °C at the baseplate above which the reliability is seriously compromised. Thus due to the size, efficiency and reliability constraints, these power converters cannot be integrated with the power section of motor drives and seriously impact the system performance. However, GaN HEMTs can provide a breakthrough required in high performance power converters, which can be integrated with the mega watt inverters to provide point of load regulation for inverter control. Uultra compact (> 150 $W/in^3$), lightweight (< 1 lbs. for 100 W DC-DC converter) and highly efficient (> 95 %) power converters can be developed on GaN HEMTs. Increasing the power supply efficiency from 85 % to 95 % corresponds to about 65 % lower loss for a 100 W converter. The temperature withstanding capability of the GaN HEMT based converters is expected to be in excess of 250 °C. Highly efficient converters will also eliminate or simplify heat-sinking requirements, resulting in greatly reduced equipment size and weight. The GaN HEMT based power converters are expected to impact a variety of electrical systems including more electric ships and aircraft, unmanned combat aerial vehicles (UCAVs), hybrid tanks for DoD applications, space exploration and warfare, and commercial motor drives used in harsh environments such as oil drilling.

As an illustrative example, power converters for aircraft flight control systems are typically located in the pressurized areas of the aircraft, where ambient

temperatures are well controlled, because of their large size, poor efficiency and rather low reliability when mounted near the actuators and other loads located near the engine section. This necessitates the use of rather long and heavy wiring to drive the actuators and other controls and adversely affects regulation, especially at low voltages, and electromagnetic compatibility. A rather substantial reduction in wiring weight can be obtained and distributed power architectures with point of load regulators can be successfully implemented if highly efficient, lightweight and high temperature resistant power converters are incorporated in fly-by-wire systems, where power supplies are located close to the loads they drive. GaN HEMT based power converters will enable high performance point of load regulators for both military and commercial power systems.

## 1.3 Research background of wide bandgap switching devices

Since the early development of a UMOSFET announced by CREE Co. in 1993, rapid progress was made in SiC MOSFETs. Denso Co. published a 450V/11m$\Omega\cdot cm^2$ vertical UMOSFET on 4H-SiC which was the first to exceed the theoretical limit of Si devices [6]. In 1998, Kansai Electrical Power Co. reported a 1400V 4H-SiC UMOSFET with $R_{on}$ of 311 m$\Omega\cdot cm^2$ [7] and Purdue University developed the 2.6 KV/550 $\Omega\cdot cm^2$ class lateral DMOSFET [8], which lately was increased to a breakdown voltage of 2.7 KV, even though the on-resistance remains relatively high [9]. RPI also announced 1200 V (4 $\Omega\cdot cm^2$) [10] and 900 V (560 m$\Omega\cdot cm^2$) class lateral RESURF MOSFETs in year 2000 [11]. The latest result

reported by Kansai Co. is a SiC "SIAFET", showing a blocking voltage of 4.5 KV with an on-resistance of 387 $m\Omega \cdot cm^2$ [12].

The above devices displayed very high voltage block capacity of SiC devices, but only capability of handling currents in the milli-ampere region. In 1999, Siemens AG Co. presented a vertical 1800 V/82 $m\Omega \cdot cm^2$ MOSFET capable of handling approx. 0.4 A [13] current, and later increased this number to 1 A with a low on-resistance of 47 $m\Omega \cdot cm^2$. They also fabricated 1800 V VJFET specified for currents of about 5 A with $R_{on}$ of 14 $m\Omega \cdot cm^2$ [14]. These values are by far the lowest on-resistance and highest total current achieved for SiC switching power devices. CREE developed a SIT on 4H-SiC with a built-in gate structure and an on-voltage of 4.5 V for 305 V breakdown with 525 $A/cm^2$ current density [15]. The achievements among those groups are labeled in Figure 1.4, as well as the theoretical limits of Si and SiC power devices for comparison.

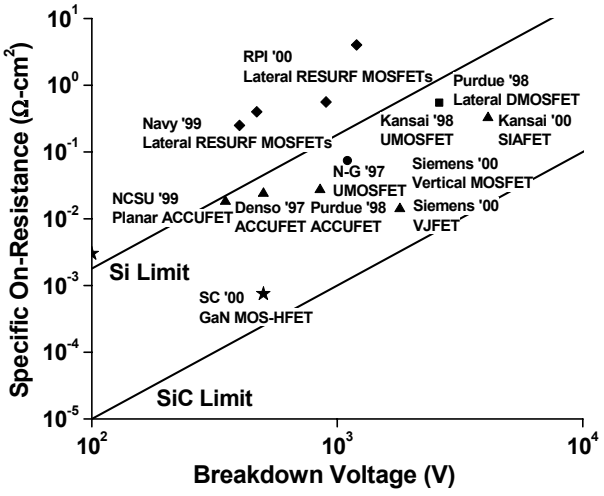



**Figure 1.4 Comparison of Si, SiC and GaN power switching devices**

The lack of commercial bulk GaN substrates combined with difficulties in processing the material due to its chemical and mechanical stability have hampered the development of GaN power devices. However, tremendous progress has been achieved in GaN microwave power devices due to better material quality and process techniques, enabling the development of GaN power switching devices. Not much work has been done on GaN switching HEMTs when this project was started, but there are several groups working on it presently. G. Simin developed AlGaN/GaN MOS-HFET with $SiO_2$ as the gate insulator and achieved 500 V breakdown voltage with very high current density of 15 A/mm$^2$ [16]. The specific on-resistance is 0.75 m$\Omega\cdot$cm$^2$. This value has exceeded all achievement on SiC devices, but the breakdown voltage needed to be improved. S. Yoshida fabricated a large periphery HEMT of 200 mm gate width (400 fingers) and obtained 15 A total drain current with 3 m$\Omega\cdot$cm$^2$ specific on-resistance [17]. Because of individual finger failure caused by the defects on the substrate, the device couldn't operate at a voltage higher than 100 V. Preliminary work on GaN power HEMTs had also been carried out in UCSB by Rama Vetury. Floating gates (guard rings) were used in his work [18]. The floating gates improve the breakdown voltage by extending the electric field buildup along the channel. 435 V breakdown voltage was obtained at a gate to drain separation of 7 μm. Another application of the floating gates is to detect the linear extension of the gate depletion region with the drain bias. It is an indication of the existence of surface states that we will discuss later in this thesis.

## 1.4 Synopsis of this thesis

Power switching devices were based on microwave GaN HEMTs to take the advantage of the well-established growth and process technology in UCSB. The additional requirements for MOCVD growth are that the buffer must be highly resistive and the total material system is not doped to minimize the leakage and to improve the gate Schottky barrier. The thesis is focused on how to improve the device design and the process technique to increase the breakdown voltage with low on-resistance. The switching speed is the other major concern in this thesis. Device simulation is also performed to understand GaN HEMT operation and the breakdown mechanism.

Physical modeling of GaN HEMTs is first introduced in Chapter 2. With proper device structure, material parameters and models, the simulations show good agreement to experimental results. The simulation is used in the subsequent chapters to understand device operation of GaN HEMTs and to optimize the device structure for higher breakdown voltage.

Chapter 3 describes the procedure to develop the power switching HEMTs from the standard microwave HEMTs. Theoretical $V_{BR}$-$R_{on}$ limit of GaN HEMTs is calculated and shows their superiority over SiC devices. Insulated-gate HEMT structure with very low buffer leakage is employed to realize more than 1000 V breakdown voltage.

Chapter 4 is the extension of the preceding chapter, aiming to solve the problem of slow switching speed brought up by the gate insulator. The interface

properties of different dielectrics on GaN are investigated by *C-V* measurement with UV light excitation. Incorporating successful passivation of GaN microwave HEMTs by SiN, a double-layer gate dielectric structure is devised to solve the apparent compromise between the breakdown voltage and switching speed.

Chapter 5 deals with large-scale devices. Several problems associated with scaling are addressed and clarified. A circuit is constructed to measure the switching characteristics of the large periphery device.

## 1.5 References:


[1] B. J. Baliga, "Trends in power semiconductor devices," *IEEE Transactions on Electron Devices*, vol. **43**, pp. 1717-1731, 1996.

[2] O. Ambacher, "Growth and applications of group III-nitrides," *Journal of Physics D (Applied Physics)*, vol. 31, pp. 2653-2710, 1998.

[3] T. P. Chow, "SiC and GaN high-voltage power switching devices," *Materials Science Forum*, vol. **338-342**, pp. 1155-60, 2000.

[4] I. P. Smorchkova, L. Chen, T. Mates, L. Shen, S. Heikman, B. Moran, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "AlN/GaN and (Al,Ga)N/AlN/GaN two-dimensional electron gas structures grown by plasma-assisted molecular-beam epitaxy," *Journal of Applied Physics*, vol. **90**, pp. 5196-201, 2001.

[5] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Letters*, vol. **10**, pp. 455-57, 1989.

[6] S. Onda, R. Kumar, and K. Hara, "SiC integrated MOSFETs," *Physica Status Solidi A*, vol. **162**, pp. 369-388, 1997.

[7] Y. Sugawara and K. Asano, "1.4 KV 4H-SiC UMOSFET with low specific on-resistance," presented at Proceedings of 1998 International Symposium on Power Semiconductor Devices & ICs, Tokyo, Japan, 1998.

[8] J. Spitz, M. R. Melloch, J. A. Cooper, and M. A. Capano, "2.6 KV 4H-SiC lateral DMOSFET's," *IEEE Electron Device Letters*, vol. **19**, pp. 100-102, 1998.

[9] J. Spitz, M. R. Melloch, J. A. Cooper, G. Melnychuk, and S. E. Saddow, "2.7 KV epitaxial lateral power DMOSFETs in 4H-SiC," presented at 58th DRC. Device Research Conference, Denver, CO, USA, 2000.

[10] K. Chatty, S. Banerjee, T. P. Chow, R. J. Gutmann, and M. Hoshi, "High-voltage lateral RESURF MOSFETs on 4H-SiC," *Electron Device Letters*, vol. **21**, pp. 356-358, 2000.

[11] S. Banerjee, K. Chatty, T. P. Chow, and R. J. Gutmann, "Improved implanted RESURF MOSFETs in 4H-SiC," presented at 58th DRC. Device Research Conference, Denver, CO, USA, 2000.

[12] Y. Sugawara, K. Asano, R. Singh, J. Palmour, and D. Takayama, "4.5 KV novel high voltage high performance SiC-FET "SIAFET"," presented at 12th International Symposium on Power Semiconductor Devices & ICs. Proceedings, Toulouse, France, 2000.

[13] D. Peters, R. Schorner, P. Friedrichs, J. Volkl, H. Mitlehner, and D. Stephani, "An 1800V triple implanted vertical 6H-SiC MOSFET," *IEEE Transactions on Electron Devices*, vol. **46**, pp. 542-545, 1999.

[14] P. Friedrichs, H. Mitlehner, K. O. Dohnke, D. Peters, R. Schorner, U. Weinert, E. Baudelot, and D. Stephani, "SiC power devices with low on-resistance for fast switching applications," presented at 12th International Symposium on Power Semiconductor Devices & ICs. Proceedings, Toulouse, France, 2000.

[15] R. Singh, K. G. Irvine, and J. W. Palmour, "4H-SiC buried gate field controlled thyristor," presented at 1997 55th Annual Device Research Conference Digest, Fort Collins, CO, USA, 1997.

[16] G. Simin, X. Hu, N. Ilinskaya, A. Kumar, A. Koudymov, J. Zhang, M. Asif Khan, R. Gaska, and M. S. Shur, "7.5 kW/mm$^2$ current switch using AlGaN/GaN metal-oxide-semiconductor heterostructure field effect transistors on SiC substrates," *IEE Electronics Letters*, vol. **36**, pp. 2043-4, 2000.

[17] S. Yoshida and H. Ishii, "A high power GaN based field effect transistor for large current operation," *phys. stat. sol. (a)*, vol. **188**, pp. 243-46, 2001.

[18] R. Vetury, Y. F. Wu, P. T. Fini, G. Parish, S. Keller, S. DenBaars, and U. K. Mishra, "Direct measurement of gate depletion in high breakdown (405 V) AlGaN/GaN heterostructure field effect transistors," presented at International Electron Devices Meeting 1998, San Francisco, CA, 1998.

# CHAPTER 2

# Simulation of AlGaN/GaN HEMTs

GaN based HEMTs are promising devices for high power, high frequency, and high temperature applications, owing to the material properties such as wide bandgap, large breakdown electric field and high saturation drift velocity. Recently, improvements in material growth and device design have produced state-of-the-art AlGaN/GaN HEMTs with power densities as high as 11.2 W/mm [1], pulsed total output power of 50 W [2], and $f_t$ of over 100 GHz [3]. On the other hand, it is well recognized that the current devices are not yet optimized, and phenomena such as the high 2-DEG density (normally $1\times10^{13}$ $cm^{-2}$) in undoped devices and the large discrepancy in predicted power from DC I-V curves compared with measured RF power need to be accommodated in computation tools. Further, there exists an emerging requirement for simulation tools to accurately predict device performance prior to fabrication because of the high inherent cost of the cut-and-try method. Additionally, there are strong polarization fields in the AlGaN/GaN material system. From theoretical calculations, the polarization charge is $3.32\times10^{13}$ $cm^{-2}$ in 27 %

AlGaN (spontaneous plus piezoelectric polarization) and $1.81\times10^{13}$ $cm^{-2}$ in GaN. Failure to include this strong polarization field will introduce distortion to the calculated band diagrams and thus hamper related simulation results. Wu, S. [4] and Albrecht [5] have conducted simulations on GaN HEMTs for given 2-DEG densities. Those simulations helped in the understanding of basic physics in GaN HEMTs, but more work needs to be done to fully integrate polarization and surface effects into device simulation.

In this chapter, a successful implementation of an AlGaN/GaN HEMT model into the commercially available device simulator ATLAS is described. With proper material parameters, the polarization field, and surface traps, simulations of *I-V* curves and internal electric field are demonstrated. ATLAS is a *physically-based* device simulator that predicts the electrical characteristics that are associated with specified physical structures and bias conditions [6]. This is accomplished by solving systems of coupled, non-linear partial differential equations that describe the semiconductor physics. Physically-based simulation provides advantages over empirical modeling by being *predictive* and providing *insight*. Using this tool is typically quicker and less expensive than performing actual experiments and provides information that is often difficult or impossible to measure. Users of ATLAS specify device simulation problems by defining:

1. The physical structure and material parameters to be simulated
2. The physical models to be used

3. The bias conditions for which electrical characteristics are to be simulated.

The subsequent sections of this chapter describe how to perform these steps in GaN HEMT simulation. The first section will discuss the AlGaN/GaN heterojunction with polarization field and surface trap model, and compare the resulting band diagrams with and without these models. Simulated channel charge density vs. AlGaN thickness curve is fitted to measured Hall data to extract the polarization field strength and surface trap density and depth. Models for mobility and impact ionization are given in the second section. In the third section, DC I-V curves, small signal frequency response, and breakdown characteristics are simulated and compared to experiments.

## 2.1 Material parameters and AlGaN/GaN heterojunction structure

GaN is far from mature as an electronic semiconductor material. It is not rare to find discrepancies between theoretically calculated material parameters and those that are experimentally measured. To make it more relevant to current research, experimental material parameters were used in the simulation except for some values that have not yet been able to be measured directly. In addition, close attention was paid to the polarization field in AlGaN/GaN heterojunction to account for the large 2-DEG density.

### *2.1.1 Material properties*

**Table 2-1 Material parameters used in GaN HEMTs simulation.**

| Parameter | Description | Units | GaN | $Al_{0.27}Ga_{0.73}N$ |
|---|---|---|---|---|
| $E_g$ | Band gap @ 300 K | eV | 3.42 | 3.95 |
| $\Delta E_c$ | Conduction Band offset between AlGaN and GaN | Fraction of $E_g$ | 0.68 | 0.68 |
| $A_n^*$ | Richardson constant for electrons | $A/cm^2K^2$ | 24 | 24 |
| $A_p^*$ | Richardson constant for holes | $A/cm^2K^2$ | 96 | 96 |
| $\mu_n$ | Low field electron mobility | $cm^2/Vs$ | 425 | 10 |
| $\mu_p$ | Low field hole mobility | $cm^2/Vs$ | 5 | 5 |
| $E_d$ | Donor energy level | eV | 0.025 | 0.025 |
| $E_a$ | Acceptor energy level | eV | 0.160 | 0.160 |
| $\epsilon_r$ | Relative permittivity | | 10.4 | 10.32 |
| $N_c$ | Conduction band effective density of states @ 300 K | $cm^{-3}$ | $2.24 \times 10^{18}$ | $2.24 \times 10^{18}$ |
| $N_v$ | Valence band effective density of states @ 300 K | $cm^{-3}$ | $1.80 \times 10^{19}$ | $1.80 \times 10^{19}$ |
| $\chi$ | Electron affinity | eV | 3.5 | 3.14 |
| $v_{sat,n}$ | Saturation velocity electrons | cm/s | $1.3 \times 10^7$ | $10^4$ |
| $v_{sat,p}$ | Saturation velocity for holes | cm/s | $10^3$ | $10^3$ |

We used the bandgap of $Al_xGa_{1-x}N$ at room temperature given by [7]:

$$E_g(x) = 6.13x + 3.42(1-x) - x(1-x)\,\text{eV}, \qquad (2.1).$$

and a linear interpolation of the dielectric constant given by[8]:

$$\varepsilon_r(x) = 10.4 - 0.3x \qquad (2.2).$$

The electron affinity was calculated assuming a conduction band offset of 68 %. Using the measured electron affinity values of 3.5 ±0.1 eV and 1.9 ±0.2 eV for GaN and AlN, respectively [9, 10], 68% is within experimental error. The effective masses of 0.20 and 0.8 for electron and holes [11], respectively, are used to compute the effective density of states for the conduction and valence bands. Table 2-1 contains the material values used for simulation of an AlGaN/GaN HEMT with an Al composition of 27 %.

### *2.1.2 Polarization field and surface traps*

Understanding and controlling the formation of the 2DEG in AlGaN/GaN HEMTs is important for the optimization of their performance. Ibbetson et al [12] and Smorchkova et al [13] proposed that surface donor-like traps are the source of the electrons in the channel, and the electrons are driven into the channel by the strong polarization field. This charge distribution model is used in our simulations along with single-level surface traps as shown in Figure 2.1. To simulate the polarization field in the AlGaN layer, a positive charge layer at the AlGaN/GaN interface and an equal amount of negative charge on the surface of the AlGaN layer

is used. For simplicity, only the net field in the AlGaN layer is included in the simulation, with no field in the GaN layer. The basis of this simplification is that the built-in voltage will be too high in the 3 $\mu$m thick GaN buffer for such a high field. Even with this simplification, the net polarization charge in the AlGaN layer is still as high as $1.51\times10^{13}$ cm$^{-2}$. We will show that the polarization field is the dominant controlling factor for the charge and electric field distribution in GaN HEMTs.

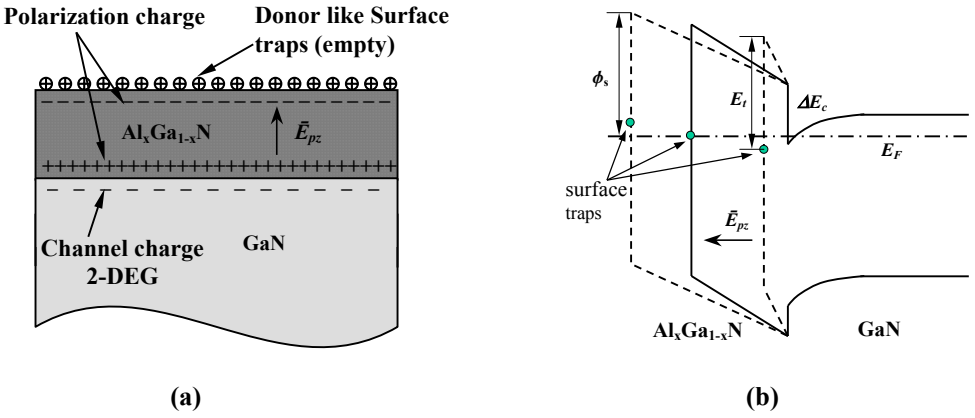
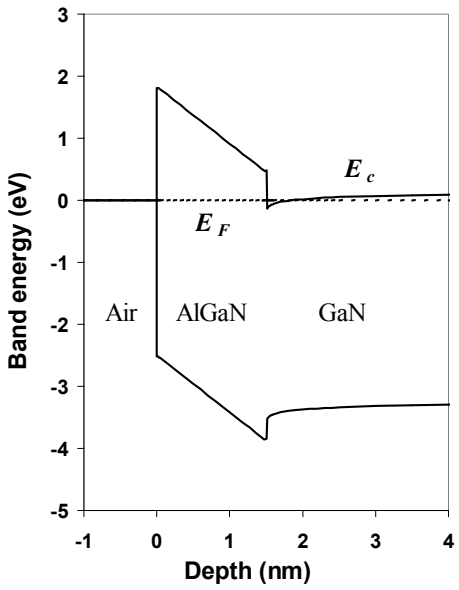
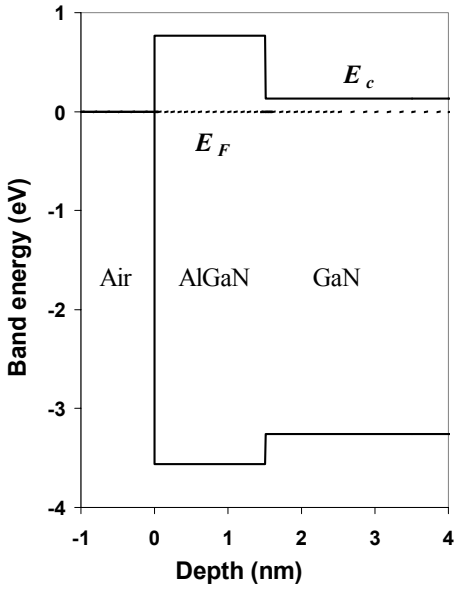


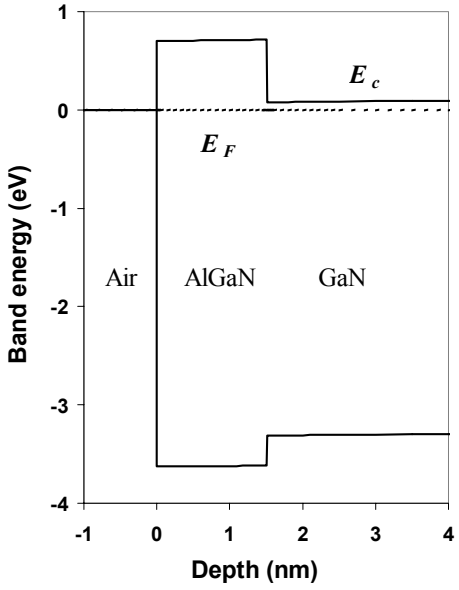

**Figure 2.1 AlGaN/GaN heterojunction with polarization electric field and surface traps: (a) cross-section of the heterojunction; (b) band diagrams with different AlGaN thickness.**

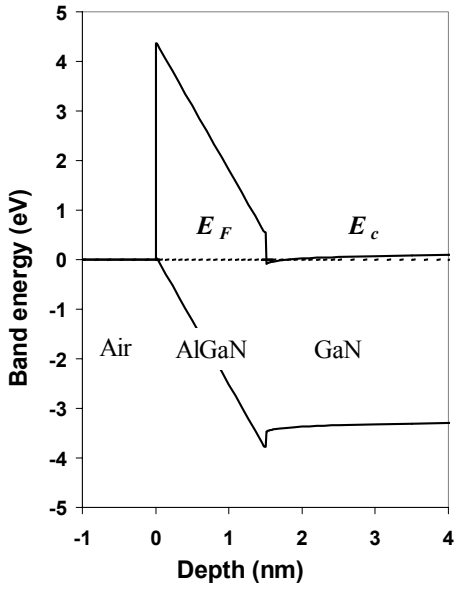
Figure 2.2 (a) shows the band diagram of an $Al_{0.27}Ga_{0.73}N$/GaN hetero-junction with both the polarization model and surface traps. The thickness of the AlGaN layer is 150Å. The background doping for all materials is $1\times10^{15}$ cm$^{-3}$. The net polarization charge is $1.75\times10^{13}$ cm$^{-2}$ (the corresponding polarization field is 3.06 MV/cm), and the density of the surface traps is $1.36\times10^{13}$ cm$^{-2}$ at a depth of 1.85 eV below the conduction band, where all these numbers were obtained by fitting experimental $n_s$ vs. $t_{AlGaN}$ curve addressed later.



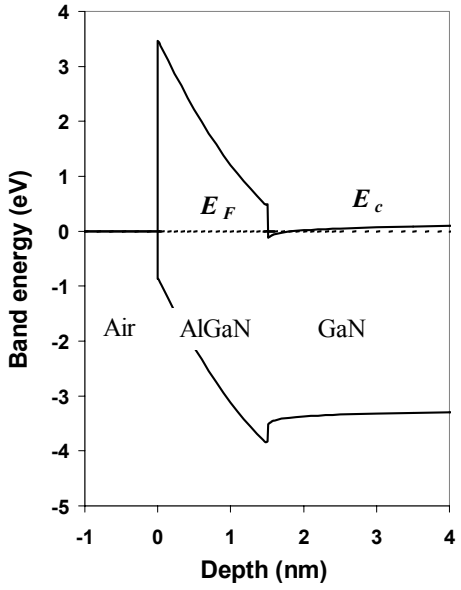




**(a) With polarization model and surface traps, $n_s = 1.34\times10^{13}$ cm$^{-2}$.**
**(b) No polarization model or surface trap, $n_s = 1.1\times10^{10}$ cm$^{-2}$.**




**(c) No polarization model but with surface traps, $n_s = 8.01\times10^{10}$ cm$^{-2}$.**
**(d) With polarization model but no surface trap, $n_s = 3.48\times10^{12}$ cm$^{-2}$.**




**(e) With polarization model but no surface trap, and AlGaN is doped to $5\times10^{18}$ $cm^{-3}$, $n_s$ = $9.87\times10^{12}$ $cm^{-2}$.**

**Figure 2.2 Comparison of band diagrams of $Al_{0.27}Ga_{0.73}N$/GaN heterojunctions with or without polarization field or surface traps. The AlGaN thickness is 150 Å.**

For comparison, Figure 2.2 (b) shows the band diagram of the junction without the polarization model or surface traps; Figure 2.2 (c) shows the band diagram of the junction with surface traps but without the polarization model; and Figure 2.2 (d) shows the band diagram of the junction with the polarization model but no surface traps. For case (a), the 2DEG charge ($n_s$) in the channel is $1.34\times10^{13}$ $cm^{-2}$, but for case (b) $n_s$ is only slightly larger than the background doping. The $n_s$ is $8.01\times10^{10}$ $cm^{-2}$ and $3.48\times10^{12}$ $cm^{-2}$ for case (c) and (d), respectively. Case (d) represents electrons in the 2-DEG being provided by the valence band of the AlGaN resulting a two-dimensional hole gas at the surface. However, experimentally, Hall measurements of undoped $Al_{0.27}Ga_{0.73}N$/GaN hetero-junctions normally give an $n_s$ of

around $1\times10^{13}$ $cm^{-2}$. In case (d), if we intentionally dope the AlGaN layer to $5\times10^{18}$ $cm^{-3}$, which is a larger number than can currently be achieved, the $n_s$ only increases to $9.87\times10^{12}$ $cm^{-2}$, a value much lower than experimentally determined $n_s$ of doped $Al_{0.27}Ga_{0.73}N$/GaN HEMTs. This band diagram is shown in Figure 2.2 (e). The simulations show that the surface traps, rather than intentional doping, is the leading source of channel electrons, and the polarization electric field is the driving force to move the trapped electrons into the channel to form 2-DEG.

To obtain the polarization electric field and the surface trap parameters, the trap energy level $E_t$, trap density $D_t$, and polarization charge density $\sigma_{pz}$ (polarization field $E_{pz}$), were adjusted until simulation data matched experimental $n_s$ vs. $Al_{0.27}Ga_{0.73}N$ cap layer thickness $t_{AlGaN}$, given in [13]. Although three parameters were adjusted, there was only one unique combination of all three parameters that led to the fitted $n_s$ vs. $t_{AlGaN}$ curve for a single trap level. As shown in Figure 2.1 (b), for very thin AlGaN thickness, the surface potential $\phi_s$ is smaller than the depth of the surface trap level $E_t$. Therefore, the Fermi-level lies above the surface trap level, and the traps are filled with electrons. As the AlGaN layer becomes thicker, the polarization field increases the surface potential. Once the fermi-level at the surface equals the trap level, the electrons in these traps begin to transfer to the channel, and $t_{crit}$, defined as the minimum thickness of the AlGaN cap layer to produce a 2DEG, is reached. The critical thickness is determined by both the surface trap depth $E_t$, and the magnitude of $E_{pz}$. As the AlGaN layer becomes thicker than $t_{crit}$, more and more electrons move to the channel. Finally, when the trap level ascends higher than the

Fermi-level ($\phi_s > E_t$), all the electrons in the surface traps have moved to the channel. At this point, no more electrons can be brought to the channel from the surface states despite further increase in the AlGaN thickness. Therefore the channel charge density saturates at a certain AlGaN thickness and the saturation level of $n_s$ is equal to the surface trap density. The rate of $n_s$ saturation with AlGaN thickness is dependent on how fast the surface trap energy rises, and therefore dependent on the magnitude of $E_{pz}$. Table 2-2 summarizes the dependence of the saturation level of $n_s$, charge saturation rate, and critical thickness $t_{crit}$, on $E_t$, $D_t$ and $\sigma_{pz}$.

**Table 2-2 General effects of changes in $\sigma_{pz}$, $E_t$, and $D_t$ on $t_{crit}$, $n_s$ saturation level and saturation quickness.**

| Parameter | $t_{crit}$ | $n_s$ saturation level | Rate of charge saturation |
|---|---|---|---|
| Increase in $\sigma_{pz}$ | Decreases | Little dependence | Faster |
| Increase depth of $E_t$ | Increases | Little dependence | Little dependence |
| Increase $D_t$ | Little dependence | Approximately equal to $D_t$ | Little dependence |

The curve fitted to $n_s$ measured by Hall effect is shown in Figure 2.3. The fitting process was also carried out in [13], but the single equation fitting in that paper neglected the width of the Fermi distribution, the Fermi level rise in the channel and the band bending near the channel and lastly. Also, the distribution of electrons in the channel was simplified to be pure two dimensional charge. These deficiencies are accounted for in the ATLAS simulations. A good fit was achieved in this paper for a polarization charge density $\sigma_{pz} = 1.75\times10^{13}$ cm$^{-2}$ (corresponding

field of 3.06 MV/cm) and a surface trap density of $1.36\times10^{13}$ $cm^{-2}$ at a depth of 1.85 eV below the conduction band. The fitted net polarization charge in AlGaN is a little higher than the theoretical value of $1.56\times10^{13}$ $cm^{-2}$. Detailed stress examination is needed to verify these results.

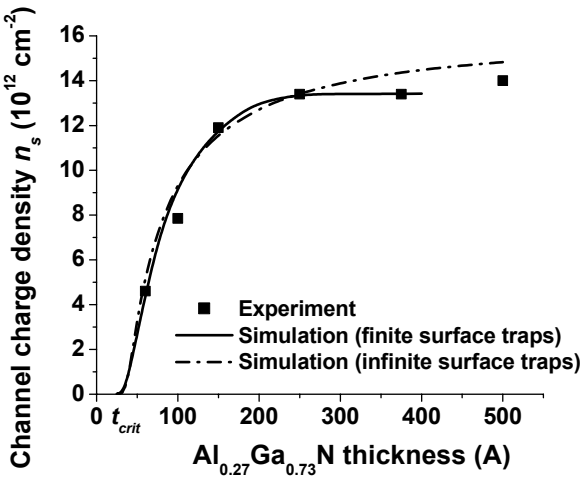



**Figure 2.3 Simulated and the experimental dependence of the channel charge density $n_s$ on the AlGaN thickness $t_{AlGaN}$.**

The fitting process was also carried on with infinite density of surface traps and is compared in Figure 2.3. The fitted trap depth $E_t$ is 1.75 eV and the polarization charge is $1.65\times10^{13}$ $cm^{-2}$. In the infinite surface case, $n_s$ will saturate when it is equal to the polarization charge density making the field in the AlGaN layer tend to zero, and the fermi-level will remain at $E_t$. There is not much difference between the results of the finite and the infinite surface trap density cases, which indicates that the polarization field is the determining factor for the 2-DEG concentration and the surface trap density is very large (between $1.36\times10^{13}$ $cm^{-2}$ and infinity).

### *2.1.3 Distributed/Multi-level surface traps*

Although ATLAS can simulate only discrete trap levels, a qualitative description of how a continuous trap distribution with a Gaussian profile should affect the channel charge can be derived from our observations. What should the Gaussian look like to fit the simulated $n_s$ vs. $t_{AlGaN}$ curve in Figure 2.3 to the experiments again? The first parameter that can be determined is the area under the Gaussian (*i.e.,* the total trap density). It should be equal to the single-level trap density $D_t$ in order to obtain the same $n_s$ saturation level for AlGaN layer thickness much larger than $t_{crit}$. To retain the same $t_{crit}$, the start of the Gaussian (1 ~ 5% of the peak value) should be at the depth of the single level. At the same time, the rate of saturation drops because of the spread of the distribution. To increase the saturation rate, a larger $\sigma_{pz}$ ($E_{pz}$) is needed. But the rise of $E_{pz}$ leads to a smaller $t_{crit}$, so the Gaussian must be moved deeper to preserve $t_{crit}$. Therefore, a more spread Guassian distribution (with lower peak value) of surface traps comes with a larger $\sigma_{pz}$ value and a deeper centroid of the Gaussian. The different Gaussian distributions of surface traps to fit to the same $n_s$ vs. $t_{AlGaN}$ curve are illustrated in Figure 2.4.

In the last section, the fitting resulted in single-level surface traps. With the reasoning in this section, if the surface traps are of a Gaussian distribution, the centroid of the distribution must be deeper than the single level and the simulated (fitted) polarization field in the AlGaN layer $E_p$ is larger than in the single-level-trap case.

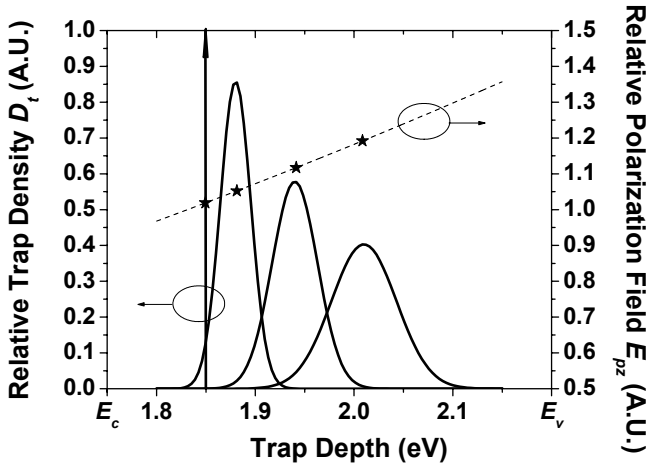



**Figure 2.4 Comparison of Gaussian distributions of surface traps and related polarization field in AlGaN to single-level surface traps. This figure only shows a trend instead of quantitative results.**

## 2.2 Models used in GaN HEMT simulation

### *2.2.1 Mobility and velocity models*

ATLAS offers two field dependent mobility models: a negative differential mobility model given by Eq. (2.3), and a standard mobility model given by Eq. (2.4).

$$\mu(E) = \frac{\mu_0 + \frac{v_{sat}}{E}\left(\frac{E}{E_0}\right)^{\gamma}}{1+\left(\frac{E}{E_0}\right)^{\gamma}} \tag{2.3}$$

$$\mu(E) = \mu_0\left[1+\left(\frac{\mu_0 E}{v_{sat}}\right)^{\beta}\right]^{-1/\beta} \tag{2.4}$$

According to Monte Carlo calculations [14], GaN should exhibit velocity overshoot and therefore a negative differential mobility. The velocity field curve can be

divided into three regions: low field region, velocity overshoot region and saturation region. Equation (2.3) does not contain enough fitting parameters to provide a good fit to both the low field region and the saturation region thus resulting in inaccuracy in either the ohmic region or in the saturation region of the I-V curves. Since velocity overshoot has not been observed in GaN devices and Polyakov's work [14] showed that the velocity overshoot has little effect on the knee voltage of the I-V curves, the standard mobility model was chosen for our simulation. Using proper fitting parameters $\mu_0$ = 630 cm$^2$/Vs, $\beta$ = 2.6, and $v_{sat}$ = 1.3 × 10$^7$ cm/s, Eq. (2.4) is able to agree with both the low field and velocity saturation regions of the Monte Carlo calculated drift velocity vs. electric field curve for GaN given by [15]. This field mobility model combined with the concentration dependent mobility model (higher mobility in the channel) provides satisfactory simulation of the 2-DEG in the channel. Very precise modeling of GaN electron mobility was given in Polyakov's paper with a complex equation format [14]. As a suggested future work, this equation could be integrated in ALTAS using the "C language interpreter".

### *2.2.2 Impact ionization model*

The generation rate of electron-hole pairs due to impact ionization is given by:

$$G = \alpha_n \frac{J_n}{q} + \alpha_p \frac{J_p}{q} \qquad (2.5)$$

where $\alpha_n$ and $\alpha_p$ are the electron and hole ionization rates. For temperature independent simulation, a Grant model is used in the GaN HEMT simulation to describe the field-dependency of the ionization rates:

$$\alpha_{n,p} = \alpha_{n,p}^{\infty} \cdot \exp\left[ -\left( \frac{E_{n,p}^{crit}}{E} \right)^{\beta_{n,p}} \right] \qquad (2.6)$$

From Monte Carlo simulation of impact ionization in Wurtzite GaN [16], the values of coefficients $\alpha_n^{\infty}$ and $E_n^{crit}$ can be calculated to be $2.60\times10^8$ cm$^{-1}$ and $3.42\times10^7$ V/cm respectively for electrons and $4.98\times10^6$ cm$^{-1}$ and $1.95\times10^7$ V/cm for holes. The simulated values showed good agreement with experimental results of $\alpha_n^{\infty} = 2.9\times10^8$ cm$^{-1}$ and $E_n^{crit} = 3.4\times10^7$ V/cm [17], so the calculated values were used in the simulations. Beyond a threshold electric field $E_{gran}$, the ionization rates increase dramatically and any higher field will cause the material to breakdown. The $E_{gran}$ was set to coincide with the electric field strength of GaN of 3.3 MV/cm. Because of the lack of sufficient ionization data of AlGaN, the above values for GaN were also applied to AlGaN except that the $E_{gran}$ of AlGaN was set to the electric field strength of AlGaN (e.g. $E_{gran}$ = 5.82 MV/cm) for $Al_{0.3}Ga_{0.7}N$ from linear interpolation.

In addition to above models, the Newton itineration method was specified in the simulation to solve up to 6 fully coupled equations defined by a combination of the models.

## 2.3 Simulations of GaN HEMTs

As probably the simplest form of a transistor, a GaN HEMT can be simulated after a proper (source-drain) ohmic contact value and gate metal work function are applied to the preceding AlGaN/GaN material structure. The input file for ATLAS of the GaN HEMT simulation is given in Appendix A.

### *2.3.1 DC I-V curves*

The simulated GaN HEMT structure is shown in Figure 2.5 with material parameters discussed above. The source and drain contact resistances were set to 0.5 Ω·mm. The gate metal is Ni with a work function of 5.15 eV. The entire device was

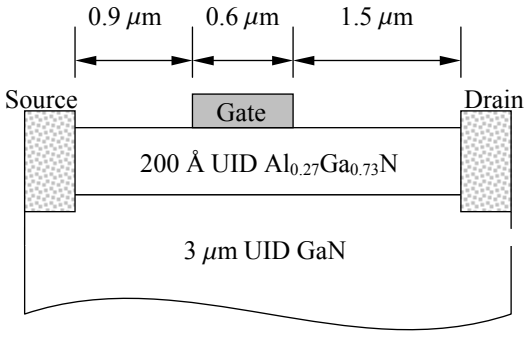
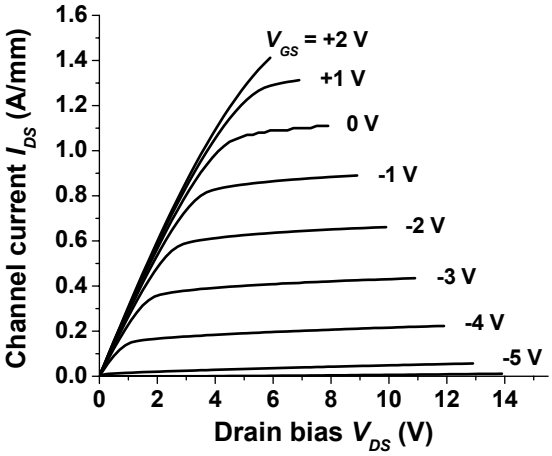


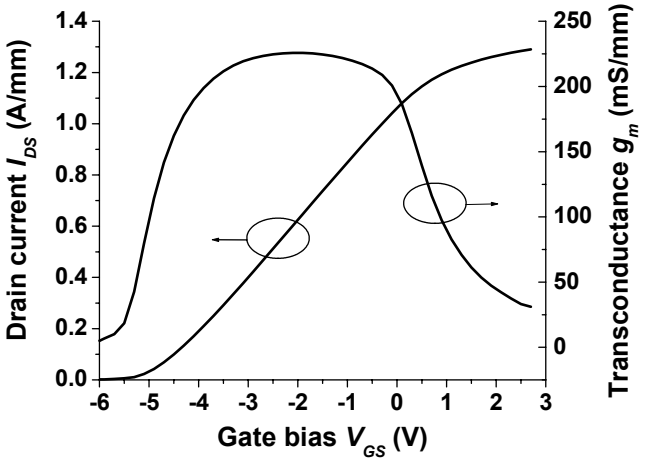

**Figure 2.5 Basic AlGaN/GaN HEMT structure used in the simulation.**

un-doped during the following simulations. The $I_{DS} \sim V_{DS}$ and $I_{DS} \sim V_{GS}$ curves are shown in Figure 2.6 (a) and Figure 2.6 (b) respectively. These output current characteristics display close agreement to measured results [18, 19]. The maximum drain current of 1.4 A/mm at $V_g$ = 1.8 V is slightly higher than experimental values, probably because the saturated velocity simulated by the Monte Carlo method is

higher than the real value in a 2-DEG, due to alloy and interface scattering in the channel. From the shape of the $g_m$ curve, the device simulation displayed much better linearity than experiments. Future simulation with more detailed examination of device structure should give an explanation to this discrepancy and help design high linearity GaN HEMTs.




**(a) $I_{DS} - V_{DS}$ curves.**




**(b) $I_{DS} - V_{GS}$ curve and $g_m$ curve.**

**Figure 2.6 *DC* simulation of the basic GaN HEMT.**

### *2.3.2 AC frequency response*

Figure 2.7 shows the frequency response of this device. The $f_t$ is 25 GHz and $f_{max}$ is 90 GHz. The current gain is in line with experimental results reported by various groups ($f_t \times L_g$ = 15 GHz·μm), but the $f_{max}$ is much higher. If the parasitic capacitance and the statistic output resistance are taken into account in the simulation (ATLAS does not offer this option), the $f_{max}$ should drop to the experimental value.

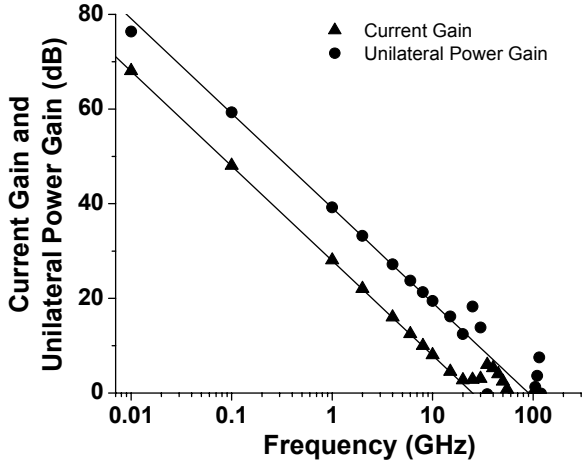



**Figure 2.7 Small signal frequency response of the basic GaN HEMT.**

### *2.3.3 Breakdown characteristics*

To simulate the breakdown voltage, the device was first biased under pinch-off, where $V_{gs}$ = –6 V is lower than the threshold voltage $V_T$ obtained from Figure 2.6 (b). Then the drain voltage was increased until the drain current rose sharply due to impact ionization. We define $V_{BR}$, as shown in Figure 2.8, to be that voltage on the simulated $I_{ds}$-$V_{ds}$ curve, where the extrapolation of the saturation segment of the curve and the impact ionization induced rapidly rising segment intersect. The current

at the intersection point is denoted $I_s$, and it is used in simulation as a compliance to halt the drain voltage sweep before a divergence problem occurs. Figure 2.9 shows a contour plot of the electric field in GaN HEMT under breakdown conditions. The electric field peak at the gate edge is around 5 MV/cm which is assumed to be the critic field strength of $Al_{0.27}Ga_{0.73}N$. The drain breakdown voltage is 70 V, very close to the practical values for a gate-drain distance of 1.5 μm.

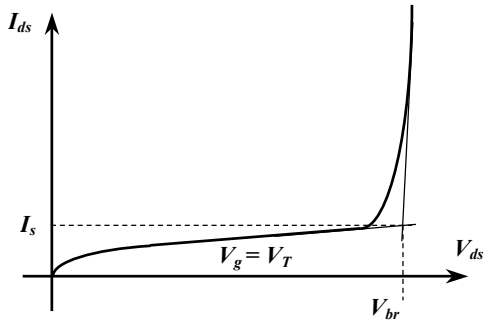



**Figure 2.8 Illustration of the definition of breakdown voltage employed in simulation.**

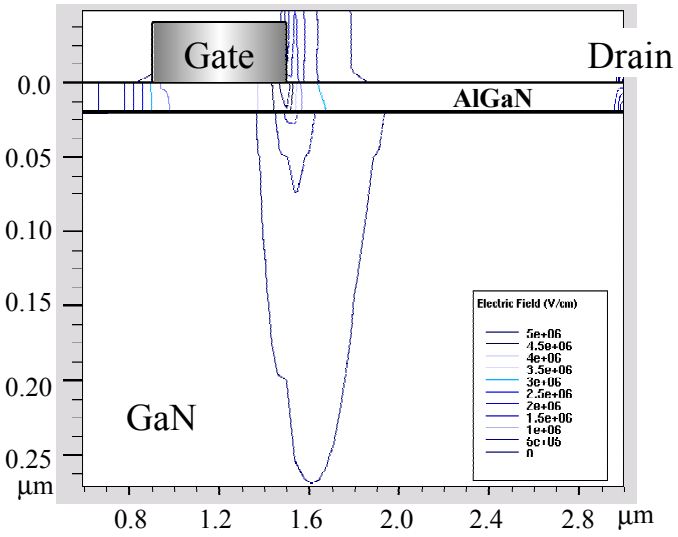



**Figure 2.9 Electric field distribution in a GaN HEMT. The device is pinched-off ($V_{gs}$ = –6 V) with drain bias $V_{ds}$ = 70 V.**

## 2.4 Summary

AlGaN/GaN material properties, polarization field and surface traps were implemented into ATLAS to perform a simulation of a GaN HEMT. The surface traps are the source of the channel 2-DEG and the polarization field is the driving force to move the charge from the traps to the channel. By precise fitting of the $n_s$ vs. $t_{AlGaN}$ curve to experimental results, this AlGaN/GaN heterojunction model was verified and the surface traps were found to be located in the middle of the bandgap of AlGaN with very high concentration. The possibility of a Gaussian surface trap distribution is also discussed qualitatively in this chapter. With proper mobility and impact ionization models, DC, AC, and breakdown simulations were performed for GaN HEMTs. The good agreement of simulations with experimental results is another validation of the GaN HEMT model. The GaN HEMT simulation developed in this chapter will be employed in the following chapters to help understand dispersion and electric field distribution in GaN HEMTs, and to help design high voltage GaN HEMTs.

## 2.5 References:


[1] L. F. Eastman, J. R. Shealy, V. Tilak, J. Smart, B. Green, and T. Prunty, "AlGaN/GaN HEMT microwave CW power limits," presented at Fourth International Conference on Nitride Semiconductors, Denver, Colorado USA, 2001.

[2] Y.-F. Wu, P. M. Chavarkar, M. Moore, P. Parikh, B. P. Keller, and U. K. Mishra, "A 50-W AlGaN/GaN HEMT amplifier," presented at International Electron Devices Meeting 2000, San Francisco, CA, USA, 2000.

[3] M. Micovic, N. X. Nguyen, P. Janke, W.-S. Wong, P. Hashimoto, L.-M. McCray, and C. Nguyen, "GaN/AlGaN high electron mobility transistors with $f_t$ of 110 GHz," *Electronics Letters*, vol. **36**, pp. 358-9, 2000.

[4] S. Wu, R. T. Webster, and A. F. M. Anwar, "Physics-based intrinsic model for AlGaN/GaN HEMTs," *MRS Internet Journal of Nitride Semiconductor Research*, vol. **4S1**, 1999.

[5] J. D. Albrecht, P. P. Ruden, S. C. Binari, and M. G. Ancona, "AlGaN/GaN heterostructure field-effect transistor model including thermal effects," *IEEE Trans. Elect. Dev.*, vol. **47**, pp. 2031-6, 2000.

[6] "Atlas User's Manual," Silvaco Inc. 1998.

[7] D. Brunner, H. Angerer, E. Bustarret, F. Freudenberg, R. Hopler, R. Mimitrov, O. Ambacher, and M. Stutzmann, "Optical constants of epitaxial AlGaN films and their temperature dependence," *J. Appl. Phys.*, vol. **82**, pp. 5090-6, 1997.

[8] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, A. J. Sierakowski, W. J. Schaff, L. F. Eastman, R. Dimitrov, A. Mitchell, and M. Stutzmann, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. **87**, pp. 334-44, 2000.

[9] C. I. Wu, A. Kahn, N. Taskar, D. Dorman, and D. Gallagher, "GaN (0001)-(1x1) surfaces: Composition and electronic properties," *J. Appl. Phys.*, vol. **83**, pp. 4349-4352, 1998.

[10] V. M. Bermudes, C. I. Wu, and A. Kahn, "AlN films on GaN: Sources of error in the photoemission measurement of electron affinity," *J. Appl. Phys.*, vol. **89**, pp. 1991, 2001.

[11] H. T. Grahn, *Introduction to Semiconductor Physics*: World Scientific Publishing Co., 1999.

[12] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Applied Physics Letters*, vol. **77**, pp. 250-2, 2000.

[13] I. P. Smorchkova, C. R. Elsass, J. P. Ibbetson, R. Vetury, B. Heying, P. Fini, E. Haus, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization-induced charge and electron mobility in AlGaN/GaN heterostructures grown by plasma-assisted molecular-beam epitaxy," *Journal of Applied Physics*, vol. **86**, pp. 4520-4526, 1999.

[14] V. M. Polyakov and F. Schwierz, "Influence of electron mobility modeling on DC I-V characteristics of WZ-GaN MESFET," *IEEE Trans. Elect. Dev.*, vol. **48**, pp. 512-16, 2001.

[15] O. Ambacher, "Growth and applications of Group III-nitrides," *J. Phys. D: Appl. Phys.*, vol. **31**, pp. 2653-2710, 1998.

[16] I. H. Oguzman, E. Bellotti, K. F. Brennan, J. Kolnik, R. Wang, and P. P. Ruden, "Theory of hole initiated impact ionization in bulk zincblende and wurtzite GaN," *J. Appl. Phys.*, vol. **81**, pp. 7827-34, 1997.

[17] K. Kunihiro, K. Kasahara, Y. Takahashi, and Y. Ohno, "Experimental evaluation of impact ionization coefficients in GaN," *IEEE Electron Device Lett.*, vol. **20**, pp. 608-10, 1999.

[18] Y.-F. Wu, D. Kapolnek, J. Ibbetson, N.-Q. Zhang, P. Parikh, B. P. Keller, and U. K. Mishra, "High Al-content AlGaN/GaN HEMTs on SiC substrates with very high power performance," presented at International Electron Devices Meeting 1999, Piscataway, NJ, USA, 1999.

[19] Y.-F. Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, and U. K. Mishra, "Very-high power density AlGaN/GaN HEMTs," *IEEE Trans. Elect. Dev.*, vol. **48**, pp. 586-90, 2001.

# CHAPTER 3

# High voltage GaN switching HEMTs

Learning from the GaAs MESFETs, the first effort to improve breakdown voltage concentrated on how to alleviate the electric field peak on the drain side gate edge. The role of a semi-insulating buffer was next investigated. However, a limit of breakdown voltage, much lower than from the theoretical analysis of GaN HEMTs, seemed to exist. Careful examination of those HEMTs with high breakdown voltage raised the importance of the gate current on breakdown. An insulated gate structure was adopted and resulted in an increased breakdown voltage over 1000 volts. This was however at the expense of low switching speed. Other aspects to improve breakdown voltage will be addressed in the end of this chapter, and measurements to preserve the switching speed will be discussed in the next chapter.

## 3.1 Analysis of breakdown voltage of GaN HEMTs

In 1982, Baliga derived a figure of merit, BFOM = $\varepsilon \cdot \mu \cdot E_c^3$ [1], which defines material parameters to maximize the breakdown voltage and minimize the

conduction losses in power FET's. Here $\mu$ is the mobility and $E_c$ is the critical electric field (breakdown field). This figure was based on the trade-off between $R_{on}$ vs. $V_{BR}$ on the doping level in a power device. For a vertical device structure with a uniform doping profile, the on resistance of a FET may be represented as:

$$R_{on} = \frac{4V_{BR}^2}{\varepsilon_r \mu_n E_c^3} \qquad \text{or} \qquad \frac{V_{BR}^2}{R_{on}} = \frac{\varepsilon_r \mu_n E_c^3}{4} \tag{3.1}$$

The $V_{BR}^2/R_{on}$ is called the power-device-figure-of-merit and BFOM was directly originated from this equation. In order for high breakdown voltages, one has to reduce the doping level to extend the depletion length. This, in turn, will increase the on resistance and thus the switching loss. As pointed out in Eq. (3.1), $R_{on}$ rises as the square of $V_{BR}$. Hence, BFOM defines the intrinsic limit of a power semiconductor. However, it was created for vertical FET structures only. A GaN HEMT, as a lateral device, has different properties: the conductive channel is a two-dimensional charge, and this 2-DEG is not related to any doping in the material. Does its on-resistance act the same way as in a vertical device? What's the operation limit of a GaN HEMT compare to other power device? These questions call upon the necessity to derive a power-device-figure-of-merit for the GaN HEMT.

For the time being, all fabricated GaN HEMTs are lateral devices (not withstanding the CAVET structure realized by Ilan Ben-Yaacov and Yan Gao). The electrons transport as a two-dimensional gas in the AlGaN/GaN heterojunction channel. It is generally assumed that in an undoped GaN HEMT, the electrons in the channel are induced from the donor-like surface traps by the strong polarization field

in the AlGaN layer [2, 3] and the surface is left positively charged by the empty traps, as shown in Figure 3.1. The 2-DEG density can be as high as $4\times10^{13}$ $cm^{-2}$ without intentional doping and its density depends solely on Aluminum composition [4]. Assume a HEMT with gate width of $W_g$, source to drain distance of $L_{ds}$ and 2-DEG density of $n_s$, the channel resistance is given by:

$$R = \frac{L_{ds}}{q\mu_n W_g n_s}\ [\Omega],$$

$$\text{or } R_{on} = \frac{L_{ds}^2}{q\mu_n n_s}\ [\Omega \cdot cm^2] \qquad \text{for specific on-resistance} \qquad (3.2).$$

The breakdown characteristics of this device are analyzed as illustrated in Figure 3.2.

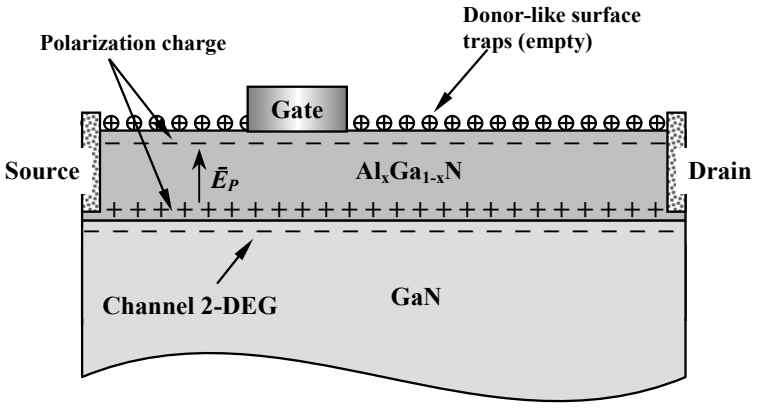



**Figure 3.1 Charge distribution in AlGaN/GaN HEMT.**

Experience in GaN HEMT operation observes that when the gate is pinched off and the drain is positively biased (in the Off-state of a switching device), electrons will inject into the surface traps from the gate. Since the surface traps are the sole source of the 2-DEG, when they are filled with the injected electrons, the channel charge is vertically depleted to keep the system electrically neutral. In the

lateral direction, the drain bias generates a constant electric field $E_x$ in the neutral region. This is distinct from a normal Si (or SiC) MESFET where the $E_x$ is of the shape of a triangle as the integration of the lateral depletion of the doping.

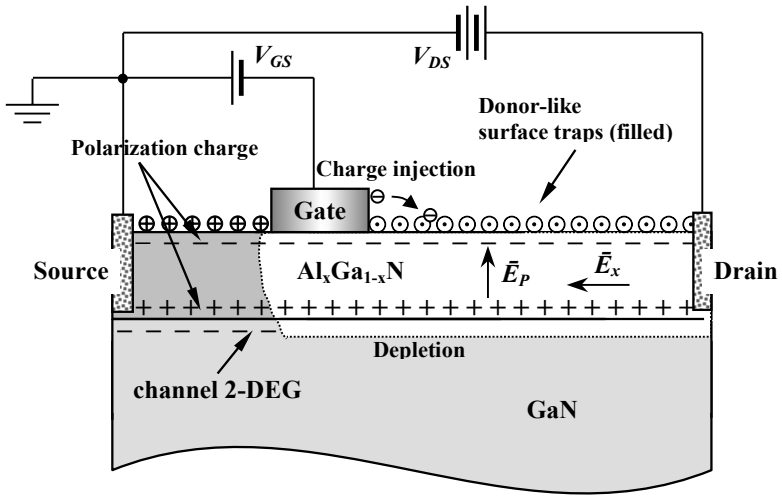



**Figure 3.2 Off-state AlGaN/GaN HEMT (under positive drain bias and pinched off).**

The polarization field $E_p$ is very strong in AlGaN. Though only the net polarization is considered (the polarization difference between AlGaN and GaN is deducted), $E_p$ is as high as several MV/cm and cannot be ignored in the analysis. Therefore, the total field in the depletion region is a combination of $E_x = V_{gd}/d_1$ (lateral) and $E_p$ (vertical): $E_{tot}^2 = E_p^2 + E_x^2$. If one assumes the gate-drain region is fully depleted when the device is biased to breakdown, then $E_x = V_{BR}/L_{gd}$, and $E_{tot}$ equals to $E_c$, the critical electric field of AlGaN. Together with Eq. (3.2) and $L_{gd} \approx L_{ds}$, the on-resistance can be expressed as:

$$R_{on} = \frac{V_{BR}^2}{q\mu_n n_s (E_c^2 - E_p^2)} \tag{3.3}$$

Eq. (3.3) reveals that, for GaN HEMTs, the on-resistance still follows a square rate with the breakdown voltage. The power device figure of merit $V_{BR}^2/R_{on}$ established for Si FET can be also applied to GaN HEMTs, which makes it possible for us to directly compare GaN HEMTs with other power devices directly. The only problem is that the 2-DEG density $n_s$ in Eq. (3.3) is not a material parameter. From the work by S. Keller to exploit the probability to grow non-relaxed $Al_xGa_{1-x}N$ with Aluminum composition ($x_{Al}$) ranged from 0.0 to 1.0, a linear dependency of $n_s$ on $x_{Al}$ was discovered [5]. Since the critical field of AlGaN is also a linear extrapolation of that of GaN and AlN, we can relate $n_s$ to $E_c$ directly as $q \cdot n_s = \zeta \cdot E_c$, where $\zeta$ is a constant with a unit of [F/cm]. Eq. (3.3) is re-formatted as

$$\frac{V_{BR}^2}{R_{on}} = \zeta \mu_n E_c (E_c^2 - E_p^2) \tag{3.4}$$

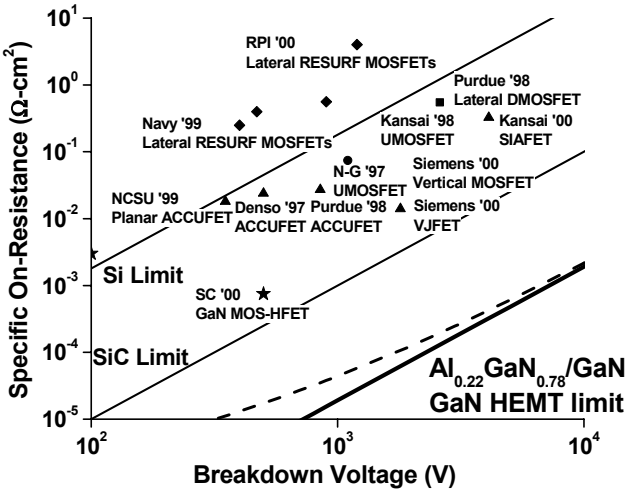



**Figure 3.3 Analytical limit for GaN switching HEMTs.**

The GaN HEMT power-device-figure-of-merit in Eq. (3.4) is now in the same form as that for Si (or SiC) devices in Eq. (3.1). Assuming the critical field $E_c$

= 5.15 MV/cm and the polarization field $E_p$ = 2.17 MV/cm for $Al_{0.22}Ga_{0.78}N$ [6], with practical value of $\mu_n$ = 1500 $cm^2/V{\cdot}s$ and $n_s = 1{\times}10^{13}$ $cm^{-2}$, the $R_{on} \sim V_{BR}$ relationship is calculated and drawn in Figure 3.3 with comparison to SiC and Si devices. The on-resistance of GaN HEMTs is about 50 times lower than that of SiC devices for the same breakdown voltage, or, the power-device-figure-of-merit is 50 times larger.

The limit for GaN HEMTs in Figure 3.3 is not the ultimate. As pointed out previously, the critical electric field of AlGaN, $E_c$, changes with the Aluminum composition. It is normally supposed that the breakdown voltage is higher with higher $x_{Al}$, but as the polarization field $E_p$ is taken into account, the assumption is not always true. Since the piezoelectric field in AlGaN is not proportional to $x_{Al}$, there is a maximum for $E_c' = \sqrt{E_c^2 - E_p^2}$. Figure 3.4 shows the variation of $E_c$', as well as the power device figure of merit given by Eq. (3.4), as a function of Aluminum composition. The highest breakdown voltage happens at 55 % Aluminum in AlGaN, while the highest power-device-figure-of-merit comes with $x_{Al}$ = 0.70, another four times improvement over an $Al_{0.22}Ga_{0.78}N$/GaN HEMT. Typically for GaN HEMTs, channel mobility decreases as Aluminum composition increases. However recently, new growth technique was developed at UCSB to increase charge density without degrading the mobility [7]. A thin layer of AlN (5 ~ 10 Å) was inserted between the AlGaN layer and GaN buffer in their work to reduce the alloy scattering brought by high Aluminum composition. Therefore, The next several years will see a further decrease in the on-resistance of GaN HEMTs.

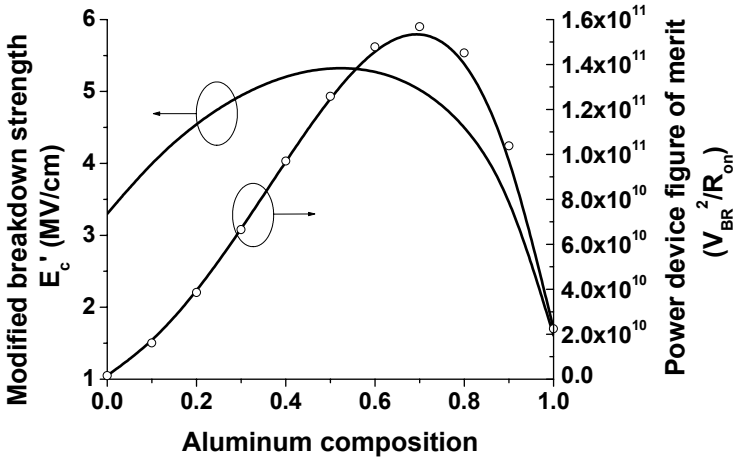


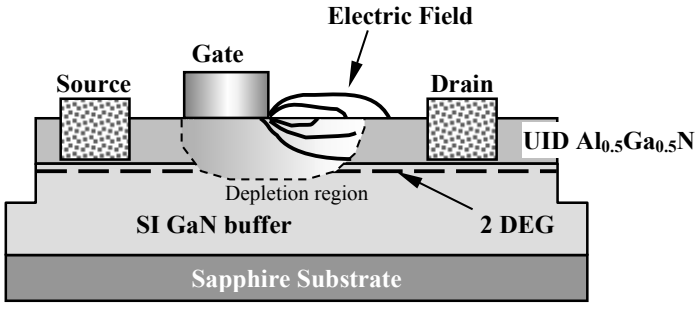

**Figure 3.4 Breakdown voltage of GaN HEMTs dependence on Aluminum composition.**

Ohmic contact resistance is always an issue in a wide bandgap material system. The latest research in UCSB exhibited a contact resistance as low as 0.23 Ω·mm [8]. When the contact resistance is taken into account, the GaN limit is modified to be the dotted line in Figure 3.3. The effect from the contact resistance has more impact in the lower breakdown voltage range, suggesting GaN HEMTs are more suitable for high voltage operation as a switching device.

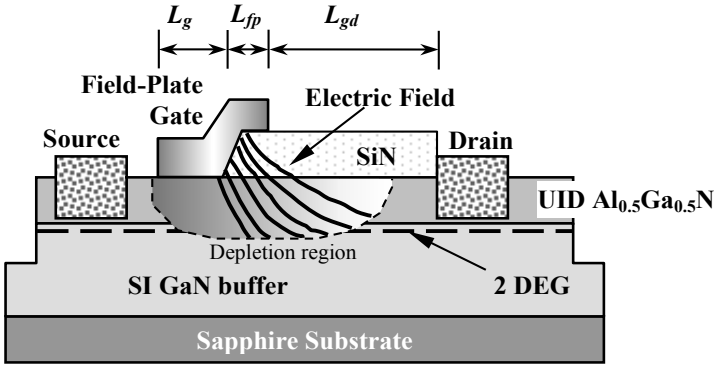
## 3.2 GaN HEMT with field-plate (overlapping gate)

Intensive work has been done to investigate the breakdown mechanism of GaAs MESFETs. The breakdown is due to an avalanche process that usually occurs near the gate edge on the drain side [9]. It is generally accepted that the essence of achieving a high breakdown voltage in a MESFET is to have an increasing depletion width at the surface of the channel from the Schottky gate to the drain [10]. Overlapping-gate (field-plate) MESFETs were realized by C.-L. Chen [11] and N.

Nguyen [12] on a low-temperature-grown (LTG) GaAs passivation layer. In a field-plate MESFET, the electric field originating from the field-plate contributes to the formation of a vertical depletion region in the passivation and conducting channel layers underneath. This is equivalent to providing additional negative charge at the surface of the channel, resulting in less charge in the channel. The depletion region in the *x*-direction is then extended by the field plate, which creates a second electric field peak at the field-plate metal edge. The second peak brings down the first peak at the gate edge, thus increasing the breakdown voltage of the device. The source-drain breakdown was improved dramatically from 22 V to 35 V by field-plates in [11, 13]. Simulations predict that the field-plate structure is also applicable to HEMTs [14]. GaN HEMT with field-plate structure shown in Figure 3.5 (b) illustrates the alleviation of the electric field peak at the gate edge, compared to conventional gate structure (Figure 3.5 (a)). SiN was used as the dielectric under the field-plate because of its high dielectric constant ($\varepsilon_r$ = 7.4) and high breakdown strength (10 MV/cm ideally), since simulation results have displayed a higher effectiveness of this structure with a higher dielectric constant [14].




**(a) Conventional gate GaN HEMT**




**(b) Field-plate GaN HEMT**

**Figure 3.5 Electric field in GaN HEMTs.**

### *3.2.1 Device fabrication*

AlGaN/GaN heterostructures with Al composition of 50% were grown by MOCVD on a *c*-plane sapphire substrate (batch # W990324A1). The epitaxial growth began with a 200-Å-thick GaN nucleation layer, followed by 3-$\mu$m-thick insulating *i*-GaN as the device buffer layer. The resistivity of the buffer was made higher than 200 MΩ·cm to minimize source-drain leakage. The structure was completed with a 200 Å unintentionally doped (UID) AlGaN layer. The AlGaN was left undoped to reduce the impact ionization, because simulation indicated that the electric field is highly concentrated in the AlGaN layer for GaN HEMTs. The room temperature sheet electron concentration ($n_s$) and electron mobility ($\mu$) obtained from Van der Pauw measurements on as-grown material were ~ $8\times10^{12}$ $cm^{-2}$ and ~ 1000 $cm^2/Vs$ respectively. This relatively high $n_s$ without doping was the result of the strong polarization field in the high Al content AlGaN [15].

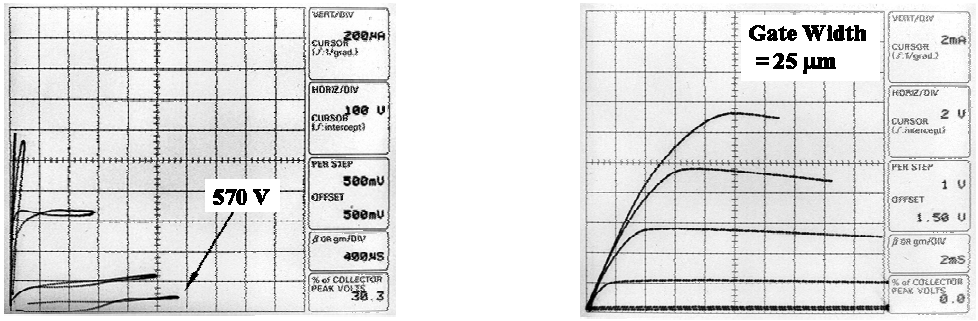
Both conventional HEMTs and field-plate HEMTs were fabricated on the same wafer for comparison. Ti/Al/Ni/Au (200/2000/500/400 Å) were evaporated and annealed at 870 $^{o}$C for 30 sec. to form ohmic contacts. 1500Å sputtered SiN was then selectively deposited in the region between source and drain using lift-off technique. Ni/Au (200/3000 Å) were evaporated next for gate metalization, with the drain side edge of the gate overlapping the SiN by approximately 0.3 $\mu$m. The final step of the process was to form a device mesa with $Cl_2$ reactive ion etching (RIE). Conventional devices were covered by photoresist during the SiN deposition step. Devices with various gate lengths ($L_g$), gate-drain spacing ($L_{gd}$) and field-plate lengths ($L_{fp}$) were fabricated to investigate the structure dependency of breakdown voltage. The gate width on all devices was 25×2 $\mu$m.

Sputtered SiN was employed in field-plate because it can be lifted-off to define the edge where the gate overlaps. To use PECVD SiN, the SiN film should be dry-etched after deposition to form the overlapping edge. Since dry-etch damages the channel surface under the gate and degrades device performance, PECVD SiN was not used.

### *3.2.2 Device performance*

Record source-drain breakdown voltage ($V_{BR}$) of 570 V was obtained on a field-plate HEMT with $L_{gd}$ = 13 $\mu$m and $L_g$ = 1.0 $\mu$m. The devices exhibited "hard" breakdown behavior, e.g. there was no significant increase in $I_{ds}$ before breakdown occurred. This suggests that the gate-drain breakdown determines the source-drain

breakdown. The off-state and on-state DC $I_{ds}$-$V_{ds}$ characteristics of this device are shown in Figure 3.6. The maximum value of drain current ($I_{max}$) of this device was 520 mA/mm and the specific on-resistance was as low as 1.5 mΩ·cm$^2$ (active region = $L_{ds} \times W_g = 3.75\times10^{-8}$ cm$^2$).




**(a) Off-state *I-V* characteristics.** **(b) On-state *I-V* characteristics.**

**Figure 3.6 The $I_{ds}$-$V_{ds}$ characteristics of a field-plate GaN HEMT.**

Figure 3.7 shows the dependency of breakdown voltage and maximum drain current on different values of $L_{gd}$ for field-plate HEMTs. $V_{BR}$ saturates at an $L_{gd}$ of about 13 μm ($V_{br} \approx$ 550 V), which suggests that the extension of the gate depletion region saturates at that length. Beyond this point, the electric field at the drain-side edge of the gate exceeds the critical breakdown field of AlGaN. At this length of $L_{gd}$, the average electric field along the channel is only 0.43 MV/cm, compared with the ideal GaN breakdown strength of 3.3 MV/cm. This means that the electric field still peaks at the gate edge, and gives room for further material and process development. The maximum drain current is the same for all lengths of $L_{gd}$, because $I_{ds}$ only depends on the $n_s \cdot v_s$ product. Conventional HEMTs are also compared in

Figure 3.7. The highest breakdown voltage of 460 V is 20 % lower than that of field-plate devices. The breakdown voltage saturates at $L_{gd}$ = 10 $\mu$m for conventional devices, while their maximum drain current is almost the same as that of field-plate devices. Breakdown voltage saturates at a longer $L_{gd}$ for field-plate HEMTs indicates that the field-plate structure extends the channel depletion length, thus increases the breakdown voltage. Passivation on conventional HEMTs with SiN has been also done on other wafers under experiment. After passivation, the surface of the conventional HEMTs between the gate and drain is the same of that in overlapping gate HEMT. But no obvious difference in breakdown voltage was noticed before and after passivation. This suggests that the field-plate, not the passivated surface, improved the breakdown voltage.

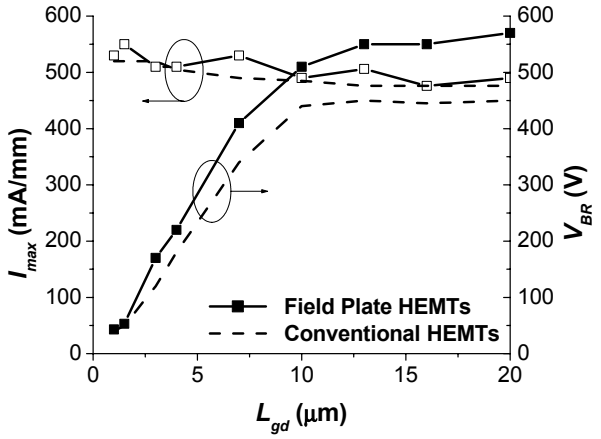



**Figure 3.7 Dependence of $V_{BR}$ and $I_{max}$ on gate-drain spacing.**

Figure 3.8 shows that at short gate-drain spacing (< 10 μm), the breakdown voltage increases with longer gate length, while at larger $L_{gd}$ the gate length does not affect $V_{BR}$ any more. When $L_{gd}$ is short, the leakage current in the channel rises

quickly with respect to high drain bias, causing pre-mature breakdown, with a short gate worsening this condition. However at large $L_{gd}$, the channel leakage does not rise apparently at high drain bias before the device breaks down. Thus gate length does not have an effect on $V_{BR}$. For a high-voltage GaN HEMT, we do not need to sacrifice the switching speed by increasing the gate length beyond 1 μm in order to obtain high breakdown voltage. This buffer leakage is also the reason that the breakdown voltages of field-plate devices are not substantially higher than those of conventional devices at short lengths of $L_{gd}$ (Figure 3.7). Another helpful observation was that the breakdown voltage did not depend on the length of the field-plate ($L_{fp}$). Since the field-plate adds to the input capacitance ($C_g$), it is favorable to minimize $L_{fp}$ for higher frequency response.

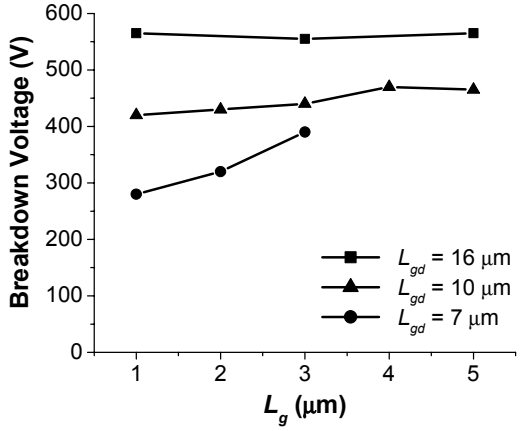



**Figure 3.8 Dependency of breakdown voltage on gate length.**

The scattering parameters of field-plate HEMTs were measured at $V_{ds}$ = 15 V and $V_{gs}$ = 0.5 V. The unity-current-gain frequency $f_T$ was 6.2 GHz for the device with $L_{gd}$ = 13 μm and $L_g$ = 1 μm, and the maximum frequency of oscillation $f_{max}$ was

8.9 GHz. Due to a low bias, the $f_T$ is primarily determined by the gate length, not the gate-drain spacing as shown in Figure 3.9. Though not measured, it is expected that $f_T$ will drop with higher bias because of the extension of the depletion region.

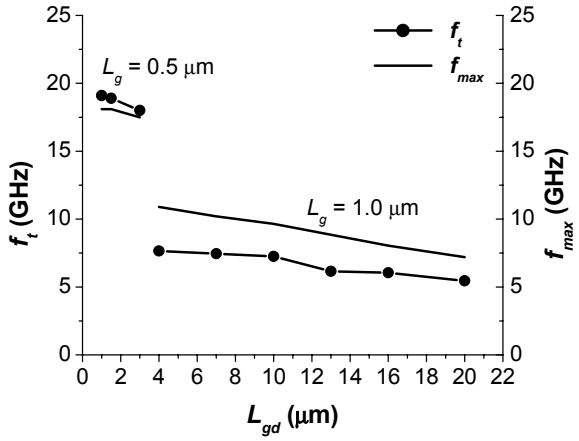



**Figure 3.9 Dependency of $f_t$ and $f_{max}$ on gate-drain spacing.**

To summarize, field-plate GaN HEMTs were studied for high voltage operations, and the breakdown voltage was increased by 30 % over conventional devices. It was discovered that gate length does not affect the breakdown voltage but influences the frequency response. So, opposite to expectation, short gate length is desired in high voltage GaN HEMTs for better switching speed.

## 3.3 Highly resistive GaN buffer

A semi-insulating buffer is the most basic requirement for high voltage devices. In switching applications, device leakage is directly connected to the power dissipation on the converter, and determines the conversion efficiency. Large amounts of power consumed on the devices would increase the temperature, thus

increase the on-resistance, leading to burnout. The leakage also limits the breakdown voltage by enhancing the impact ionization. In addition to the above effort on electric field reduction, a buffer with low leakage was also investigated.

### *3.3.1 Buffer grown on Sapphire*

Our initial research on high voltage HEMTs was based on GaN grown by MOCVD on Sapphire, given its relatively cheap price and well-established growth procedure at UCSB. To fabricate semi-insulating films, the residual background carrier concentration in the GaN film had to be reduced. Detailed investigations suggested that oxygen impurities, rather than nitrogen vacancies, are the major source of residual electrons. Oxygen either comes from the impurities in the gases, during wafer loading, or from out-diffusion from the Sapphire substrate. By using *ex-situ* baked substrates and inserting a long flush time after wafer loading, the residual carrier concentration in the GaN films could be reduced to $2.2\times10^{16}$ $cm^{-3}$ [16]. Figure 3.10 shows the typical behavior of devices made on GaN grown by above

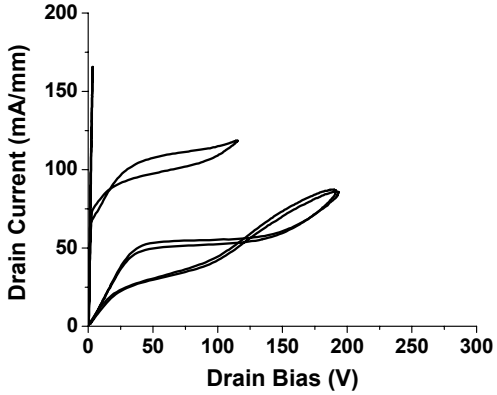



**Figure 3.10 Device biased to pinch-off with leaky GaN buffer grown on Sapphire.**

techniques. The device could not be pinched off with the channel leakage as high as 50 mA/mm, and avalanche ionization started to appear at $V_{DS}$ = 150 V.

Besides system purity, the residual background carrier concentration depends on the growth conditions, e.g. highly resistive buffer were generally obtained at reduced reactor pressure (LP), characterized by a higher carbon impurity concentration. Under these conditions, the background donors were compensated by a deep acceptor, the so-called yellow level in photoluminescence (PL) spectrum. Carbon may be associated with the defects characterized by the yellow level. A second GaN layer was deposited under atmospheric pressure (AP) on top of the LP i-GaN to ensure a low density of point defects in the GaN layer close to the AlGaN/GaN interface.

Figure 3.11 shows the output *I-V* characteristics of a device with AP/LP GaN buffer on Sapphire (sample # 990428A). The channel leakage was reduced to below 20 mA/mm and no apparent ionization current was observed. This device could support drain voltage up to 500 V and most likely failed due to excess heat generated

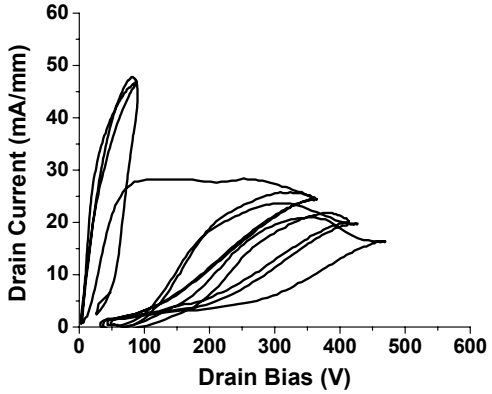



**Figure 3.11 Device with AP/LP GaN buffer grown on Sapphire.**

by the leakage. With 16 mA leakage, 500 V bias will produce 8 Watts heat on 1 mm wide device. It is desirable to lower the channel leakage to less than 1 mA/mm. The large hysteresis (loop) in the *I-V* curves with drain bias sweep is a strong trap effect which is supposedly from the deep traps in the LP buffer.

### *3.3.2 Buffer grown on SiC*

To search for lower buffer leakage, SiC was investigated as a reliable substrate for the epitaxial growth of a semi-insulating GaN buffer. Brendan Moran conducted all of the material growth on SiC for this thesis. Figure 3.12 shows a device made on AP buffer grown on SiC (sample # N000923A). This buffer growth

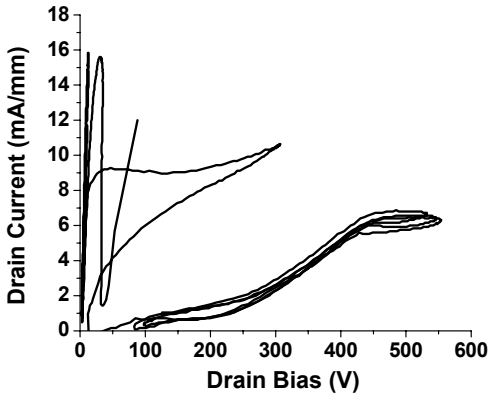



**Figure 3.12 Device with Atmosphere-Pressure grown GaN buffer on SiC.**

procedure was originally utilized to fabricate highly-resistive buffer for microwave power HEMTs. Owing to much lower oxygen out-diffusion during the growth, the buffer leakage is less than 10 mA/mm at more than 500 V drain bias, which was already a large improvement from GaN buffer on Sapphire.

LP/AP growth technique was also employed in buffer grown on SiC to further reduce the leakage. Figure 3.13 shows that the source-drain leakage decreased to 0.2 mA/mm for a device made on LP/AP buffer (sample #001001A).

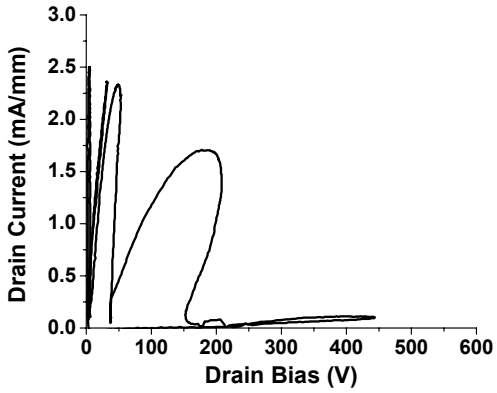
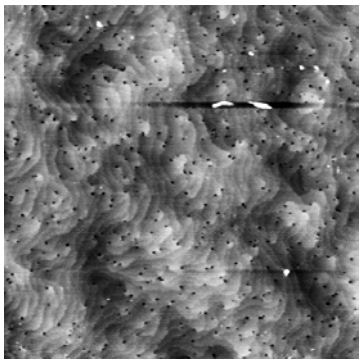
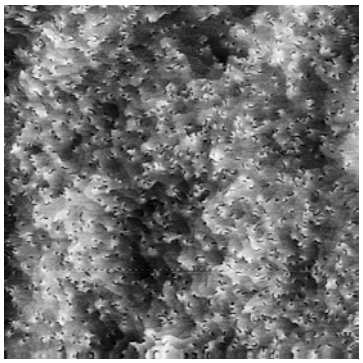



**Figure 3.13 Device with Low-Pressure grown GaN buffer on SiC.**

This LP/AP growth on SiC was then implemented as a standard procedure to produce consistent low leakage buffer for high voltage GaN HEMTs. The low leakage current is believed to related to higher buffer resistivity due to high dislocation density and high carbon impurity level. Figure 3.14 displays AFMs made on the two samples in Figure 3.12 and Figure 3.13. The dislocation density of the LP buffer is $3.9\times10^{9}$ $cm^{-2}$, much higher than that of the AP buffer of $2.7\times10^{9}$ $cm^{-2}$. Moreover, SIMS measurement of the LP buffer revealed a carbon level of $4\times10^{17}$ $cm^{-3}$, compared to that of $2\times10^{16}$ $cm^{-3}$ in an AP buffer. The deep traps and deep acceptors created by the dislocations and carbon impurities compensate the residual background carriers and result in the considerably lower leakage in the buffer layer.



**(a) AP GaN buffer on SiC.**



**(b) LP GaN buffer on SiC.**

**Figure 3.14 AFMs taken on devices with AP and LP GaN buffer grown on SiC substrates.**

Besides the off-state current, the sub-threshold swing (*SW*) is another criterion to characterize the buffer layer of an FET. Due to Debye tail in charge distribution, it is impossible to turn off an FET abruptly. *SW* represents how fast the drain current is shut off by the gate bias below the threshold. The drain current in the sub-threshold regime can be expressed as $I_d \propto \exp\left(-\eta \frac{V_{gs}}{KT/q}\right)$, where $\eta$ is the ideality factor. The *SW* is defined as:

$$SW = \frac{dV_{gs}}{d\left(\lg I_d\right)} = \eta\left(\frac{KT}{q}\ln 10\right) = 60\left(T/300\right)\cdot\eta \qquad (3.5)$$

The smaller $\eta$ ($\geq 1$), the lower *SW* and the faster turn-off of the device.

The sub-threshold swing was measured on a heated stage with the gate-control characteristics shown in Figure 3.15 and ideality factors in Figure 3.16. At room temperature, the off-state current is below the measurement limit and the corresponding ideality factor is 1.2, comparable to the best value achieved on GaN

HEMTs [17]. The results indicate that the LP/AP GaN buffer layer is suitable for high voltage switching devices. However, the gate pinch-off voltage increased from −9 V to −17 V and the *SW* ideality factor increased to 3 at 300 $^{o}$C. The degradation of the sub-threshold characteristic at elevated temperature comes from the traps in the buffer. More electrons are released from the traps at a higher temperature; therefore, device pinch-off is more difficult and occurs at a slower rate.

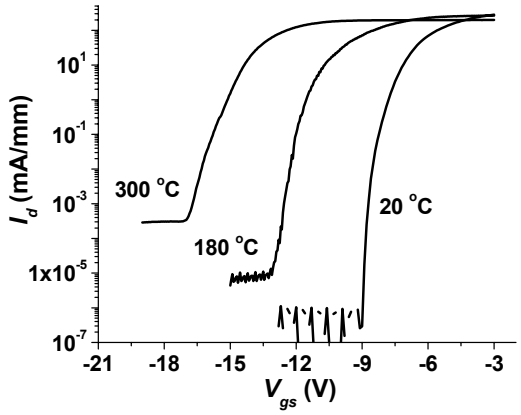



**Figure 3.15 Gate control characteristics at various temperatures ($V_{ds}$ = 10 V).**

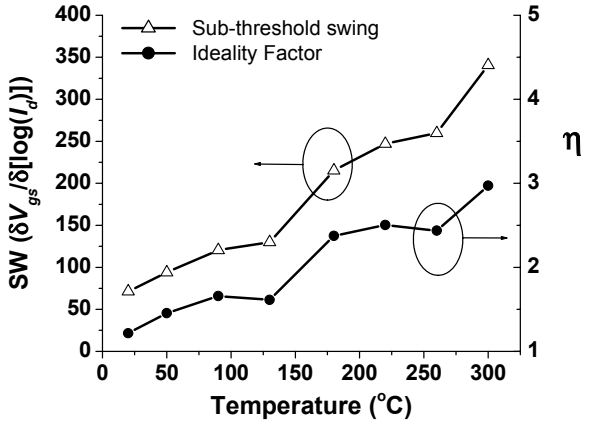



**Figure 3.16 Sub_threshold swing and its ideality factor vs. temperature.**

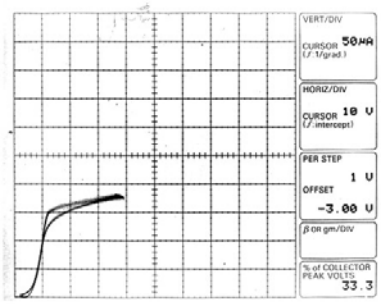
As mentioned before, an advantage of using SiC as a substrate is that its thermal conductivity is 15 times higher than that of sapphire. Calculation shows that the temperature rise for HEMTs on sapphire substrate can be 10 times higher in comparison with that for HEMTs on SiC substrate [18]. This advantage of SiC substrate is highly desired when GaN HEMTs are operated at elevated temperature and with ultra-high power density.

As a summary, the buffer leakage of high voltage GaN HEMTs was reduced from 20 mA/mm to 0.2 mA/mm by growing LP/AP GaN layer on SiC substrates. Unfortunately, the breakdown voltage remained at around 500 V, regardless of the improvement of the buffer. From previous analysis, the ideal on-resistance for a GaN HEMT with 13 μm gate-drain spacing should be 1.32 $m\Omega \cdot cm^2$ (Eq. (3.2)), and the breakdown voltage should be 6000 V (Eq. (3.4))! The on-resistance is consistent with experimental result, but the breakdown voltage is apparently too high. Device simulation disclosed that the field crowding effect usually elevates the electric field at the gate edge by 3 to 6 times. Despite this effect, the breakdown voltage should be above 1000 V. There must exist something else that prevents those devices from sustaining a higher voltage.

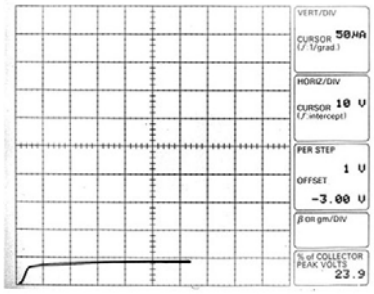
## 3.4 Insulated gate HEMTs

Devices with different breakdown voltages were examined carefully and it was noticed that the lower breakdown voltage was usually accompanied with higher gate leakage current (Figure 3.17). The detrimental effect of gate leakage on

breakdown voltage had long been observed for GaAs MESFETs. A low-temperature-grown (LTG) GaAs epitaxial layer under the gate was believed to have reduced the gate leakage and increased the breakdown voltage from 21 V (of typical GaAs MESFET) to 35 V [19]. The avalanche ionization was alleviated with the reduced gate leakage by the gate insulator. Similarly, GaAs MISFETs structure demonstrated record microwave power of 1.57 W/mm on a device with $V_{BR}$ of 43 V [20]. A MOS structure was also applied to GaN HEMTs and lowered the gate leakage by 5 orders with a breakdown voltage of 500 V [21]. Therefore, it is appealing to investigate the high voltage performance of our GaN HEMTs with insulator under the gate.




**(a) Device with $V_{BR}$ = 310 V.**




**(b) Device with $V_{BR}$ = 400 V.**

**Figure 3.17 Gate leakages of devices with different breakdown voltage.**

### *3.4.1 Insulated gate GaN HEMTs with JVD $SiO_2$ as the insulator*

GaN epi-layers were grown on a semi-insulating SiC substrate by MOCVD (batch # N001001B). The device structure is shown in Figure 3.18. An 85-nm thick AlN nucleation layer was followed by the deposition of 1 μm un-intentionally doped

GaN layer grown at 76 Torr (low pressure, LP) for semi-insulating buffer, a 150-nm GaN layer at 760 Torr (atmospheric pressure, AP) for low impurity channel, and finally capped with 25-nm UID $Al_{.27}Ga_{.73}N$ barrier layer. A room temperature Hall measurement showed sheet electron concentration $n_s = 8.1\times10^{12}$ $cm^{-2}$ and mobility $\mu_n$ = 1460 $cm^2/V\cdot s$. The high mobility/low charge configuration is the result of no doping and low Aluminum composition. The buffer leakage is 50 μA at 1000 V on two Indium contacts 1 mm apart.

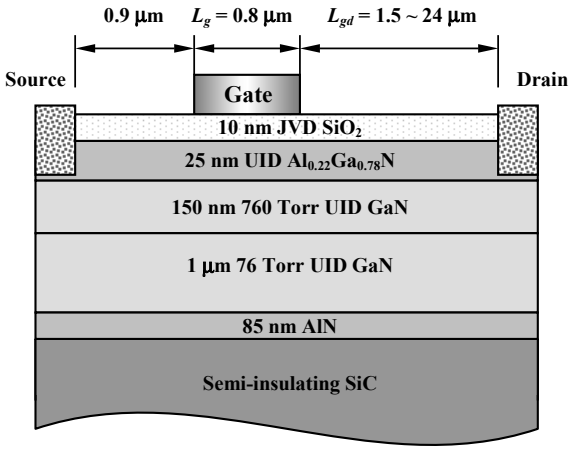



**Figure 3.18 Cross sections of GaN HEMT with JVD $SiO_2$ as the gate insulator.**

When a GaN HEMT is biased to breakdown, the electric field at the gate edge is close to the critical field of AlGaN (around 5 MV/cm). Therefore, the breakdown strength of the gate dielectric must be higher than this value to be effective. Otherwise the dielectric will cause the device failure before it breaks down. JVD (Jet Vapor Deposition) $SiO_2$ was selected as the gate insulator because it was proven to possess very high breakdown electric field strength (≥ 12 MV/cm) with low leakage current even at 450 $^oC$ (Figure 3.19) [22]. 10 nm JVD $SiO_2$ film was directly

deposited on the as-grown sample at Yale University before device processing. Before the sample was loaded into the JVD chamber, it was treated with 30 % $NH_4OH$ solution at 50 $^oC$ for 10 minutes after the solvent clean to remove the surface oxide. Research at Yale University have claimed that the interface trap density between the $SiO_2$ and the GaN layer is below $5\times10^{10}$ $cm^{-2}eV^{-1}$, which is comparable to good Si based MOS devices [22]. Experiments at UCSB suggested a larger interface state density as will be discussed in the next chapter.

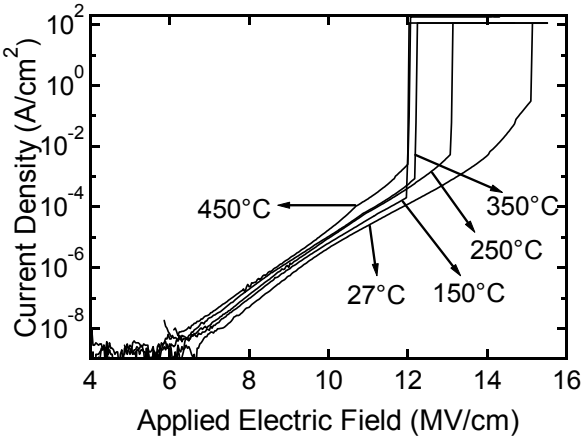



**Figure 3.19 Temperature dependent I-V measurement on JVD ONO dielectrics.**

The device process followed the standard procedure of GaN HEMT processing, except that before ohmic contact metal evaporation, the $SiO_2$ film was RIE etched to open the contact window. The etch conditions are: $SF_6/O_2$ gas flow = 5/2 sccm; pressure = 10 mTorr and bias = 100 V; and the etch rate is around 20 nm per minute. No degradation of the contact resistance was observed due to the $SiO_2$ etch. Devices with different gate-drain distances ($L_{gd}$ = 4 ~ 20 μm) and gate width ($W_g$ = 500 & 1,000 μm) were fabricated, and the gate length is 1 μm fixed.

The gate diodes were first tested to compare the gate leakage with and without gate insulator (the control sample was cut from the same piece). The insulated gate with 100 Å JVD $SiO_2$ exhibited more than 2 orders lower gate leakage than that of a normal Schottky gate (Figure 3.20). Moreover, the turn-on voltage of the insulated gate was around 10 V, much larger than that of the Schottky gate of ~ 1.2 V (Figure 3.21). Such a high turn-on voltage gives us an opportunity to bias the gate higher for less on-resistance.

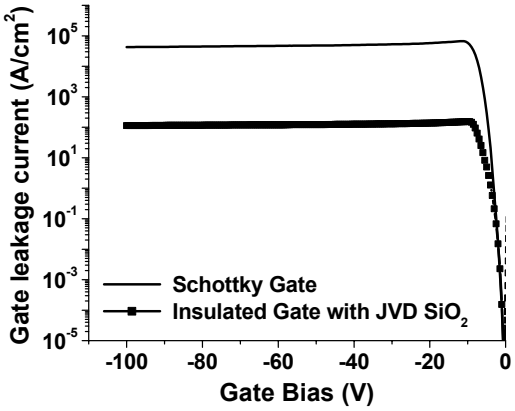



**Figure 3.20 Reverse gate characteristics.**

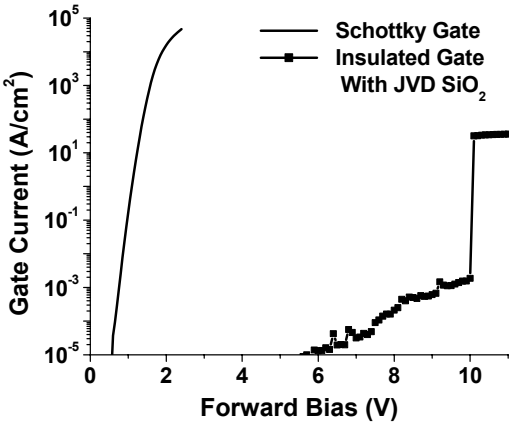
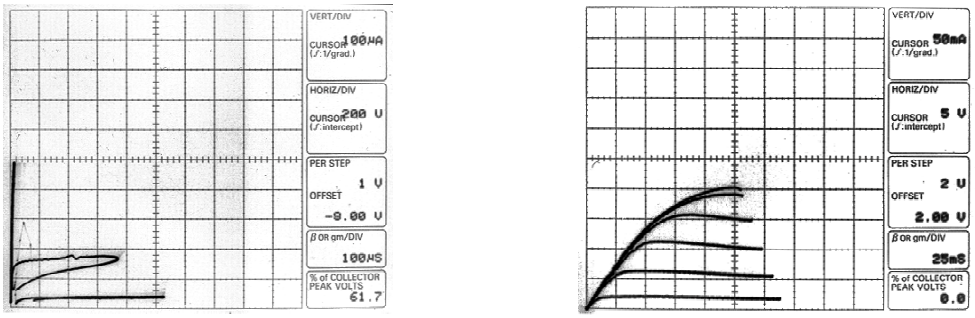



**Figure 3.21 Forward gate characteristics.**

The $I_{DS}$ - $V_{DS}$ characteristics for an insulated gate GaN HEMT with $L_g$ = 4 μm, $L_{gd}$ = 20 μm and $W_g$ = 200 μm are shown in Figure 3.22. The breakdown voltage of this device was 1050 V, a remarkable improvement from the field-plate GaN HEMT. The specific on-resistance was 3.1 mΩ·cm$^2$ (active area ~ 5×10$^{-5}$ cm$^2$) with a gate bias of 2 V ($R_{on}$ can also be expressed as 12.5 Ω·mm for lateral device). Even though the gate could be biased at a higher voltage, a larger drain current was not observed since unlike GaAs FETs, the access region of GaN HEMTs does not have higher charge density than the channel under the gate. The threshold voltage of this device was –9 V and gate control ratio $\Delta V_{DS}/\Delta V_{GS} \approx 110$. This high ratio is highly preferred in low-voltage controlled high-voltage applications like a power converter in megawatt power systems. The on-resistance is slightly higher than previous results due to the long gate-drain spacing and large ohmic contact resistance of 0.8 Ω·mm measured by TLM pattern.




**(a) Off-state *I-V* characteristics.** **(b) On-state *I-V* characteristics.**

**Figure 3.22 The $I_{ds}$-$V_{ds}$ characteristics of an insulated gate GaN HEMT with JVD $SiO_2$ as the gate insulator.**

Besides the improvement of gate characteristics, the device layout design was also investigated to achieve breakdown voltage higher than 1 kV. Figure 3.23 shows two device layout designs for high voltage GaN HEMTs. The left one is the regular CPW design with T-shape gate-finger; the right one is a circular device with drain in the center. Normally, electric field crowds at the end of the gate-finger for a regular device and causes local breakdown of the device. However for a circular device, there is no start or end of the gate finger and the electric field distributes evenly all along the finger. The two kinds of devices were fabricated side by side on the same sample for comparison. Measurement revealed that the highest breakdown voltage detected on regular devices was 700 V, while it was 1050 V for circular devices, with an average of 900 V. Consequently, circular devices were used in the following research.

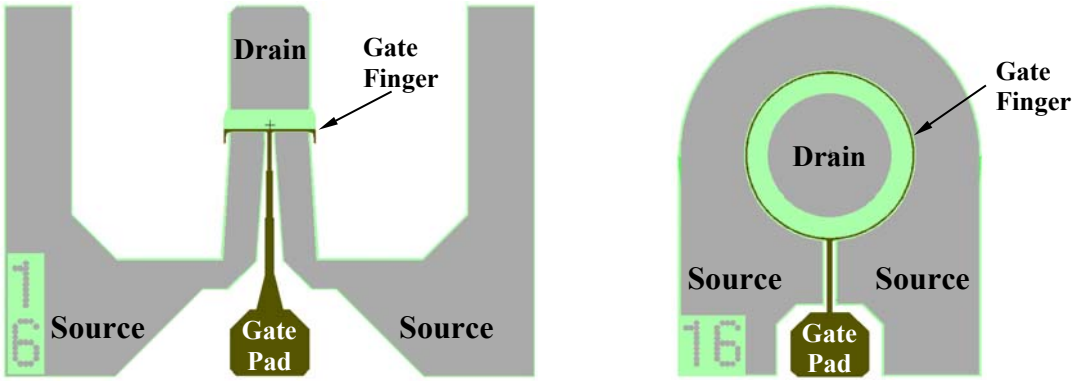



**Figure 3.23 Two different layout designs of high voltage GaN HEMTs.**

### *3.4.2 Insulated gate GaN HEMTs with e-beam $SiO_2$ as the insulator*

From the process point of view and for quick fabrication turn-around, E-beam evaporated $SiO_2$ is the best choice because it can be deposited in the same evaporation with the gate metal without any modification of the standard GaN HEMT process. The experiment was made on sample N010413C ($\mu$ = 1284 $cm^2/V{\cdot}s$, $n_s$ = $9.54\times10^{12}$ $cm^{-2}$ and buffer leakage < 10 μA at 1000 V). Since the dielectric constant of $SiO_2$ (~ 3.9) is much less than that of AlGaN (~ 9), the devices with $SiO_2$ as gate insulator are harder to pinch off than conventional HEMTs. The thickness of the AlGaN layer of this sample was made to be 160 Å for easy pinch-off. 100 Å $SiO_2$ was e-beam evaporated under the gate metal. The new device structure is shown in Figure 3.24.

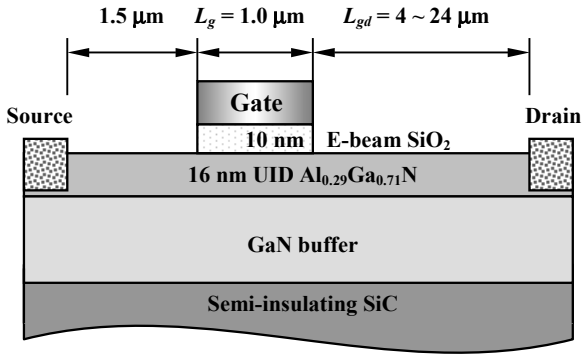



**Figure 3.24 Insulate gate HEMT with e-beam $SiO_2$.**

Figure 3.25 shows the temperature dependent gate leakage under reverse bias. The measurement was conducted in atmospheric ambient on a QuieTemp S-1060 heated stage. The gate leakage at room temperature is 5 orders lower than that of a conventional Schottky gate. This result is better than the one using JVD $SiO_2$ because on sample N001001B, the JVD deposition was finished with a thin layer

SiN. The excess leakage is believed from the SiN layer. The leakage current did not rise before 120 °C (the temperature of the stage), probably due to the temperature gradient in the SiC substrate. At 270 °C, the gate leakage is still lower than that of a Schottky gate at room temperature, suggesting that the insulated gate structure is ideal for high temperature environment where major applications of GaN switches will be found. The gate turn-on voltage is 10 V, corresponding to an electric field strength of 6 MV/cm for $SiO_2$.

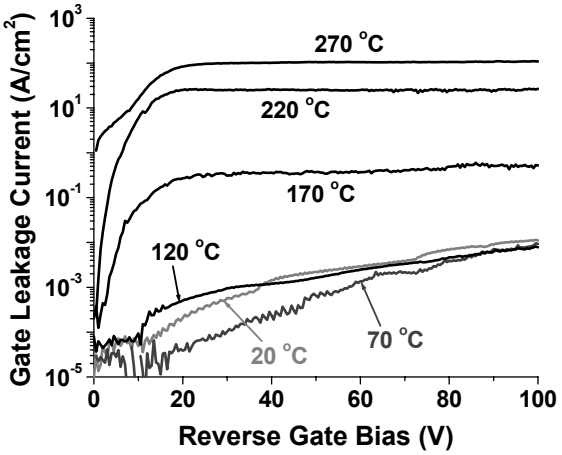
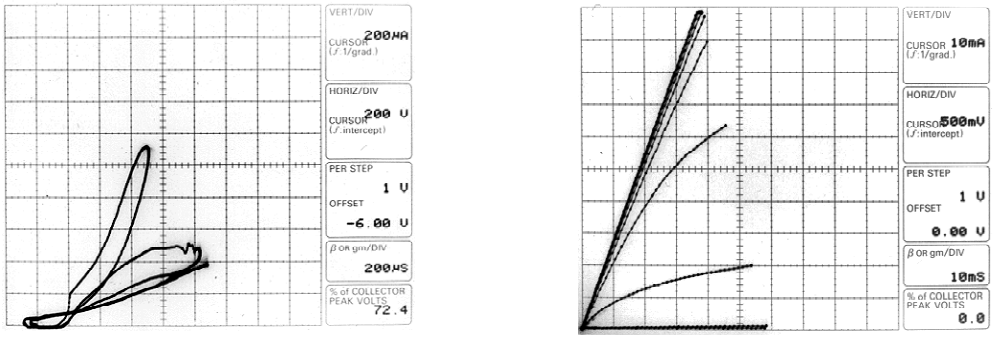



**Figure 3.25 Temperature dependent gate leakage under reverse bias.**

The off- and on-state characteristics of a HEMT with $L_g$ = 1 μm, $L_{gd}$ = 16 μm and $W_g$ = 500 μm are shown in Figure 3.26. The breakdown voltage is 1300 V and the specific on-resistance is 1.65 mΩ·cm$^2$ (9.1 Ω·mm)(active area ~ 9.25×10$^{-5}$ cm$^2$) at gate bias of 0 V. The threshold voltage of this device is –8 V and $\Delta V_{DS} / \Delta V_{GS} \approx 160$. The breakdown voltage is by far the highest achieved on all switches based on GaN material, and the on-resistance is lower than any SiC switching devices. The power

device figure of merit $V_{BR}^2 / R_{on} = 9.94\times10^8$ [$V^2\cdot\Omega^{-1}cm^{-2}$] is also higher than any kind of switching devices reported. This number also approaches the theoretical SiC limit as shown in Figure 3.27. This experiment successfully demonstrated that, with low leakage at high temperature, e-beam evaporated $SiO_2$ is a good candidate for gate insulator in GaN HEMT switches.




**(a) Off-state *I-V* characteristics.** **(b) On-state *I-V* characteristics.**

**Figure 3.26 The $I_{ds}$-$V_{ds}$ characteristics of an insulated gate GaN HEMT with e-beam $SiO_2$ as the gate insulator.**

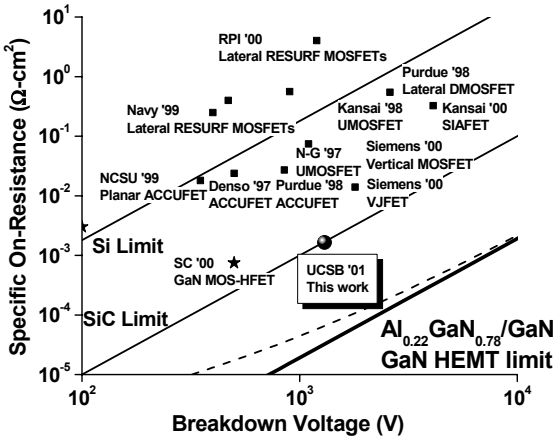



**Figure 3.27 Compare insulated gate GaN HEMTs to other power switches.**

The breakdown voltage and on-resistance were measured with respect to the gate-drain spacing (Figure 3.28). Increasing source-drain leakage before breakdown was detected with $L_{gd}$ shorter than 8 μm due to channel punch-through and space charge limited current, while devices with longer $L_{gd}$ displayed no channel leakage (destructive breakdown). Consequently, the devices with short $L_{gd}$ suffered from pre-mature breakdown and sustained less voltage per unit gate-drain spacing than those devices with longer $L_{gd}$. Discounting this, the breakdown voltage is approximately linear with $L_{gd}$, complying with previous analysis, and $V_{BR}$ saturates at $L_{gd}$ = ~ 17 μm. Additionally, $R_{on}$ shows accurate 2nd-order polynomial fit to Eq. (3.2): $R_{on} = \frac{L_{ds}^2}{q\mu_n n_s}$ $[\Omega \cdot cm^2]$ with the fitting equation of $R_{on} = 0.00348 \times (L_{gd} + 4.9)^2 + 0.03136$. The last part is from the ohmic contact and the contact resistance is extracted to be 0.3 Ω·mm. The $\mu \cdot n_s$ products is extracted to be $1796 \times 10^{13}$ [1/V·s], similar to the Hall data.

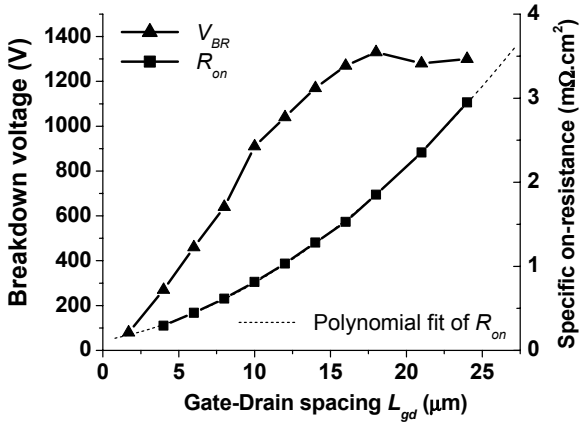



**Figure 3.28 $V_{BR}$ and $R_{on}$ dependency on gate-drain spacing.**

The variation of $R_{on}$ as a function of temperature was measured on a device with 14 μm gate-drain distance (Figure 3.29). The device exhibited a positive temperature coefficient with a temperature dependence of $T^n$ where *n* was fit to be 1.75. From Eq. (3.2), we can induce a mobility dependency on temperature of ~ $T^{-1.75}$, which is close to the phonon-scattering term of $T^{-3/2}$. A positive temperature coefficient is extremely desirable, since it allows paralleling of smaller cells into a large device and also improves reliability by avoiding current filamentation problems. This may be a crucial advantage for obtaining good yields on large devices as uniformity of GaN epitaxial growth is not quite as mature compared to silicon and GaAs.

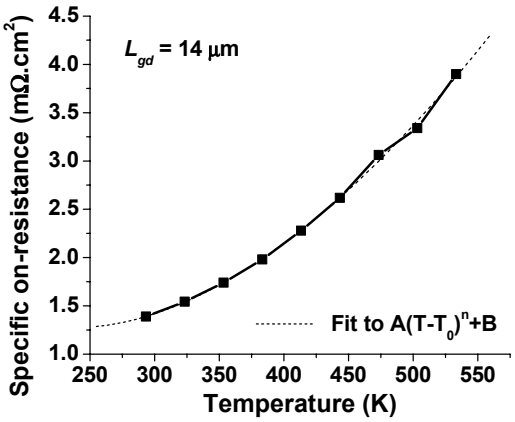



**Figure 3.29 Temperature dependent on-resistance.**

### *3.4.3 Problem with insulated gate GaN HEMTs: slow switching speed*

$I_{DS}$ - $V_{DS}$ curves measured under pulsed conditions were compared with DC measurement in Figure 3.30. The period of the gate bias pulse is 67 milli-second and the pulse width is 80 micro-second. The pulsed current level is much lower than the

DC measurement. The discrepancy between the DC and pulse measurements is referred to "dispersion" in microwave power electronics. Pulse measurement is an indirect way to probe the device switching speed. If the device is turned-on at a speed higher than the pulse, the current that can pass the switch will be limited by the pulsed current level (much lower than the DC current level). A longer pulse width is needed to fully recover the drain current. An 80 μs pulse width implies the switching speed of this device is slower than 6.25 KHz.

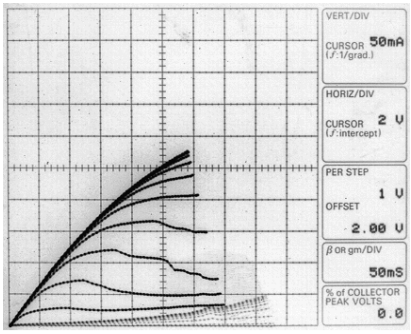



**Figure 3.30 $I_{ds}$-$V_{ds}$ curves measured under DC and pulsed conditions. The doted lines were measured under pulsed condition.**

Dispersion is caused by deep traps in the material, especially surface traps. Under reverse gate bias (turn-off), the electrons from gate are injected into the surface traps between gate and drain, and the channel is depleted by the trapped electrons. When the device switches to forward bias (turn-on), those trapped electrons should emit from the traps and let current pass through the channel. If the trap levels are deep, the emission process is considerably slow, resulting slow channel current recovery, or slow switching speed. As to be discussed in the next chapter, *C-V* measurement revealed that the $SiO_2$ film forms deep surface traps on

GaN (time constant can be as long as seconds). It is imperative to look for a device passivation scheme which mitigates dispersion while maintaining the high breakdown voltage. A double layer gate dielectric scheme to solve this problem will be discussed next chapter.

## 3.5 High voltage GaN HEMT simulation

The electric field illustrated in Figure 3.2 is only an ideal case where electric field in the *x*-direction is constant. But in an actual device, there is always electric field crowding for planar device. Figure 3.31 displays the simulated electric field in a GaN HEMT biased to breakdown when pinched-off. The field in the AlGaN layer is a combination of $E_x$ and $E_y$ which is the polarization field. Due to field crowding,

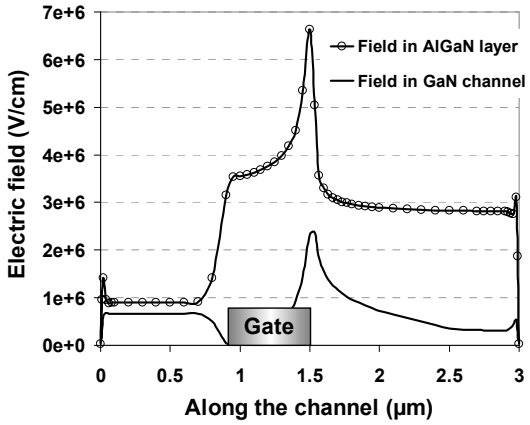



**Figure 3.31 Electric field in GaN HEMT biased to breakdown. The device is under pinch-off and $V_{ds}$ = 80 V.**

the peak at the gate edge is more than two times higher than in other region along the channel. To increase the breakdown voltage, this electric field peak has to be relieved. Field-plates proposed in the beginning of this chapter achieved this and

helped increase the breakdown voltage by 30 %. Here the effectiveness of the field-plate is investigated further by way of device simulation in ATLAS. Other device structures for high breakdown voltage will be discussed subsequently.

### *3.5.1 Field-plate GaN HEMTs*

As an example, Figure 3.32 compares the electric field distribution in field-plate GaN HEMTs with that in a conventional HEMT. The dielectric layer under the field-plate is SiN ($\varepsilon_r$ = 7.6). A second electric field generated at the edge of the field-plate is seen evidently in this figure. An optimum SiN thickness $t$ = 800 Å lowered the first field peak from 6.6 MV/cm to 4.3 MV/cm, given the field plate length $L_{fp}$ = 0.5 μm (refer to Figure 3.5 for detailed device structure). The second field peak is adjusted equal to the first one for the optimum $t$.

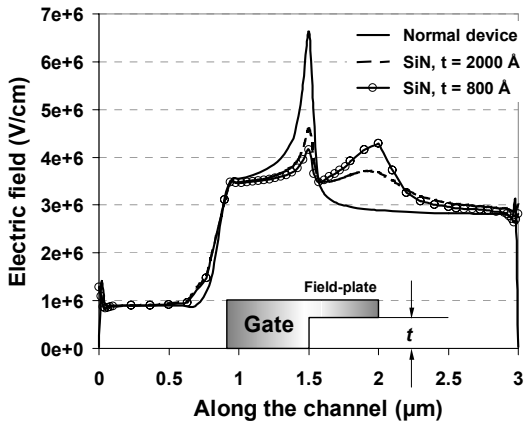



**Figure 3.32 Compare electric field for field-plate GaN HEMT and normal HEMT.**

The optimization process was continued by Dr. Shreepad Karmalkar [23]. Figure 3.33 shows that the breakdown voltage $V_{br}$ increases with field-plate length

$L_{fp}$ as the two field peaks are moving apart. After the two peaks are separated far enough to be electrically distinct, there is no significant gain in $V_{br}$ obtained for longer $L_{fp}$. The dielectric thickness under the field-plate, namely $t$, is then optimized for this minimum $L_{fp}$. Figure 3.34 exhibits that $V_{br}$ also increases with $t$. Beyond a critical value of $t$, the ionization current $I_s$ will rise sharply to invalidate the breakdown voltage (refer to section 2.3.3 for definitions of $V_{br}$ and $I_s$). The optimum $t$ for $1\times10^{13}$ $cm^{-2}$ channel charge density is found to be 0.8 μm.

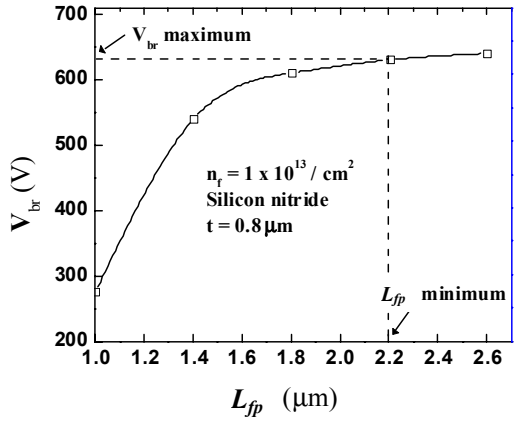



**Figure 3.33 Minimum field-plate length to achieve the maximum breakdown voltage.**

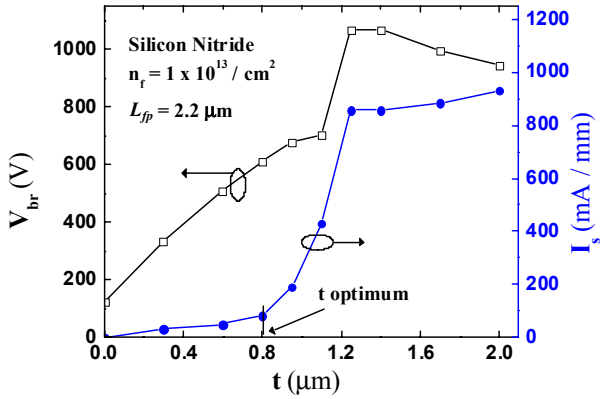



**Figure 3.34 Breakdown voltage as a function of dielectric thickness.**

Field-plate GaN HEMTs were optimized for various 2-DEG concentrations $n_f$ and the optimum geometry values are summarized in Figure 3.35. The minimum $L_{gd}$ required for the maximum $V_{br}$ represents a longest extension of the depletion region. All geometrical parameters shrink with higher channel concentration, which can be expected from shorter depletion length. Figure 3.36 shows the highest breakdown voltages achieved with above optimum geometry with comparison to devices without a field-plate. Furthermore, simulations reveal that field-plate HEMTs with $SiO_2$ as the insulator are less effective to improve the breakdown voltage, due to its lower dielectric constant ($\varepsilon_r = 3.9$) than that of SiN.

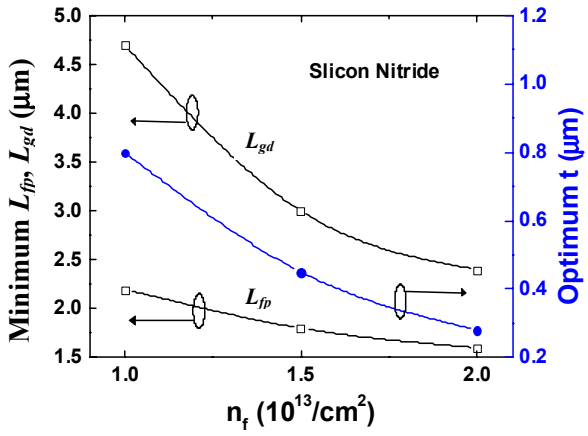



**Figure 3.35 Optimized field-plate GaN HEMT geometries for different channel charge densities.**

It is noticed that the simulated maximum $V_{br}$ is much less than that has been achieved experimentally. A plausible explanation is that the same impact ionization coefficients of GaN were used for AlGaN in the simulation, which may cause the AlGaN layer to breakdown at lower bias. In addition, the optimum SiN thickness varies from 0.5 to 0.8 μm for typical channel concentration of 1.0 to $1.4\times10^{13}$ cm$^{-2}$.

At the field-plate edge, the electric field in the SiN layer will exceed 10 MV/cm. It is currently difficult to obtain high dielectric strength on thick PECVD or sputtered SiN ($E_{max} \approx 6$ MV/cm). On the other hand, JVD SiN may sustain electric field as high as 10 MV/cm, but the maximum thickness achievable by JVD is only 0.1 μm for the time being. The future progress in high quality dielectrics will further increase the experimental value of $V_{BR}$ on GaN field-plate HEMTs.

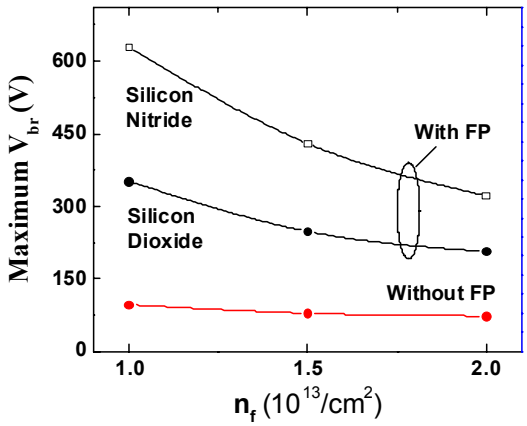



**Figure 3.36 Maximum $V_{br}$ obtained using the optimized geometrical parameters.**

### *3.5.2 Other device structures to improve breakdown voltage*

In the following discussion, only the electric field for different HEMT structures under the same bias voltage (80 V) are compared. A RESURF (REduced SURface Field) structure shown in Figure 3.37 is first considered. The RESURF structure uses p-type doping under the channel to vertically deplete the channel. Since the junction doping is uniform while the voltage across the junction varies along the channel, increasing toward the drain, the 2-DEG depletion solely due to

this junction is weaker near the gate and strong near the drain. The second peak appearing at the drain edge thus reduces the peak at the gate edge. To increase the breakdown voltage, the distance from the p-type doping to the channel, $t_{pc}$, was optimized to make these two peaks equal.

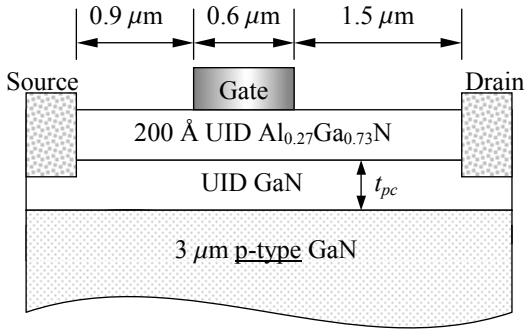



**Figure 3.37 Device structure of a RESURF GaN HEMT.**

As shown in Figure 3.38, with the optimum $t_{pc}$ of 1.23 $\mu$m, the electric field peak at the gate edge was reduce to 5 MV/cm from 6.6 MV/cm at the same drain bias. Simulation also indicates that the p-type doping level has little effect on the

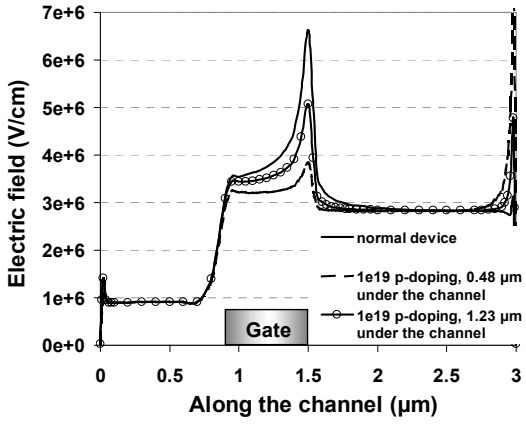



**Figure 3.38 Electric field in the AlGaN layer of a RESURF GaN HEMT.**

optimization process as long as it is higher than $1\times10^{18}$ $cm^{-3}$ and the channel charge reduction due to the p-type buffer is less than 4%. The large tolerance of p-doping level and small decrease of the channel concentration make the RESURF GaN HEMTs easy to be realized.

A p-type doped AlGaN surface layer with a recessed gate structure (Figure 3.39) can also be used to increase breakdown voltage. Like in a RESURF device, the depletion from the surface p-type doping generates a second peak field at the drain edge and compresses the peak at the gate edge. The recess edge also generates

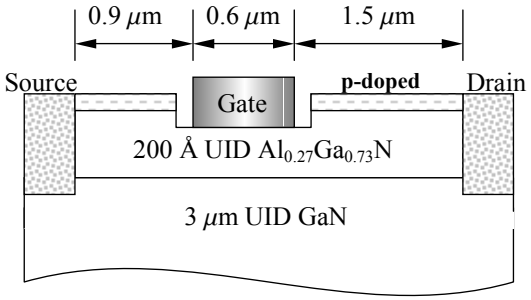



**Figure 3.39 Device structure of a recessed-gate GaN HEMT with p-doping cap.**

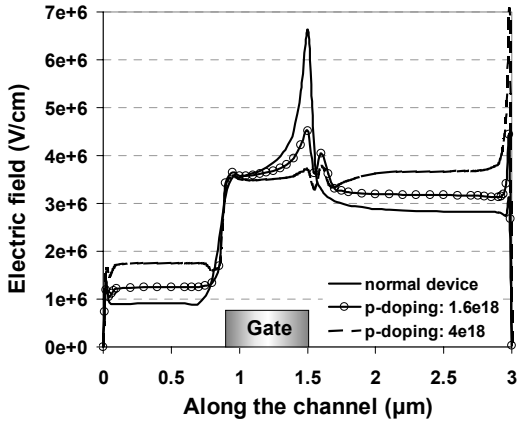



**Figure 3.40 Electric field in the AlGaN layer of a recessed-gate GaN HEMT with p-doping cap.**

another small peak close to the primary one, but this effect is smaller compared to the field plate. In this structure, the doping level of the p-type cap-layer was optimized to increase the breakdown voltage, since the thickness of the AlGaN cap layer is usually constrained to several hundred angstroms by the lattice mismatch strain. Figure 3.40 shows that the gate edge field peak dropped to 4.5 MV/cm by increasing the 100 Å thick p-doping level to $4\times10^{18}$ $cm^{-3}$.

## 3.6 Summary

Field-plate GaN HEMT was fabricated as the first attempt to operate at high drain bias. 570 V breakdown voltage, or 30 % improvement over previous efforts, was achieved, with a reasonable current level of 520 mA/mm and on-resistance of 1.5 $m\Omega\cdot cm^2$. Measurements on devices with different geometry revealed that, at large $L_{gd}$, the gate length $L_g$ does not affect the breakdown voltage, but the frequency response. This information was used in subsequent device designs to avoid unnecessary compromise of $R_{on}$ or switching speed. As an essential requirement for high voltage devices, insulating GaN buffer was successfully grown on SiC substrate combined with LP/AP growth technique, with the buffer leakage current reduced to 0.2 mA/mm. Even with such a low buffer leakage, the breakdown voltage seemed to saturate at 500 V. Further investigation into the device characteristics disclosed that the gate leakage current might be the major limit for high voltage operation. Insulated-gate HEMTs were then exploited to reduce the gate leakage 2 to 4 orders lower than normal Schottky gate HEMT with 100 Å JVD or E-beam deposited $SiO_2$

underneath the gate metal. 1300 V source-drain breakdown was realized on an insulated-gate GaN HEMT with a low $R_{on}$ of 1.65 m$\Omega \cdot cm^2$. The power device figure of merit of this device approached the theoretical limit for SiC devices. Nevertheless, the $V_{BR}$ is still much lower than theoretical analysis for GaN HEMTs due to field crowding at the gate edge. Device simulation in ATLAS pointed out that field-plate HEMTs should be able to further increase the breakdown voltage, but high dielectric constant, high quality (10 MV/cm field strength) and thick dielectric is a prerequisite.

## 3.7 References:


[1] B. J. Baliga, "Semiconductors for high-voltage, vertical channel FET's," *J. Appl. Phys.*, vol. **53**, pp. 1759-64, 1982.

[2] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Applied Physics Letters*, vol. **77**, pp. 250-2, 2000.

[3] I. P. Smorchkova, C. R. Elsass, J. P. Ibbetson, R. Vetury, B. Heying, P. Fini, E. Haus, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization-induced charge and electron mobility in AlGaN/GaN heterostructures grown by plasma-assisted molecular-beam epitaxy," *Journal of Applied Physics*, vol. **86**, pp. 4520-4526, 1999.

[4] I. P. Smorchkova, L. Chen, T. Mates, L. Shen, S. Heikman, B. Moran, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "AlN/GaN and (Al,Ga)N/AlN/GaN two-dimensional electron gas structures grown by plasma-assisted molecular-beam epitaxy," *Journal of Applied Physics*, vol. **90**, pp. 5196-201, 2001.

[5] S. Keller, G. Parish, P. T. Fini, S. Heikman, C.-H. Chen, N. Zhang, S. P. DenBaars, U. K. Mishra, and Y.-F. Wu, "Metalorganic chemical vapor deposition of high mobility AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. **86**, pp. 5850-57, 1999.

[6] O. Ambacher, "Growth and applications of group III-nitrides," *Journal of Physics D (Applied Physics)*, vol. 31, pp. 2653-2710, 1998.

[7] L. Shen, S. Heikman, B. Moran, R. Coffie, N.-Q. Zhang, D. Buttari, I. P. Smorchkova, S. Keller, S. P. DenBaars, and U. K. Mishra, "AlGaN/AlN/GaN high-power microwave HEMT," *IEEE Electron Device Letters*, vol. **22**, pp. 457-9, 2001.

[8] S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra, "Mass transport regrowth of GaN for ohmic contacts to AlGaN/GaN," *Applied Physics Letters*, vol. **78**, 2001.

[9] W. R. Frensley, "Power-limiting breakdown effects in GaAs MESFET's," *IEEE transactions on electron devices*, vol. 28, pp. 962-970, 1981.

[10] T. M. Barton and P. H. Ladbrooke, "The role of the device surface in the high voltage behaviour of the GaAs MESFET," *Solid-State Electronics*, vol. 29, pp. 807-813, 1986.

[11] C.-L. Chen, L. J. Mahoney, M. J. Manfra, F. W. Smith, D. H. Temme, and A. R. Calawa, "High-breakdown-voltage MESFET with a low-temperature-grown GaAs passivation layer and overlapping gate structure," *IEEE Electron Device Letters*, vol. 13, pp. 335-337, 1992.

[12] N. X. Nguyen, J. P. Ibbetson, W.-N. Jiang, and U. K. Mishra, "Low temperature grown AlGaAs passivation in GaAs power MESFET," presented at IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Ithaca, NY, USA, 1995.

[13] L.-W. Yin, N. X. Nguyen, K. Kiziloglu, J. P. Ibbetson, A. C. Gossard, and U. K. Mishra, "Device performance of submicrometre MESFETs with LTG passivation," *Electronics Letters*, vol. 29, pp. 1550-1551, 1993.

[14] C.-L. Chen, "Breakdown of overlapping-gate GaAs MESFET's," *IEEE Transactions on Electron Devices*, vol. 43, pp. 535-542, 1996.

[15] Y.-F. Wu, B. P. Keller, S. Keller, N. X. Nguyen, S. P. DenBaars, and U. K. Mishra, "Short channel AlGaN/GaN MODFET's with 50-GHz f/sub T and 1.7-W/mm output-power at 10 GHz," *IEEE Electron Device Letters*, vol. 18, pp. 438-440, 1997.

[16] S. Keller, Y.-F. Wu, G. Parish, N.-Q. Zhang, J. J. Xu, B. Keller, S. P. DenBaars, and U. K. Mishra, "Gallium nitride based high power heterojunction field effect transistors: process development and present status at UCSB," *IEEE Transactions on Electron Devices*, vol. **48**, pp. 552-9, 2001.

[17] Y.-F. Wu, "Ph.D. dissertation: AlGaN/GaN microwave power high-mobility-transistors," in *ECE Department*. Santa Barbara: Unversity of California, 1997, pp. 37.

[18] R. Gaska, Q. Chen, J. Yang, A. Osinsky, M. A. Khan, and M. S. Shur, "High-temperature performance of AlGaN/GaN HFET's on SiC substrate," *IEEE Electron Devices Letters*, vol. **18**, pp. 492-494, 1997.

[19] L.-W. Yin, Y. Hwang, J. H. Lee, R. M. Kolbas, R. J. Trew, and U. K. Mishra, "Improved breakdown voltage in GaAs MESFETs utilizing surface layers of GaAs grown at a low temperature by MBE," *IEEE Electron Device Letters*, vol. **11**, pp. 561-3, 1990.

[20] C.-L. Chen, F. W. Smith, B. J. Clifton, L. J. Mahoney, M. J. Manfra, and A. R. Calawa, "High-power-density GaAs MISFET's with a low-temperature-grown epitaxial layer as the insulator," *IEEE Electron Device Letters*, vol. **12**, pp. 306-8, 1991.

[21] M. A. Khan, X. Hu, G. Simin, A. Lunev, J. Yang, R. Gaska, and M. S. Shur, "AlGaN/GaN metal oxide semicondutor heterostructure field effect transistor," *IEEE Electron Device Letters*, vol. **21**, pp. 63-5, 2000.

[22] B. Gaffey, L. J. Guido, X. W. Wang, and T. P. Ma, "High-quality oxide/nitride/oxide gate insulator for GaN MIS structures," *IEEE Transactions on Electron Devices*, vol. **48**, pp. 458-464, 2000.

[23] S. Karmalkar and U. K. Mishra, "Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate," *IEEE Transactions on Electron Devices*, vol. **48**, pp. 1515-21, 2001.

# CHAPTER 4

# Surface passivation and improved switching speed

As discovered in the last chapter, $SiO_2$, as the gate insulator, suffered from slow on switching speed (large dispersion in *I-V* curves) for GaN HEMTs. It is imperative to search for an insulator with no dispersion while maintaining low gate leakage for high breakdown voltage. The first part of this chapter investigates the interface properties of GaN MIS capacitors formed with various dielectrics. Then in the second part, those dielectrics are applied to GaN HEMTs as passivation to minimize dispersion. Finally, combinations of those dielectrics are utilized in insulated-gate structure for both low dispersion and high breakdown voltage.

## 4.1 Interface properties of GaN MIS structures

The most important figures-of-merit for MIS interface are: 1. the density of interface traps, symbol $D_{IT}$ (in $eV^{-1}cm^{-2}$); 2. the density of fixed charges at the

interface, symbol $Q_F$ (in $cm^{-2}$); 3. the density of mobile ions in the insulator, symbol $N_{IONS}$ (in $cm^{-2}$); 4. insulator leakage current as a function of electric field and temperature, and 5. insulator breakdown field. It must be emphasized that measurement of these parameters in wide bandgap semiconductors is decidedly different from similar measurement in silicon. Before reviewing the MIS properties of the Insulator/GaN interface, we first consider the proper measurement techniques to characterize it.

### *4.1.1 Response times of interface states in wide bandgap semiconductors*

The response time of interface states increase exponentially with energy from the band edge. In a wide bandgap semiconductor such as GaN, the response time of deep interface states can be extremely long (years) at room temperature. The time constant for electron emission from an interface state to the majority carrier band in a n-type semiconductor can be written as,

$$\tau_n(E) = \frac{1}{\sigma_n v_T N_v} \exp(\frac{E_T}{kT}) \qquad (4.1)$$

where $\sigma_n$ is the capture cross section for holes, $v_T$ is the electron thermal velocity, $N_v$ is the effective density of states in the valence band, $E_T$ is the energy depth of the interface states. Using fundamental constant values of 2 x $10^7$ cm/sec for the mean thermal velocity of an electron in GaN, 8.4 x $10^{18}$ $cm^{-3}$ for the density of states in the conduction band, and an experimentally measured value for $\sigma_n = 2.4\times10^{-17}$ $cm^2$ by *ac*

conductance technique [1], we can estimate the response times as a function of energy and temperature in Figure 4.1.

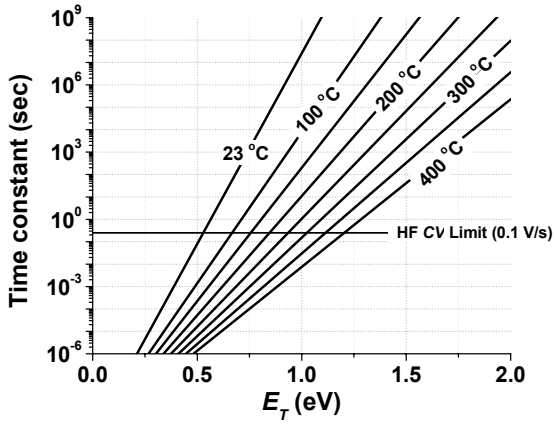



**Figure 4.1 Response times of interface states at the MOS/GaN interface.**

Commonly used techniques for measuring interface state density on MOS capacitors includes the Terman high frequency (HF) *C-V* technique, the hi-lo frequency *C-V* technique and the AC conductance technique. Instrumentation bandwidth places a limit on each of the characterization techniques and only a small part of the bandgap would be able to respond at room temperature. In a HF *C-V* measurement, if the voltage sweep rate on the MOS capacitor is 0.1 V/sec, the time for the interface states to emit is approximately 250 ms (10 sec/V times *kT*, to make sure the states are *kT* (eV) higher than the Fermi-level). From Figure 4.1, this emission time corresponds to an energy depth of about 0.5 eV. This technique is more useful at elevated temperatures where emission time constant is shorter. For example, at 400 $^{o}$C, HF *C-V* can measure states 1.2 eV below the conduction band. Unfortunately, as discussed below (and in the chapter 2 of simulation), the surface traps of GaN are highly centralized around the mid-bandgap (~ 1.65 eV below $E_c$).

This fact may not been fully recognized by all investigators, and could explain a number of underestimations of the actual interface state density in GaN MOS structures [1-3].

### *4.1.2 Photo C-V measurement on GaN MIS structures*

A quick method to estimate the total number of interface states across the bandgap is the room temperature photo *C-V* technique. Figure 4.2 illustrates a plot of this measurement, where an n-type GaN MIS capacitor is measured at 1 MHz. The bias is first swept from accumulation to deep depletion in dark. The sample does not go into inversion, since the thermal generation rate is too low to supply an inversion layer in a reasonable period of time at room temperature. In deep depletion, the capacitor is illuminated and the capacitance rises. The photo-generated minority carriers also populate the interface states. The bias is then swept back to accumulation. Initially the interface states retain their minority charge, but during the voltage sweep, when the majority carrier density becomes appreciable at the interface, the interface states begin to capture majority carriers, resulting in the characteristic "interface state ledge". Please refer to Figure 4.8 for the band diagram. The hysteresis in the *C-V* curve just below the onset of the ledge corresponds to the total density of interface states that are not able to respond to the *C-V* sweep, and is represented as $D_{IT}$:

$$D_{IT} = \frac{C_{ox} \cdot \Delta V_{IT}}{q} \qquad (4.2)$$

At room temperature $D_{IT}$ accounts for a majority of the interface states in GaN MIS capacitors, and thus is a qualitative representation of the total interface state density. The simulated *C-V* curves are also shown in Figure 4.2, and the Mathematica™ file for *C-V* simulation is listed in Appendix B. The shift from the simulation to the "*C-V* in dark" curve represents the fixed charge in the interface $Q_F$. From accumulation to mid-gap, the "*C-V* in UV light" starts to split from "*C-V* in dark". This is an indication of shallow traps (< 0.7 eV) with relatively lower density than the mid-gap traps.

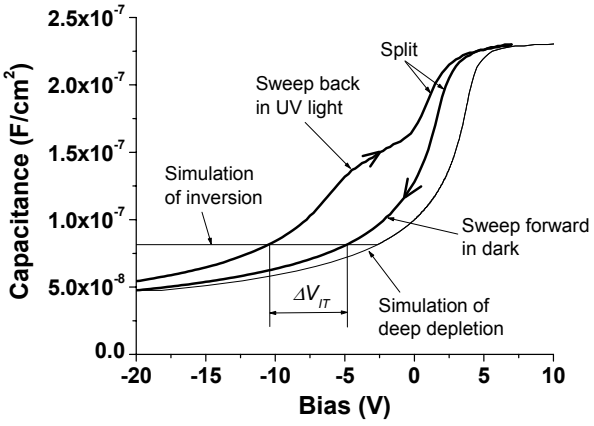



**Figure 4.2 Room temperature photo *C-V*.**

### *4.1.3 Interface properties of different dielectrics on GaN*

SiN and $SiO_2$ deposited on n-GaN by various deposition methods were investigated of the interface properties, as summarized in Table 4-1. The interface trap and fixed charge densities were functions of deposition conditions. The results reflect the lowest $D_{IT}$ achieved with each deposition method ($Q_F$ was not optimized). An MOCVD grown SiN film had relatively high interface charge and interface trap

densities, but the etch rate of it in buffered HF is the lowest. This rate is close to the ideal value of 7 Å/min, which is an indication of good quality of the film itself. PECVD deposited SiN presented the lowest interface trap density and moderate etch rate in BHF. The $SiO_2$ films deposited by both PECVD and E-Beam showed enormous interface trap densities, while the fixed interface charge densities are much lower than those of SiN films. Figure 4.2 is a typical photo-CV measurement on PECVD SiN, while that of $SiO_2$ films is shown in Figure 4.6. The high etch rate in BHF suggested poor quality of E-Beam deposited $SiO_2$ (ideal value is 1000 Å/min). Since PECVD SiN displayed the least interface trap density and it is easy to be deposited, it was chosen to investigate the effect of process on the interface properties.

**Table 4-1: Properties of dielectrics on n-type GaN.**

| | $Q_F$ ($cm^{-2}$) | $D_{IT}$ ($cm^{-2}$) | Etch rate in BHF |
|---|---|---|---|
| **MOCVD SiN** | $-2.6\times10^{12}$ | $7.9\times10^{12}$ | ~ 8 Å/min |
| **PECVD SiN** | $-4.1\times10^{12}$ | $5.8\times10^{12}$ | ~ 40 Å/min |
| **PECVD $SiO_2$** | $-5\times10^{11}$ | $> 1\times10^{13}$ * | > 1500 Å/min |
| **E-Beam $SiO_2$** | $6.4\times10^{11}$ | $> 1\times10^{13}$ * | > 2000 Å/min |
| **Sputtered SiN** | $-3.6\times10^{12}$ | high $10^{12}$ ** | 20 ~ 50 Å/min |

* The interface trap density of PECVD and E-Beam deposited $SiO_2$ exceeded the measurement limit of the *C-V* meter.

** The properties of sputtered SiN will be discussed in the next section.

### *4.1.4 Process to improve the interface quality of SiN/GaN MIS structure*

In silicon MOS technology, subsequent low temperature anneal after oxidation causes hydrogen to be released to the $SiO_2$/Si interface where hydrogen ties up dangling bonds at the interface [4]. Such a low temperature anneal routinely results in interface state densities in the low $10^{10}$ $cm^{-2}eV^{-1}$ range, reduced from $10^{11}$ $cm^{-2}eV^{-1}$. Hydrogen is introduced either by using a forming gas ambient or by the reduction of trace amount of $H_2O$ in the oxide by an aluminum gate. However, a low temperature (400 – 500 $^oC$) anneal either in nitrogen ambient or forming gas was found not to affect any property of SiC MOS capacitors [5]. Therefore our experiments started with a high temperature anneal of a GaN MIS structure in forming gas (4 % $H_2$ / 96 % $N_2$). The anneal time was set to be 3 minutes. Figure 4.3 shows the dependency of interface charge and trap densities after high temperature anneal. The anneal actually did not affect the interface charge, and the interface trap density was increased at some temperatures.

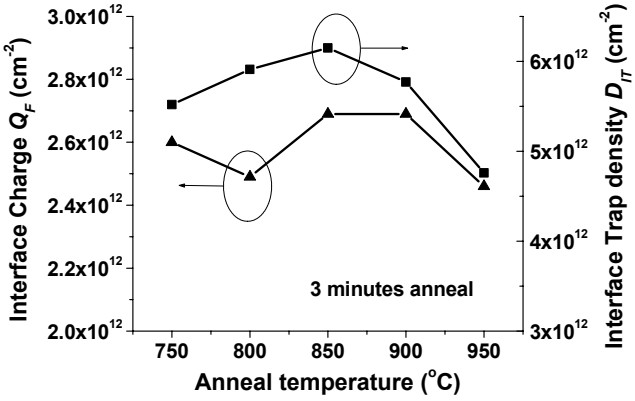



**Figure 4.3 High temperature anneal of GaN MIS capacitors in forming gas (3 min).**

During each of the anneals, a dummy Si wafer was included with the same PECVD SiN film on it. The optical index of the SiN film was monitored before and after the anneal. It was noticed that the index always increased from ~ 2.00 to ~ 2.15 after 3 minutes high temperature anneal. The etch rate of the SiN, however, decreased from ~ 40 Å/min to ~ 15 Å/min. The transparent SiN on GaN was also found to have changed to pale canary color after the anneal. These signs together indicate that the high temperature anneal changed the composition of the SiN film. It is supposed that nitrogen was driven out of the SiN film during the anneal, leaving a silicon-rich film. As displayed in Figure 4.3, there is a trend showing a decrease in the interface trap density at a temperature higher than 850 $^{o}$C. To preserve the quality of the SiN film, a series of shorter duration (30 seconds) high temperature anneals was conducted at temperatures higher than 900 $^{o}$C. These the results are shown in Figure 4.4. The effect is apparent: the interface trap density dropped from $5.2\times10^{12}$ cm$^{-2}$ to $3.3\times10^{12}$ cm$^{-2}$. However, the interface charge density increased to

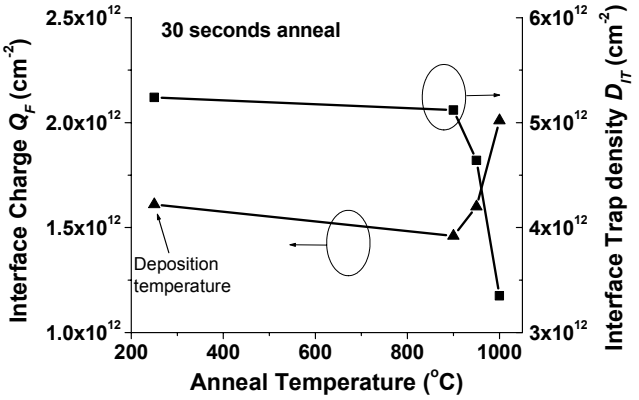



**Figure 4.4 High temperature anneal of GaN MIS capacitors in forming gas (30 sec).**

$2\times10^{12}$ $cm^{-2}$ from $1.5\times10^{12}$ $cm^{-2}$. Additionally, after this short time anneal the optical property of the SiN film did not change.

Even though a low temperature anneal seemed not to affect the interface of MOS capacitor on SiC, some research groups working on GaN MOS structure reported an improved interface after low temperature anneal. T. Sawada reported the shallow trap density lowered to one-third after 15 minutes 500 $^{o}$C anneal in $H_2$ [6]. Therefore the effect of a low temperature anneal on the deep level interface traps was examined. The sample was annealed at 450 $^{o}$C in forming gas for 5 minutes after the initial 30 second high temperature anneal. Photo-*CV* measurements showed a great reduction of interface charge from $4.7\times10^{12}$ $cm^{-2}$ to $6.8\times10^{11}$ $cm^{-2}$ and moderate reduction of interface traps from $4.4\times10^{12}$ $cm^{-2}$ to $3.4\times10^{12}$ $cm^{-2}$. The influence of surface clean was also investigated. After solvent clean, a sample was dipped in $HCl:H_2O$ = 1:8 solution for 30 seconds (then DI water rinse) before PECVD SiN deposition. The sample showed the lowest interface trap and charge densities of

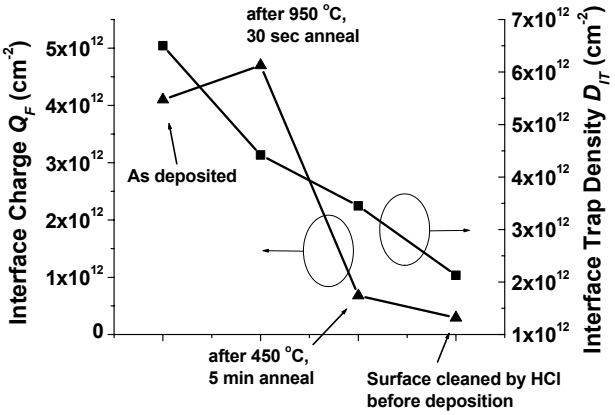



**Figure 4.5 Interface properties after anneal and surface clean.**

$2.13\times10^{12}$ $cm^{-2}$ and $2.93\times10^{11}$ $cm^{-2}$ respectively after the low temperature anneal, as shown in Figure 4.5. This result is in accordance with previous observation reported by Nakasaki [7].

### *4.1.5 Photo-CV measurement on JVD SiN/GaN MIS structure*

A photo-*CV* measurement was also made on JVD $SiO_2$/GaN MOS capacitors at Yale University and is shown in Figure 4.6 along with *C-V* simulations by the author. After a –2.5 V shift ($1.8\times10^{12}$ $cm^{-2}$ interface charge accordingly), the simulated curve of deep depletion fits well with the *C-V* measurement in dark. The UV light was turned on when the MOS capacitor was biased at deep depletion (–18 V), which caused the capacitance to jump abruptly to a level much higher than the simulated inversion capacitance. This photo-*CV* behavior is almost identical to what

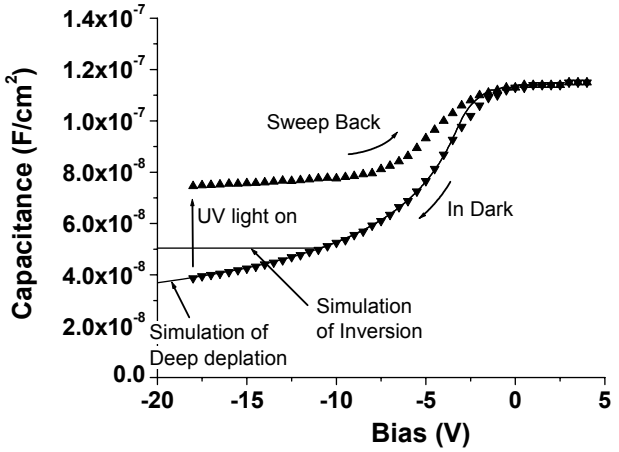



**Figure 4.6 Photo-*CV* measurement on JVD $SiO_2$.**

was observed on E-beam and PECVD $SiO_2$/n-GaN MOS structures fabricated in our group. Gaffy (Yale Univ., [1]) suggested that this abrupt rise of the capacitance

signified inversion of the MOS capacitor. Its interface trap density is as low as 5 x $10^{10}$ $cm^{-2}eV^{-1}$, based on the explanation given by the band diagrams in Figure 4.7.

According to Gaffy, when the UV light is shone on the MOS capacitor, electron-hole pairs are generated and cause the quasi fermi-levels of electrons and holes to separate. The holes accumulate at the $SiO_2$/GaN interface and form the inversion layer. The band bending at inversion is $\psi_S = 2\psi_B - (E_{fn} - E_{fp})$, where $\psi_B$ is the potential difference between the intrinsic fermi-level and the fermi-level in dark, and $E_{fn}$, $E_{fp}$ are quasi fermi-levels. This band bending in this case is smaller than without quasi-fermi level separation, so it results in larger inversion capacitance than simulation as shown in Figure 4.7. The inversion layer is maintained even after the UV light is turned off because the minority-carrier recombination rate is low due to the wide bandgap of GaN. The low recombination rate prevents the system from reaching quasi-equilibrium and thus makes it difficult for the inversion charge to follow the finite voltage sweep.

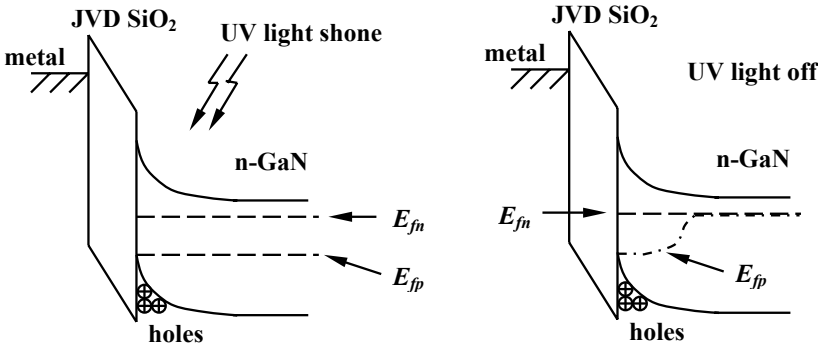



**Figure 4.7 Band diagrams of JVD $SiO_2$/GaN MOS capacitor with and after UV light shone, proposed by Gaffy [1]. In this case, there is no interface trap.**

However, there is another possibility of MOS structure with the same photo-*C-V* behavior. There may be a high density (> $10^{13}$ $cm^{-2}$) of single level of interface traps in the middle of the bandgap. Under UV illumination, holes are photo-generated and recombine with the electrons in the traps. If the trap density is high, the fermi level will be kept from moving below the trap level. The band bending in this case is smaller than that with inversion, leading to a higher capacitance than the simulated inversion capacitance as shown in Figure 4.8. From simple calculation, the *CV* curve (after UV illumination) in Figure 4.6 reveals a band bending of 1.55 V in the GaN. Assuming the $E_c$ and $E_f$ difference is zero for n-GaN, the interface traps are 1.55 V below the conduction band. An effective method to distinguish these two possible cases is to fabricate a p-MOSFET from the MOS capacitor and to inspect if there is hole current during negative gate bias. From our experience with HEMT passivation by $SiO_2$ discussed later, an inversion of the $SiO_2$/GaN MOS is unlikely to exist.

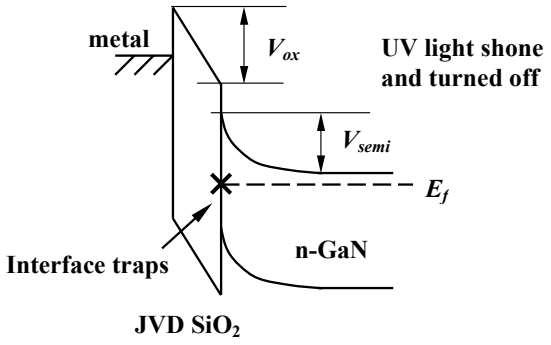



**Figure 4.8 An alternative explanation of the photo-*CV* behavior of JVD $SiO_2$/GaN MOS structure shown in Figure 4.6. In this case, the interface trap density is very high.**

In a short summary, GaN MIS structures with dielectrics deposited by various methods were investigated using photo-*CV* measurement. SiN was found to form much lower interface trap density on n-GaN than $SiO_2$, regardless of deposition methods. Pre-deposition surface clean and low temperature post-deposition anneal improved the interface quality and will be adopted into GaN HEMT passivation process in the following section. Because of the wide bandgap of GaN, it is not easy to probe into properties of the mid-gap interface traps. Advanced device structures need to be employed to assist in understanding GaN MIS capacitors.

## 4.2 Surface passivation on microwave GaN HEMTs

As a candidate for future power devices in microwave and millimeter frequencies, GaN HEMT has been consistently improving its performance in output power, efficiency, and operating frequency. One of the prominent limitations on GaN HEMT performance is frequency "*dispersion*" shown in Figure 4.9, where *I-V* curves were measured under pulsed condition to simulate AC operation and compared with DC *I-V* curves. The difference between the AC and DC *I-V* curves is called *dispersion*. Dispersion reduces device output power and PAE due to the reduction in current and increase in knee voltage under large signal conditions. Research efforts [8, 9] have attributed the dispersion to the presence of slow-acting surface traps between the gate and drain. Even though it is not clear if the surface traps are intrinsic (e.g. due to dangling bonds) or impurity-related, these traps are deep and their time constants are expected to be very long. When the device is in

off-state, these traps become negatively charged by the injection of electrons from the gate and thus deplete the channel. When the gate bias is turned to positive by a short pulse or during RF operation, the slow response of the deep surface traps freezes the channel modulation, causing DC-RF dispersion. Surface passivation was investigated using dielectrics studied in the preceding section to improve this condition. Sputtered SiN was found to be able to successfully eliminate dispersion in GaN HEMTs despite the fact that its MIS capacitor on GaN showed existence of interface traps.

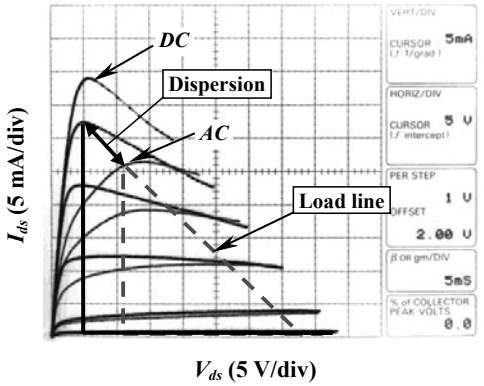



**Figure 4.9 Dispersion between pulsed and DC *I-V* curves in an un-passivated GaN HEMT.**

### *4.2.1 Surface passivation by sputtered SiN*

The epi-structure under study was grown by Stacia Keller (sample # 981218FA) on sapphire by MOCVD. It consisted of a 3 $\mu$m semi-insulating GaN buffer and a 220 Å $Al_{0.33}Ga_{0.67}N$ layer which included a 30 Å unintentionally doped ($n \sim 5\times10^{16}$ $cm^{-3}$) spacer, a 100 Å Si doped region ($n \sim 5\times10^{18}$ $cm^{-3}$) and a 90 Å cap layer. The sheet electron concentration and Hall mobility of the as-grown

modulation doped structure were ~ $1.21\times10^{13}$ $cm^{-2}$ and ~ 1150 $cm^2/V\cdot s$ at room temperature. The device was processed using standard GaN HEMT process, and 100 nm sputtered SiN was deposited afterwards only on the channel region of some selected devices. Before sputtering, the sample was cleaned by solvent and dipped in $HCl:H_2O$ = 1:8 solution for 30 seconds. The ohmic contact resistance was measured to be around 0.8 Ω·mm. The gate length and the gate-drain separation were 0.7 $\mu$m and 1.5 $\mu$m respectively, and the gate width was 2×50 $\mu$m.

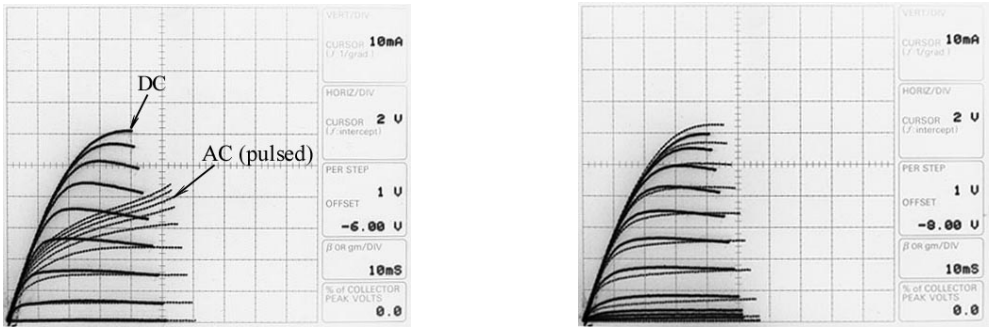



**Figure 4.10 Dispersion characteristics without and with 100 nm sputtered SiN passivation. $W_g$ = 50 μm.**

*I-V* curves of two immediately adjacent devices without and with the sputtered SiN are shown on Figure 4.10. The thin lines represent measurement under pulsed conditions with pulse width of 80 microseconds. The device without passivation displayed approximately 50 % dispersion, while the device with SiN passivation showed even higher pulsed *I-V* currents than DC currents, which were partly due to lower temperature rise compared to under DC conditions. The maximum current density of the passivated device was 1.2 A/mm and the maximum extrinsic trans-conductance $g_m$ was 190 mS/mm. The forward turn-on voltage of the

gate-drain diode was 2 V and the pinch-off voltage is −6 V which was slightly higher than that of un-passivated device of −5.5 V. The reverse breakdown voltage was higher than 70 V, and there was no clear evidence that the breakdown voltage of GaN HEMTs was either increased or decreased by SiN passivation. Small signal microwave characterization performed on 100 $\mu$m gate-width device obtained current-gain and power-gain cutoff frequency ($f_t$ and $f_{max}$) of 19 and 18 GHz respectively as shown in Figure 4.11 at a drain bias of 12 V with $I_{ds}$ = 350 mA/mm. The $f_t$ is comparable to normal un-passivated device, while the $f_{max}$ is much lower, likely because the $C_{gd}$ was increased by presence of SiN with $\varepsilon_{SiN} > \varepsilon_{Air}$. Another reason could be reduced gate extension with the SiN passivation which was discounted because this should have led to a higher $f_t$.

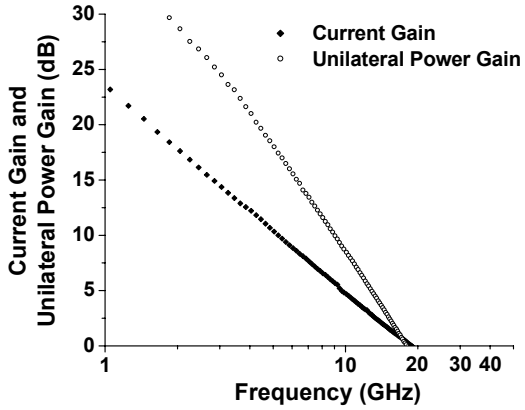



**Figure 4.11 Small signal frequency response of passivated GaN HEMT on Sapphire.**

An active load-pull system was used for continuous-wave (CW) power measurements at 6 GHz. Figure 4.12 shows the measurement result of the passivated device with a gate width of 100 $\mu$m. The device was biased in class-AB mode with a

quiescent drain current of 203 mA/mm and a source-drain bias of 27 V. At the peak output power, the drain current was self-adjusted to 455 mA/mm with the input drive. The peak output power was 28.2 dBm which was normalized to a power density of 6.6 W/mm. The corresponding large signal gain and power added efficiency are 9.2 dB and 47.2% respectively. Such CW power density (measured uncooled on sapphire substrate) was significantly higher than the best result previously reported (4.6 W/mm [10]), and it still defines the state-of-art of output power of GaN HEMTs on sapphire. This result was largely limited by the low thermal conductivity of sapphire and may be further improved by flip-chip bonding schemes [11].

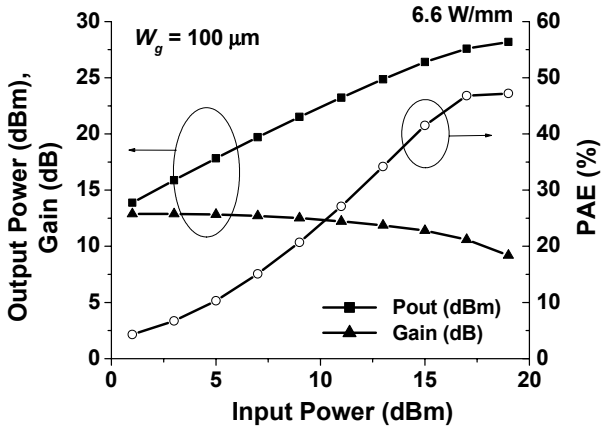



**Figure 4.12 Power measurement on passivated GaN HEMT on Sapphire at 6 GHz.**

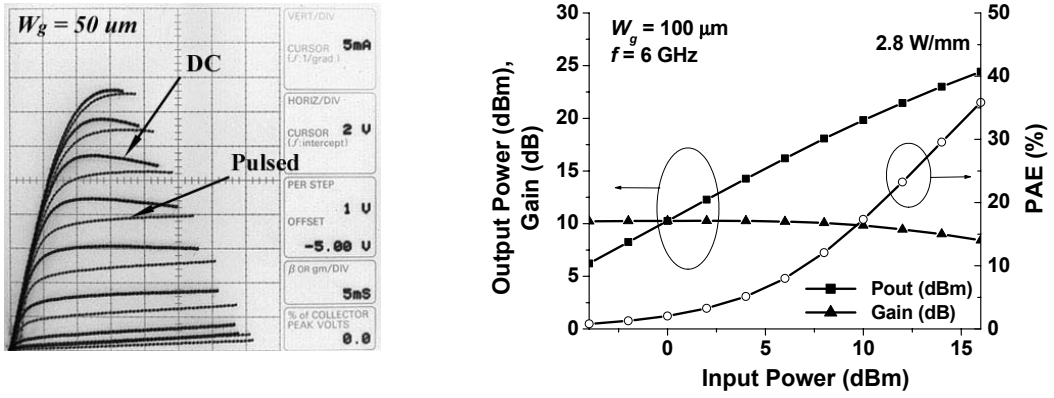
This device also showed decent linearity with $P_{1dB}$ of 3.1 W/mm. Even though the device was tuned for the highest output power, its power added efficiency at the maximum $P_{out}$ reached 47.2 %. Only 3.3 W/mm output power was obtained from the un-passivated control device at $V_{ds}$ = 25 V, with very large gain

compression (8 dB). The passivated device could be biased at higher drain voltage of 27 V because of its PAE was higher than that of the un-passivated device of 32 %. Higher PAE means lower power dissipated on the device and lower temperature rise, and thus the ability to withstand higher bias.

A simple estimate of the maximum saturated output power based on the *I-V* characteristics of the device is given by $P_{out} = \Delta I \cdot \Delta V/8$, where $\Delta V = 2(V_D - V_{knee})$ and $\Delta I = I_{D,max}$ [mA/mm]. The calculated $P_{out}$ should be approximately 6.3 W/mm at $V_D$ = 27 V. Since the device was biased at class-AB at 0.4 $I_{D,max}$, the $P_{out}$ is slightly higher than this value. The close power measurement result of 6.6 W/mm indicates that there is nearly no dispersion between the DC characteristics and RF output power for passivated GaN HEMTs.

Assuming passivation removes trapping effect from the surface, the passivated device will mainly exhibit deterioration effect from bulk traps. In an attempt to investigate if the surface traps are the major source of dispersion for GaN HEMTs, another passivation experiment was conducted on a sample with thin GaN buffer layer (sample # 981221FC). The material structure was identical to the previous one except that the thickness of the GaN buffer was only 0.3 μm. Since this thin buffer layer is right above the nucleation layer, it is generally considered to possess high density of dislocations as a main source of bulk traps. Therefore, this experiment was designed to extract the maximum dispersion effect from bulk traps. The Hall mobility was only 810 $cm^2/V \cdot s$ ($n_s = 1.13 \times 10^{13}$ $cm^{-2}$), a direct result from the high dislocation density.

Figure 4.13 (a) shows the dispersion measured on a passivated GaN HEMT on 0.3 μm buffer. The $I_{D,max}$ is only 0.76 A/mm presumably due to the low mobility. The pulsed current was 4 mA lower than the DC current at low current level, which denoted a dispersion of 10 %. Because of the poor thermal conductivity of Sapphire under the thin buffer, the current compression, or negative output conductance, due to temperature rise is evident for DC *I-V* curves for this device. Consequently, the pulsed current was close to DC current at high current level. The $P_{out}$ was measured to be 2.8 W/mm at $V_D$ = 24 V, while it is calculated to be 3.6 W/mm from the *I-V* curves. Figure 4.13 (b) shows that the output power has not saturated before the device was burnt at high temperature. The $P_{out}$ might be improved if heat could be extracted effectively from the device. Measurement on an un-passivated device yielded a highest output power density of 1.4 W/mm. Hence, the power improvement as a result of surface passivation was 2.8 – 1.4 = 1.4 W/mm, while the




**(a) *I-V* characteristics.** **(b) Microwave power performance.**

**Figure 4.13 Passivation of GaN HEMT with 0.3 μm buffer layer.**

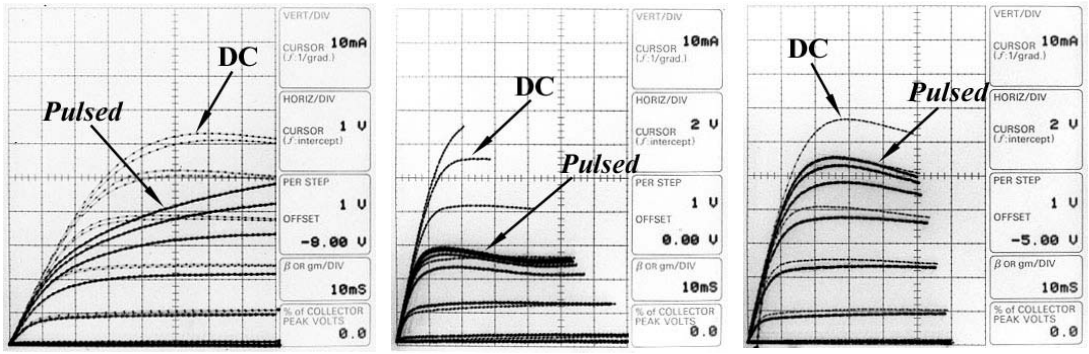
degradation of power due to bulk traps was less than 3.6 – 2.8 = 0.8 W/mm. In conjunction with the *I-V* curves, this phenomenon is a sign that though a high density of bulk traps contributes to dispersion, surface traps are the major cause of DC-RF dispersion of GaN HEMTs.

### *4.2.2 Surface passivation by JVD deposited SiN*

Other types of dielectrics deposited in UCSB were also applied to passivate GaN HEMTs, including PECVD SiN and $SiO_2$, E-beam $SiO_2$ and sputtered AlN. However, each resulted in worse dispersion and lower $P_{out}$ than before dielectric deposition. It is not difficult to accept that $SiO_2$ is not suitable for GaN HEMT passivation, since last section has shown a high density deep interface traps between $SiO_2$ and GaN. It is difficult to explain why PECVD SiN did not work as a passivation process. This is probably more related to the investigated deposition conditions rather than an inherent problem. In fact, research in other groups has shown that PECVD of SiN is effective as a passivant [12].

In order to explore other passivation possibilities, JVD $SiO_2$ and SiN were deposited on sample # 001116FC and # 001117FA, respectively, at Yale University. The cleaning process before deposition was the same as described earlier. The thickness of $SiO_2$ was 600 Å and SiN 200 Å. Figure 4.14 shows the comparison of dispersion before and after JVD SiN passivation. Before passivation, the device displayed 30 % dispersion and very large knee voltage. The maximum output power was 1.4 W/mm at 6 GHz. After deposition of JVD SiN, the device showed even

more $I_{D,max}$ compression for pulsed measurement, and no output power could be measured from it. As instructed by Yale Univ., the sample was annealed in $N_2$ ambient at 350 $^{o}$C for 5 minutes afterwards. Considerable improvement of pulsed *I-V* curves was observed with increased RF output power of 2.4 W/mm. More improvement is expected with thicker SiN passivation (> 500 Å).




**(a) Before JVD SiN.** **(b) After JVD SiN.** **(c) After 350 $^{o}$C, 5 min anneal.**

**Figure 4.14 Passivation of GaN HEMTs with JVD deposited SiN.**

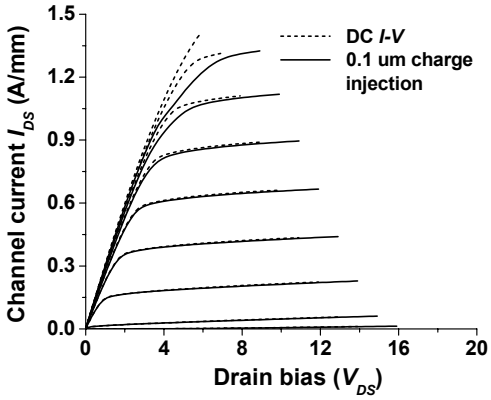
An optimum anneal temperature of 600 $^{o}$C was originally suggested by Yale Univ. for the best film quality, but it was lowered by us to preserve the gate metal schottky contact. More work needs to be done to optimize the anneal temperature and duration for passivation. Also, the reason for the improvement of passivation after annealing needs investigation.

### *4.2.3 Electron injection length and dispersion*

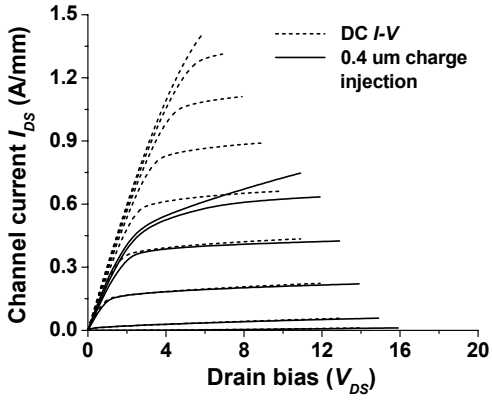
Surface traps and electrons injected into those traps are generally considered to be the major causes of dispersion in GaN HEMTs [8, 9]. Here, we first investigate

the dependency of dispersion on electron injection length. The distance from the gate to the drain, in which the surface traps will be filled with the electrons injected from the gate during channel pinch-off, is defined as the injection length ($L_{inj}$). The injection length determines how severe the dispersion could be. As in GaAs devices, surface states effects can be minimized through heavy doping of the top layer and using a recessed-gate structure to maintain breakdown voltage. An important parameter for recessed-gate structures is the gate-to-recess spacing. If the gate-to-recess spacing is made larger than the injection length of electrons from gate to drain, then recessing will have little improvement on the dispersion.

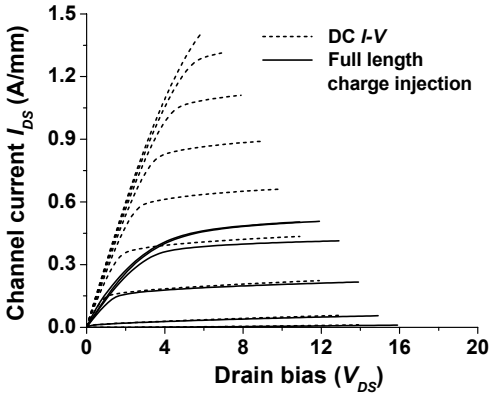
Using the GaN HEMT model described in chapter 2, an inspection of the injection length on the knee voltage and maximum current has been performed using the device simulator ATLAS. Injection lengths of 0.1 μm, 0.4 μm and 1.5 μm have been simulated by filling the surface traps with electrons at the indicated lengths from gate edge towards the drain. Infinite surface trap density is used from the fitting result in chapter 2. Figure 4.15 shows the simulated *I-V* curves for the indicated injection lengths. At an injection length of 0.1 $\mu$m, there is less than 5% loss of $I_{max}$, while with an injection length of 0.4 $\mu$m, $I_{max}$ is reduced by 60%. When all gate-to-drain surface ($L_{inj}$ = 1.5$\mu$m) traps are filled with injected electrons, the reduction of $I_{max}$ is 70%. Therefore, the majority of the dispersion occurs when surface traps located in the first several tenths of micron next to the gate are filled with electrons.




**(a) Charge injection length = 0.1 μm.**




**(b) Charge injection length = 0.4 μm.**

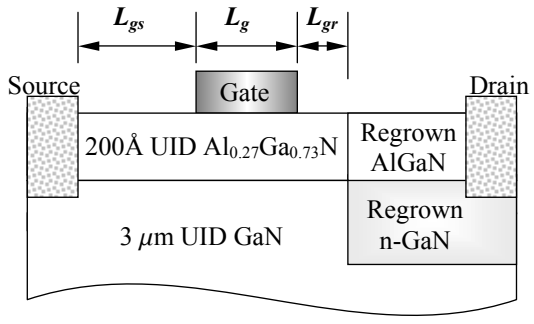



**(b) Charge injection length = Full channel length.**

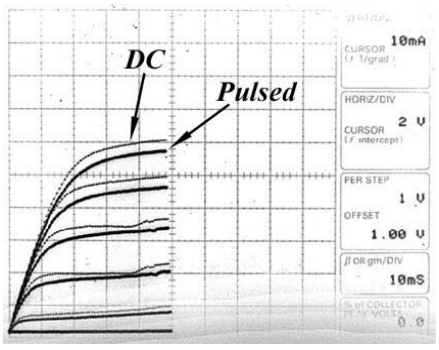
**Figure 4.15 Simulated dispersion of $I_{DS} - V_{DS}$ curves dependent on the surface charge injection lengths.**

This trend of dispersion with injection length has been experimentally verified by Robert Coffie using regrown-drain HEMTs. The device cross-section for a regrown-drain HEMT is shown in Figure 4.16 (a). Part of the material between gate and drain was etched vertically 4000 Å. 3800 Å of n-GaN doped at $5 \times 10^{17}$ cm$^{-3}$ was then regrown in the etched trenches followed by a 200 Å UID AlGaN cap. Keeping other device dimensions constant, the gate-regrowth spacing ($L_{gr}$) was

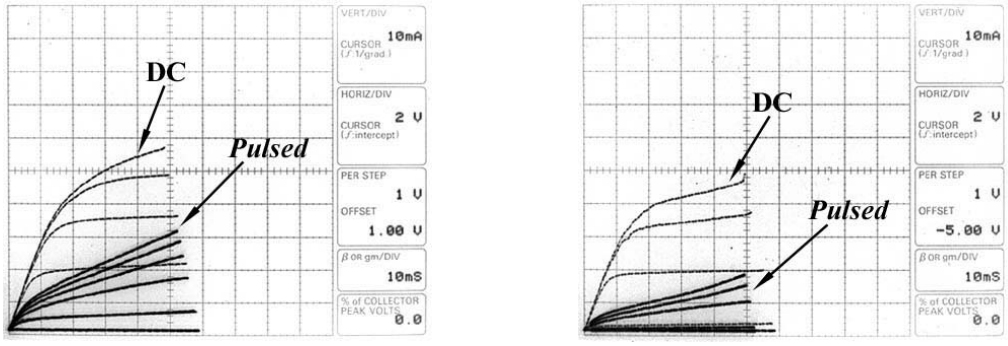
varied from 0 $\mu$m to 2.0 $\mu$m (entire gate to drain spacing). The channel region with regrown material contains a charge density much larger than the surface trap density. Therefore, charging of surface states in the regrown region no longer limits the channel current and the injection length can be assumed to equal the gate-regrowth spacing ($L_{gr} = L_{inj}$). Figure 4.16 (b) – (d) show the dispersion between static *I-V* curves and 80 μsec pulsed *I-V* curves for gate-regrowth spacings of 0.12 μm, 0.38 μm (as measured by SEM), and no regrowth between gate and drain ($L_{gr}$ = 2.0 $\mu$m). At a gate-regrowth spacing of 0.12 $\mu$m, 95% of the current is preserved for the pulsed I-V curves, but at 0.38 μm, 60 % of the current is lost, which is very close to the case of no regrown region between gate and drain. This is in very good agreement with previous simulations. The regrown drain HEMT also experimentally verifies that it is the surface traps next to the drain side of the gate that are the cause for dispersion. Therefore, a recessed gate GaN HEMT should have a gate-to-recess spacing well below 0.4 μm on the drain side to minimize dispersion.




**(a) Device structure.**




**(b) $L_{gr}$ = 0.12 μm.**

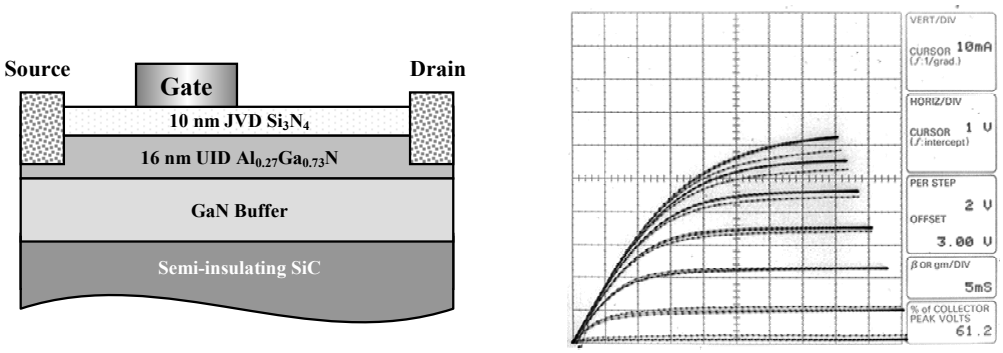



**(c) $L_{gr}$ = 0.38 μm.** **(d) $L_{gr}$ = Full channel length.**

**Figure 4.16 Experimental dispersion of $I_{DS} - V_{DS}$ curves dependent on the surface charge injection length $L_{gr}$.**

## 4.3 Double-layer gate dielectrics for high speed switching

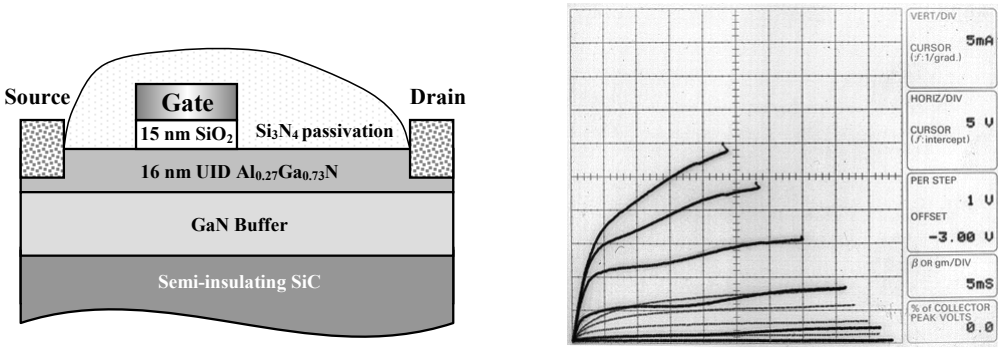
Since SiN passivation was known to eliminate the current dispersion of microwave GaN HEMTs, it was also applied to insulated-gate HEMTs to reduce dispersion for improved switching speed. First, JVD SiN was used as the gate dielectric as shown in Figure 4.17 (a). 100 Å SiN was deposited right after the material growth and before device fabrication (sample # N001001A). The dielectric was then dry-etched using $SF_6$ gas to open the window for ohmic contact metal. After device processing, the HEMTs were annealed in $N_2$ at 350 $^oC$ for 5 min. The devices with JVD SiN gate dielectric showed negligible dispersion (Figure 4.17 (b)), implying a high switching speed. However, the breakdown voltage of these devices was only about 500 V. Gate diode measurement showed large leakage current compared to normal GaN HEMTs without gate dielectric as shown in Figure 4.21. The breakdown voltage is believed to be limited by leakage enhanced impact ionization.




**(a) Device structure # 1.** **(b) *I-V* curves.**

**Figure 4.17 Insulated-gate GaN HEMT structure # 1 with dispersion measurement.**

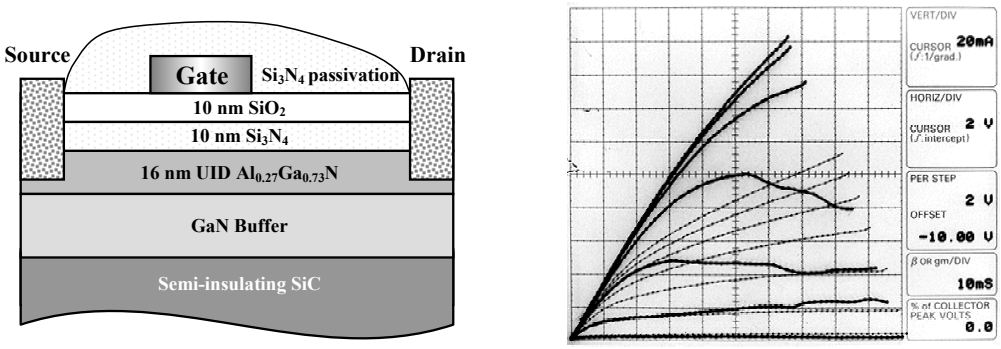
In order to maintain low gate leakage, E-beam $SiO_2$ was placed under the gate as described in the last chapter (sample # N010512B2). After processing, the device was passivated by thick 1000 Å sputtered SiN to remove dispersion as shown in Figure 4.18 (a). The gate leakage decreased by 4 orders lower than a normal HEMT (Figure 4.21), but significant dispersion (75 %) was still observed in the pulsed measurement (Figure 4.18 (b)). This implies that the deep traps beneath the $SiO_2$ under the gate still cause dispersion. No change of the *I-V* curves was observed after low temperature anneal. The $V_{BR}$ of this device was only 500 V which was attributed to the leaky GaN buffer.




**(a) Device structure # 2.** **(b) *I-V* curves.**

**Figure 4.18 Insulated-gate GaN HEMT structure # 2 with dispersion measurement.**

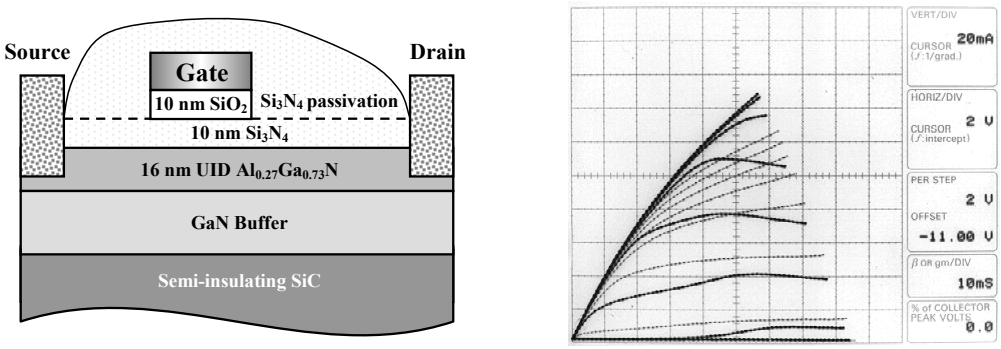
The third insulated-gate structure is the $SiO_2$/SiN double layer shown in Figure 4.19 (a). The rationale is that the good interfacial properties of the bottom SiN layer with the AlGaN surface yields low dispersion, while the top $SiO_2$ layer helps reduce the gate leakage. The 100 Å sputtered SiN and 100 Å E-beam $SiO_2$ were deposited respectively after the ohmic contact anneal, so there was no need for the dry etch step. 1000 Å sputtered SiN was added on top after device processing for better AC response (sample # N010512B3). The dispersion from this structure was improved considerably but still large (44 %, Figure 4.19 (b)). It was suspected that the top $SiO_2$ layer limited the communication of the electrons between the gate and the traps at the SiN/AlGaN interface even at the 80 $\mu$s time constant of the measurement. The gate leakage of this structure was between structure # 1 and # 2, and the $V_{BR}$ was 500 V, still limited by the buffer leakage.




**(a) Device structure # 3.** **(b) *I-V* curves.**

**Figure 4.19 Insulated-gate GaN HEMT structure # 3 with dispersion measurement.**

To minimize the impact of the $SiO_2$ layer in the access region, the double-layer gate dielectric scheme was modified into Figure 4.20 (a). A thin layer of sputtered SiN was first applied all over the device after ohmic contact anneal, then the second $SiO_2$ layer was only deposited under the gate as in structure # 2, and the device process was completed with thick, planar SiN passivation (sample # N010512B4). The dispersion from this device was the least (10 %, Figure 4.20 (b)) among all insulated-gate structures. The greatly reduced gate leakage was nearly 4 orders lower than that of a normal GaN HEMT and was comparable to the best insulated-gate structure # 2 as shown in Figure 4.21. As a result, the breakdown voltage of this device exceeded 1000 V as exhibited in Figure 4.22. No hysteresis is displayed in these high bias *I-V* curves as compared to the high breakdown device obtained in the last chapter in Figure 3.26 (a). This well-behaved characteristic is another indication of low dispersion and high switching speed.




**(a) Device structure # 4.** **(b) *I-V* curves.**

**Figure 4.20 Insulated-gate GaN HEMT structure # 4 with dispersion measurement.**

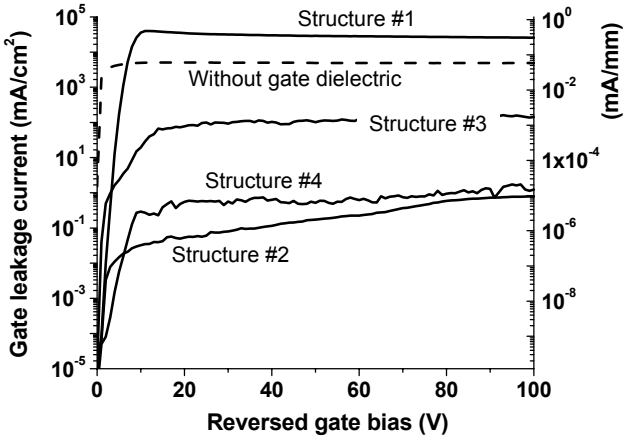



**Figure 4.21 Compare the gate leakage currents of four different insulated-gate GaN HEMT structures to that of a normal Schottky-gate device.**

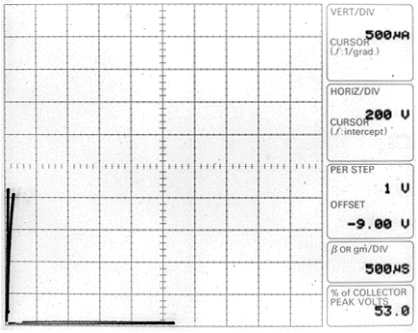



**Figure 4.22 Breakdown characteristics measured from insulated-gate GaN HEMT structure # 4.**

## 4.4 Summary

In the search for a gate-dielectric with low dispersion for high switching speed and with low gate leakage for high breakdown voltage, the interfaces of GaN MIS structures with different types of dielectrics were examined by photo-*CV* measurements. SiN deposited by various methods produced lower interface trap density (~ $5\times10^{12}$ $cm^{-2}$) than $SiO_2$ on n-GaN (> $1\times10^{13}$ $cm^{-2}$). Pre-deposition clean and post-deposition anneal were found to further reduce the interface trap and charge densities to $2.1\times10^{12}$ $cm^{-2}$ and $2.9\times10^{11}$ $cm^{-2}$ respectively. When these dielectrics were applied to GaN HEMTs for passivation, only sputtered SiN could eliminate the dispersion from the devices. The power density of GaN HEMTs on Sapphire was increased from 3.3 W/mm to 6.6 W/mm by passivation. Further study found that JVD could also passivate GaN HEMTs after a low-temperature post-deposition anneal. The mechanism of SiN passivation is still unclear. One possibility is that the SiN layer provides a path for electrons to communicate with the surface traps at high frequency in a region close to the gate. Consequently, SiN was used as the gate-dielectric and achieved low dispersion on high voltage GaN HEMTs, but the gate leakage is even higher than without gate-dielectric. Low gate leakage and low dispersion were achieved simultaneously on devices with double gate-dielectrics and thick SiN passivation. High bias *I-V* curves displayed over 1000 V breakdown and hysteresis-free characteristics.

## 4.5 Reference:


[1] B. Gaffey, L. J. Guido, X. W. Wang, and T. P. Ma, "High-quality oxide/nitride/oxide gate insulator for GaN MIS structures," *IEEE Transactions on Electron Devices*, vol. **48**, pp. 458-464, 2000.

[2] H. C. Casey, G. G. Fountain, R. G. Alley, B. P. Keller, and S. P. DenBaars, "Low interface trap density for remote plasma deposited $SiO_2$ on *n*-type GaN," *Appl. Phys. Lett.*, vol. **68**, pp. 1850-2, 1996.

[3] M. Sawada, T. Sawada, Y. Yamagata, K. Imai, H. Kimura, M. Yoshino, K. Iizuka, and H. Tomozawa, "Electrical characterization of n-GaN Schottky and PECVD-$SiO_2$/n-GaN interface," *Journal of Crystal Growth*, vol. **189/190**, pp. 706-10, 1998.

[4] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: John Wiley & Sons, 1982 (pp. 781-85).

[5] J. N. Shenoy, "Ph.D. dissertation: Basic MOS studies for Silicon Carbide power devices," in *ECE Department*: Purdue University, 1996.

[6] T. Sawada, Y. Ito, K. Imai, K. Suzuki, H. Tomozawa, and S. Sakai, "Electrical properties of metal/GaN and $SiO_2$/GaN interfaces and effects of thermal annealing," *Applied Surface Science*, vol. **159-160**, pp. 449-55, 2000.

[7] R. Nakasaki, T. Hashizume, and H. Hasegawa, "Insulator-GaN interface structures formed by plasma-assisted chemical vapor deposition," *Physica E*, vol. **7**, pp. 953-7, 2000.

[8] R. Vetury, **N.-Q. Zhang**, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Elect. Dev.*, vol. **48**, 2001.

[9] S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Trapping effects and microwave power performance in AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. **48**, pp. 465-71, 2001.

[10] Y. F. Wu, B. P. Keller, S. Keller, J.-J. Xu, B. J. Thibeault, S. P. Denbaars, and U. K. Mishra, "GaN-based FETs for microwave power amplification," *IEICE Trans. Electron.*, vol. **E82-C**, pp. 1895-1904, 1999.

[11] Y. F. Wu, B. J. Thibeault, B. P. Keller, S. Keller, S. P. Denbaars, and U. K. Mishra, "3-watt AlGaN-GaN HEMTs on sapphire substrates with thermal management by flip-chip bonding," presented at 56th Annual Device Research Conference Digest, 1998.

[12] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMT's," *IEEE Elect. Dev. Lett.*, vol. **21**, pp. 268-70, 2000.

# CHAPTER 5

# Large scale devices and switching measurements

One of the advantages of GaN HEMTs over SiC FETs as switching devices is its high switching speed brought by the high mobility 2-DEG. Previous chapters have shown that double-layer gate-dielectric structure with SiN passivation eliminates dispersion between the DC and pulsed *I-V* curves of GaN HEMTs while maintaining high breakdown voltage. However, the pulsed-*IV* measurement is only an indirect characterization of the switching speed. Precise measurement of the switching speed is necessary to prove that the GaN HEMTs are really faster than SiC or Silicon switching devices. In addition, the switching devices usually handle tens of amperes of current in the proposed applications of GaN HEMTs. It is therefore necessary to measure the switching speed on large periphery devices for a complete exploration of the switching capacity of GaN HEMTs.

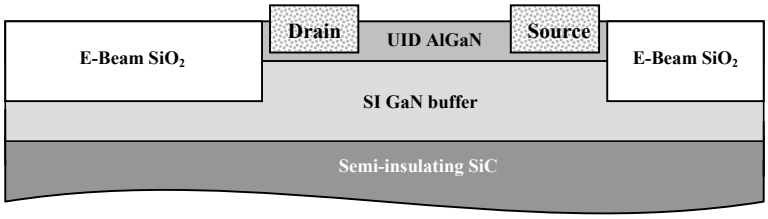
## 5.1 Large periphery GaN switching HEMTs

As discussed in Chapter 3, circular gate design eliminated the field crowding at the end of a T-shape gate and increased the $V_{BR}$ from 700 V of a regular T-shape-gate device to 1050 V. To accommodate the circular design for high breakdown voltage, wire bonding is used to connect discrete small device units into one large periphery device. Yield is the primary focus since a large device usually consists tens of small devices. Uniformity is of similar importance because the failure of one single unit will cause the whole parallelly wired large device to fail.

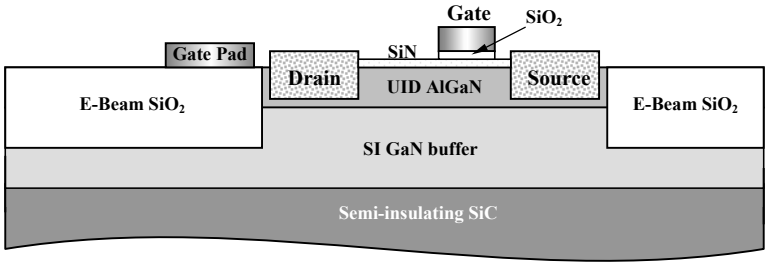
### *5.1.1 Device design and fabrication*

The epilayers for large-scale device fabrication were of the same structure as described in Figure 3.18, except that the $Al_{0.28}Ga_{0.72}N$ layer was only 200 Å thick for easy pinch-off with gate-dielectrics (sample # N011121A). The 2-DEG concentration was $1.24\times10^{13}$ $cm^{-2}$ and mobility was 1725 $cm^2/V\cdot s$, using the high mobility structure introduced in [1]. The device process starts with ohmic contact metal deposition. Ti/Al/Ni/Au = 220/1600/550/450 were annealed at 870 $^oC$ for 30 s to obtain a transfer contact resistance of 0.8 Ω·mm. The thickness of Aluminum was reduced from 2000 Å of standard HEMT processing to control the surface morphology of the annealed contacts. Bad morphology of the source-drain contacts will induce pre-mature breakdown due to field non-uniformity. Then the devices were isolated by mesa etching using $Cl_2$ RIE down to the low-pressure-grown

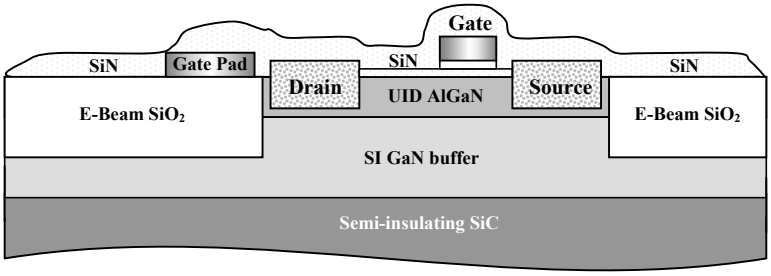
insulating buffer. The etched trench was re-filled with E-beam evaporated $SiO_2$, as shown in Figure 5.1 (a). This would serve as a base for the wire bonding pads and connection lines. After surface clean, the sample was covered by 120 Å sputtered SiN as the bottom layer of gate-dielectrics, and next, the gate metals were E-beam evaporated on to the thin SiN layer. The second layer of gate-dielectric, 60 Å $SiO_2$ was then evaporated followed by the gate metals (Figure 5.1 (b)). After that, the sample was passivated by 1000 Å sputtered SiN. Not only does this SiN layer improve the transient response, but also it protects the devices from damages brought by following processes (Figure 5.1 (c)). To make contacts to the devices, the SiN layer was dry-etched through to the electrodes and 3 μm gold was evaporated on the opening windows as the connection lines and wire bonding pads. The detailed process flow is described in Appendix C.



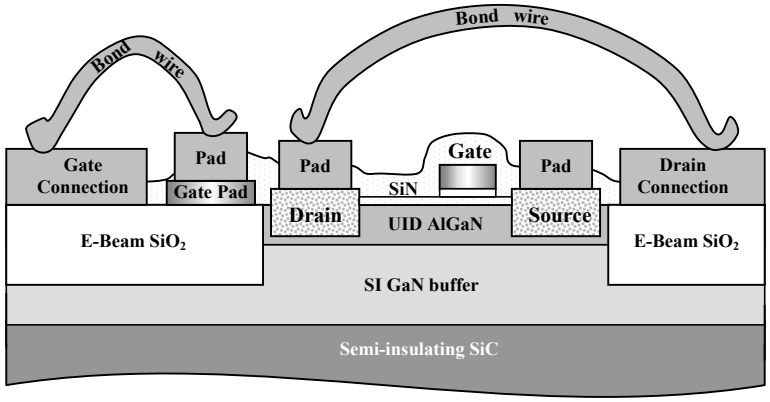

**(a)**




**(b)**




**(c)**




**(d)**

**Figure 5.1 Process flow of large periphery high voltage GaN switching HEMTs.**

Figure 5.2 shows the configuration of a large device. The device consists of a series of cells in one column. Shown in this figure is one cell with links to other cells above and below it. Each circle in this figure represents one small device unit. The drain is in the center, surrounded by the gate finger which is connected to the gate pads. The source is around the drain and the gate, and covers most of the sample. There are two rows of small devices in every cell, and eight units in each row. The gate pads are wire bonded to the center gate line and then bonded to the gate line to the left of the cell; the drain pads are bonded to the two drain lines above and below

the cell. The source is all connected during sample processing for static charge protection. The drain lines are separate for each small device row, so every row can be tested individually before the device is bonded to the circuit board. The number of cells connected together only depends on the on-resistance requirement: more cells result in lower $R_{on}$.

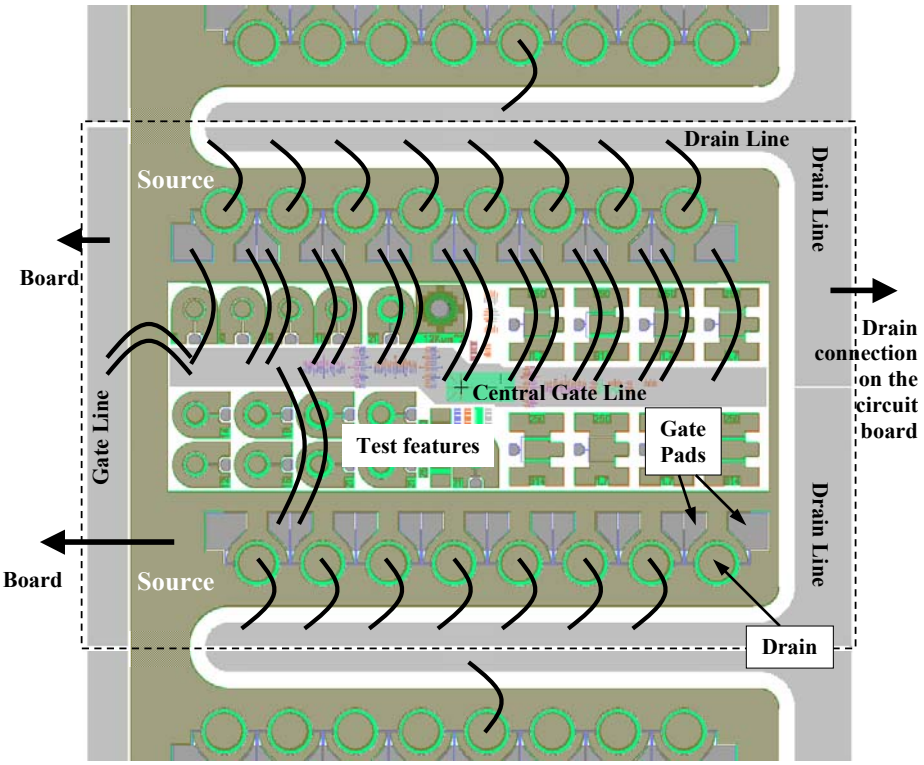



**Figure 5.2 The layout of one cell of the large periphery high voltage GaN switching HEMTs.**

The gate width of the small device is 0.6 mm, which was decide both by the drain pad size and the current densities of different gate widths. Figure 5.3 shows the drain current density dependence on the gate finger width. There is a sharp drop of the current density around $W_g$ = 400 μm, probably due the current crowding on one

side of the circle. With gate width of 300 μm, the diameter is only 65 μm which is too small for the footprint of the bond wire. The diameter of the bond wire is 25 μm and the footprint is around 90 μm wide determined by the size of the bonding tip. Eventually a gate width of 600 μm was chosen, but with two feed points. It is an equivalent of two-finger device with 300 μm wide for each finger. After the large device is soldered to the circuit board, the terminals of the device are wire bonded to the corresponding electrodes on the board, as shown in Figure 5.4.

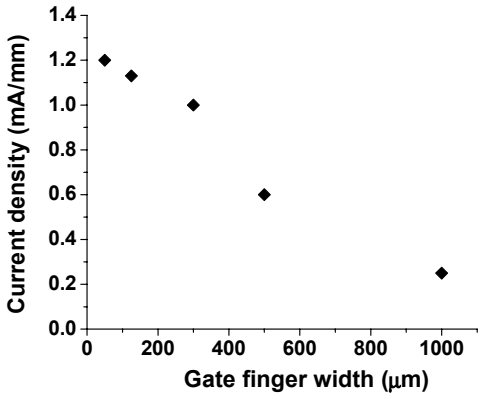



**Figure 5.3 Drain current density versus the gate width.**

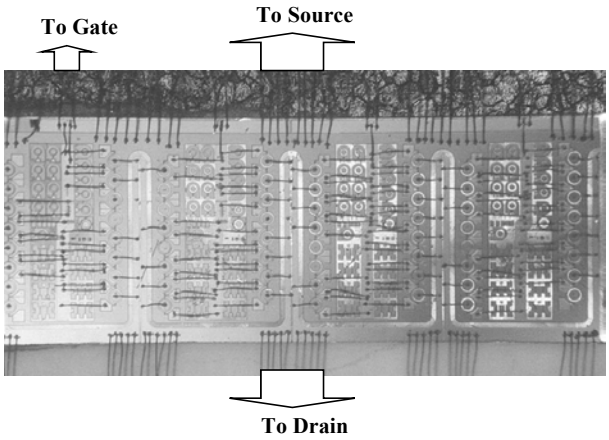



**Figure 5.4 Picture of a bonded device with 4 cells.**

### *5.1.2 Characterization of large periphery devices*

The highest breakdown voltage measured on small periphery devices was 1300 V and no dispersion was seen on these devices under low drain bias as shown in Figure 5.5. In the first attempt to build a large device, 4 cells (64 small devices) were bonded together with a total gate width of 38.4 mm. Figure 5.6 (a) shows the low bias *I-V* curves measured on a probe station. The on-resistance of this device was 1.8 Ω or 70 Ω·mm, which was nearly 8 times higher than that taken on a small device. Careful examination revealed that the total connection resistance of the measurement setup was as high as 1.4 Ω, which was normally ignored during small

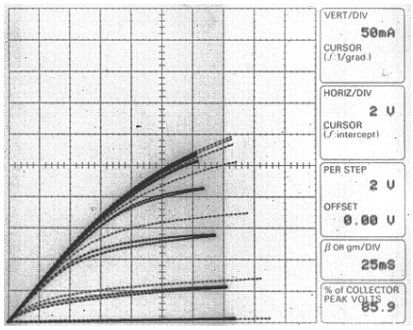



**Figure 5.5 Dispersion measurement on a device with $W_g$ = 300 μm.**

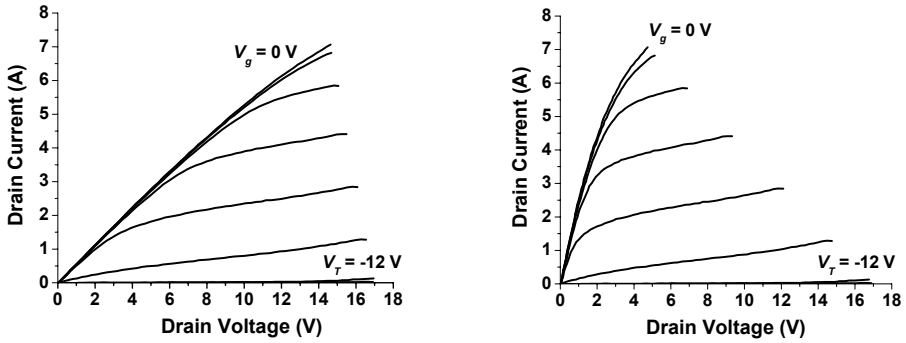



**Figure 5.6 *I-V* curves of a large periphery device with 4 cells and $W_g$ = 38.4 mm.**

device measurement. With this resistance taken into account, the $R_{on}$ of this device was only 0.4 Ω (14.8 Ω·mm) or 2.7 mΩ·cm$^2$ as shown in Figure 5.6 (b).

The connection resistance also explains the low current level ($I_{max}$ = 7 A, as shown in Figure 5.6 (b)) measured on the large device, as illustrated in Figure 5.7. Since there is a resistance $R_M$ = 0.7 Ω on the source of the device, the real gate voltage applied to device $V_{gs} = V_g - I_{ds} \times R_M$, where $V_g$ is the gate output voltage of the curve tracer. The same limit is also applied to the drain bias. For example, even at maximum $V_g$ = 10 V, $V_d$ = 12 V and $I_{ds}$ = 7 A, the $V_{gs}$ is 5 V and $V_{ds}$ is only 2 V on the device! The connection resistance actually placed a current choke for the *I-V* measurement. Further increase of the bias is constrained by the curve tracer power limit.

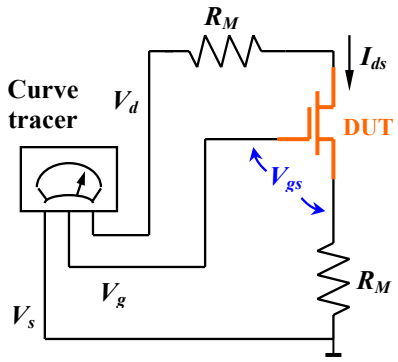



**Figure 5.7 Measurement setup of the large device with large measurement resistance.**

Because of material and process non-uniformity, the breakdown voltage of this large device was only 600 V. Large devices with varied numbers of small devices connected in parallel were fabricated and measured for $V_{BR}$ and $R_{on}$, and the results are shown in Figure 5.8. The $V_{BR}$ decreases rapidly as the number increases,

because the breakdown of the large device is determined by the small device with the lowest $V_{BR}$. The native of the breakdown voltage vs. small device number is not understood and requires detailed statistic study. The specific on-resistance [Ω·mm] increases slowly as more small devices are connected. The parasitic resistance brought up by the connection lines and bond wires, as well as the non-uniformity, lead to the increase.

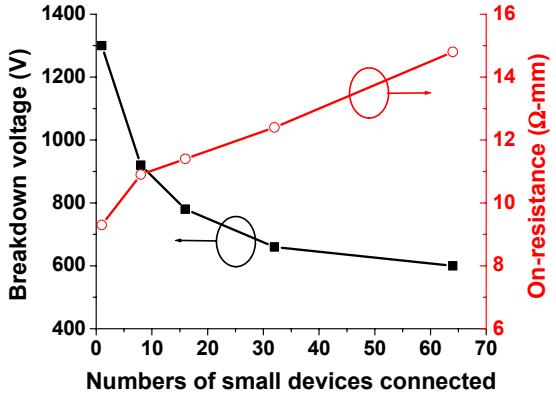



**Figure 5.8 The on-resistance and breakdown voltage of large periphery devices with different gate widths.**

## 5.2 Switching measurement of high voltage GaN HEMTs

### *5.2.1 Switching speed measurement*

The switching speed of high voltage GaN HEMTs was measured in Rockwell Science Center (RSC) with Dr. Vivek Mehrotra. Figure 5.9 shows the measurement setup. The DUT (device under test) is connected in series with a resistor to the power supply. The resistor acts both as a current choke and a current sensor. The voltage measured on the resistor by the Oscilloscope divided by the resistance is the

current flowing through the DUT. The Oscilloscope also takes the voltage across the DUT at the same time. The gate controller (pulse generator) was custom-made in RSC and it can generate two pulses with variable pulse width and pulse separation. The pulse levels were set to be 0 V and –15 V, which were the turn-on and pinch-off voltage for the large periphery GaN HEMTs, respectively.

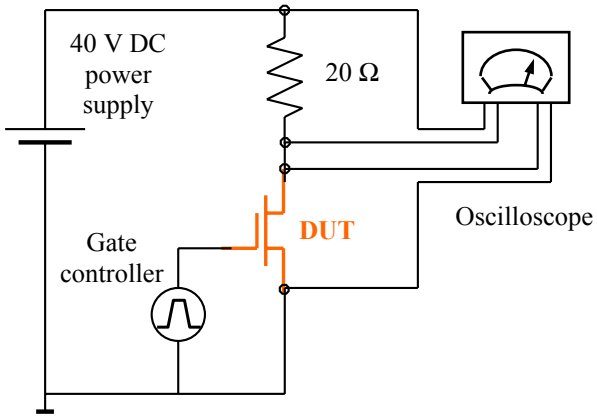
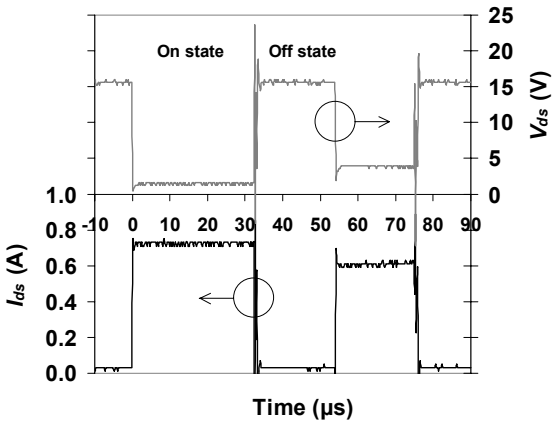


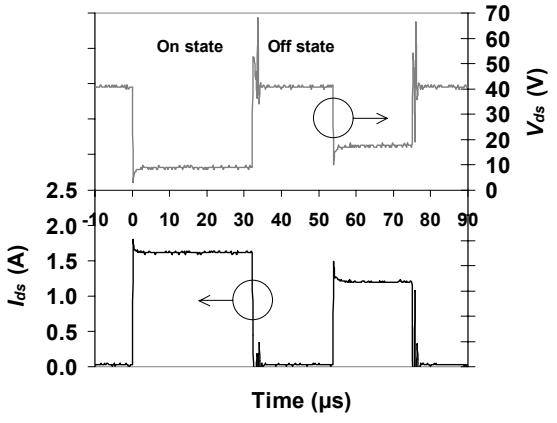

**Figure 5.9 Switching speed measurement setup.**

New samples with the same material structure were processed for the switching measurement. Before wire bonding, each small device was tested individually. Only those that could withstand 650 V drain bias were bonded into the large periphery devices (the highest $V_{BR}$ of small devices on the new samples was only 750 V due to buffer leakage). After that, no breakdown measurement was taken on the large devices. A totally of 45 small devices were bonded into a large device ($W_g$ = 27 mm) on sample N010421B and yielded a $R_{on}$ of 1.0 Ω, and 42 small devices for sample N011127D1 ($W_g$ = 25.2 mm) with $R_{on}$ = 1.5 Ω.

Figure 5.10 shows the switching measurement made on N010421B with two different power supply voltages of 15 V and 40 V. The turn-on and turn-off transients were very short and they do not depend on the $V_{supp}$. For $V_{supp}$ = 15 V, the on-resistance of the device ($V_{ds}/I_{ds}$) was 1 Ω in the first turn-on pulse, and it increased to 5.7 Ω in the following turn-on pulse. While for $V_{supp}$ = 40 V, the $R_{on}$ of the device increased from 4.5 Ω in the first turn-on pulse to 13.4 Ω in the next pulse.




**(a) $V_{supp}$ = 15 V.**

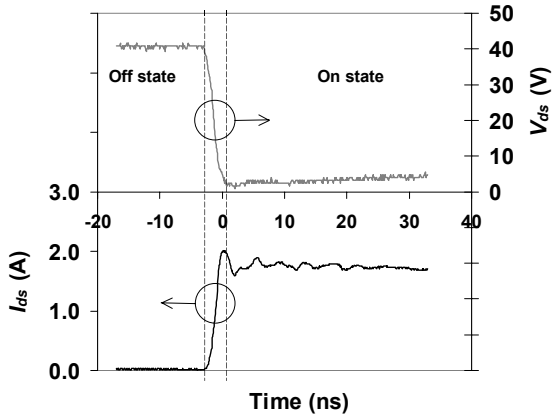



**(b) $V_{supp}$ = 40 V.**

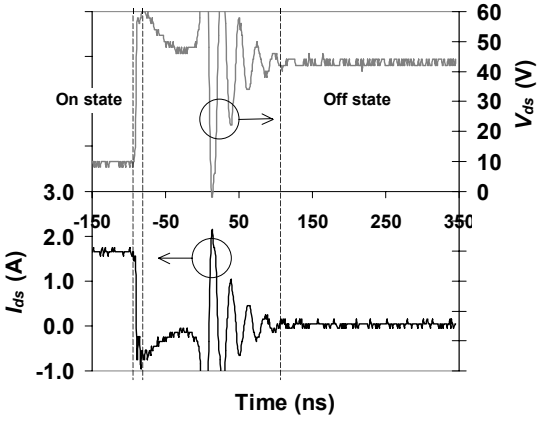
**Figure 5.10 Switching measurements with two different supply voltages.**

The change of $R_{on}$ was not permanent, since the subsequent measurement would repeat the same increase of $R_{on}$. The exact origin of this problem is under investigation in RSC.

The turn-on and turn-off characteristics were measured in a shorter time scale and are shown in Figure 5.11. The turn-on time is only 3.5 ns with the fact that the transient time of the gate pulse is 2 ns. The turn-off transient shows ringing after the




**(a) Turn on.**




**(b) Turn off.**

**Figure 5.11 Turn-on and turn-off edges measured in short time scale.**

device was turned off. The ringing was brought by the resonance of the device input capacitance and the connection inductance. The input capacitance of the HEMT is much lower in off-state than in on-state, hence it caused the high frequency ringing after the device was turned off. If we do not consider the ringing, the turn-off time of the GaN HEMT is 7 ns.

### *5.2.2 Constant current switching measurement*

In the previous measurement, the current choke resistor will affect the voltage and current on the switch during the turn-on and turn-off transient. It is equivalent to force the voltage and current on the switch to change along a load line. To measure the real switching characteristics of GaN HEMTs in a converter, the devices should be tested in the constant current switching setup shown in Figure 5.12. The ideal voltage and current waveforms of this circuit are shown in Figure 5.13. In the first on-state gate pulse, the power supply charges the inductor through the GaN HEMT switch. The inductance and the pulse width determine the final current through the inductor at the end of the pulse. Then the switch is turned off. The current in the inductor will flow freely in the loop formed by the inductor and the diode. So the inductor will serve as a current source in the following measurement. After the switch is totally off, a second gate pulse will turn on the switch again. A measurement will be trigged at the turn-on edge of the second gate pulse to record how the current through the switch rises to the current level in the inductor (current source) and how the voltage drops from blocking voltage to zero. Another

measurement will be trigged at the turn-off edge of the second pulse to record the turn-off current and voltage waveforms. The second pulse is set to be short enough to prevent large current rise on the inductor.

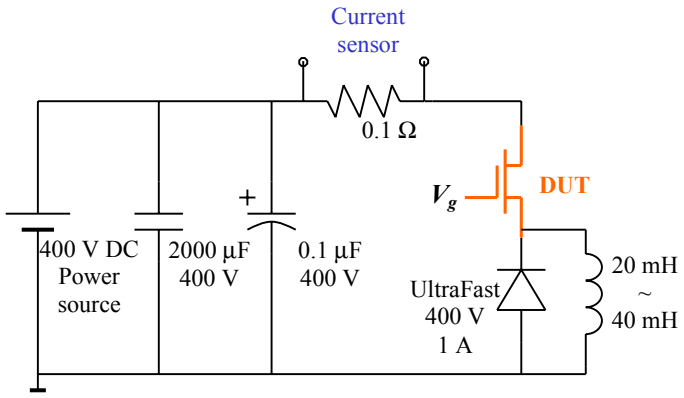



**Figure 5.12 Constant current switching measurement setup.**

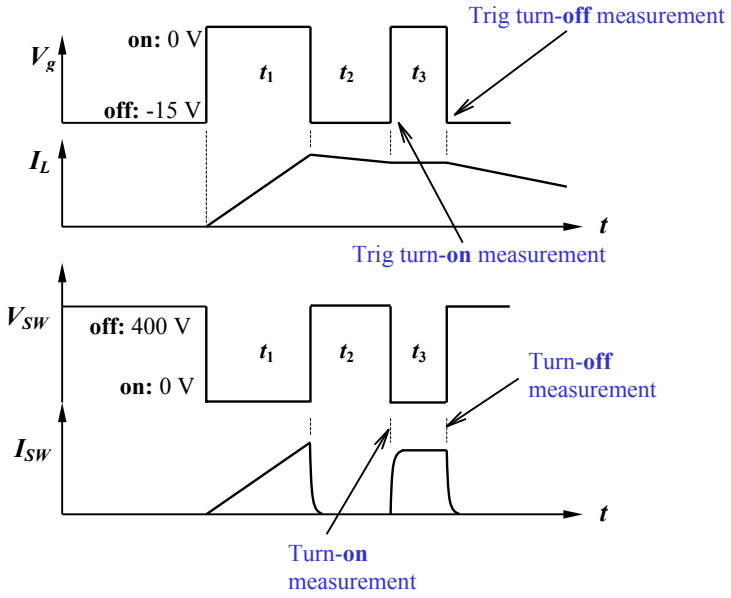



**Figure 5.13 Ideal circuit waveforms of a constant current measurement.**

The circuit board for constant current switching measurement with a GaN HEMT bonded on it is shown in Figure 5.14. The preliminary measurement taken in

RSC has shown a turn-on time of 7 ns with 600 V switched voltage, compared to that of 100 ns of the fastest SiC switching device (with 1200 V switched voltage) [2]. The detail will be published later.

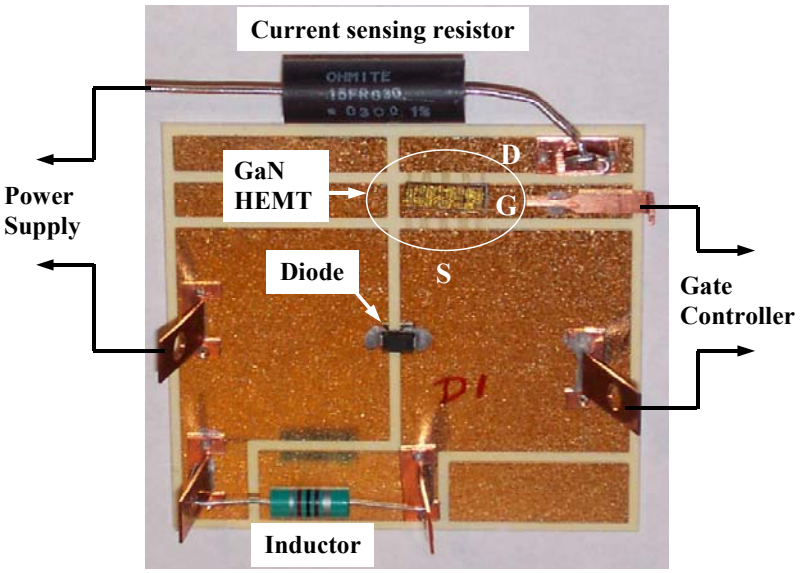



**Figure 5.14 Circuit board for constant current switching measurement. The GaN HEMT was wire bonded to the board.**

## 5.3 Summary

Large periphery high voltage GaN HEMTs were fabricated by wire bonding of small circular devices. 0.4 Ω on-resistance and 600 V breakdown voltage were achieved on a large device with a total gate width of 38.8 mm. 64 small devices were bonded together to obtain this large device with 100 % yield. Since large periphery devices require large substrate size, the poor uniformity of GaN material is still an obstacle to achieve the same breakdown voltage on large devices as on small devices. As expected from material advantages of AlGaN/GaN system, the large

devices demonstrated very fast switching speed. The turn-on time of the GaN HEMT switch was 3.5 ns and the turn-off time was 7 ns.

## 5.4 Reference:


[1] L. Shen, S. Heikman, B. Moran, R. Coffie, N.-Q. Zhang, D. Buttari, I. P. Smorchkova, S. Keller, S. P. DenBaars, and U. K. Mishra, "AlGaN/AlN/GaN high-power microwave HEMT," *IEEE Electron Device Letters*, vol. **22**, pp. 457-9, 2001.

[2] P. Friedrichs, H. Mitlehner, K. O. Dohnke, D. Peters, R. Schorner, U. Weinert, E. Baudelot, and D. Stephani, "SiC power devices with low on-resistance for fast switching applications," presented at 12th International Symposium on Power Semiconductor Devices & ICs. Proceedings, Toulouse, France, 2000.

# CHAPTER 6

# Conclusions and suggested future work

## 6.1 Conclusions

The intrinsic material advantages of AlGaN/GaN HEMT and the advances in microwave power GaN HEMTs initiated the research on high voltage GaN HEMTs for switching applications. The merits of AlGaN/GaN HEMTs are that they possess lower specific on-resistance and faster switching speed than SiC switching devices (MOSFETs and JFETs). There was not much research background for switching GaN HEMTs at the start of this work, except that 435 V breakdown was achieved with a low saturated current level of 160 mA/mm [1]. The progress made in switching GaN HEMTs research in this work is summarized below.

### *6.1.1 Device analysis and simulation*

Until the onset of this work, there was no quantitative breakdown analysis of GaN HEMTs to illustrate their operation advantages over SiC devices derived from the material advantages of GaN. With the analysis of the charge and field

distribution, the structure dependent breakdown voltage and on-resistance relationship were obtained and compared to that of SiC FETs. The power-device-figure-of-merit of 22 % Aluminum composition AlGaN/GaN HEMTs is 50 times higher than that of SiC devices. Higher Aluminum composition in AlGaN was pointed out to be the direction to further increase the $V_{BR}$ and reduce the $R_{on}$, and an optimum 70 % *Al* in AlGaN will lead to 4 more times higher power-device-figure-of-merit than with $Al_{0.22}Ga_{0.78}N$.

Device simulation is faster and more cost efficient than experiments, and it provides information of devices that is impossible to measure. AlGaN/GaN HEMTs were modeled and simulated for the first time in ATLAS, based on the charge distribution model previously developed in our group. The polarization field and surface traps cannot be ignored in device modeling and their parameters were obtained by fitting the simulated $n_s$ vs. $t_{AlGaN}$ relationship to the experiment one. With proper mobility and impact ionization models, the simulated DC and small signal AC characteristics agree well to the experimental results. The simulation of the field in the device reveals that the field peaks at the drain-side gate edge. Alternative FET structures, such as field-plate HEMTs, RESURF HEMTs and recessed-gate HEMTs, were simulated to investigate the reduction of the peak field.

### *6.1.2 High breakdown voltage with low on-resistance*

Low buffer leakage is the first requirement for high voltage operation of GaN HEMTs. GaN grown on Sapphire normally contains high concentration background

charge due to the out-diffusion of oxygen from Sapphire, while GaN grown on SiC displayed much lower leakage current. Low-pressure growth of GaN incorporates large amount of carbon into the buffer layer. The carbon impurities appear as deep traps and compensate most of the background charge. By applying low-pressure growth on SiC substrates, the leakage of the GaN buffer was reduced to 0.2 mA/mm from 50 mA/mm at the beginning of the work.

Field-plate GaN HEMTs were fabricated to increase the breakdown voltage to 570 V, a 30 % increase over previous achievements. The current level was increased to 520 mA/mm due to progress in growth techniques, and the on-resistance was 1.5 $m\Omega \cdot cm^2$. This result was already comparable to the best result achieved on SiC switching devices. Simulation on field-plate HEMTs shows that further improvement of $V_{BR}$ requires thick (up to 1 μm) and high quality (> 10 MV/cm field strength) dielectric process which is currently unavailable at UCSB but will be developed as future work.

More detailed investigation revealed that the gate leakage is a major cause of reduced breakdown voltage. Hence, the insulated-gate HEMT structure was adopted to reduce the gate leakage. 100 Å $SiO_2$ JVD deposited under the gate metal brought down the gate leakage 2 to 4 orders lower than that of a schottky contact gate. As a result, the breakdown voltage of the insulated-gate HEMT exceeded 1000 Volts. The breakdown voltage is also affected by the device layouts. A circular gate design eliminated the field non-uniformity along the gate finger and led to an increase of $V_{BR}$ from 700 V to 1050 V. Also, E-beam deposited $SiO_2$ was investigated as the

gate dielectric and showed the same promising results: 1300 V breakdown voltage along with 1.65 $m\Omega \cdot cm^2$ on-resistance were achieved. The power-device-figure-of-merit of $9.94 \times 10^8$ $[V^2 \cdot \Omega^{-1} cm^{-2}]$ is the highest for any power switching devices to date, and it is on the theoretical limit of SiC switching devices. Temperature dependent and structure dependent measurements taken on the devices were close to the theoretical analysis.

### *6.1.3 High switching speed*

One problem brought by the $SiO_2$ gate-dielectric was large current "dispersion", a sign of low switching speed. Different dielectric-on-GaN MIS structures were investigated of the interface using the photo-*CV* technique to search for a proper "passivation" material for GaN HEMTs. SiN was found to form much lower interface trap density on n-GaN than $SiO_2$, regardless of deposition methods, and the interface quality could be improved by pre-deposition surface clean and low temperature post-deposition anneal. Interface trap density and charge density of $2.1 \times 10^{12}$ $cm^{-2}$ and $2.9 \times 10^{11}$ $cm^{-2}$, respectively, were achieved for PECVD SiN on n-GaN. When these dielectrics were applied to GaN HEMTs for passivation, only sputtered SiN could eliminate the dispersion from the devices at that time (Current research suggests that PECVD SiN is also effective). The power density of GaN HEMTs on Sapphire was increased by passivation from 3.3 W/mm to 6.6 W/mm at 6 GHz with a PAE of 47.2 %. This result extended the previous achievement by nearly 50 % and it still defines the state-of-art of output power of GaN HEMTs on sapphire

[2]. Further experiments on JVD SiN and other group's research on PECVD SiN also showed successful passivation of GaN HEMTs by these dielectrics [3].

Consequently, SiN was used as the gate-dielectric on high voltage GaN HEMTs and achieved low dispersion, but the gate leakage is even higher than without gate-dielectric. In order to combine the advantage of passivation from SiN and low leakage from $SiO_2$, double-layer gate-dielectric structure was implemented in insulated-gate GaN HEMTs and exhibited low dispersion and low gate leakage simultaneously. High bias *I-V* curves displayed over 1000 V breakdown with no hysteresis. Switching measurements (with a supply voltage of 40 V) showed a short turn-on time of 3.5 ns and turn-off time of 7 ns for a large periphery device with a gate width of 27 mm.

### *6.1.4 Large scale devices*

Large periphery devices were fabricated by wire bonding small circular devices. Yield was the highest priority in the design and process of the large scale devices. A large device exhibited 0.4 Ω on-resistance and 600 V breakdown voltage with 64 bonded small device ($W_g$ = 38.8 mm). The relatively low $V_{BR}$ was caused by the non-uniformity of GaN material.

Table 6-1 summarizes the advances of GaN switching HEMTs. For comparison with SiC switching devices, please refer to Figure 3.27.

**Table 6-1 Progress of GaN switching HEMTs.**

| References | Small Devices | | Large Devices | | | |
|---|---|---|---|---|---|---|
| | $V_{BR}$ (V) | Specific $R_{on}$ ($\Omega \cdot cm^2$) | Gate Width (mm) | $V_{BR}$ (V) | Total $R_{on}$ ($\Omega$) | Specific $R_{on}$ ($\Omega \cdot cm^2$) |
| N.-Q. Zhang, et al. [4] | 1300 | 1.65 | 38.4 | 600 | 0.4 | 2.7 |
| G. Simin, et al. [5] | 500 | 0.75 | 6 | N/A | N/A | N/A |
| S. Yoshida, et al. [6] | 600 | 3 | 200 | 100 | 0.4 | 70 |

## 6.2 Suggested future work

Although the preliminary results obtained in this dissertation opened a door to the switching applications for AlGaN/GaN HEMTs, the performance of the devices is still far from the prediction of the theoretical analysis. Besides, many problems are remained unsolved. Some important aspects of future work are suggested below.

1. For planar devices, the electric field peak at the gate edge is always the biggest obstacle for high voltage operation. Experimental work needs to be done to realize the three high voltage HEMT structures with reduced field peak (Field-plate HEMTs, RESURF HEMTs and recessed-gate HEMTs) discussed in Chapter 3. Moreover, AlGaN/GaN HEMTs with higher *Al*-composition should be investigated, since device analysis indicated the highest power-device-figure-of-merit corresponds to an *Al*-content of 70 %.

2. The breakdown simulation in this work showed a trend of structural dependent of $V_{BR}$, but the simulated breakdown voltages are not exactly the same as the experimental results. To optimize the device structure, more accurate material parameters such as impact ionization coefficient and more precise GaN HEMT model are required in the simulation.

3. The performance of present GaN HEMTs normally degrades as a function of time, no matter whether the devices are passivated or not. To investigate this problem, the cause of dispersion and the mechanism of SiN passivation should be first inspected.

4. GaN HEMTs are normally-on devices. A Si MOSFET can be used in combination with the GaN HEMT to make a normally-off configuration [7], but then the switching speed and the maximum allowed ambient temperature are determined by the silicon device. New AlGaN/GaN HEMT structures should be exploited to achieve normally-off devices.

5. The specific on-resistance of the large device with $W_g$ = 38.4 mm is 80 $m\Omega \cdot cm^2$ if the wire bonding pads are taken into account for the device area. This value is 50 times larger than that of a small device. The wire-bonding scheme also brings complexity to device fabrication and reduces the device reliability. If the drain electrodes can be connected to the backside of the substrate by via holes, wire-bonding will not be required, and the area of the large device will shrink by 5 to 10 times. Then the specific on-resistance will decrease to 8 to 16 $m\Omega \cdot cm^2$.

The potential of GaN HEMTs as high voltage switching devices was demonstrated in this dissertation. With improved material growth, better device design and advanced process techniques, GaN HEMTs will show great promise for high voltage, low-loss switching applications in high temperature environment.

## 6.3 References:


[1] R. Vetury, Y. F. Wu, P. T. Fini, G. Parish, S. Keller, S. DenBaars, and U. K. Mishra, "Direct measurement of gate depletion in high breakdown (405 V) AlGaN/GaN heterostructure field effect transistors," presented at International Electron Devices Meeting 1998, San Francisco, CA, 1998.

[2] Y.-F. Wu, N.-Q. Zhang, J. Xu, and L. McCarthy, "Group III Nitride base FETs and HEMTs with reduced trapping and method of producing the same." U.S.: patent pending.

[3] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMT's," *IEEE Elect. Dev. Lett.*, vol. **21**, pp. 268-70, 2000.

[4] N.-Q. Zhang, B. Moran, S. P. DenBaars, U. K. Mishra, X. W. Wang, and T. P. Ma, "Kilovolts AlGaN/GaN HEMTs as switching devices," *phys. stat. sol. (a)*, vol. **188**, pp. 213-7, 2001.

[5] G. Simin, X. Hu, N. Ilinskaya, A. Kumar, A. Koudymov, J. Zhang, M. Asif Khan, R. Gaska, and M. S. Shur, "7.5 kW/mm$^2$ current switch using AlGaN/GaN metal-oxide-semiconductor heterostructure field effect transistors on SiC substrates," *IEE Electronics Letters*, vol. **36**, pp. 2043-4, 2000.

[6] S. Yoshida and H. Ishii, "A high power GaN based field effect transistor for large current operation," *phys. stat. sol. (a)*, vol. **188**, pp. 243-46, 2001.

[7] B. J. Baliga, *Power Semiconductors Devices*: PWS Publishing Company, 1996.

# APPENDIX A

# ATLAS Input File for GaN HEMT simulation

```
############################################################
# Normal Gate GaN HEMTs
# Lg=0.6um, Lgd=1.5um
# AlGaN thickness: 200A
# Undoped, surface trap everywhere
############################################################
go atlas
Title    GaN HEMT IV characteristics
#
# SILVACO International 1996
#
####################################
# SECTION 1: Mesh input
####################################
mesh         nx=57 ny=85
#
x.m        n=1    l=0.0   r=1.0
x.m        n=3    l=0.02  r=1.0
x.m        n=7    l=0.1   r=1.0
x.m        n=15   l=0.9   r=1.0
x.m        n=27   l=1.5   r=1.0
x.m        n=36   l=1.8   r=1.0
x.m        n=40   l=2.0   r=1.0
x.m        n=47   l=2.7   r=1.0
x.m        n=51   l=2.9   r=1.0
x.m        n=55   l=2.98  r=1.0
x.m        n=57   l=3.0   r=1.0
#
y.m        n=1     l=0.0      r=1.0
```

```
y.m        n=6     l=0.05     r=1.0
y.m        n=8     l=0.0502   r=1.0
y.m        n=11    l=0.0505   r=1.0
y.m        n=16    l=0.0550   r=1.0
y.m        n=21    l=0.06     r=1.0
y.m        n=26    l=0.065    r=1.0
y.m        n=31    l=0.0695   r=1.0
y.m        n=34    l=0.0698   r=1.0
y.m        n=36    l=0.07     r=1.0
y.m        n=46    l=0.071    r=1.0
y.m        n=55    l=0.08     r=1.0
y.m        n=57    l=0.1      r=1.0
y.m        n=75    l=1.0      r=1.05
y.m        n=85    l=3.0      r=1.05
#
###################################
# SECTION 2: Structure Specification
###################################
region     num=1  material=GaAs y.min=0.07
region     num=2  material=Air y.min=0.0 y.max=0.05
region     num=3  material=AlGaAs x.min=0.0 x.max=1.5 \
                  y.min=0.05 y.max=0.0502 x.composition=0.27
region     num=4  material=AlGaAs x.min=1.5 x.max=1.8 \
                  y.min=0.05 y.max=0.0502 x.composition=0.27
region     num=5  material=AlGaAs x.min=1.8 x.max=3.0 \
                  y.min=0.05 y.max=0.0502 x.composition=0.27
region     num=6  material=AlGaAs y.min=0.0502 y.max=0.0698 \
x.composition=0.27
region     num=7  material=AlGaAs y.min=0.0698 y.max=0.07 \
x.composition=0.27
#
# electrodes specification
#
elec     num=1  name=source x.min=0.0 x.max=0.0 \
y.min=0.05 y.max=0.085
elec     num=2  name=drain x.min=3.0 x.max=3.0 \
y.min=0.05 y.max=0.085
elec     num=3  name=gate x.min=0.9 x.max=1.5 \
y.min=0.01 y.max=0.05
#
contact  num=1 name=source resistance=500
contact  num=2 name=drain resistance=500
contact  num=3 name=gate workfun=5.1
#
# Background doping
#
doping uniform y.min=0.05 n.type conc=1e15
#
# Ohmic contact doping
#
doping      uniform x.min=0.0 x.max=0.01 y.min=0.05 y.max=0.075 \
            n.type conc=1.5e21
doping      uniform x.min=2.99 x.max=3.0 y.min=0.05 y.max=0.075 \
```

```
            n.type conc=1.5e21
#
# Piezo-electric simulation
#
doping      uniform y.min=0.05 y.max=0.0502 p.type conc=6.0e20
doping      uniform y.min=0.0698 y.max=0.07 n.type conc=6.0e20
#
# Surface trap providing electrons to channel. Cancel one of
# the region when electrons are injected into that region
#
trap e.level=2.02 donor density=7.1e20 degen=1 \
taun0=1e-12 taup0=2e-11 region=3
trap e.level=2.02 donor density=7.1e20 degen=1 \
taun0=1e-12 taup0=2e-11 region=4
trap e.level=2.02 donor density=7.1e20 degen=1 \
taun0=1e-12 taup0=2e-11 region=5
#
####################################
# SECTION 3: Material Models
# (The names of AlGaAs/GaAs were used for AlGaN/GaN)
####################################
#
# material parameters
#
material material=AlGaAs eg300=3.95 align=0.68 arichn=23 arichp=72 \
            mun=100 mup=5 edb=0.025 eab=0.16 permittivity=10.32 \
            nc300=2.07e18 nv300=1.16e19 copt=9.75e-10 \
            taun0=1e-9 taup0=2e-8 nsrhn=4e18 nsrhp=4e18 \
affinity=3.14 vsatn=1e4 vsatp=1e3
#
material material=GaAs eg300=3.42 align=0.68 arichn=23 arichp=72 \
            mun=630 mup=5 edb=0.025 eab=0.16 permittivity=10.4 \
            nc300=2.07e18 nv300=1.16e19 copt=6.84e-10 \
            taun0=1e-9 taup0=2e-8 nsrhn=4e18 nsrhp=4e18 \
affinity=3.5 vsatn=1.3e7 vsatp=1e3
#
material material=Air
#
#material material=SiN
#
# Impact ionization parameters (After Oguzman's paper)
#
impact  selb an1=2e26 bn1=3.42e7 ap1=2e26 bp1=1.95e7 \
            an2=2.6e8 bn2=3.415e7 ap2=4.98e6 bp2=1.95e7 \
            egran=3.e6 betan=1.0 betap=1.0
#
# mobility velocity model
#
model  srh fldmob
mobility material=GaAs fldmob.n evsatmod=0 betan=2.6 vsatn=1.3e7
#
####################################
# SECTION 4: Id-Vg Calculation
```

```
####################################
#
# itineration methods
#
method newton trap itlim=35 maxtrap=6 \
      vsatmod.inc=0.1 carriers=1 elec
output con.band val.band j.total
#
solve initial
#
# Bias Vg to –6 V first
#
solve vgate=0
save outf=IV_band_0d.str
tonyplot IV_band_0d.str -set IV_band_0.set
#
solve vgate=-0.5 vstep=-0.5 name=gate vfinal=-6
#
# Then bias Vds to 5 V
#
solve vgate=-6.0 vdrain=0.01
solve vgate=-6.0 vdrain=0.02
solve vgate=-6.0 vdrain=0.05
#
solve vdrain=0.1 vstep=0.2 name=drain vfinal=5
#
# Finally, calculate from Vg=-6V to Vg=3V
#
log outf=IV_gm_d.log master
solve vgate=-6.0
solve vgate=-5.99
solve vgate=-5.97
solve vgate=-5.9 vstep=0.2 name=gate vfinal=3
#
tonyplot IV_gm_d.log
#
####################################
# SECTION 5: Ids-Vds calculation
####################################
log off
#
method newton trap itlim=35 maxtrap=6 \
      vsatmod.inc=0.1 carriers=1 elect
#
solve init
#
# Apply a set of biases at the gate and save solutions
#
solve vgate=0     outf=IV_Vg+0d.out
solve vgate=2     outf=IV_Vg+2d.out
solve vgate=-2    outf=IV_Vg-2d.out
solve vgate=-4    outf=IV_Vg-4d.out
solve vgate=-6    outf=IV_Vg-6d.out
```

```
#
# Calculate IV characteristic at Vg=-6
#
load inf=IV_Vg-6d.out
log outf=IV_Vg-6d.log
solve outf=IV_Vg-6d.out master
solve vdrain=0.01
solve vdrain=0.02
solve vdrain=0.05
solve vdrain=0.08
solve vdrain=0.16
solve vdrain=0.30
solve vdrain=0.50  vstep=0.2  name=drain vfinal=16
#save outf=IV_Vg-6_I.out master
#
# Calculate IV characteristic at Vg=-4
#
load inf=IV_Vg-4d.out
log outf=IV_Vg-4d.log
solve outf=IV_Vg-4d.out master
solve vdrain=0.01
solve vdrain=0.02
solve vdrain=0.05
solve vdrain=0.08
solve vdrain=0.16
solve vdrain=0.30
solve vdrain=0.50  vstep=0.2  name=drain vfinal=14
#save outf=IV_Vg-4_I.out master
#
# Calculate IV characteristic at Vg=-2
#
load inf=IV_Vg-2d.out
log outf=IV_Vg-2d.log
solve outf=IV_Vg-2d.out master
solve vdrain=0.01
solve vdrain=0.02
solve vdrain=0.05
solve vdrain=0.08
solve vdrain=0.16
solve vdrain=0.30
solve vdrain=0.50  vstep=0.2  name=drain vfinal=12
#save outf=IV_Vg-2_I.out master
#
# Calculate IV characteristic at Vg=0
#
load inf=IV_Vg+0d.out
log outf=IV_Vg+0d.log
solve outf=IV_Vg+0d.out master
solve vdrain=0.01
solve vdrain=0.02
solve vdrain=0.05
solve vdrain=0.08
solve vdrain=0.16
```

```
solve vdrain=0.30
solve vdrain=0.50  vstep=0.2  name=drain vfinal=9
#save outf=IV_Vg+0_I.out master
#
# Calculate IV characteristic at Vg=2
#
load inf=IV_Vg+2d.out
log outf=IV_Vg+2d.log
solve outf=IV_Vg+2d.out master
solve vdrain=0.01
solve vdrain=0.02
solve vdrain=0.05
solve vdrain=0.08
solve vdrain=0.16
solve vdrain=0.30
solve vdrain=0.50  vstep=0.2  name=drain vfinal=7
#save outf=IV_Vg+2_I.out master
#
# plot all Ids-Vds curves together
#
tonyplot -overlay IV_Vg+2d.log IV_Vg+0d.log IV_Vg-2d.log \
IV_Vg-4d.log -set IV_curves.set
#
####################################
# SECTION 6: Frequencny domain AC simulation
####################################
log off
#
method newton trap itlim=35 maxtrap=6 \
      vsatmod.inc=0.1 carriers=1 elect
#
solve init
#
# Bias the device to Vgs=-3V and Vds=12V first.
#
solve vgate=-1
solve vgate=-2
solve vgate=-3
#
solve vdrain=0.01
solve vdrain=0.05
solve vdrain=0.60  vstep=0.4  name=drain vfinal=1.8
#
solve vdrain=2.5  vstep=1.0  name=drain vfinal=12
#
# Apply device parasitic components.
# Parasitics are from Volker's thesis pp.36.
#
log outf=ac.log master gains s.params Rin=2.66 Rout=13.77 \
Rground=7.02 Lin=6.726e-11 Lout=2.993e-11 \
Lground=7.78e-12 inport=gate outport=drain width=150
#
# AC calculation
```

```
#
solve ac freq=10 fstep=10 mult.f nfstep=7
solve ac freq=1e9
solve ac freq=2e9 fstep=2e9 nfstep=3
solve ac freq=1e10 fstep=5e9 nfstep=22
#
tonyplot ac.log
#
####################################
# SECTION 7: Breakdown calculation
####################################
log off
#
method newton trap itlim=35 maxtrap=6 \
      vsatmod.inc=0.1 carriers=2
#
solve init
#
# Bias the device to pinch off (Vg=-6)
#
log outf=breakdown_0.log
solve vdrain=0.01
solve vdrain=0.16
solve vdrain=0.60  vstep=0.2  name=drain vfinal=4.8
#
# Step the Vds until the drain current exceeds the compliance
# current level and the Vds is the breakdown voltage
#
solve vdrain=5  vstep=1  name=drain vfinal=200 comp=9.e-5 e.comp=2
#
save outf=breakdown_1.str
tonyplot breakdown_1.str -set band.set
#
tonyplot breakdown_0.log -set Ids_Vds.set
#
####################################
quit
```

# APPENDIX B

# Mathematica File for C-V Simulation

- **Constants**

```
phys = {k → 1.38×10^-23 (* J/K, Boltzmann's constant *),
    q → 1.6×10^-19 (* C, electron charge *),
    ε0 → 8.85×10^-14 (* F/cm, permittivity *),
    T → 300 (* K, temperature *)};
Semiconductor = {ni → 2.0×10^-10 (* (/cm)^3, GaN intrinsic carrier conc. *),
    εSemi → 10.1 (* GaN relative permittivity *),
    εg → 3.4 (* eV, GaN bandgap *),
    χSemi → 4.1(* V, GaN electron affinity *)};
Insulator = {εInsu → 7.1, dInsu → 263×10^-8(* cm *),
    ψMetal → 4.5(* V, Chromium work function *)};
dope = {Nd → 3.43×10^17 (* (/cm)^3, donor doping *)};
```

- **Fermi Potentials and Equilibrium Concentrations**

```
β = q/(k T); (* 1/VT, inverse thermal voltage *)
ψFn = (k T)/q Log[Nd/ni];
(* V, Quasi-Fermi, Intrinsic Fermi level difference *)
Print["ψFn=", ψFn /. Semiconductor /. Insulator /. dope /. phys, " V"];
UFn = Log[Nd/ni]; (* Normalized Fermi level difference *)
VFB = ψMetal - (χSemi + 1/2 εg - ψFn); (* V *)
```

```
Print["Flatband Voltage, V_FB = ",
  V_FB /. Semiconductor /. Insulator /. dope /. phys, " V"];
```

## ▪ Potentials

$$L_D = \sqrt{\frac{k\,T\,\epsilon_{Semi}\,\epsilon_o}{q^2\,N_d}}$$ ; (* cm, Electron Debye length *)

$\psi_B = \psi_{Fn}$; (* V, Bulk Fermi difference *)

```
Print["ψ_B = ", ψ_B /. Semiconductor /. Insulator /. dope /. phys, " V"]
```

$$E_S = \text{Sign}[\psi_S]\,\frac{\sqrt{2}\,k\,T}{q\,L_D}\,\sqrt{(\text{Exp}[-\beta\,\psi_S] + \beta\,\psi_S - 1) + \frac{n_i^2}{N_d^2}\,(\text{Exp}[\beta\,\psi_S] - \beta\,\psi_S - 1)}$$ ;

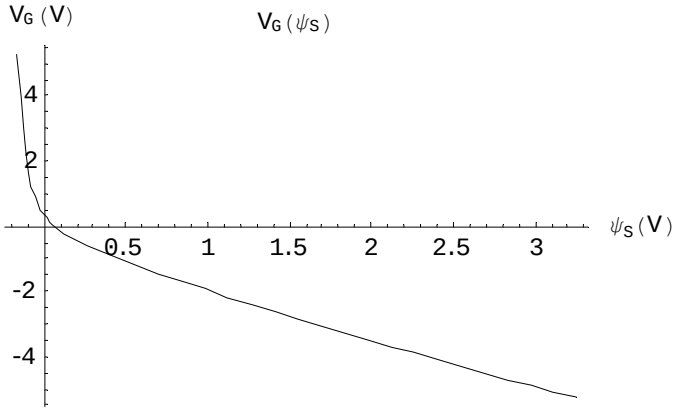
(* V/cm, Surface E-field *)

$$V_G = V_{FB} - \left(\frac{\epsilon_{Semi}}{\epsilon_{Insu}}\,E_S\,d_{Insu} + \psi_S\right)$$; (* V, Gate/Oxide-semiconductor voltage *)

$V_{Th} = V_G /. \psi_S \to (2\,\psi_B)$;

```
Print["Inversion threshold voltage = ",
 V_Th /. Semiconductor /. Insulator /. dope /. phys, " V"]
```

```
<< Graphics`Graphics`
Plot[{V_G /. Semiconductor /. Insulator /. dope /. phys /. ψ_S → ψS},
  {ψS, (-.1 ψ_B /. Semiconductor /. dope /. phys),
   (2 ψ_B /. Semiconductor /. Insulator /. dope /. phys)},
  AxesLabel → {"ψ_S(V)", "V_G(V)"}, PlotLabel → "V_G(ψ_S)"];
```



## ▪ Capacitances

```
<< Calculus`DiracDelta`
```

$$C_{sc} = \text{Sign}[\psi_S]\ \frac{\epsilon_{Semi}\,\epsilon_o}{\sqrt{2}\ L_D}\ \frac{\left(1 - \text{Exp}[-\beta\,\psi_S] + \frac{n_i^2}{N_d^2}\ (\text{Exp}[\beta\,\psi_S] - 1)\right)}{\sqrt{(\text{Exp}[-\beta\,\psi_S] + \beta\,\psi_S - 1) + \frac{n_i^2}{N_d^2}\ (\text{Exp}[\beta\,\psi_S] - \beta\,\psi_S - 1)}};$$

```
(* F/cm^2, semiconductor cap *)
```

$$C_{Insu} = \frac{\epsilon_{Insu}\,\epsilon_o}{d_{Insu}};$$ (* Oxide cap *)

$$C_T = \frac{C_{Insu}\,C_{sc}}{C_{Insu} + C_{sc}};$$ (* total cap *)

$$C_{FB} = \frac{\epsilon_{Insu}\,\epsilon_o}{d_{Insu} + \frac{\epsilon_{Insu}}{\epsilon_{Semi}}\ L_D};$$ (* flat band cap *)

$$C_{schf} = \sqrt{\frac{q^2\,\epsilon_{Semi}\,\epsilon_o\,N_d}{2\,k\,T\,(2\beta\ \psi_B - 1 + \text{Log}[1.15\ (\psi_B\,\beta - 1)])}};$$ (* hf semiconductor cap *)

$$C_{Thf} = \frac{C_{Insu}\,C_{schf}}{C_{Insu} + C_{schf}};$$

$$V_o = \frac{q\,\epsilon_{Semi}\,\epsilon_o\,N_d}{C_{Insu}^2};$$

$$C_{scdd} = \frac{C_{Insu}}{\sqrt{1 + 2\ \frac{-(V_G - V_{FB})}{V_o}} - 1};$$ (* deep depletion semiconductor cap *)

$$C_{Tdd} = \frac{C_{Insu}\,C_{scdd}}{C_{Insu} + C_{scdd}};$$

$$W_m = \sqrt{\frac{2\,\epsilon_{Semi}\,\epsilon_o\,(2\,\psi_B)}{q\,N_d}};$$ (* cm, maximum depletion width *)

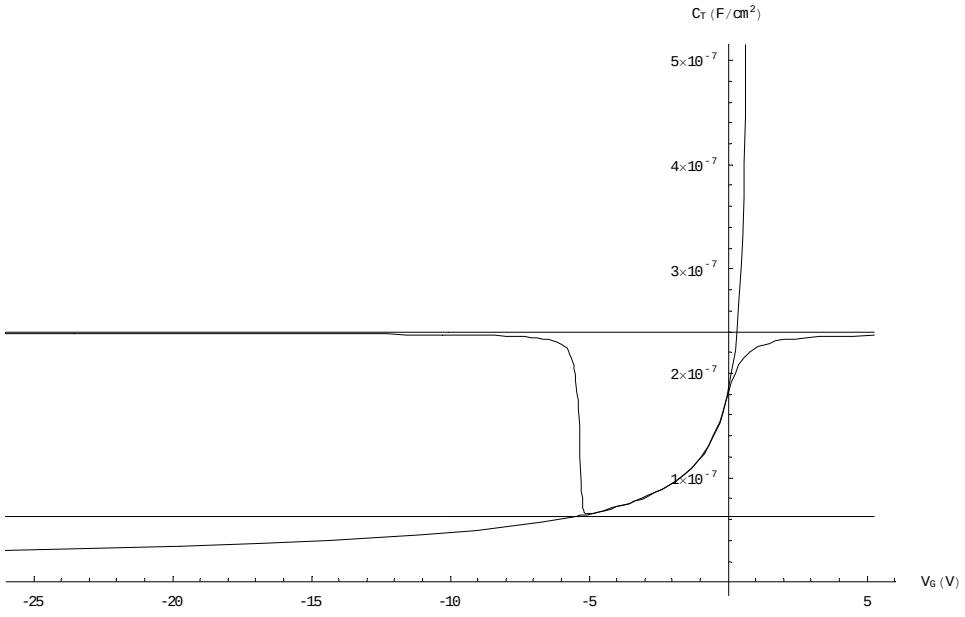
$$C_{min} = \frac{\epsilon_{Insu}\,\epsilon_o}{d_{Insu} + \frac{\epsilon_{Insu}}{\epsilon_{Semi}}\ W_m};$$

```
(* minimum capacitance by maximum dep width *)
```

```
Print["Flatband capacitance = ",
  C_FB /. Semiconductor /. dope /. Insulator /. phys, " F/cm^2"];
Print["Maximum depletion width = ", W_m /. Semiconductor /. phys /. dope,
  " cm"];
Print["Minimum capacitiance = ",
  C_min /. Semiconductor /. dope /. Insulator /. phys, " F/cm^2"];
Print["High-freq capacitiance = ",
  C_Thf /. Semiconductor /. dope /. Insulator /. phys, " F/cm^2"];
Print["Deep-Depl capacitiance = ",
  C_min /. Semiconductor /. dope /. Insulator /. phys, " F/cm^2"];
```

- **Plot the curves and save them in a file**

```
A = ParametricPlot[
    {{{V_G, C_T} /. Semiconductor /. Insulator /. dope /. phys /. ψ_S → phs},
     {{V_G, C_Insu} /. Semiconductor /. Insulator /. dope /. phys /. ψ_S → phs},
     {{V_G, C_Tdd} /. Semiconductor /. Insulator /. dope /. phys /. ψ_S → phs},
     {{V_G, C_Thf} /. Semiconductor /. Insulator /. dope /. phys /. ψ_S → phs}},
    {phs, (-.1 ψ_B /. Semiconductor /. dope /. phys),
     (2.2 ψ_B /. Semiconductor /. dope /. phys)},
    AxesLabel → {"V_G(V)", "C_T(F/cm^2)"}];
```



```
Vlist = {};
(* Remember to chang the range of phs according to previous setting *)
For[phs = (-.1 ψB /. Semiconductor /. dope /. phys),
  phs < (2.2 ψB /. Semiconductor /. dope /. Insulator /. phys),
  phs = phs + 0.01,
  AppendTo[Vlist, VG /. Semiconductor /. dope /. Insulator /. phys /.
    ψS → phs]];
MatrixForm[Vlist];

Clist1 = {}; (* Quasi CV *)
For[phs = (-.1 ψB /. Semiconductor /. dope /. phys),
 phs < (2.2 ψB /. Semiconductor /. dope /. Insulator /. phys),
 phs = phs + 0.01,
 AppendTo[Clist1, CT /. Semiconductor /. dope /. Insulator /. phys /.
   ψS → phs]];
MatrixForm[Clist1];

Clist2 = {}; (* Deep depletion CV *)
For[phs = (-.1 ψB /. Semiconductor /. dope /. phys),
 phs < (2.2 ψB /. Semiconductor /. dope /. Insulator /. phys),
 phs = phs + 0.01,
 AppendTo[Clist2, CTdd /. Semiconductor /. dope /. Insulator /. phys /.
   ψS → phs]];
MatrixForm[Clist2];

Clist3 = {}; (* High-freq CV *)
For[phs = (-.1 ψB /. Semiconductor /. dope /. phys),
 phs < (2.2 ψB /. Semiconductor /. dope /. Insulator /. phys),
 phs = phs + 0.01,
 AppendTo[Clist3, CThf /. Semiconductor /. dope /. Insulator /. phys /.
   ψS → phs]];
MatrixForm[Clist3];

Whole = {Vlist, Clist1, Clist2, Clist3};
file = OpenWrite["a2", PageWidth -> 140];
Write[file, Transpose[Whole]];
Close[file];
```

# APPENDIX C

# Process Flow of High Voltage GaN HEMTs

## 1. Ohmic contacts (mask: S/D)

1. Solvent clean: 3 min ultrasonic in ACE; 3 min ultrasonic in ISO; DI water rinse.
2. 120 $^{o}$C oven bake 5 min.
3. Spin OCG 825 at 6 k rpm for 30 s; 95 $^{o}$C hotplate bake 1 min. Thickness = 1 μm.
4. Spin 950 at 4 k rpm for 30 s; 90 $^{o}$C hotplate bake 1 min. Thickness = 0.7 μm.
5. Spin 365 at 4 k rpm for 30 s.
6. Expose in stepper for 1.8 s. 100 $^{o}$C hotplate bake 2 min.
7. DI water rinse 30 s; develop in MF 701:$H_2O$ = 3:1 for 1 min; DI water rinse.
8. Dry etch in RIE # 5: Press. = 10 mT, $Cl_2$ flow = 5 sccm, P = 100 W, etch rate = 10 Å/s. Etch until the thickness of the remaining AlGaN layer is 150 Å.
9. Clean: dip in HCl:$H_2O$ = 8:1 for 20 s; DI water rinse.
10. E-beam evaporate Ti/Al/Ni/Au = 220/1600/550/450 Å. Lift off and solvent clean.
11. RTA anneal at 870 $^{o}$C for 30 s.

## 2. Mesa definition (mask: Mesa)

12. Solvent clean: 3 min ultrasonic in ACE; 3 min ultrasonic in ISO; DI water rinse.
13. 120 $^{o}$C oven bake 5 min.
14. Spin 950 at 4 k rpm for 30 s; 90 $^{o}$C hotplate bake 1 min. Thickness = 0.7 μm.
15. Expose in stepper for 2.5 s.
16. Develop in straight MF 701 for 2 min; DI water rinse.
17. Dry etch in RIE # 5: Press. = 10 mT, $Cl_2$ flow = 5 sccm, P = 200 W, etch rate = 20 Å/s. Etch 4000 Å.
18. Clean: dip in HCl:$H_2O$ = 8:1 for 20 s; DI water rinse.
19. E-beam evaporate $SiO_2$ = 4000 Å. Lift off and solvent clean.

## 3. Gate metalization (mask: Gate)

20. Solvent clean: 3 min ultrasonic in ACE; 3 min ultrasonic in ISO; DI water rinse.
21. Clean: dip in HCl:$H_2O$ = 8:1 for 20 s; DI water rinse.
22. Sputter SiN: Press = 2.7 mT, Ar/$N_2$ flow = 12/8 sccm, P = 200 W, deposition rate = 90 Å/min. Final SiN thickness is 120 Å.
23. 120 $^{o}$C oven bake 5 min.
24. Spin OCG 825 at 6 k rpm for 30 s; 95 $^{o}$C hotplate bake 1 min. Thickness = 1 μm.
25. Spin 950 at 4 k rpm for 30 s; 90 $^{o}$C hotplate bake 1 min. Thickness = 0.7 μm.
26. Spin 365 at 4 k rpm for 30 s.
27. Expose in stepper for 3.5 s. 100 $^{o}$C hotplate bake 2 min.
28. DI water rinse 30 s; develop in MF 701:$H_2O$ = 3:1 for 1 min; DI water rinse.

29. E-beam evaporate SiO2/Ni/Au/Ni = 50/200/4000/500 Å. Lift off and solvent clean.
30. Clean: dip in HCl:$H_2O$ = 8:1 for 20 s; DI water rinse.
31. Sputter SiN: Press = 2.7 mT, Ar/$N_2$ flow = 12/8 sccm, P = 200 W, deposition rate = 90 Å/min. Final SiN thickness is 2000 Å.

## 4. Bonding pad formation (mask: Pad)

32. 120 $^oC$ oven bake 5 min.
33. Spin OCG 825 at 800 rpm for 5 min; 90 $^oC$ oven bake 30 min. Thickness = 4 μm.
34. Spin 950 at 4 k rpm for 30 s; 90 $^oC$ hotplate bake 1 min. Thickness = 0.7 μm.
35. Spin 365 at 4 k rpm for 30 s.
36. Expose in stepper for 3 s. 100 $^oC$ hotplate bake 2 min.
37. DI water rinse 30 s; develop in MF 701:$H_2O$ = 3:1 for 1.5 min; DI water rinse.
38. Dry etch in PE-II A (descum machine): $CF_4$ flow = 300 sccm, P = 150 W, etch rate = 500 Å/min for SiN. Etch 5 min.
39. Clean: dip in HCl:$H_2O$ = 8:1 for 20 s; DI water rinse.
40. E-beam evaporate Ti/Au = 200 Å/3 μm. Lift off and solvent clean.

## 5. Dice

## 6. Wire bonding