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Oxide Aperture Heterojunction Bipolar Transistors

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by

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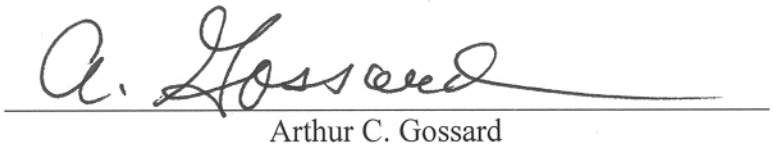

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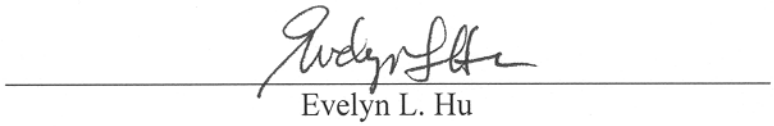

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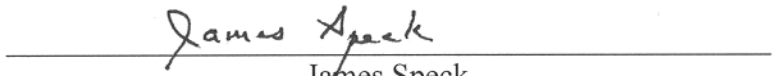

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Oxide Aperture Heterojunction Bipolar Transistors

Dedicated to

my parents,
who taught me how to be a student of life,

and to

my sister Catherine,
who taught me not to waste the gifts I was given

Acknowledgments

My time in graduate school at UCSB has been a true learning experience. The lessons that I have learned, both in and out of school, and the experiences I have collected will be with me always. I will always be indebted to Umesh Mishra for giving me the opportunity to be part of such an eclectic group of researchers, which granted me the benefit of being exposed to and part of a wide variety of research always on the cutting edge of technology, and for his guidance and support, which carried me through some of the more frustrating parts of my research. I'd also like to thank the remainder of my committee: Art Gossard who always gave a new and extraordinary view to the problem, Evelyn Hu whose insightful suggestions concerning oxidation and processing were of great benefit, and Jim Speck for his support and general interest in oxides and their applications.

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Abstract

Oxide Aperture Heterojunction Bipolar Transistors

by
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The increasing demand in communication and radar technology for higher bit-rates and increased frequency resolution is eventually reflected in the requirement of devices being capable of operating at higher and higher frequencies. Currently, the greatest limitations on heterojunction bipolar transistor (HBT) speed are the extrinsic or parasitic components of the device, most notably the extrinsic base-collector capacitance. Various techniques and technologies have been employed to reduce the extrinsic base-collector capacitance in order to increase the frequency performance of the HBT: selective regrowth techniques, sidewall-contacted bases, undercut collectors, implanted emitters, and the transferred substrate technology. The oxide aperture HBT represents an alternative method to achieving a high frequency transistor.

Concerns relating to the growth of arsenide-antimonide materials for transistor applications, the effect of an oxide on junction characteristics, and the high frequency performance of the oxide aperture HBT have been addressed. The placement of the oxide aperture, formed from the wet oxidation of $AlAs_{0.56}Sb_{0.44}$, was found to have a strong impact on the current-voltage characteristics of the base-emitter *pn* junction. Oxide apertures placed too close to the *pn* junction resulted in recombination

dominated characteristics; oxide apertures placed far from the *pn* junction resulted in poor channeling of the injected carriers, reducing the effectiveness of the aperture. Only oxide apertures placed within a critical range with respect to the *pn* junction, determined by material structure and doping, resulted in near ideal characteristics.

Investigation into the high frequency performance of the oxide aperture HBT showed that a parasitic base-emitter capacitance, inherent to the collector-up design adopted for the oxide aperture HBT, in conjunction with the relatively high emitter resistance of the oxide aperture HBT, due to the low mobility of electrons in the $AlAs_{0.56}Sb_{0.44}$ emitter, resulted in an additional delay term in and thereby reduction of the current-gain cutoff frequency (f_τ). The added delay term was unexpectedly shown not to impact the maximum frequency of oscillation (f_{max}). Oxide aperture HBTs with an f_τ of 8 ~ 10 GHz and an f_{max} of 12 ~ 17 GHz, with a maximum measured f_{max} of 17.76 GHz, were demonstrated.

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CHAPTER 1

Introduction

The ever-growing demand in communication and radar technology for increased bit-rates and frequency resolution requires systems capable of providing increased bandwidth and clock rates.[1,2] This demand is eventually reflected in the requirement that the devices, which are the building blocks of these systems, must be capable of operating at higher and higher frequencies (Figure 1.1).[3-6]

For example, integrated circuits for optical fiber communications that are capable

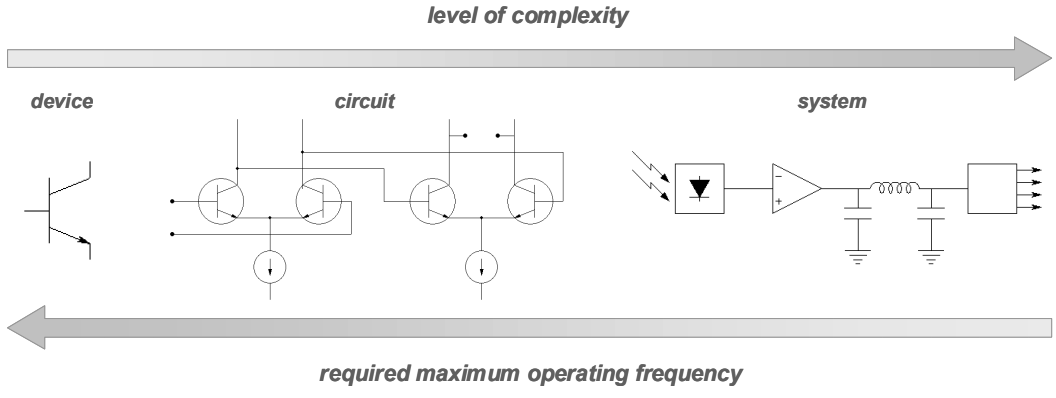

Figure 1.1 Relationships between device, circuit, and systems.

of providing transmissions at 40 Gb/s are currently in development. The eventual emergence of higher bit-rate systems (i.e., 160 Gb/s) will require amplifiers with larger bandwidths (i.e., ~100 GHz). High bandwidth military radar and communication systems require analog-digital converters (ADCs), digital-analog converters (DACs), and direct-digital frequency synthesizers (DDFSs) with very high frequency resolution. This demands devices that can operate well over 100 times the signal bandwidth of the system.[2]

1.1 Motivation for Oxide Aperture HBTs

Two measures or figures-of-merit useful in evaluating the high frequency performance of a transistor are the current-gain cutoff frequency, f_τ, and maximum frequency of oscillation, f_{max}. f_τ is defined as the frequency at which the short-circuit current gain goes to unity. f_{max} is defined as the frequency at which the power gain goes to unity. Though finally dependent on the application, transistors with increased f_τ and f_{max} must be realized in order to meet the demand in bandwidth of the next generation of systems.

Roughly speaking, f_τ corresponds to the transit time of carriers through the device. For a heterojunction bipolar transistor (HBT), f_τ is written as:

$$f_\tau = \frac{1}{2\pi\left(\tau_E + \tau_B + \tau_C + \tau_{CC}\right)} \tag{1.1}$$

where τ_E and τ_{CC} are time constants related to the charging and discharging of the device and τ_B and τ_C are transit times through the device. In order to increase f_τ in bipolar transistors, the relative time constants/transit times must be reduced. Without going into detail, this entails scaling the device vertically to decrease the distances across which the carriers transit. With the advent of precise growth techniques, like molecular beam epitaxy (MBE), which allow for the control of device layer thicknesses down to the atomic scale, vertical or epitaxial scaling is easily achieved, and transistors with f_τ on the order of a few hundred gigahertz are possible.[7,8]

On the other hand, f_{max}, which is related to f_τ, is strongly dependent upon the magnitude of the base resistance (R_B) and base-collector capacitance (C_{BC}) time constant:

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi R_B C_{BC}}} \tag{1.2}$$

f_{max} is increased by reducing R_B and C_{BC} chiefly through increased doping in the base and horizontal or lithographic scaling. State-of-the-art conventional emitter-up

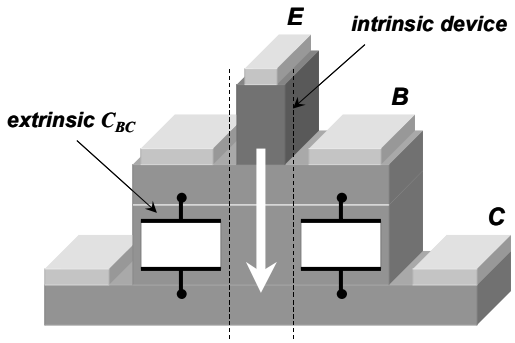

Figure 1.2 Illustration of the extrinsic base-collector capacitance present in a conventional emitter-up HBT.

transistors with ~0.4 μm wide emitters demonstrate f_{max} of up to 300 GHz.[8] But commonly, conventional emitter-up transistors are still limited by the extrinsic base-collector capacitance underneath the base contacts (Figure 1.2). In contrast to the extrinsic (commonly referred to as "parasitic") base resistance that carries current between the base contacts and the intrinsic device, the extrinsic base-collector capacitance serves no purpose in the operation of the transistor and is truly "parasitic".

Various technologies and techniques that directly address the reduction of the extrinsic base-collector capacitance (C_{BC}) with the purpose of increasing f_{max} have been examined: emitter-up transistors with regrown base-emitter junction,[9] sidewall contacted bases,[10] or undercut collectors;[11] collector-up transistors with regrown base-collector junction or implanted extrinsic emitters;[12,13] and the transferred substrate HBT (Figure 1.3).[14] The oxide aperture HBT offers an alternative method to reducing C_{BC} while maintaining a high gain device.

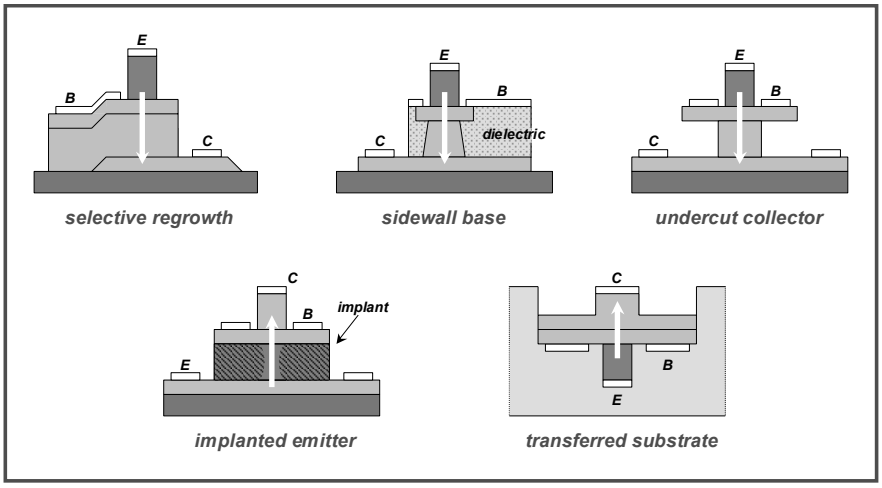

Figure 1.3 Various methods used to reduce the base-collector capacitance of a HBT.

1.2 The Oxide Aperture HBT

The oxide aperture HBT reduces the base-collector capacitance (C_{BC}) simply by reducing the area of the base-collector junction (referred to as the collector area, A_C). To reduce the collector area the device is "flipped" from the standard emitter-up into a collector-up configuration. This allows the collector area to be reduced through straightforward processing (Figure 1.4a).

Simply flipping the device is not sufficient to produce a high-quality transistor. If we were to stop here, we would be left with a transistor in which the collector area (A_C) is much smaller than the emitter area (A_E). In such a device, the majority of the current injected into the base from the emitter would be collected at the base contacts

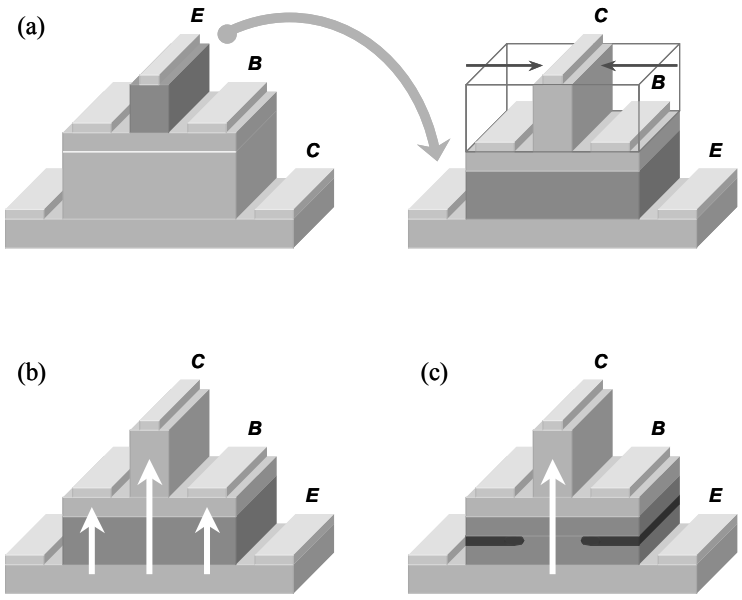

Figure 1.4 Illustration of the "development" of the oxide aperture HBT. (a) The emitter-up HBT is "flipped" and the collector area is reduced. (b) A simple collector-up device suffers from a greatly reduce current gain. (c) The oxide aperture HBT offers a device with a reduce base-collector capacitance while maintaining a high gain.

and not at the collector, resulting in a greatly reduced common-emitter current gain (β), possibly reduced below $\beta = 1$ (Figure 1.4b). In order to maintain a high gain device in a collector-up configuration, the current injected from the emitter must be channeled into the collector. In the oxide aperture HBT, this is achieved by means of an insulating oxide current aperture in the emitter. The end result is a collector-up transistor designed for high frequency operation by reducing C_{BC}, while maintaining the high-gain of an emitter-up transistor by means of an oxide current aperture (Figure 1.4c).

1.3 Synopsis of the Dissertation

This dissertation deals with the first work undertaken toward producing an RF compatible oxide aperture HBT. Chapter 2 presents a short history of oxides in semiconductors. The currently understood chemistry of the oxidation process as related to III-V semiconductors is presented, as well as various applications to opto-electronic and electronics devices. The chapter concludes with the only research to date on oxide aperture HBTs, begging the question, "What is the high frequency performance of these devices?"

Chapter 3 discusses the design and growth of the oxide aperture HBT. Issues regarding growth of transistors for high frequency operation, MBE growth of $GaAs_{0.49}Sb_{0.51}$ and $AlAs_{0.56}Sb_{0.44}$, and the oxidation of $AlAs_{0.56}Sb_{0.44}$ are examined. Concerns relating to achieving and maintaining lattice-matched compositions for

$GaAs_{0.49}Sb_{0.51}$, $AlAs_{0.56}Sb_{0.44}$, and $Al_xGa_{1-x}As_ySb_{1-y}$ and the *n*-type doping of arsenide-anitmonides by tellurium, as opposed to silicon, are discussed.

The design of the base-emitter junction as related to the oxide aperture HBT, referred to as the oxide aperture diode, is presented in Chapter 4. The effect of the "placement" of the oxide aperture within the device on the current-voltage characteristics of the diode is investigated. Current scaling with relation to diode and aperture size and the ideality of the conduction mechanism is examined. "Selection rules" or guidelines concerning the appropriate design of the base-emitter junction for the oxide aperture HBT are discussed.

In Chapter 5, work on the development of a high frequency oxide aperture HBT is examined. A final generation of transistors, designed and fabricated with improvements based on the results of previous generations, is analyzed. The high frequency performance of these devices is evaluated, and additional issues that arise as a result of the collector-up design and oxide aperture, such as a parasitic capacitance in the base-emitter junction, are discussed.

Conclusions and suggested future work concerning material selection, device design, and device processing are presented in Chapter 6.

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CHAPTER 2

Oxides and Oxide Technology

2.1 Introduction

Given that this dissertation is not concerned with the specifics of the $AlAs_{0.56}Sb_{0.44}$ wet oxidation reaction and the material aspects of the resultant oxide, other than its insulating nature, an overview of oxides and associated technologies was deemed fitting. Therefore, the following sections present a summary of oxides: their beginnings, applications, and some of the more salient issues related to the work presented in this dissertation.

2.2 The First Oxide: Silicon Dioxide

An oxide was employed as an integral element of an electronic device for the first time in 1960, when Kahng and Atalla proposed and fabricated the first metal-oxide-semiconductor field-effect transistor (MOSFET) using thermally oxidized silicon as the gate oxide (Figure 2.1).[1] The native oxide of silicon, silicon dioxide (SiO_2), has

since been employed in innumerable fashions in the silicon electronics industry, from

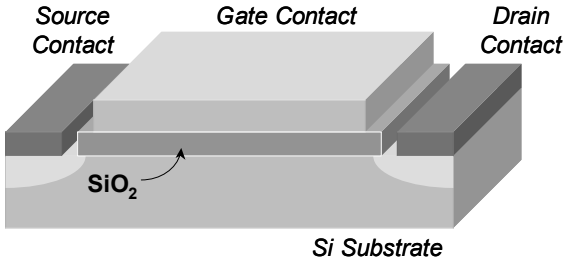

Figure 2.1 Illustration of a Si MOSFET.

gate insulators to device passivation, from device isolation to doping diffusion masks (Figure 2.2). The means by which silicon dioxide has been produced are as widely varied.[2,3] The result is an integrated circuit technology that has generated multibillion-dollar markets.

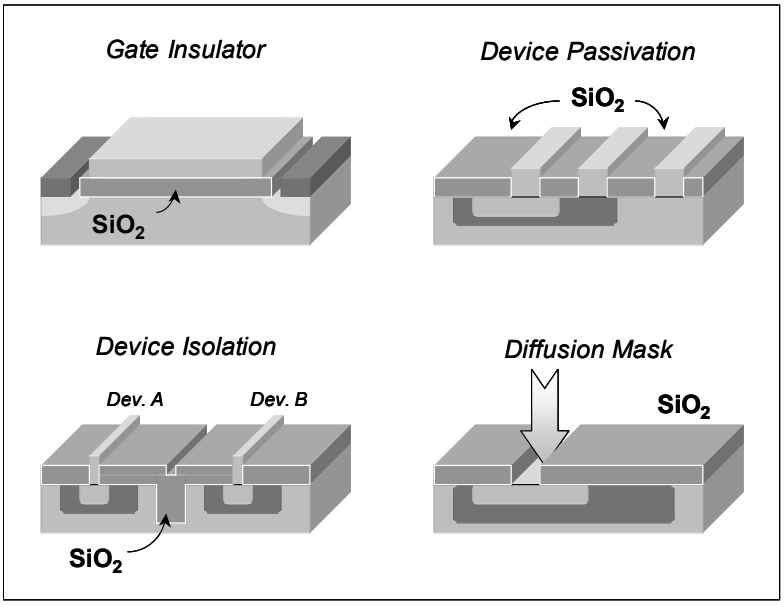

Figure 2.2 Various applications for silicon dioxide (SiO_2)

Similar techniques have been attempted with GaAs to achieve a native oxide with similar properties to SiO_2 (e.g., high density, low interface state density, mechanically

stable, insulating),[2] but the results have been disappointing.[3-5] Not until the past decade has any progress been made into developing oxides for III-V semiconductor materials.[4-21]

2.3 History of III-V Oxides

Most of the initial work on III-V oxides was centered on the native oxides of GaAs.[3,22] The resultant oxide films invariably consisted of a nonstoichiometric combination of gallium oxide (Ga_2O_3), arsenic oxide (As_2O_3), and arsenic, and tended to be mechanically and chemically unstable, in addition to being poor electrical insulators.[3-5] Deposited oxides or dielectrics have proved to be useful as passivation films, diffusion masks, or simply as physical protection for III-V semiconductors, but due to their usually high interface state densities, deposited oxides have shown to be useless for electronic applications.[23,24] It wasn't until the work of Dallesasse *et al.*[5,6] that the hope of having a stable oxide for use in the III-V materials system was renewed.

Though the first reported work on the wet oxidation of $Al_xGa_{1-x}As$ compounds was in 1979, when a native oxide of AlAs was formed at a very low oxidation temperature of 100 °C,[25] it wasn't until 1990 when Dallesasse discovered that the wet oxidation of AlAs at temperatures above ~300 °C resulted in a mechanically robust form of the native oxide of AlAs.[5] Since that time much work and research has gone into the wet oxidation of $Al_xGa_{1-x}As$ and its resultant oxide, Al_2O_3.[6-18,26-29] Applications for the oxide have been found in all aspects of electronics and opto-

electronics; ranging from gate insulators[19,30] to insulating backgates and buffers,[10,17] from low index waveguides and current apertures[15,29,31] to mirrors and lenses.[9,13,20]

Ashby *et al.* have proposed the following chemical reactions for the formation of Al_2O_3 from AlAs by wet oxidation:[32]

$$2\ AlAs + 6\ H_2O(g) \rightarrow Al_2O_3 + As_2O_3(l) + 6\ H_2 \qquad \Delta G^{698} = -473\ \text{kJ/mol} \tag{2.1}$$

$$As_2O_3(l) + 3\ H_2 \rightarrow 2\ As + 3\ H_2O(g) \qquad \Delta G^{698} = -131\ \text{kJ/mol} \tag{2.2}$$

$$As_2O_3(l) + 6\ H \rightarrow 2\ As + 3\ H_2O(g) \qquad \Delta G^{698} = -1226\ \text{kJ/mol} \tag{2.3}$$

It should be noted that the values presented here for the Gibb's free energy, ΔG, are for reactions carried out at a temperature of 400 °C (698 K). The negative values for ΔG indicate that these reactions are spontaneous at the given temperature; in other words, they will occur without additional energy being introduced into the system.

Replacing AlAs with GaAs in Equation (2.1) results in a $\Delta G^{698} = +10$ kJ/mol for that reaction.[4] This suggests that exchanging Al for Ga, as in $Al_xGa_{1-x}As$, would make the reaction in Equation (2.1) less favorable, retarding the wet oxidation reaction as the Ga content increases (Figure 2.3). Work by Choquette *et al.*,[4] as well as others,[13,15,29] supports this proposal (Figure 2.4).

In addition to the composition of the oxidizing layer, Naone *et al.* found that the wet oxidation reaction of $Al_xGa_{1-x}As$ was dependent upon the thickness of the

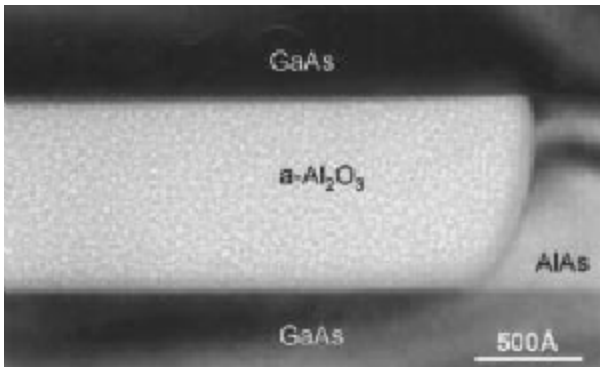

Figure 2.3 From Choquette *et al.*.[4] Cross-sectional TEM image of an oxidized layer converted from a 100 nm thick AlAs layer surrounded by layers of GaAs demonstrating the selective oxidation of AlAs over GaAs.

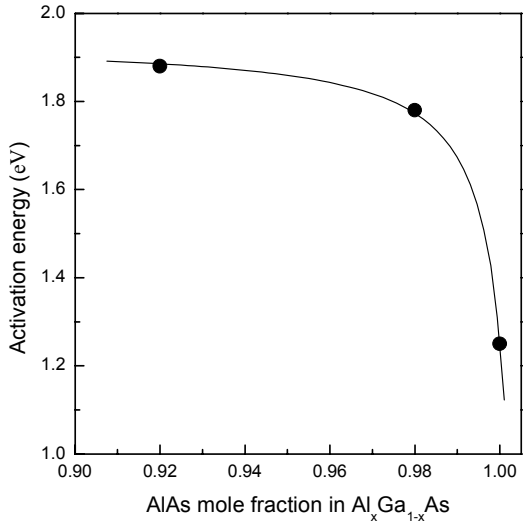

Figure 2.4 After Choquette *et al.*.[4] Arrhenius activation energy for the oxidation reaction of $Al_xGa_{1-x}As$ versus Al composition.

oxidizing layer. In short, it was proposed that the interfacial energies between the relevant materials (i.e., GaAs, AlAs, and Al_2O_3) produced a "drag" on the oxidation front. As a result of the balancing of these energies, this drag increased as the AlAs

layer thickness decreased, increasing the activation energy of the reaction and reducing the oxidation rate (Figure 2.5). It was also proposed that varying the composition of the layers cladding the oxidation layer would modify the oxidation reaction, due to an alteration to the interfacial energy balance.[16] Further work by Naone *et al.*,[15,29] as well as others,[9,13] supports this statement.

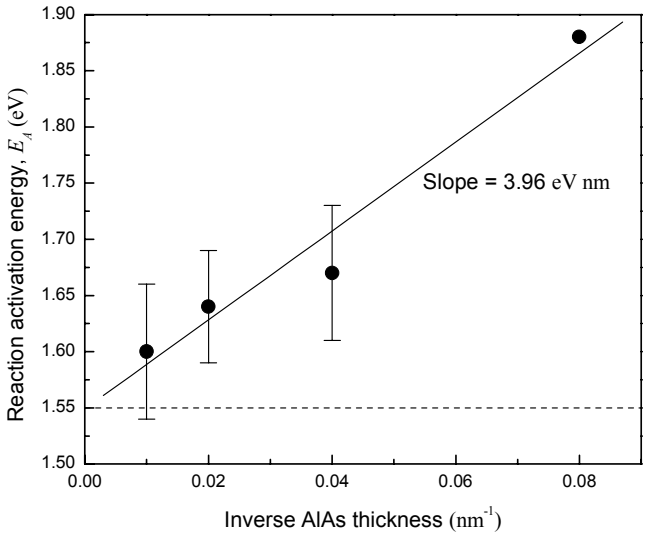

Figure 2.5 After Naone *et al.*.[16] The activation energies of the linear rate coefficient, k_l, as a function of 1/thickness.

In contrast to the work seen with the oxidation of $Al_xGa_{1-x}As$, the oxide formed from the wet oxidation of $AlAs_{0.56}Sb_{0.44}$ has seen little use.[33,34] This is primarily due to the formation of a thin "float layer" of antimony metal (a mixture of amorphous and crystalline antimony) at the interface between the oxide and semiconductor during oxidation (Figure 2.6).[35,36] This metallic antimony layer tends to be highly conductive, generally resulting in electrical shorts in devices that partially or completely degrade the electronic performance of devices.[33] Nonetheless, in at least

one case these antimony layers have been used in a beneficial manner to reduce the extrinsic base resistance seen in a collector-up HBT.[34]

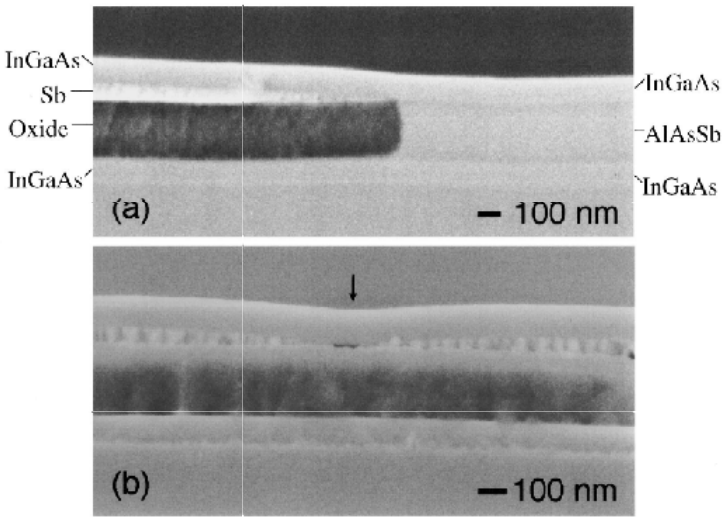

Figure 2.6 From Blum *et al.*.[35] Cross-sectional scanning electron micrograph of oxidized InGaAs/AlAsSb/InGaAs structure. (a) partially oxidized layer and (b) fully oxidized layer.

The most extensive study done on the wet oxidation of $AlAs_{0.56}Sb_{0.44}$ to date was by Mathis *et al.*.[36] The lateral oxidation kinetics of $AlAs_{0.56}Sb_{0.44}$ and $Al_xGa_{1-x}As_ySb_{1-y}$ (lattice-matched to InP) were found to be similar to $Al_xGa_{1-x}As$ in terms of temperature, thickness, and composition dependence, with a few noteworthy exceptions.

In addition to the formation of an antimony float layer, it was found that this float layer lagged behind the oxidation front, and that the amount of lag increased with increasing oxidation temperature (Figure 2.7). At temperatures higher than 450 °C, $AlAs_{0.56}Sb_{0.44}$ experiences self-limiting oxidation and the apparent diffusion constant approaches zero. It was proposed that this self-limiting oxidation is a result of a

physical change of the reaction layer at the oxidation front that is due to an increased solubility of antimony in Al_2O_3. At higher temperatures antimony may be increasingly incorporated into the oxidation layer, given that the antimony mobility is small compared to the rate of mass transport through the reaction layer. The result of this can be seen in the increasing lag distance for the antimony float layer at higher

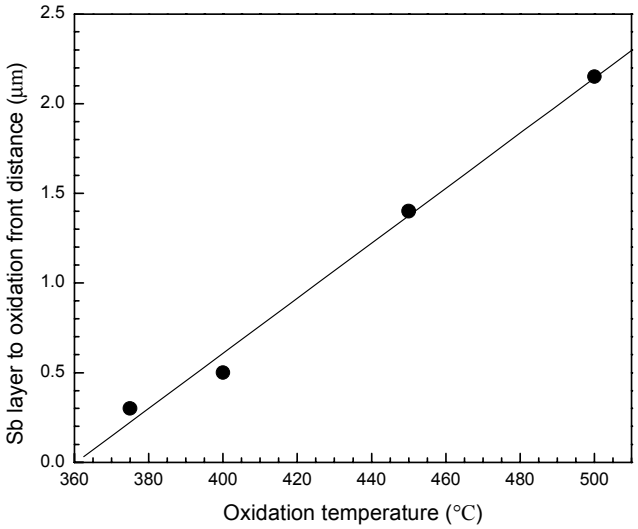

Figure 2.7 After Mathis *et al.*.[36] Distance from oxidation front to antimony segregation layer, measured by cross-sectional SEM, as a function of oxidation temperature after oxidation for 30 min. The antimony segregation layer lags the oxidation front for each sample, and increases to a maximum measured distance of 2.2 μm at 500 °C.

temperatures (Figure 2.7). Increased incorporation of oxidized antimony into the reaction layer prevents further diffusion of reactants, resulting in the oxidation slowing until lateral oxidation is no longer measurable.[36]

2.4 The First Oxide Aperture Devices: Laser Diodes

The first devices that used the native oxide formed from the wet oxidation of $Al_xGa_{1-x}As$ were planar edge-emitting laser diodes,[37,38] where the oxide layers were used for index guiding[39] and as current apertures (Figure 2.8).[40]

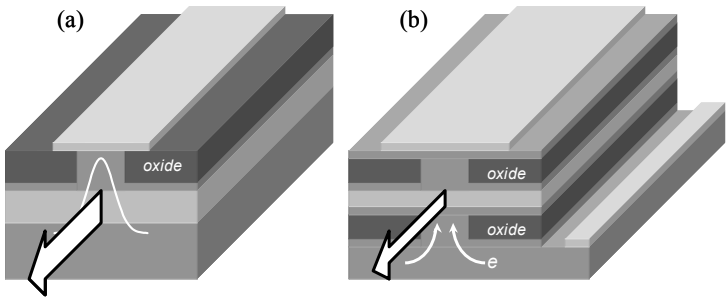

Figure 2.8 (a) Example of a planar laser diode with oxide for index guiding. (b) Example of a planar laser diode with oxide as a current aperture.

Vertical-cavity surface-emitting lasers (VCSELs) that incorporate buried oxide apertures for electrical and optical confinement have shown dramatic increases in performance. VCSELs have used oxide apertures underneath dielectric distributed Bragg reflectors, significantly reducing their threshold current.[41] Monolithic VCSELs have exploited the oxidation selectivity of the low refractive index $Al_xGa_{1-x}As$ layers within a semiconductor distributed Bragg reflector to form one or more oxide apertures.[42,43] VCSELs of this form have demonstrated the lowest threshold current[44] and voltage,[42] in addition to record high power conversion efficiencies.[45] Moreover, the relative refractive index of the oxidized regions is ~1.6, reduced from that of the original $Al_xGa_{1-x}As$ (~3.0),[39] resulting in index guiding optical confinement, evident by the emission characteristics[46] and reduced threshold

currents.[41,44] The low index oxide has also been utilized in high index contrast mirrors consisting of GaAs-Al_2O_3 layers.[47]

2.5 Oxide Aperture HBTs: High-Speed Devices?

To date, only two groups have produced HBTs using a native oxide as a current aperture. The first was Massengale *et al.*, who fabricated an Npn collector-up $Al_xGa_{1-x}As$/GaAs HBT using oxidized AlAs as a current aperture in the emitter (Figure 2.9). Devices displayed current gains on the order of 35~50, with current densities up to 10^5 A/cm^2.[12]

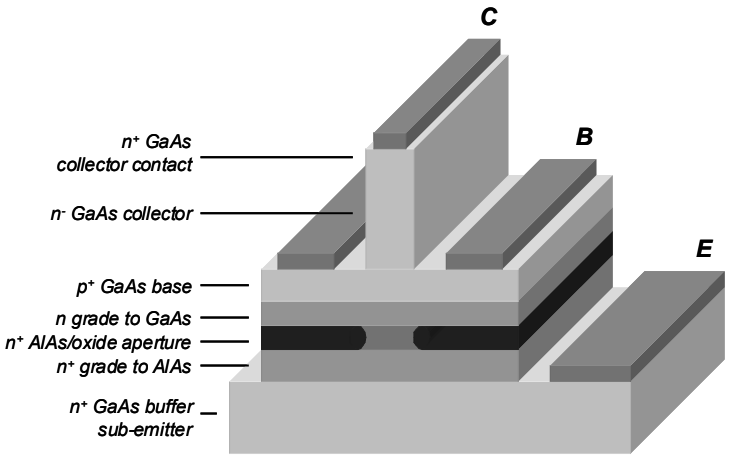

Figure 2.9 Illustration of the collector-up AlGaAs/GaAs HBT presented by Massengale *et al.*.[12]

The only other work with HBTs having a native oxide current aperture was by Lear *et al.*. A Pnp collector-up HBT in the InP lattice-matched material system was fabricated using the native oxide of $AlAs_{0.56}Sb_{0.44}$ as the current aperture in the emitter. The result was devices with current gains of approximately 20~30 at current densities of 10^4 A/cm^2. A reduced extrinsic base resistance was also observed, due to

the formation during oxidation of a highly conductive float layer of antimony directly below the base.[34]

In both cases, the claimed motivation behind fabricating such a device is the reduction of the base-collector capacitance commonly associated with mesa structure HBTs,[34] with the ultimate goal of improved frequency performance.[12,48] But in neither case were anything but DC results reported, leaving the high-speed performance of such devices in question.

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CHAPTER 3

Transistor Design and Growth

3.1 Introduction

Materials such as $In_{0.53}Ga_{0.47}As$, $Al_{0.48}In_{0.52}As$, and their alloys, which are lattice-matched to InP (Figure 3.1), are desirable for high-speed and low power applications

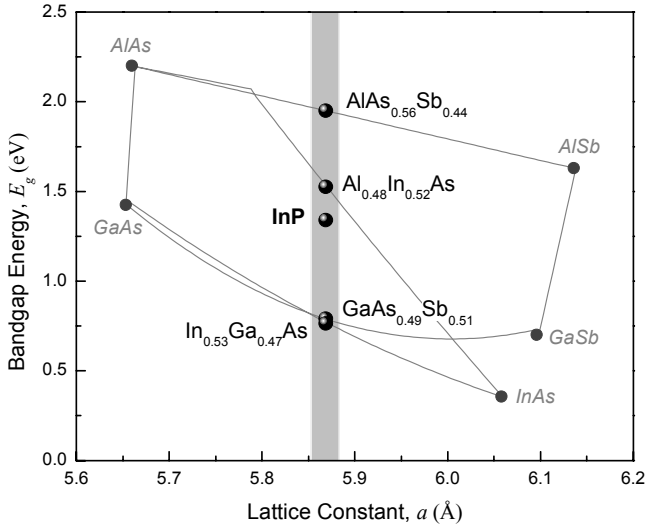

Figure 3.1 Bandgap versus lattice constant for various III-V semiconductors. The shaded region contains materials lattice-matched to InP.

due to, for example, the high electron saturation velocity ($v_{sat,InGaAs} \approx 1 \times 10^7$ cm/sec),[1] high mobility ($\mu_{n,InGaAs} \approx 15{,}000$ cm^2/Vsec),[2] and low bandgap ($E_{g,InGaAs} \approx 0.77$ eV)[3] of $In_{0.53}Ga_{0.47}As$, and the ability to produce heterostructures with $Al_{0.48}In_{0.52}As$ ($\Delta E_c = 0.50$ eV, $\Delta E_v = 0.22$ eV).[4] The applications of such materials have been varied and numerous,[5-14] but the antimony-based materials lattice-matched to InP (i.e., $GaAs_{0.49}Sb_{0.51}$, $AlAs_{0.56}Sb_{0.44}$, and their

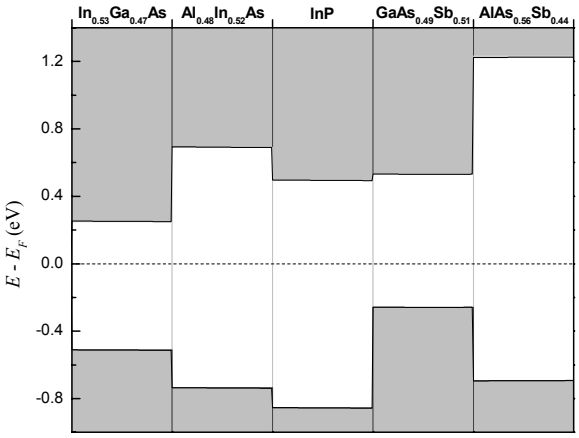

Figure 3.2 Band diagram showing the relative bandgaps and band line-ups for InGaAs, AlInAs, GaAsSb, AlAsSb, and InP.

alloys) have been overlooked until recently as candidates for use in electronic and opto-electronic devices. The benefits of the antimony-based materials, such as larger band offsets ($\Delta E_c \approx 0.62$ eV, $\Delta E_v \approx 0.46$ eV),[15-17] larger bandgap material ($E_{g,AlAsSb} \approx 1.92$ eV),[18] larger index of refraction difference ($\Delta n_r \approx 0.5$),[19] and a material that readily oxidizes ($AlAs_{0.56}Sb_{0.44}$),[20-22] have only of late been seen in electronic and opto-electronic applications.[22-32] Table 3.1 shows some material parameters of $In_{0.53}Ga_{0.47}As$, $Al_{0.48}In_{0.52}As$, $GaAs_{0.49}Sb_{0.51}$, $AlAs_{0.56}Sb_{0.44}$, and InP.

	InP	$In_{0.53}Ga_{0.47}As$	$Al_{0.48}In_{0.52}As$	$GaAs_{0.49}Sb_{0.51}$	$AlAs_{0.56}Sb_{0.44}$
Bandgap Energy, E_g (eV)	1.34 [3]	0.77 [3]	1.5 [3]	0.72 [17]	1.92 [18]
ΔE_c relative to InP (meV)	-	-250 [4]	250 [4]	120 - 180 [16,17]	740 [33]
ΔE_v relative to InP (meV)	-	350 [4]	130 [4]	620 - 810 [16,17]	160 [15]
μ_n (cm^2/Vsec)	4000 [34]	~15,000 [2]	~ 4,000 [1]		~ 50
μ_p (cm^2/Vsec)	100 [34]	≤ 300 [2]		~ 35	
v_{sat} (cm/sec)		1×10^7 [1]	$2.5 - 4 \times 10^6$ [1]		

Table 3.1 Material properties of InP, InGaAs, AlInAs, GaAsSb, and AlAsSb.

3.2 Transistor Design: High Frequency Issues

Given that the goal of this dissertation is the fabrication of a high-speed heterojunction bipolar transistor (HBT) and validation of the oxide aperture HBT design, it is important to understand how material structure and device layout can affect the frequency performance of a device. For HBTs, there are two figures-of-merit that relate various device aspects, which are dependent upon material selection and device layout, to the frequency performance of the transistor: the current-gain cutoff frequency, f_τ, and the maximum frequency of oscillation, f_{max}.

Figure 3.3 gives a classical example of a transistor's common-emitter current gain (β) as a function of operating frequency. f_τ is defined as the frequency at which β drops to unity, Equation (3.1).

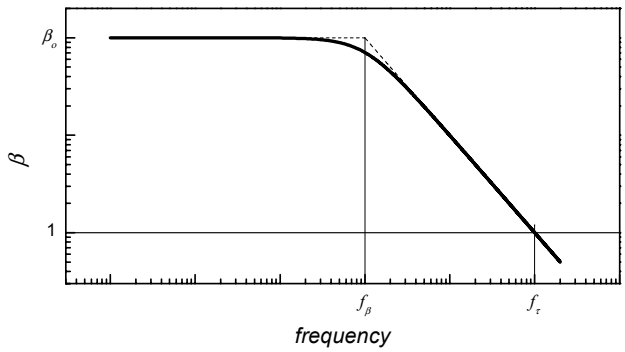

Figure 3.3 Bode plot of common-emitter current gain (β) versus frequency. f_τ indicates the frequency at which $\beta = 1$. $f_\beta = f_\tau/\beta_o$ indicates the 3 dB "rolloff" frequency.

$$f_\tau = \frac{1}{2\pi}\left(\tau_E + \tau_B + \tau_C + \tau_{CC}\right)^{-1} \tag{3.1}$$

$$\begin{aligned} \tau_E &= \frac{\eta kT}{qI_E}\left(C_{BE} + C_{BC}\right) \simeq \frac{\eta V_T}{I_C}\left(C_{BE} + C_{BC}\right) \\ \tau_B &= \frac{W_B^{\,2}}{2D_n} \\ \tau_C &= \frac{W_C}{2v_{sat}} \\ \tau_{CC} &\simeq \left(R_E + R_C\right)C_{BC} \end{aligned} \tag{3.2}$$

τ_E is the emitter-charging time associated with charging the base-emitter junction capacitance (C_{BE}) and the base-collector junction capacitance (C_{BC}) through the base-emitter junction's dynamic resistance ($r_E = \eta V_T / I_E$); τ_B is the base transit time; τ_C is the collector transit time; and τ_{CC} is the collector-charging time associated with charging the C_{BC} through the transistor's emitter and collector resistances, R_E and R_C respectively. $V_T = kT/q$ is the thermal voltage, where k is Boltzmann's constant (8.62×10^{-5} eV/K), T is the absolute temperature of the semiconductor in Kelvin, and

q is the electronic charge (1.602×10^{-19} C); I_E and I_C are the emitter and collector currents, respectively; W_B is the width of the neutral base layer; D_n is the electron diffusion constant in the neutral base; W_C is the width of the depleted collector; and v_{sat} is the saturation velocity of electrons in the depleted collector.

A more straightforward understanding of f_τ may be achieved by examining the roles of the various time constants. As stated previously, τ_E and τ_{CC} are RC charging times associated with the base-emitter and base-collector junctions. These charging times represent the time that the junctions require to adjust the potential in the base, under given bias conditions (e.g., I_C, V_{CE}), in response to a variation in the input current. τ_B and τ_C are carrier transit times through the neutral base and depleted collector, respectively. Together, ($\tau_B + \tau_C$) represents the time it takes for a charge carrier, once ejected from the emitter, to be imaged or "collected" at the collector contact. Therefore, f_τ may be thought of representing the total time that the transistor requires to respond to a variation in its input and collect the resultant transited carrier. Figure 3.4 illustrates the various aspects of a HBT and their relations to f_τ, as presented in Equations (3.1)-(3.2).

A transistor is said to be "unilateral" when no feedback path exists from the output and to the input of the device. In practice, some amount of feedback always exists, but this can commonly be removed through the use of a lossless feedback network that cancels the innate feedback of the device. The unilateral power gain is the maximum power gain achievable by the transistor. f_{max} is defined as the

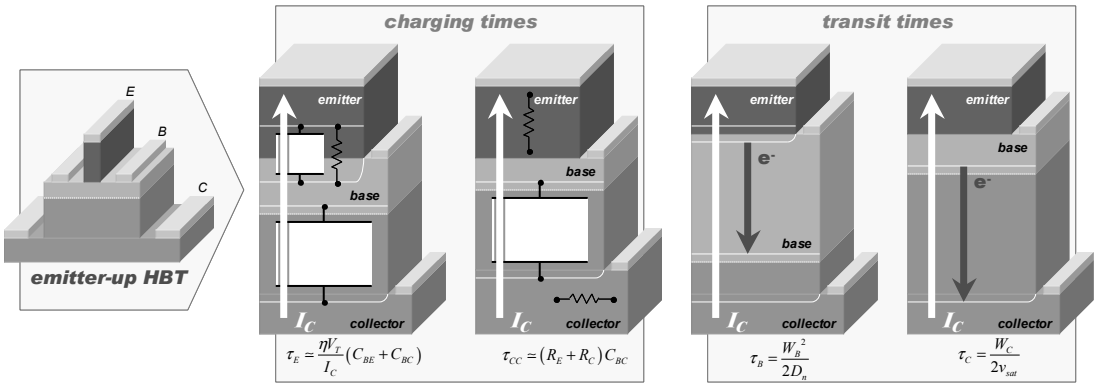

Figure 3.4 Illustration of the various transistor aspects which influence f_τ.

frequency at which the transistor's unilateral power gain drops to unity, in addition to delineating the boundary between the transistor behaving as an active or passive network, Equation (3.3).

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi R_B C_{BC}}} \tag{3.3}$$

R_B is the transistor's base resistance.

The intent of the oxide aperture HBT design is to introduce a method to increase f_{max} that can be adopted into nearly any material system and existing transistor design. Though it is not of direct concern within the scope of this dissertation, it should be mentioned that there are various means to increase f_τ. Most of these approaches are dependent upon device layer design and material selection, such as bandgap grading in the base,[7,35] base doping profiles,[36,37] and Schottky collectors;[38] all of which may be adopted into the oxide aperture HBT design.

In order to increase the f_{max} of the transistor, a collector-up design, as opposed to the conventional emitter-up design (Figure 3.5a), was adopted. Using a collector-up

design makes possible the reduction of the transistor's relatively large C_{BC} by physically reducing the active base-collector junction area, thereby increasing the device's f_{max}. Simply adopting a plain collector-up design would result in a reduced current gain, or possibly no gain at all, due to an active emitter-base junction that is larger than the corresponding base-collector junction, giving rise to an increased recombination of carriers into the base contacts (Figure 3.5b). Therefore, in order to maintain a high current gain, a current aperture must be introduced into the emitter to channel the carriers that are injected into the base (Figure 3.5c). An additional benefit of the collector-up design is that it easily facilitates the use of a Schottky collector, as

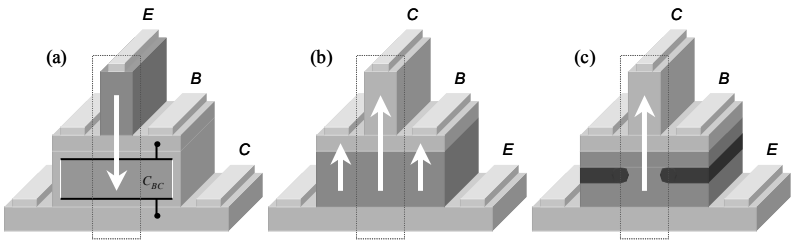

Figure 3.5 (a) Emitter-up design: high gain, high C_{BC}. (b) Collector-up design: reduced gain, reduced C_{BC}. (c) Oxide aperture, collector-up design: high gain, reduced C_{BC}. The arrows represent injected carriers. The dashed perimeter outlines the intrinsic HBT, where transistor action occurs.

opposed to a conventional ohmic collector/sub-collector commonly used in emitter-up designs (Figure 3.6). The benefit of using a Schottky contact for the collector contact is that it removes the collector resistance (R_C) from Equation (3.2), reducing the collector-charging time (τ_{CC}), increasing both f_τ and f_{max}.[38]

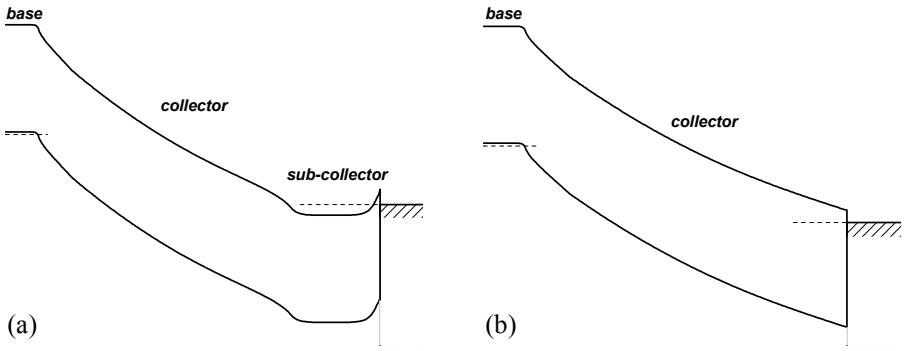

Figure 3.6 (a) Ohmic collector. The sub-collector, though highly conductive, contributes largely to the collector resistance, R_C. (b) Schottky collector.

3.3 Transistor Design: Material Selection

The majority of high-speed HBTs produced today have been InP-based emitter-up HBTs.[6,7,39-42] A layer structure and band diagram representative of most $Al_{0.48}In_{0.52}As/In_{0.53}Ga_{0.47}As$ HBTs is presented in Figure 3.7. Alternative designs incorporate an InP emitter, an InP emitter and collector, or an InP emitter and collector with a $GaAs_{0.49}Sb_{0.51}$ base.[25,43,44]

Simply adopting a material structure similar to that in Figure 3.7 for use in the oxide aperture design is not feasible for one reason: $Al_{0.48}In_{0.52}As$ does not readily oxidize ($R_{oxidation} \approx 2.4$ μm/hr at 520 °C),[45,46] and consequently cannot be used to form a current aperture in the emitter. Therefore, another wide bandgap semiconductor that meets this requirement must be selected. With the advent of the valved antimony source for molecular beam epitaxy (MBE), the growth of mixed group-V compounds, such as $GaAs_{0.49}Sb_{0.51}$, $AlAs_{0.56}Sb_{0.44}$, and their alloys, is possible without much difficulty.[47] Therefore, the $Al_{0.48}In_{0.52}As$ emitter may be replaced with an

$AlAs_{0.56}Sb_{0.44}$ emitter, which readily oxidizes, in addition to having a somewhat wider bandgap ($\Delta E_g \approx 0.4$ eV). Since the band line-up between $AlAs_{0.56}Sb_{0.44}$ and

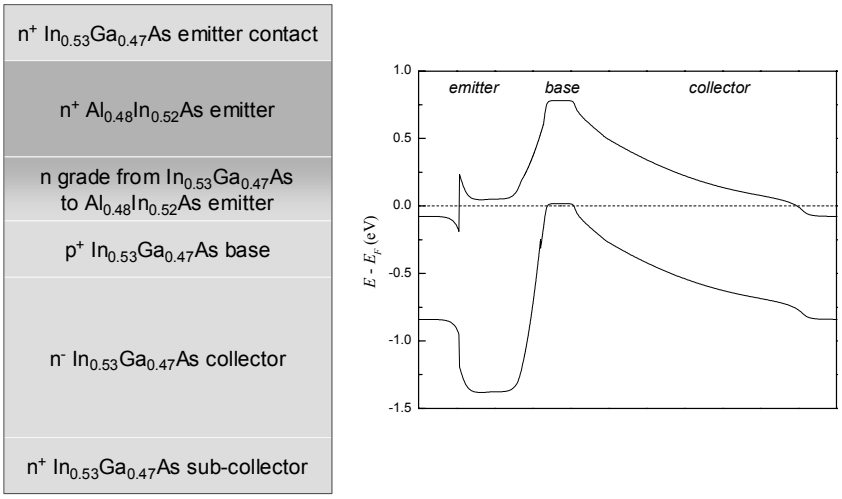

Figure 3.7 Layer structure and band diagram of an emitter-up InP-based HBT.

$In_{0.53}Ga_{0.47}As$ is not favorable to the fabrication of an abrupt heterojunction Npn HBT ($\Delta E_c \approx 0.99$ eV, $\Delta E_v \approx 0.19$ eV) and compositional grading between the two materials is difficult given the disparate group-V elements, $GaAs_{0.49}Sb_{0.51}$ was selected to replace $In_{0.53}Ga_{0.47}As$ as the narrow bandgap material in the emitter and base so as to easily facilitate compositional grading and growth of a graded heterojunction HBT. An $In_{0.53}Ga_{0.47}As$ collector is retained due to its high v_{sat} and the high selectivity of some wet etches between $In_{0.53}Ga_{0.47}As$ and $GaAs_{0.49}Sb_{0.51}$, simplifying the fabrication of devices.[48]

A layer structure of the resultant HBT, accompanied by its band diagram, is shown in Figure 3.8. Detailed layer structures and band diagrams of actual fabricated devices are presented in Chapters 4 and 5.

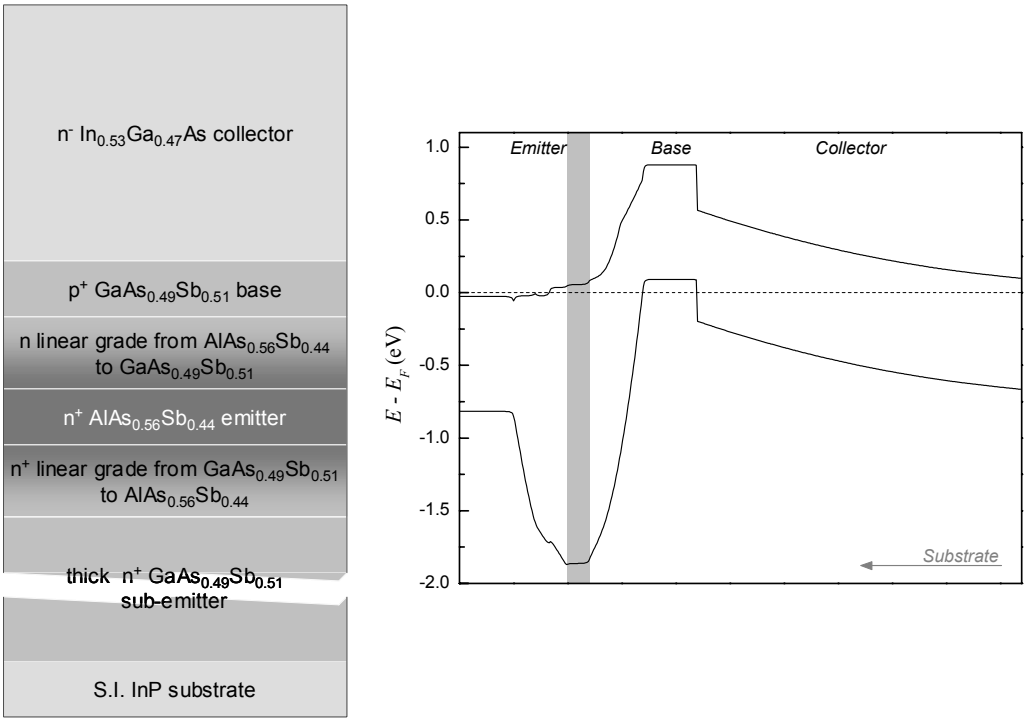

Figure 3.8 Layer structure and band diagram of the oxide aperture HBT. The shaded region indicates the location of the oxide aperture.

3.4 Growth of $GaAs_{0.49}Sb_{0.51}$ and $AlAs_{0.56}Sb_{0.44}$

"MBE is basically sophisticated thermal evaporation."

—James G. Champlain

The reality is not quite that simple, but essentially the statement is to some extent correct. MBE *is* the condensation of a vapor into a solid, but while it is desirable to form the crystalline solid phase of the semiconductor in question, care must be taken to avoid the formation of other undesirable condensed phases. In order to do so requires that the growth be performed within a series of thermodynamic constraints. These thermodynamic boundaries are commonly referred to as the "MBE growth window". A commonly accepted definition is that, *"MBE will thermodynamically be*

preferred if it occurs at an overall system composition, temperature, and pressure for which the equilibrium mix of phases is [the crystalline solid and vapor] …"[49] Though this is generally a good rule of thumb, it should be noted that there are exceptions; such as the MBE growth of GaN, where the preferred growth conditions are those for a mixture of the crystalline solid phase and Ga-rich liquid, otherwise known as metal-rich or Ga-rich growth;[50] or the MBE growth of low-temperature (LT) grown GaAs, which results in the desirable formation of arsenic precipitates within the GaAs crystal solid due to growth under excessive arsenic flux at low growth temperatures.[51]

Figure 3.9 shows examples of growth windows for GaAs, a well-established III-V compound semiconductor, presented in terms of phase diagrams. As can be seen

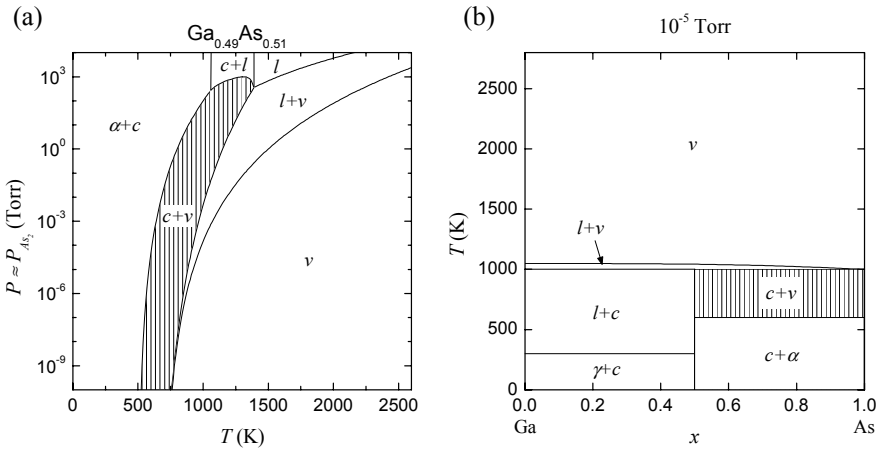

Figure 3.9 After Tsao.[49] (a) *P-T* phase diagram of $Ga_{1-x}As_x$ for an overall system composition of $x = 0.51$. (b) *x-T* phase diagram for $Ga_{1-x}As_x$ at a pressure of 10^{-5} Torr. The shaded regions are the preferred MBE growth windows.

from the diagrams, even for the growth of a "simple" binary compound such as GaAs, the grower must monitor and maintain various aspects of the growth environment (e.g., system temperature, pressure, composition) within a specific window. As one

might deduce, as additional elements are added to the crystal; as in classical ternary compounds like $Al_xGa_{1-x}As$ and $In_xGa_{1-x}As$, and the mixed group-V compounds like $GaAs_{0.49}Sb_{0.51}$ and $AlAs_{0.56}Sb_{0.44}$; the growth window becomes much more restrictive.[49,52-56]

The growth of the mixed group-V compounds $GaAs_{0.49}Sb_{0.51}$ and $AlAs_{0.56}Sb_{0.44}$ is further complicated by the non-unity sticking coefficients of antimony and arsenic and by the pronounced temperature dependent exchange of antimony and arsenic atoms on the growth surface. This results in the composition of the arsenide-antimonide compound being not only dependent on the relative arsenic and antimony fluxes, but also on growth temperature, total group-V flux, and growth rate.[27,57] Figure 3.10 shows additional examples of how the composition of various arsenide-antimonide compounds lattice-matched to InP vary with growth temperature and growth rate.

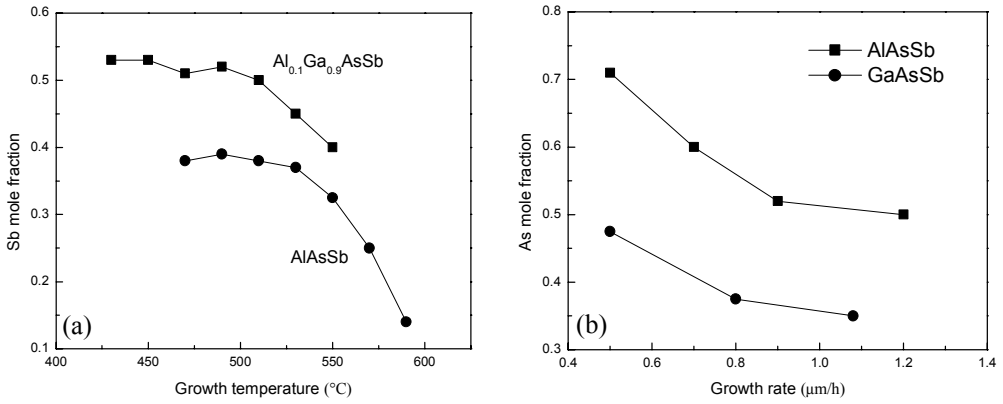

Figure 3.10 After Harmand *et al.*.[27] (a) Antimony mole fraction in AlAsSb and $Al_{0.1}Ga_{0.9}AsSb$ versus growth temperature. (b) Influence of the growth rate of GaAsSb and AlAsSb on their arsenic mole fraction. Arsenic and antimony fluxes were fixed for each experiment.

To overcome the difficulties encountered during the growth of arsenide-antimonide compounds, two growth methods have been developed for the growth of $GaAs_{0.49}Sb_{0.51}$ and $AlAs_{0.56}Sb_{0.44}$ lattice-matched to InP.[48] The first of the two methods involves the growth of the arsenide-antimonide compound in the form of a digital alloy consisting of the two constituent binary compounds (GaAs/GaSb for $GaAs_{0.49}Sb_{0.51}$ or AlAs/AlSb for $AlAs_{0.56}Sb_{0.44}$) (Figure 3.11). The composition of layers grown by this method has been shown to be highly dependent on group-V shutter duty cycle, while relatively insensitive to any group-V flux variations (especially in the case of arsenic flux variations), resulting in a highly reproducible growth. The major drawback to this method is simply the wear and tear on the MBE

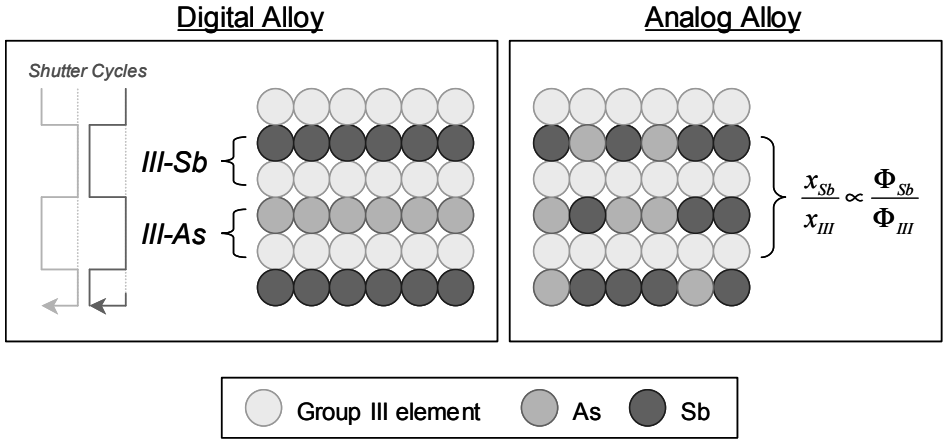

Figure 3.11 Illustration of a digital and an analog arsenide-antimonide alloy.

growth system imposed by the numerous shutter operations required. For example, approximately 170 shutter operations per group-V source would be required for just 1000 Å of $GaAs_{0.49}Sb_{0.51}$ or $AlAs_{0.56}Sb_{0.44}$.

The second method requires the correlation of the group-V incorporation rate with its beam equivalent pressure to grow the arsenide-antimonide compound as an analog compound. At growth temperatures below 500 °C the sticking coefficient of antimony approaches unity,[58] this allows for the growth of the arsenide-antimonide compound at its desired composition by simply matching the antimony incorporation rate with the group-III growth rate in the proper ratio (Figure 3.11). For example, if an arsenide-antimonide compound with a desired antimony composition of approximately 50 % (a lattice-matched composition to InP) is grown with a group-III growth rate of 1.0 μm/hr, then the antimony growth rate must be selected to be 0.5 μm/hr. Given that the arsenic sticking coefficient under these conditions is much less than unity, excess arsenic can be supplied to provide an excess group-V background. The group-V incorporation rates can be obtained in-situ by means of group-V reflection high-energy electron diffraction (RHEED) oscillations, similar to ordinary group-III RHEED oscillations.[48]

The major drawback to this method of growth is the strong sensitivity of the resultant growth's composition on the relative fluxes of all constituent species. Figure 3.12 shows the variation in lattice mismatch, and hence composition, of $GaAs_xSb_{1-x}$ and AlAsxSb1$_{-x}$ ($x \approx 0.50$) on group-III flux. It can be seen that even small deviations in group-III flux (growth rate) results in dramatic effects on composition and the resultant material quality (Figure 3.13).

Though the analog growth of arsenide-antimonide compounds could be considered to be more difficult as compared to the digital growth, once the growth

has been calibrated, little upkeep is required to maintain high quality crystal growth, given a stable growth system and periodic calibrations. For this reason, in addition to

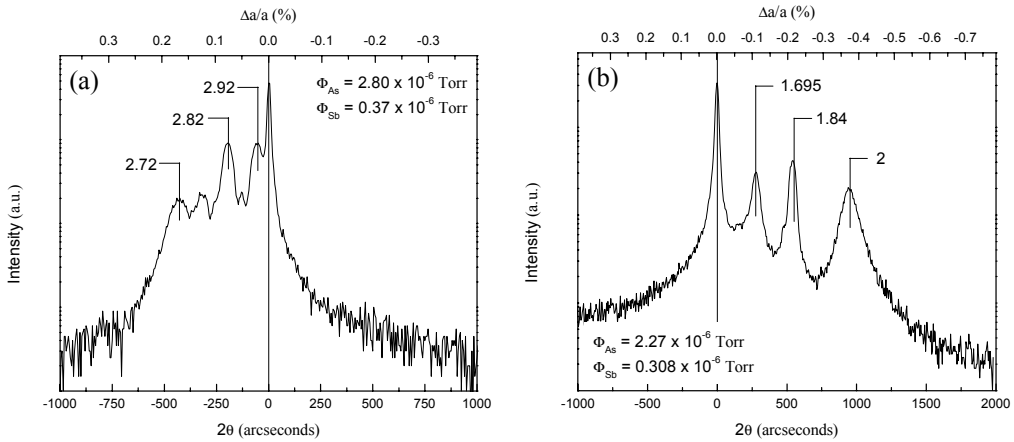

Figure 3.12 X-ray diffraction calibrations for (a) GaAsSb and (b) AlAsSb.[59] Both plots are zeroed to the InP substrate x-ray peak. The beam equivalent pressure for both gallium and aluminum fluxes are indicated on the plots in multiples of 10^{-7} Torr.

the greatly reduced wear on the growth system, the analog method of growth was adopted for all growths of $GaAs_{0.49}Sb_{0.51}$ and $AlAs_{0.56}Sb_{0.44}$ in this dissertation.

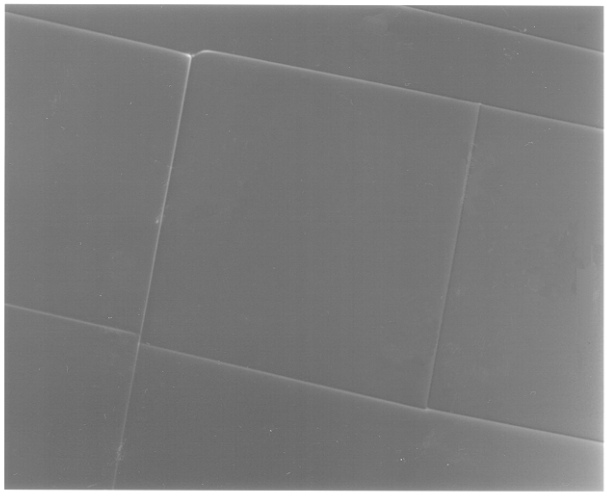

Figure 3.13 Photograph of 0.37 % mismatch growth of AlAsSb.[60]

3.5 Growth of $Al_xGa_{1-x}As_ySb_{1-y}$ Lattice-Matched to InP

By selecting a single set of arsenic and antimony fluxes for both $GaAs_{0.49}Sb_{0.51}$ and $AlAs_{0.56}Sb_{0.44}$, the growth of $Al_xGa_{1-x}As_ySb_{1-y}$ lattice-matched to InP ($0 \le x \le 1$, $y \approx 0.50$) is easily achieved as a simple digital alloy of both ternaries, permitting the trouble-free growth of compositionally graded junctions.

Though growing quarternary alloys and compositional grades by digital methods increases the wear on the system, it is nearly impossible and highly impractical to perform such growths using analog growth techniques. To do so would require calibrations of all constituent fluxes for each composition to be grown and radically increase the difficulty of the growth itself, due to an increased number of group-III cell temperature adjustments and group-V valve adjustments. Therefore, all quarternary alloys in this dissertation have been grown using a digital alloy of both ternaries, $GaAs_{0.49}Sb_{0.51}$ and $AlAs_{0.56}Sb_{0.44}$. Additionally, all grades have been grown using piece-wise step approximations (Figure 3.14 and Figure 3.15).

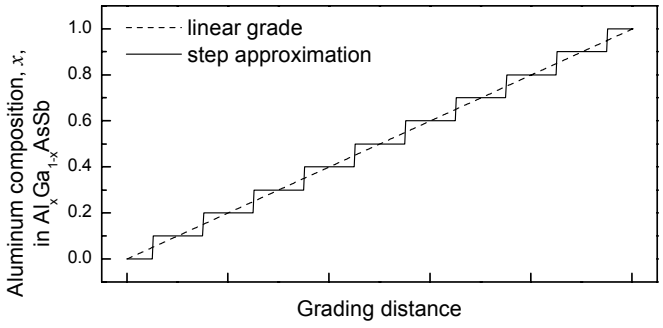

Figure 3.14 Example of a linear grade of $Al_xGa_{1-x}AsSb$ from $x = 0$ to $x = 1$ using a step approximation. Growth of $Al_xGa_{1-x}AsSb$ is achieved using a digital alloy of AlAsSb and GaAsSb (Figure 3.15).

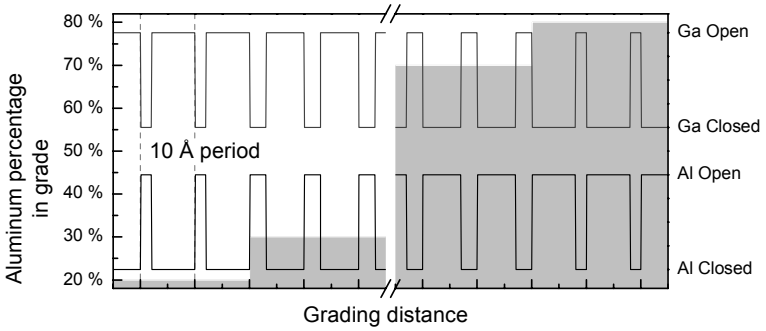

Figure 3.15 Detail of the digital composition grade in Figure 3.14. The shutter operations for gallium and aluminum (corresponding to GaAsSb and AlAsSb growth, respectively) are shown in overlay. The period of the digital alloy is 10 Å. Therefore to achieve 20 % Al composition requires the growth of 2 Å of AlAsSb and 8 Å of GaAsSb. 70 % Al composition: 7 Å AlAsSb/3 Å GaAsSb.

3.6 n-type Doping with Tellurium

Silicon is the most widely used element for n-type doping in III-V semiconductors, but as a result of it being a group-IV element, it is also amphoteric by nature. This means that the crystal site (group-III or group-V) that silicon, or any group-IV dopant, occupies determines its doping nature (donor or acceptor). As a consequence of their amphoteric nature, group-IV dopants tend to self-compensate, and at higher concentrations this self-compensation tends to result in a saturation of the carrier concentration.[61]

For most III-V semiconductors, silicon largely occupies the group-III site as a donor, with a small fraction occupying the group-V site as acceptors, resulting in very little compensation and an overall n-type crystal. Conversely, for antimony-based compounds silicon has been shown to generally incorporate as an acceptor,

attributable to the silicon mostly residing on the antimony (group-V) sites, resulting in a p-type crystal.[62,63]

For this reason, tellurium, a group-VI element, has been used as an n-type dopant for antimony-based compounds.[26,27,64] Because tellurium is not a group-IV element, it does not suffer from self-compensation as silicon does. But like silicon, tellurium suffers from donor-complex (DX) center formation in compounds containing aluminum, which can greatly reduce its doping efficiency.[65]

An additional problem encountered with doping the arsenide-antimonides is the poor mobility of carriers at high doping levels, especially in $AlAs_{0.56}Sb_{0.44}$ (Figure 3.16). This along with the restricted doping level leads to relatively high resistivities, complicating device design.

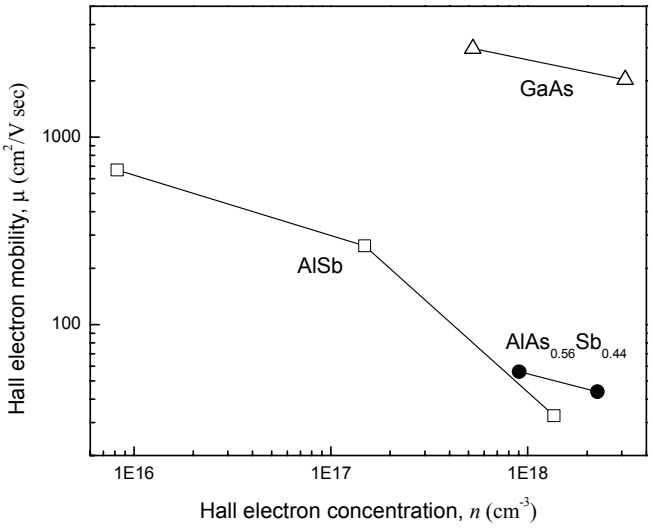

Figure 3.16 Plot of electron mobility versus electron concentration, measured by Hall effect, for various semiconductors doped with tellurium, Te.

3.7 Oxidation of $AlAs_{0.56}Sb_{0.44}$

The oxidation of $AlAs_{0.56}Sb_{0.44}$, like $Al_xGa_{1-x}As$,[66-68] can be described using the Deal-Grove model for oxidation.[69] Equation (3.4) shows the characteristic equation associated with this model.

$$t = \frac{d}{k_l} + \frac{d^2}{k_p} \tag{3.4}$$

Where t is the oxidation time, d is the oxidation depth, k_l is the linear oxidation constant, and k_p is the parabolic oxidation constant. Figure 3.17 shows an exemplar of the oxidations performed in this work and the associated fitted curves using

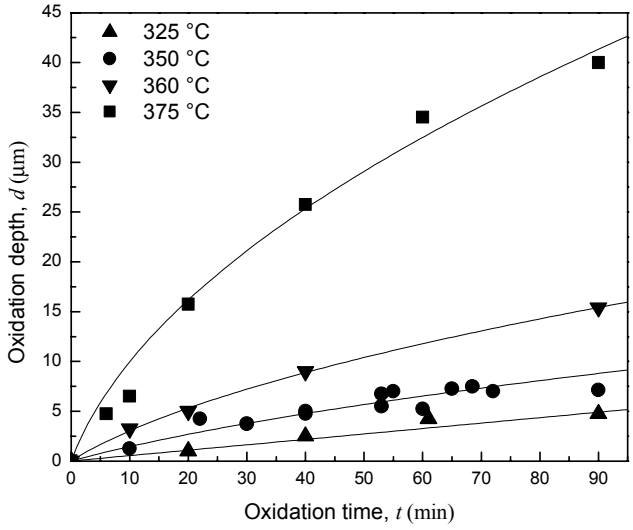

Figure 3.17 Oxidation depth versus oxidation time for a sample with a 500 Å emitter grade, a 200 Å AlAsSb layer, and a 500 Å base-emitter (BE) grade. Water temperature was 90 °C, nitrogen flow rate was 1.2 lpm, furnace temperature is indicated on the plot.

Equation (3.4). The oxidations in this work were performed using a three-zone furnace; into which pre-heated water vapor was carried by nitrogen gas. Unless

otherwise stated, the water temperature and nitrogen flow rate may be assumed to have been 90 °C and 1.2 lpm, respectively. An illustration of the furnace is shown in Figure 3.18.

Though a conclusive study has not been performed, the work in this dissertation suggests that there were no semi-metallic antimony layers formed. It is hypothesized

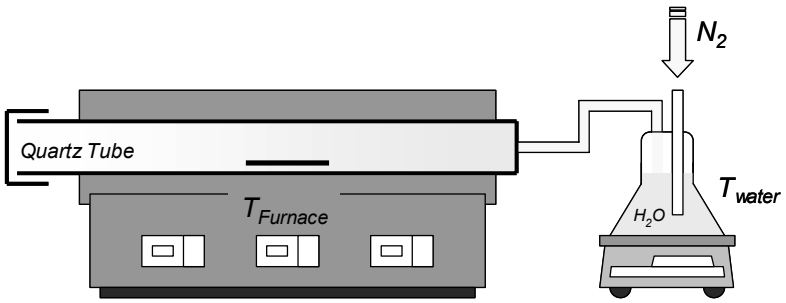

Figure 3.18 Illustration of the oxidation furnace and water vapor bubbler.

that this is due to the fact that the $AlAs_{0.56}Sb_{0.44}$ layers oxidized in this work were simply too thin to supply enough antimony to form a continuous layer.

As is the case with $Al_xGa_{1-x}As$ compounds,[66,68,70-72] $AlAs_{0.56}Sb_{0.44}$ exhibits an oxidation characteristic that is dependent upon oxidation temperature.[20,22,69,73] From Figure 3.17 it can be seen that as the oxidation temperature increases, the oxidation rate of $AlAs_{0.56}Sb_{0.44}$ rapidly increases. This is reflected in how the linear oxidation constant, k_l, and the parabolic oxidation constant, k_p, vary with temperature. Figure 3.19 shows a plot of k_l and k_p versus $1/kT$ for the curves presented in Figure 3.17.

From Figure 3.19, as the oxidation temperature increases, both k_l and k_p increase with an Arrhenius-like behavior. Though it appears that the oxidation characteristic

in Figure 3.17 becomes more diffusion limited at higher temperatures, the activation energies of the linear and parabolic rate constants, E_{A,k_l} and E_{A,k_p} respectively, are nearly equivalent ($E_{A,k_l} = 3.32$ eV, $E_{A,k_p} = 3.87$ eV) for the temperature range examined in this dissertation.

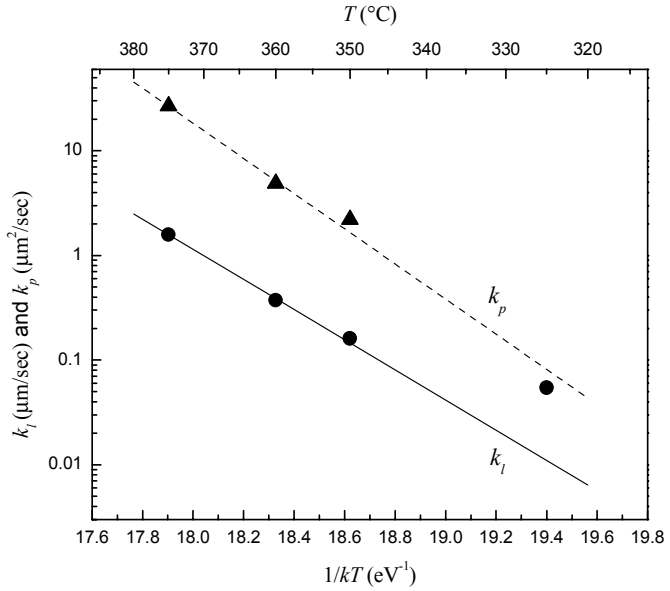

Figure 3.19 Arrhenius plot of k_l and k_p from fitted curves in Figure 3.17

Similar characteristics and trends were observed for all structures oxidized. Appendix A contains a complete tabulation of the oxidations performed in this dissertation.

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CHAPTER 4

The Oxide Aperture Diode

4.1 Introduction

At the heart of all bipolar transistors are two *pn* junctions or diodes, the base-emitter junction and the base-collector junction. Under forward-active operation, in which the base-emitter junction is forward biased and the base-collector junction is reverse biased, the base-emitter junction acts as a source of carriers and the base-collector junction acts as a sink for carriers (Figure 4.1). Due to the nature of this operation, much of the transistor's current and current-related characteristics (i.e., the emitter, collector, and base currents: I_E, I_C, and I_B; and the common-base and common-emitter current gains: α and β) can be related back to the base-emitter junction, the source of carriers.

Experiments have shown that interface recombination velocities are increased for interfaces between GaAs and the oxide formed from the wet oxidation of $Al_xGa_{1-x}As$,

as compared to unoxidized interfaces. Additionally, reduced minority carrier diffusion lengths are also observed in the vicinity of these interfaces.[1,2]

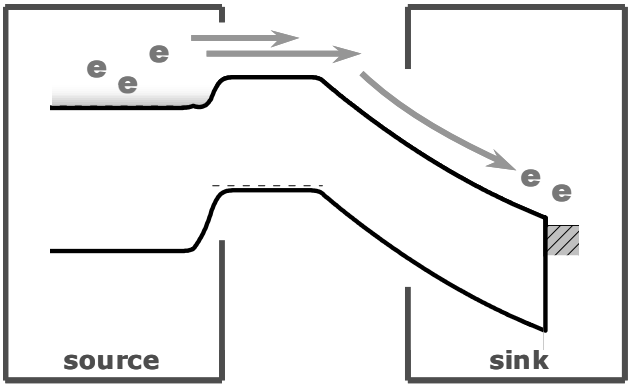


Figure 4.1 Illustration of the source and sink aspects of HBTs. Carriers, in this case electrons, are *emitted* from the emitter, transit the base, and are *collected* at the collector.

For these reasons, oxide aperture diodes, similar to those used in the base-emitter junction of the oxide aperture transistor, were fabricated and studied to better understand the role and potential effect of the oxide aperture on diode performance, and thus transistor performance.

4.2 Diode Characteristics: Ideal versus Non-Ideal

In an ideal *pn* junction or diode, the current that flows through the device is results from the diffusion of carriers across the depletion region of the junction. Equation (4.1), which describes this current, is commonly referred to as the *ideal diode equation*.

$$J_{diff} = J_{S,diff}\left(e^{V_{app}/V_T} - 1\right) \tag{4.1}$$

J_{diff} is the total current density (current per unit area); $J_{S,diff}$ is the reverse saturation current density; V_{app} is the applied voltage; and $V_T = kT/q$ is the thermal voltage, where k is Boltzmann's constant (8.62×10^{-5} eV/K), T is the absolute temperature of the semiconductor in Kelvin, and q is the electronic charge (1.602×10^{-19} C). Equation (4.1) is regarded as ideal because the formulation of the equation is based on the following assumptions, which result in an idealized representation of the total current in a *pn* junction: **(1)** the built-in potential of the junction and all applied bias are supported solely by a depletion region having abrupt boundaries and outside of that region the semiconductor is neutral (the abrupt depletion region approximation), **(2)** carrier statistics are determined with reference to their relative quasi-Fermi level following the Maxwell-Boltzmann function (the Maxwell-Boltzmann approximation), **(3)** the injected minority carrier concentrations are small enough that the relative majority carrier concentrations remain unperturbed from their equilibrium values (the low injection assumption), and **(4)** the individual electron and hole currents are constant throughout the depletion region (no recombination-generation current exists in the depletion region).

Non-idealities in diode current are commonly introduced through additional current terms. One such example is recombination-generation current due to the net recombination (under forward bias) and net generation (under reverse bias) of carriers via a recombination center (trap) in the depletion region:

$$J_{rec} \simeq J_{S,rec} e^{V_{app}/2V_T} \tag{4.2}$$

$J_{S,rec}$ is the recombination reverse saturation current density. Here, J_{rec} is calculated using the Shockley-Read-Hall (SRH) theory of recombination, assuming conditions for maximum recombination rate (i.e., a trap energetically located at mid-gap). The result is a recombination current with an exponential dependence on applied voltage of $V_{app}/2V_T$, contrasted to the V_{app}/V_T dependence of Equation (4.1). The total diode current can now be expressed as the summation of the ideal diffusion current and recombination current (Equation (4.3) and Figure 4.2).[3]

$$J_{total} = J_{diff} + J_{rec} \simeq J_{S,diff}\left(e^{V_{app}/V_T} - 1\right) + J_{S,rec}e^{V_{app}/2V_T} \tag{4.3}$$

Realistically, it is nearly impossible to determine the fraction of the total diode current that the diffusion current or recombination current comprises. Additionally,

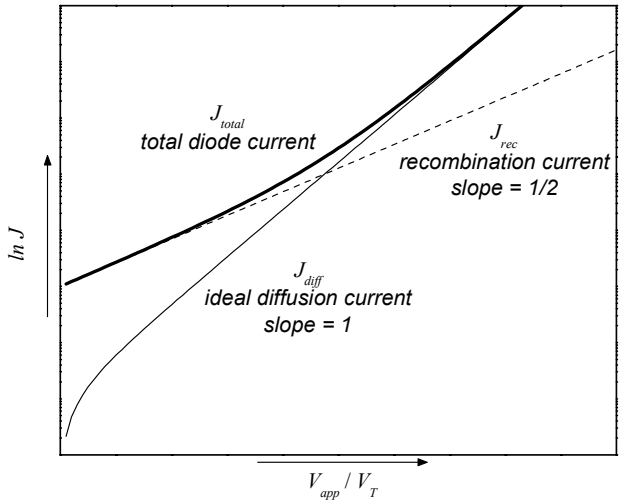


Figure 4.2 Ideal diffusion, recombination, and total diode current density under forward bias.

the assumption of a single trap located at mid-gap is somewhat simplistic, and it can be shown that a single trap located off of mid-gap or a distribution of traps located

within the bandgap of the semiconductor can result in SRH recombination currents with dependencies ranging from V_{app}/V_T to $V_{app}/2V_T$, as a consequence of voltage division within the junction.[4] Therefore, the total diode current is generally written as:

$$J_{total} = J_S\left(e^{V_{app}/\eta V_T} - 1\right) \tag{4.4}$$

J_S is the reverse saturation current density of the diode and η is the diode ideality factor. Here, η can vary between 1 (ideal, diffusion dominated) and 2 (non-ideal, recombination dominated) depending upon the relative magnitudes of the diffusion and recombination currents.

Experimentally the ideality factor of a diode may be determined using one of two methods: either by fitting Equation (4.4) or applying Equation (4.5) to the measured current-voltage characteristic.

$$\eta \simeq \frac{J}{V_T}\left(\frac{\partial J}{\partial V_{app}}\right)^{-1} \tag{4.5}$$

For applied voltages greater than a few kT/q, Equation (4.4) may be approximated as $J \simeq J_S e^{V_{app}/\eta V_T}$. Differentiation and algebraic manipulation results in Equation (4.5).

Equation (4.5) is used in this dissertation, as opposed to simply fitting the data, because it easily permits an examination of ideality factor as a function of applied voltage, and thereby the relative influence of the various current components (i.e.,

diffusion current and recombination current) on the total diode current at different applied voltages. Figure 4.3 shows examples of Equation (4.5) applied to a variety of cases.

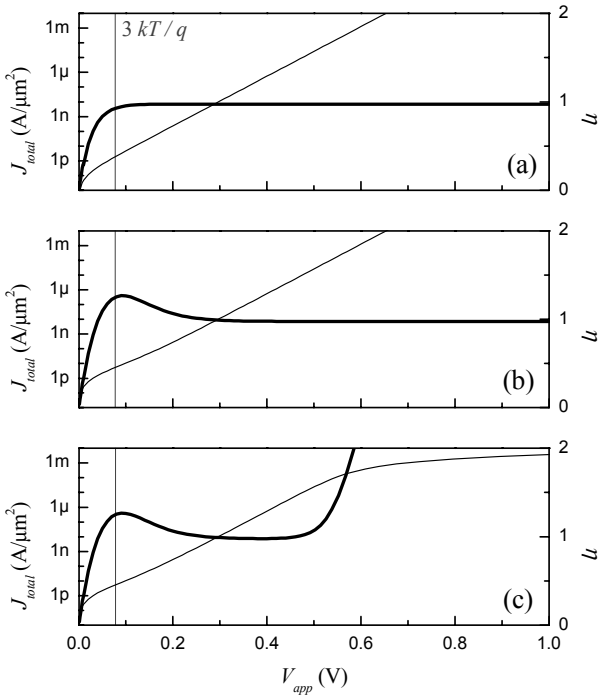


Figure 4.3 Diode characteristics and their associated ideality factor, calculated using Equation (4.5). The light line represents total diode current, J_{total}; the heavy line, diode ideality factor, η. (a) Plot of an ideal (diffusion current only) diode characteristic. (b) Ideal diode characteristic with the addition of a recombination term. The recombination current tends to increase the ideality factor at low biases. (c) Ideal + recombination diode characteristic with the addition of a series resistance. At high biases the characteristic becomes resistively limited and Equation (4.5) is no longer valid.

In addition to the diode ideality factor, the geometric dependence of the total current provides further information on the nature of current conduction in a diode. For example, Equation (4.4) was derived independent of *pn* junction area (A_j).

Therefore, for uniform junctions the absolute current should scale with junction area ($I = J \cdot A_j$).

In actual diodes, surface effects (e.g., surface conduction or surface recombination) can introduce additional currents that do not scale with junction area but instead scale with junction perimeter (P_j). If these effects begin to dominate the conduction mechanisms in the diode, then the absolute current will no longer scale with junction area. The result is an apparent bulk current density ($J_{apparent} = I_{measured} / A_j$) that varies with junction area, as opposed to remaining constant. In situations where both bulk and surface currents exist, the total absolute current may be written as a sum of the two:

$$I_d = J \cdot A_j + K \cdot P_j = J_S \left(e^{V_{app}/\eta_j V_T} - 1 \right) A_j + K_S \left(e^{V_{app}/\eta_k V_T} - 1 \right) P_j \tag{4.6}$$

I_d is the absolute measured current flowing through the diode; J is the bulk current density as described by Equation (4.4); K is the surface current sheet density (current per unit length), which obeys dynamics similar to J; and η_j and η_k are the ideality factors for J and K, respectively. The relative contributions of the bulk and surface currents to the total current can be found by rewriting Equation (4.6) in terms of perimeter-to-area ratio (P_j / A_j) and fitting to the measured data (Figure 4.4).

$$\frac{I_d}{A_j} = J + K \frac{P_j}{A_j} \tag{4.7}$$

For a given applied bias, the y-intercept and the slope of Equation (4.7) equal J and K, respectively. Once J and K are found as functions of bias, their relative ideality factors may be found using Equation (4.5).

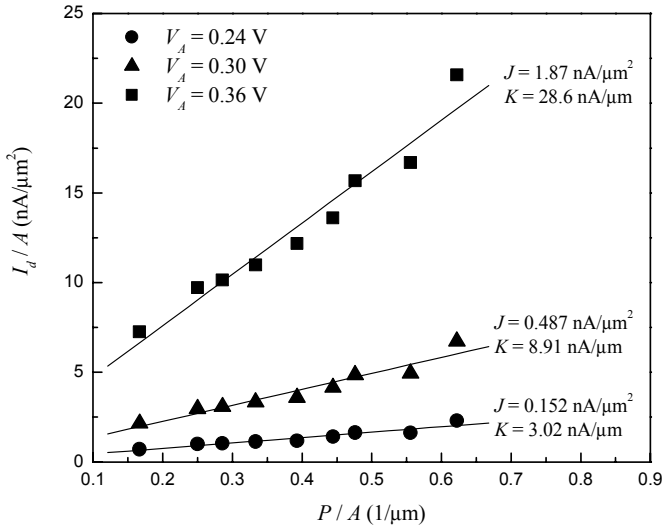


Figure 4.4 Example plot of I_d/A versus perimeter-to-area ratio for different applied biases. By fitting Equation (4.7) to multiple curves, J and K can be reconstructed as functions of bias.

4.3 Design and Fabrication

The layer structure, accompanied by its band structure, used in the fabrication of the oxide aperture diodes (oxide diodes) is shown in Figure 4.5; the thickness of the base-emitter grade (t_{BE}) was varied between 100 Å, 500 Å, and 1000 Å with the thickness of the emitter grade held at 500 Å. The diodes were fabricated using a standard airbridge, mesa diode structure. The process, in essence, consisted of etching the diode mesa down to the sub-emitter to expose the $AlAs_{0.56}Sb_{0.44}$ layer for oxidation (Figure 4.6a). After the $AlAs_{0.56}Sb_{0.44}$ layer was oxidized to form the

aperture, base and emitter contacts were deposited (Figure 4.6b). Devices were completed with an isolation etch and airbridge process (Figure 4.6c and d).

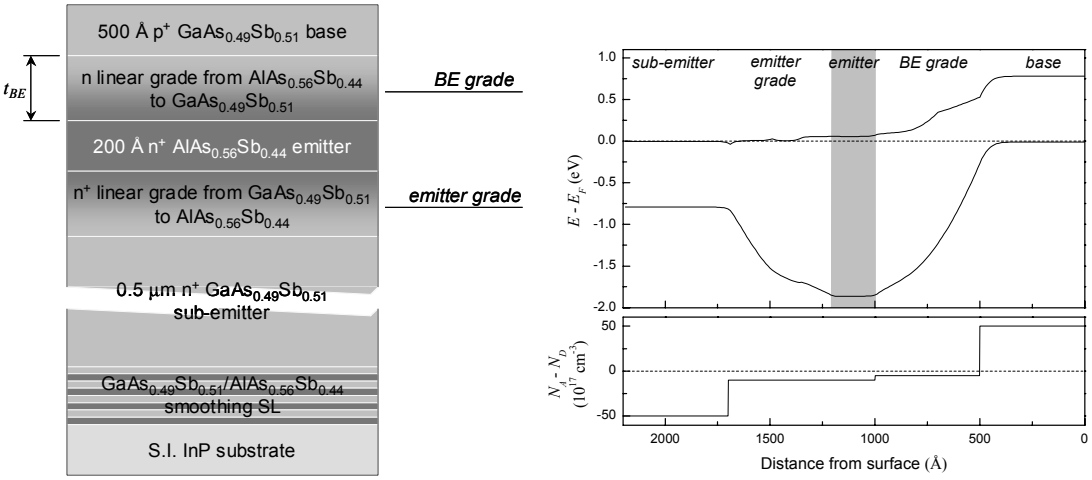


Figure 4.5 Layer structure and band diagram of the oxide aperture diodes used in this dissertation. The band diagram is for a diode with a 500 Å base-emitter grade. The shaded region indicates the location of the oxide aperture.

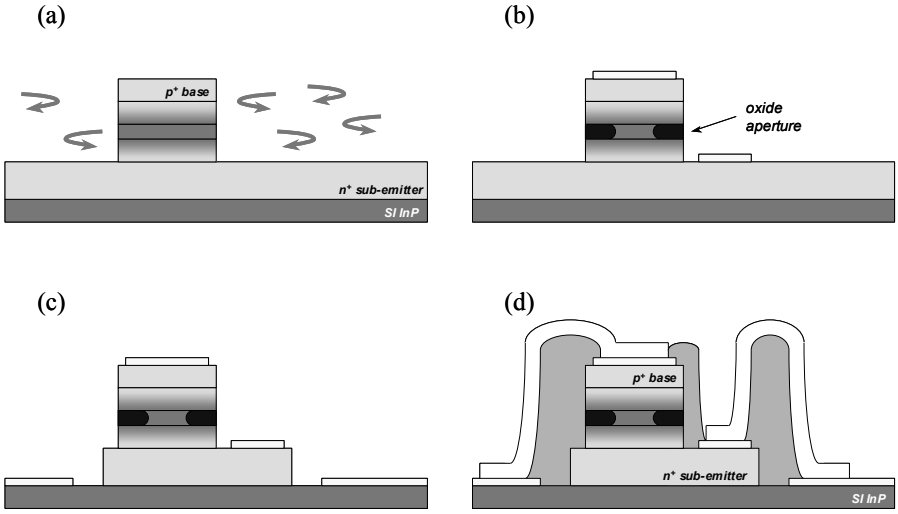


Figure 4.6 Illustration of the oxide aperture diode fabrication process. (a) Etch to expose AlAsSb for oxidation. (b) Oxidation followed by deposition of the base and emitter contacts. (c) Device isolation etch and contact pad deposition. (d) Completed device with airbridge.

Unoxidized diodes, in addition to the oxide diodes, were fabricated for comparison. A detailed description of the diode fabrication process is located in Appendix B.

4.4 Diode Characteristics: Oxide Aperture Diodes

Figure 4.7 gives an illustration of the diode outlining the various areas and perimeters used in the following discussion: A_{mesa}, mesa area, is the area of the *entire* diode mesa and P_{mesa}, mesa perimeter, is the perimeter of that area; $A_{aperture}$, aperture area, is the area of the diode *enclosed* by the oxide aperture and $P_{aperture}$, aperture perimeter, is the perimeter of that area. For example, a 13×17 μm^2 diode that has been oxidized to form an oxide aperture with a depth (d_{ox}) of 6 μm has $A_{mesa} = 13 \times 17 = 221$ μm^2, $P_{mesa} = 2 \times (13 + 17) = 60$ μm, $A_{aperture} = 1 \times 5 = 5$ μm^2, and $P_{aperture} = 2 \times (1 + 5) = 12$ μm.

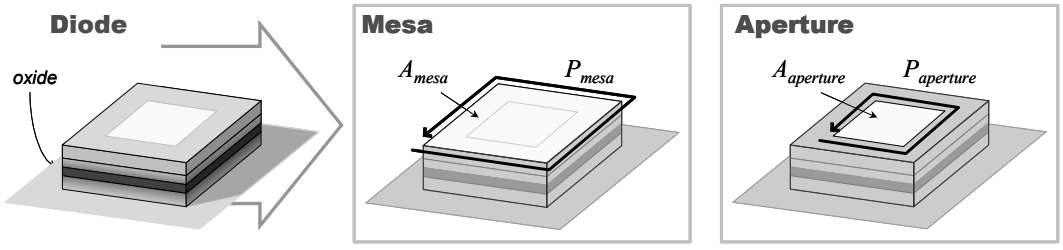


Figure 4.7 Illustration of the various areas and perimeters used in the discussion of oxide aperture diodes.

A summary of the dominant active geometry and diode ideality factor for diodes fabricated in this dissertation, extracted from current-voltage characteristics, are presented in Table 4.1. A plot of ideality factor versus base-emitter grade thickness,

t_{BE}, is shown in Figure 4.8. The ideality factor is found to be a minimum for oxide diodes with t_{BE} = 500 Å.

t_{BE} (Å)	Dominant active geometry	Ideality factor, η
unoxidized	Mesa area, A_{mesa}	~1
100	Aperture perimeter, $P_{aperture}$	1.88
500	Aperture area, $A_{aperture}$	1.01
1000	Between $A_{aperture}$ and A_{mesa}	1.36

Table 4.1 Summary of active geometry and ideality factor for diodes fabricated in this dissertation.

Figure 4.9 presents an illustration of the hypothesized physics underlying the observed characteristics, which are similar to those seen in conventional emitter-up heterojunction bipolar transistors (HBTs) with emitter ledges.[5] For oxide diodes with t_{BE} = 100 Å, the close proximity of the oxide surface to the depletion region of the *pn* junction results in carrier recombination along the inner periphery of the oxide

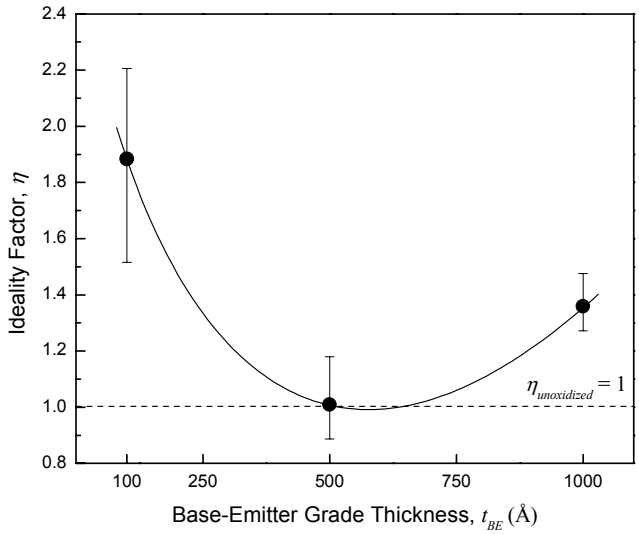


Figure 4.8 Plot of ideality factor, η, versus base-emitter grade thickness, t_{BE}. The average η as a function of bias for each thickness found using Equation (4.5) is plotted, with the error bars indicating the maximum and minimum measured η.

aperture (Figure 4.9a). If t_{BE} is increased, the oxide is removed away from the *pn* junction depletion region, removing its influence on the junction's carrier dynamics (Figure 4.9b and c). In the t_{BE} = 1000 Å case, the region above the oxide aperture becomes undepleted, allowing for lateral diffusion of carriers outside of the aperture area, reducing the effectiveness of the aperture, and resulting in injection of carriers outside of the aperture area (Figure 4.9c).

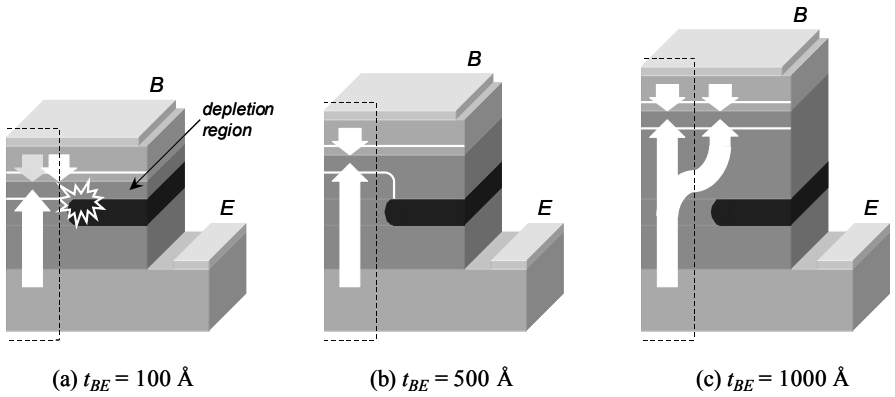


Figure 4.9 Illustration of oxide aperture half-diodes with (a) t_{BE} = 100 Å, (b) t_{BE} = 500 Å, and (c) t_{BE} = 1000 Å. The dashed line outlines the region bounded by the oxide aperture.

To properly channel the carriers injected into the base from the emitter, the material above the oxide aperture must remain depleted, in order to prevent lateral carrier diffusion. Therefore, the base-emitter grade must be sufficiently thick to remove the oxide's influence on the *pn* junction's carrier dynamics, but not so thick that the region above the aperture becomes undepleted, allowing diffusion outside of the aperture area (Figure 4.9b).

Simulations of the oxide aperture diodes using ATLAS Device Simulation Software[6] support these conclusions (Figure 4.10).[7]

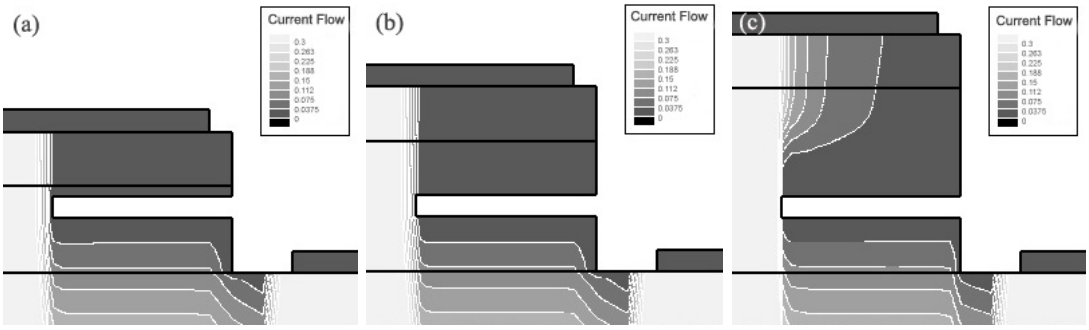


Figure 4.10 Simulations of the oxide aperture diodes: (a) t_{BE} = 100 Å (without recombination), (b) t_{BE} = 500 Å, and (c) t_{BE} = 1000 Å. The light regions indicate areas of high current density; the dark, low current density.

Unoxidized Diodes

Unoxidized diodes, ranging from 13×17 μm^2 to 32×32 μm^2, were fabricated and measured. Figure 4.11 shows the measured current-voltage characteristics (t_{BE} = 500 Å). The plot of I_d/A_{mesa}, Figure 4.11b, strongly suggests that the unoxidized diodes scale with mesa area (A_{mesa}), as expected. Evaluation of J and K, using Equation (4.7), verifies this statement (Figure 4.12). The ideality factors for J and K were found using Equation (4.5) (Figure 4.13). Independent of t_{BE} all

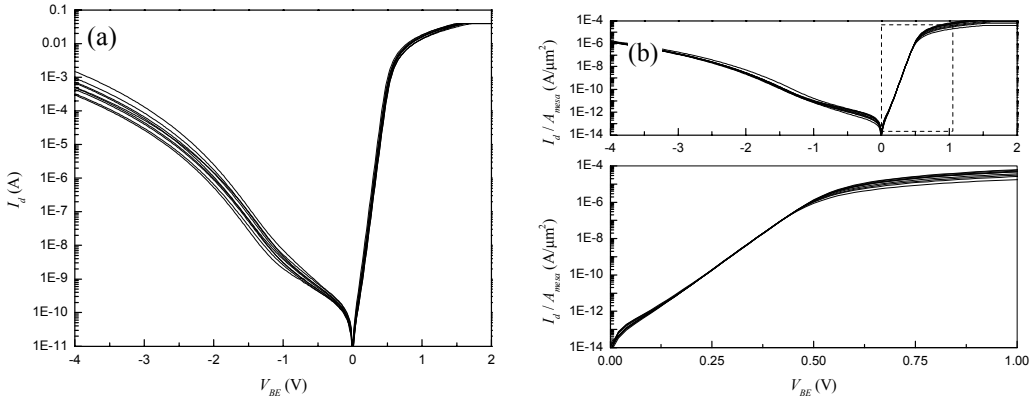


Figure 4.11 Plots of (a) absolute measured current (I_d) and (b) I_d/A_{mesa} for unoxidized diodes of various sizes (t_{BE} = 500 Å).

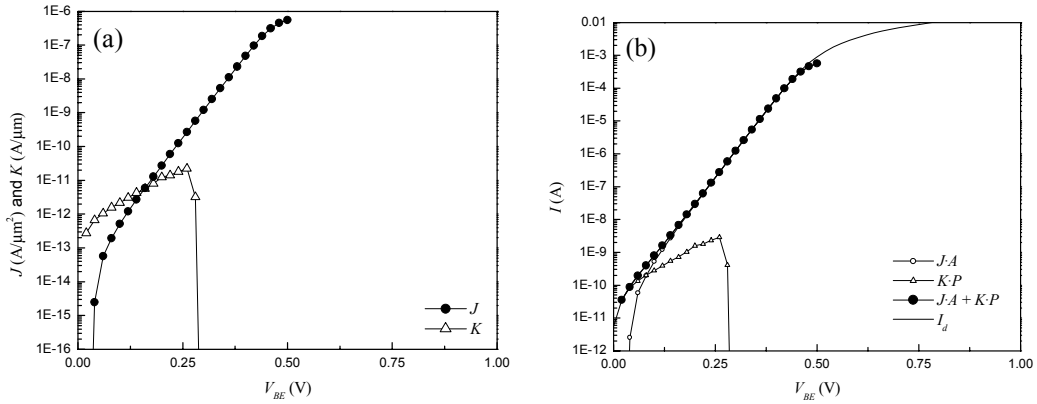


Figure 4.12 (a) Plot of *J* and *K*, derived using Equation (4.7) (t_{BE} = 500 Å). (b) Calculated I_d, using Equation (4.6), plotted against measured I_d for a 32 μm x 32 μm diode, showing very good agreement. The calculated I_D begins to deviate from the measured I_d at higher bias where the latter becomes resistively limited.

unoxidized diodes, in general, showed similar characteristics.

It should be noted that the rise in η_k above 2 is due to errors in fitting Equation (4.7) to regions of the measured data where the characteristic is dominated by bulk

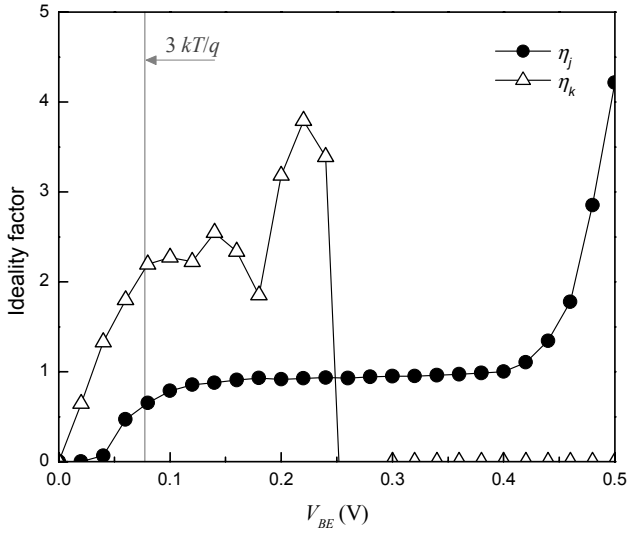


Figure 4.13 Plot of ideality factor versus bias for *J* (η_j) and *K* (η_k) (t_{BE} = 500 Å).

current, J, and is not related to any physical phenomenon.

Oxide Aperture Diodes: 100 Å

Measured current-voltage characteristics for oxide diodes with t_{BE} equal to 100 Å are shown in Figure 4.14. The oxidation depth, d_{ox}, for these devices was 4 μm. As a result, $A_{aperture}$ varies from $5 \times 9\ \mu m^2$ to $24 \times 24\ \mu m^2$. Figure 4.14b suggests that these diodes scale with $P_{aperture}$, which is verified in Figure 4.15a. The ideality factors

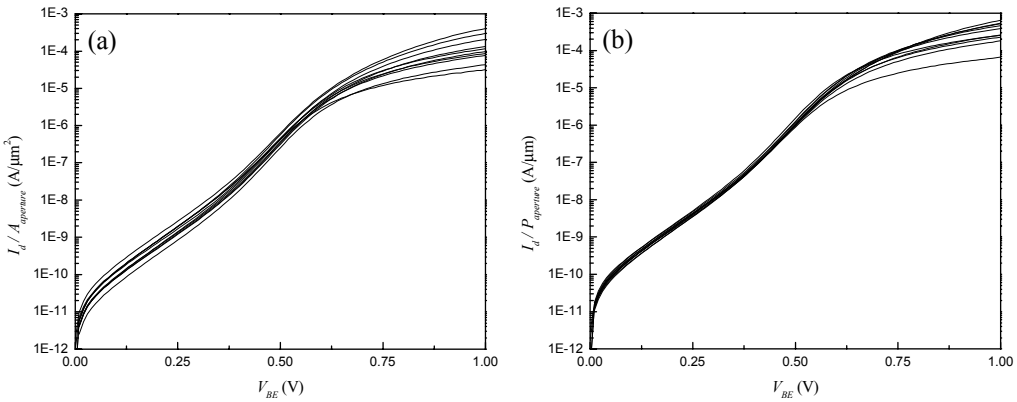


Figure 4.14 Plots of (a) $I_d/A_{aperture}$ and (b) $I_d/P_{aperture}$ versus bias for oxide diodes with t_{BE} = 100 Å.

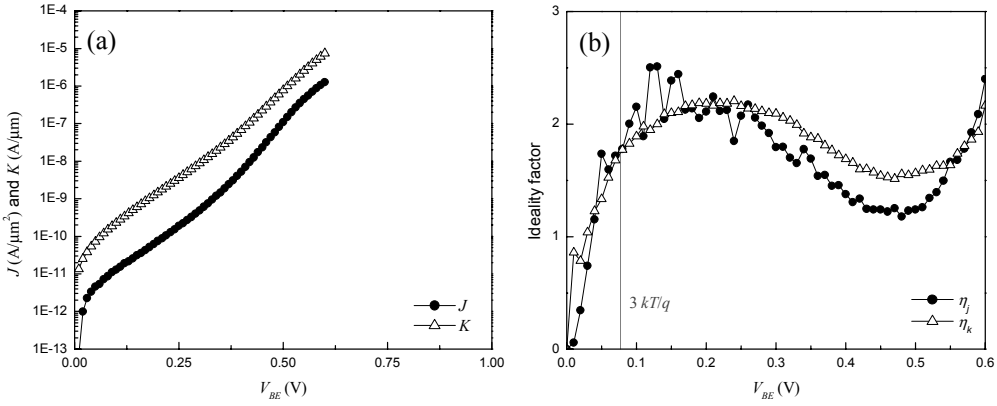


Figure 4.15 (a) Plot of J and K derived using Equation (4.7) and $A_{aperture}$ as the active junction area. (b) Ideality factor versus bias for J (η_j) and K (η_k).

for J and K are shown in Figure 4.15b.

The strong geometric dependence of the absolute current on $P_{aperture}$ and an ideality factor between 1.5 and 2 suggests that the majority of the current in these diodes was due to recombination at the interior periphery of the oxide aperture.

Oxide Aperture Diodes: 500 Å

Figure 4.16 presents the measured current-voltage characteristics for oxide diodes with $t_{BE} = 500$ Å. $A_{aperture}$ for these devices varied from 1.5×5.5 μm^2 to 20.5×20.5 μm^2 ($d_{ox} = 5.75$ μm). The characteristic for these diodes strongly scales

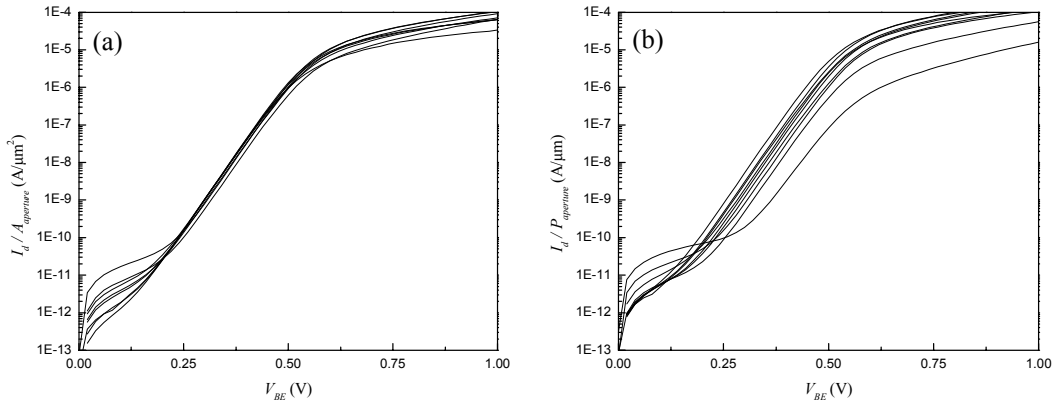


Figure 4.16 Plots of (a) $I_d/A_{aperture}$ and (b) $I_d/P_{aperture}$ versus bias for oxide diodes with $t_{BE} = 500$ Å.

with $A_{aperture}$ and exhibit an ideality factor approximately equal to 1 (Figure 4.16a and Figure 4.17). This result suggests that, at least for $t_{BE} = 500$ Å, the oxide aperture properly channels the injected carriers while introducing no ill effects upon the diode characteristic.

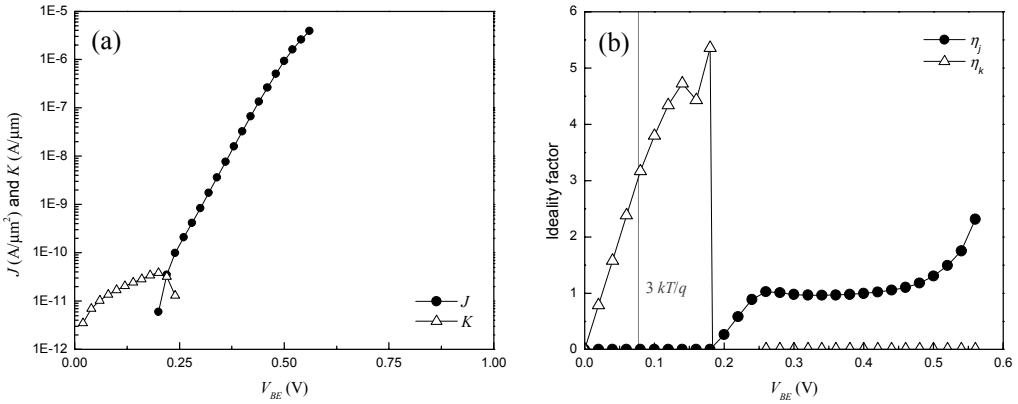


Figure 4.17 (a) Plot of *J* and *K* derived using Equation (4.7) using $A_{aperture}$ as the active junction area. (b) Ideality factor versus bias for *J* (η_j) and *K* (η_k).

Oxide Aperture Diodes: 1000 Å

The measured current-voltage characteristics for oxide diodes with a base-emitter grade thickness of $t_{BE} = 1000$ Å are presented in Figure 4.18. The oxidation depth, d_{ox}, for these devices was 7 μm, resulting in an $A_{aperture}$ that varies from 2×8 μm^2 to 18×18 μm^2. Unlike the previous cases, there is no clearly distinctive geometry to which the characteristic scales.

Evaluation of *J* and *K* using A_{mesa} as the active junction area (A_j) results in a current density (I_d / A_{mesa}) that decreases with increasing perimeter-to-area ratio (Figure 4.19a). From Equation (4.7) this would suggest the presence of a non-physical, negative sheet current density (*K*). Setting $K = 0$ A/μm, the smallest physically allowable value, results in the characteristics plotted in Figure 4.20.

Taking $A_{aperture}$ as the active junction area results in a characteristic that is comprised of nearly equal portions of bulk and surface currents (Figure 4.21). At first glance, there is nothing inherently wrong with this conclusion; but the result of the

t_{BE} = 500 Å oxide diodes, a current-voltage characteristic that clearly scales with $A_{aperture}$ without a strong surface current component present, suggests that a similar result should be expected here.

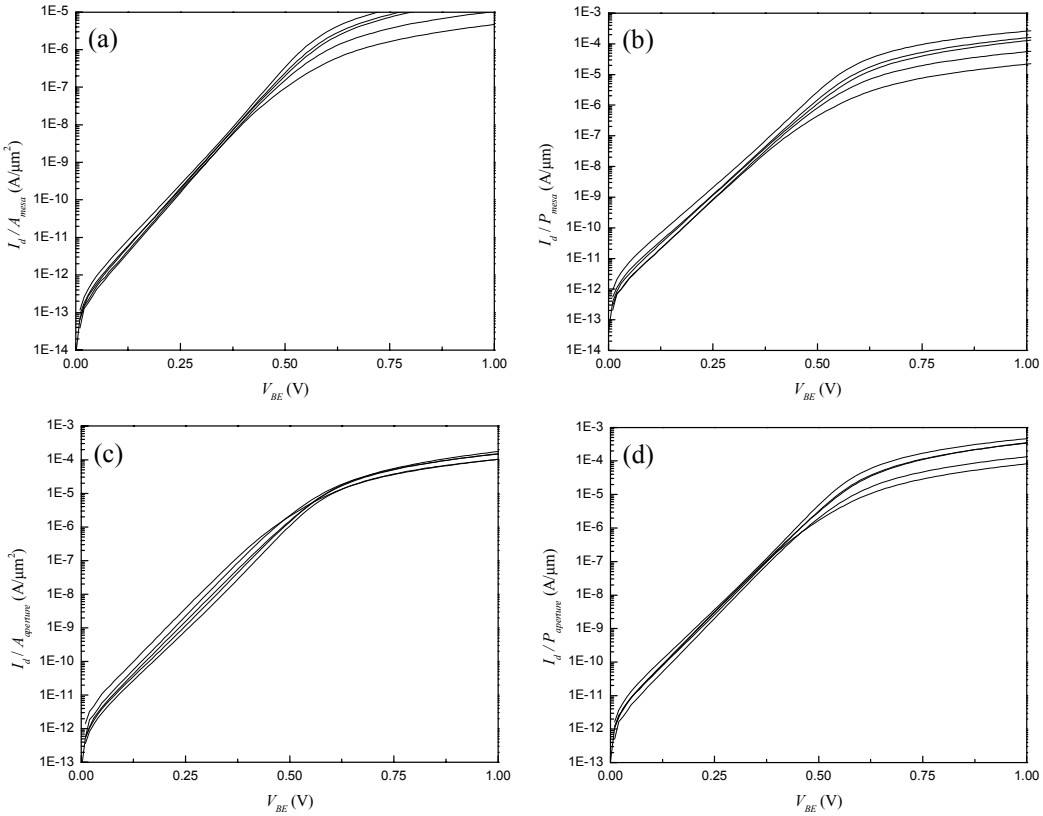


Figure 4.18 Plots of (a) I_d/A_{mesa}, (b) I_d/P_{mesa}, (c) $I_d/A_{aperture}$, and (d) $I_d/P_{aperture}$ versus bias for oxide diodes with t_{BE} = 1000 Å.

Review of the I_d/A versus P/A data suggests that the assumed active junction area strongly effects the determination of *J* and *K*, in some cases resulting in non-physical solutions (Figure 4.19a). To better understand the affect of the assumed active junction area on the determined *J* and *K*, the following thought experiment was performed.

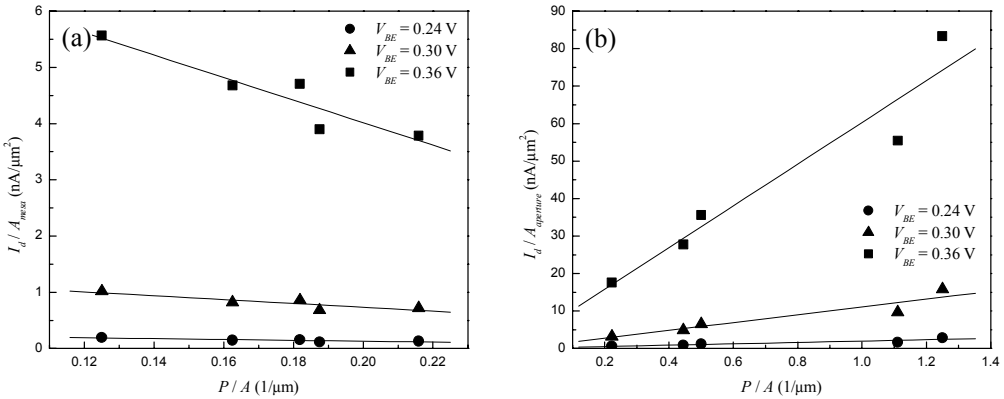


Figure 4.19 Plots of (a) I_d/A_{mesa} and (b) $I_d/A_{aperture}$ versus perimeter-to-area ratio (t_{BE} = 1000 Å).

Assuming a set of idealized diodes of various sizes for which the true active junction area (A_{true}) is known, the measured current density (I_d / A_{true}) should be a constant. If the active junction area is assumed to be larger than A_{true} ($A_{assumed} > A_{true}$), the result is an underestimation of the measured current density ($I_d / A_{assumed}$) and determined sheet current density (K) (Figure 4.22). In this case, an underestimation of K results in a negative value, as in the case of $A_j = A_{mesa}$ (Figure 4.19a).

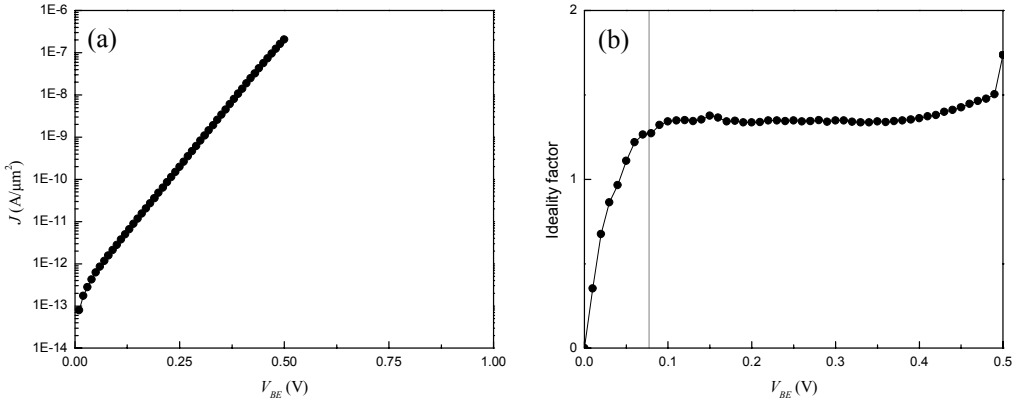


Figure 4.20 (a) Plot of J derived using Equation (4.7) using A_{mesa} as the active junction area. (b) Ideality factor versus bias.

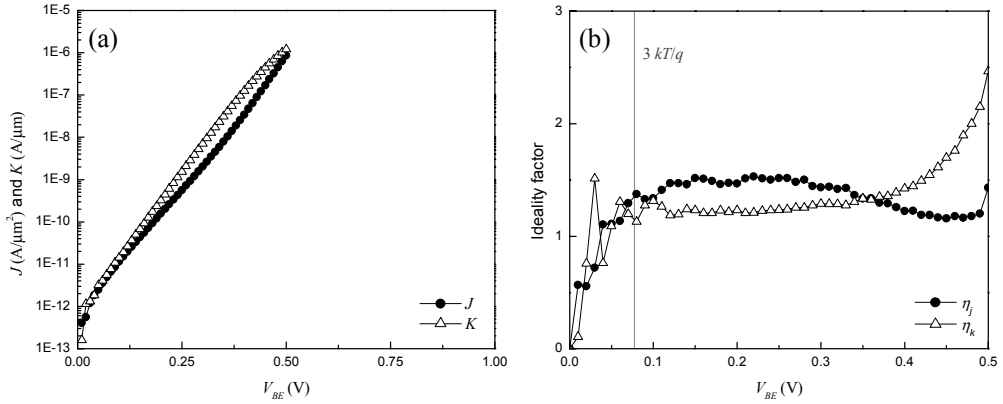


Figure 4.21 (a) Plot of *J* and *K* derived using Equation (4.7) using $A_{aperture}$ as the active junction area. (b) Ideality factor versus bias for *J* (η_j) and *K* (η_k).

Assumption of a smaller than true active junction area ($A_{assumed} < A_{true}$) results in an overestimation of $I_d / A_{assumed}$ and *K* (Figure 4.22).

Considering the results from this "experiment", it appears that A_{mesa} and $A_{aperture}$ may be an overestimate and underestimate, respectively, of the active junction area in

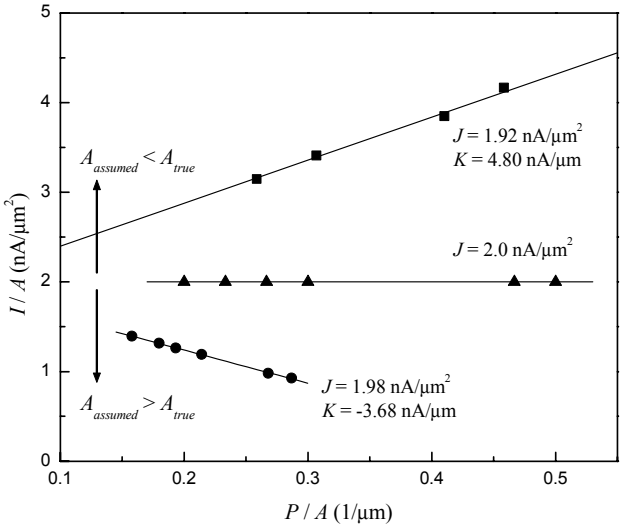


Figure 4.22 Plot of I_d/A showing the error introduced due to the assumption of a larger than true and smaller than true active junction are.

the t_{BE} = 1000 Å diodes. Therefore, the true active junction area is believed to lie somewhere between $A_{aperture}$ and A_{mesa} and is a consequence of lateral carrier diffusion in the undepleted portion of the base-emitter grade above the oxide aperture. Re-evaluation of the measured current-voltage characteristics, assuming no surface currents are present, results in an estimated active junction area between 3.75 μm and 4 μm larger than the aperture area on each side. Again, simulations of the diodes support this conclusion (Figure 4.10).

Independent of knowledge of the actual active junction area, it is clear that the absolute current does not solely scale with aperture area, as would be desired.

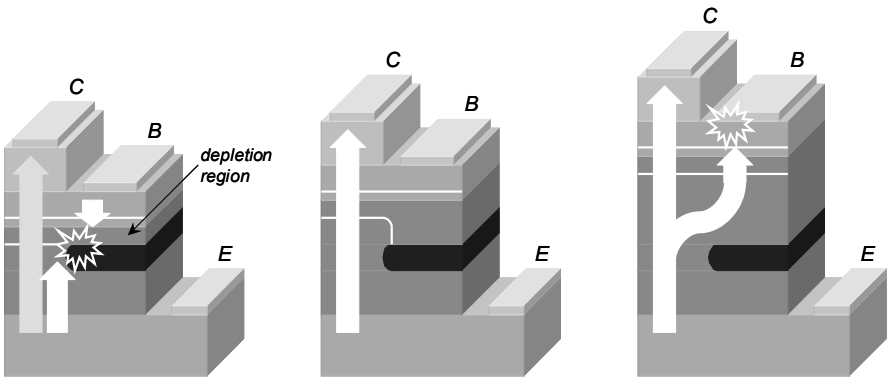
4.5 Diode Design for Oxide Aperture HBTs

In selecting an appropriate diode design for the base-emitter junction of the oxide aperture HBT, there are a few criteria that must be met:

---

(1) *The oxide aperture must effectively channel carriers injected from the emitter into the base.*

If the oxide aperture does not channel the carriers injected from the emitter effectively, injection will occur outside of the aperture area. In the oxide aperture HBT, the portion of carriers that are injected outside of the aperture area do not transit to the collector, but instead recombine into the base contacts (Figure 4.23c). For a constant collector current, the result is an increase in base current and consequent reduction in current gain. Therefore, designs like the t_{BE} = 1000 Å oxide diode are excluded from the possible choices for use in the oxide aperture HBT.



(a) t_{BE} = 100 Å (b) t_{BE} = 500 Å (c) t_{BE} = 1000 Å

Figure 4.23 Illustration of an oxide aperture half-HBTs. (a) t_{BE} = 100 Å. (b) t_{BE} = 500 Å. (c) t_{BE} = 1000 Å.

(2) *The current-voltage characteristic should scale with aperture area.*

A current-voltage characteristic that does not scale with area suggests the presence of phenomena such as high surface conduction, high surface recombination, or simply non-uniform injection across the junction. Such phenomena are highly undesirable due to the lack of control the device engineer has over them, resulting in unpredictable diode characteristics. Instead it is desirable to have a characteristic that scales with area and is therefore dependent upon device parameters such as doping concentration, carrier diffusion length, and carrier lifetime; all of which are directly or indirectly adjustable by the device engineer. This allows the device engineer to have a high degree of control over device characteristics and performance. Therefore, designs like the t_{BE} = 100 Å oxide diode are excluded.

(3) *The diode ideality factor should be as close to ideal (η = 1) as possible.*

The ideality factor of a diode generally reflects the dominant conduction mechanism in the device. A diode that is dominated by recombination current,

therefore having a high ideality factor, is undesirable because at a constant collector current, a higher base current is necessary to satisfy the additional carriers required by the recombination process. The result is a reduction in the current gain or no current gain at all.

Designs like the remaining oxide diode (t_{BE} = 500 Å) satisfy this criterion, in addition to the first two requirements, making them the desired design for application in the oxide aperture HBT.

4.6 References

[1] J. A. Kash, B. Pezeshki, F. Agahi, and N. A. Bojarczuk, "Recombination in GaAs at the AlAs oxide-GaAs interface." *Applied Physics Letters* **67**, 2022-4 (1995).

[2] H. Gebretsakik, K. Zhang, K. Kamath, X. Zhang, and P. Bhattacharya, "Recombination characteristics of minority carriers near the Al_xO_y/GaAs interface using the light beam induced current technique." *Applied Physics Letters* **71**, 3865-7 (1997).

[3] D. A. Neamen, *Semiconductor physics and devices: basic principles* (Richard D. Irwin, Inc., Burr Ridge, 1992).

[4] J. Pallares, L. F. Marsal, X. Correig, J. Calderer, and R. Alcubilla, "Space charge recombination in p-n junctions with a discrete and continuous trap distribution." *Solid-State Electronics* **41**, 17-23 (1997).

[5] W. Liu and J. S. Harris, Jr., "Critical passivation ledge thickness in AlGaAs/GaAs heterojunction bipolar transistors." *Journal of Vacuum Science & Technology B* **11**, 6-9 (1993).

[6] ATLAS Device Simulation Software is a product of SILVACO International, Inc.

[7] All simulations performed by Yee Kwang Seck.

CHAPTER 5

The Oxide Aperture HBT

5.1 Introduction

The advancement towards a high-frequency oxide aperture heterojunction bipolar transistor (HBT) occurred in a series of progressive steps or generations. The first generation of HBTs presented in this dissertation, fabricated before the oxide aperture diode study of Chapter 4, represent the very first attempt to produce an oxide aperture HBT. The results from these initial devices prompted the examination of the oxide aperture's affect on the current-voltage dynamics of a *pn* junction diode as presented in Chapter 4. The next generation of HBTs was fabricated with the benefit of the knowledge gained from the work presented in Chapter 4, but suffered from high extrinsic resistances that limited the transistor's performance. The final generation of oxide aperture HBTs presented in this dissertation showed vastly improved DC performance over previous generations, and was the first generation of oxide aperture HBTs to show high-frequency operation.

The three different generations of oxide aperture HBTs in this dissertation are classified as follows:

GENERATION Ø: The first generation of oxide aperture HBTs, fabricated *prior* to the oxide aperture diode study presented in Chapter 4.

GENERATION I: The first generation of HBTs to show true transistor action, fabricated *after* the oxide aperture diode study presented in Chapter 4.

GENERATION II: The first generation of oxide aperture HBTs to produce high-frequency (RF) results.

5.2 Oxide Aperture HBT Growth and Fabrication

Given that the majority of the analysis in this dissertation was performed on the final generation of oxide aperture HBTs, Generation II, its growth and fabrication will be presented here. The relative differences of the previous two generations, Generation Ø and Generation I, will be presented during the discussion of their analysis.

The layer structure and band diagram for the Generation II oxide aperture HBTs fabricated in this dissertation is presented in Figure 5.1. The structure (from substrate to surface) consisted of a semi-insulating (SI) InP substrate, a 0.5 μm n^+ $GaAs_{0.49}Sb_{0.51}$ sub-emitter (Te: 1×10^{19} cm^{-3}), a 500 Å n+ linear grade from $GaAs_{0.49}Sb_{0.51}$ to $AlAs_{0.56}Sb_{0.44}$ (Te: 1×10^{19} cm^{-3}), a 200 Å n^+ $AlAs_{0.56}Sb_{0.44}$ emitter (source layer for the oxide aperture) (Te: 5×10^{18} cm^{-3}), a 500 Å n linear grade from

$AlAs_{0.56}Sb_{0.44}$ to $GaAs_{0.49}Sb_{0.51}$ (Te: 1×10^{18} cm^{-3}), a 500 Å p^+ $GaAs_{0.49}Sb_{0.51}$ base (Be: 5 x 10^{19} cm^{-3}), and a 3000 Å n^- $In_{0.53}Ga_{0.47}As$ collector (Te: 5×10^{16} cm^{-3}).

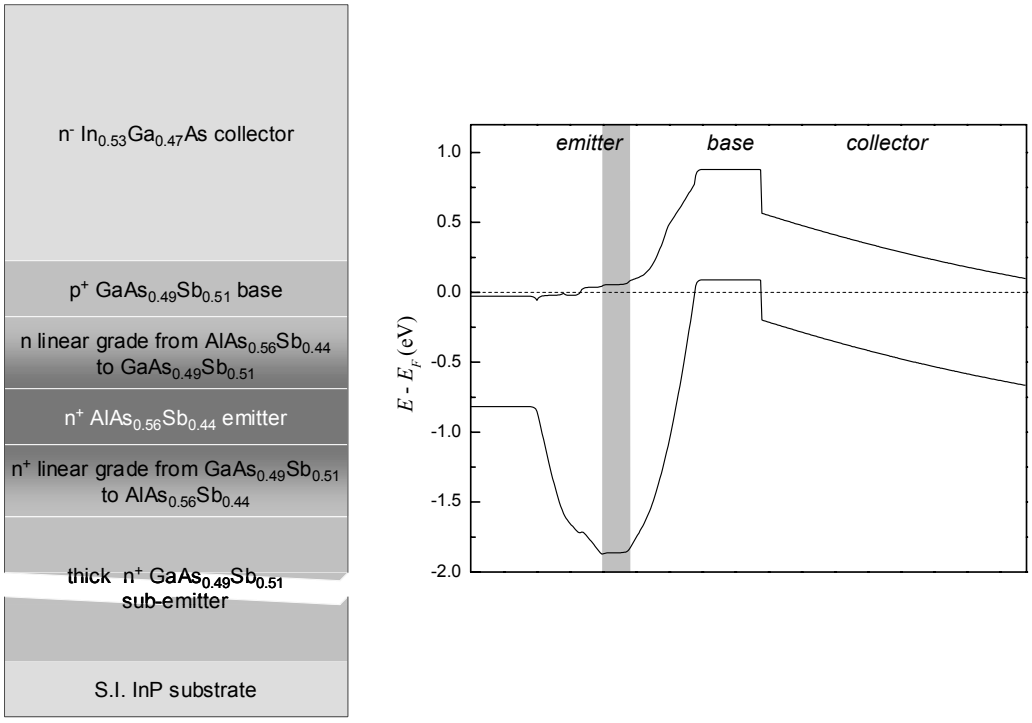


Figure 5.1 Layer structure and band diagram of the Generation II oxide aperture HBT.

The fabrication of the oxide aperture HBT, with the exception of the oxidation of the $AlAs_{0.56}Sb_{0.44}$ emitter, is nearly identical to most conventional three-tiered mesa RF HBTs, which makes the device attractive from a production point-of-view. The fabrication process began with the deposition of a 1 μm SiO_2 dummy collector by standard photolithography, SiO_2 e-beam evaporation, and lift-off. A SiO_2 dummy collector was used at this stage to facilitate the fabrication of a Schottky collector, as opposed to a metal collector that would undergo an anneal during the oxidation process, forming an ohmic collector. Following the deposition of the SiO_2 dummy

collector, the base mesa was defined using photolithography and a phosphoric acid-based etch. The mesa was etched down to the sub-emitter with the intention of exposing the $AlAs_{0.56}Sb_{0.44}$ emitter for oxidation (Figure 5.2a). After the $AlAs_{0.56}Sb_{0.44}$ emitter was oxidized to form the oxide aperture, the collector mesa was defined using photolithography and a selective citric acid-based etch.[1] The base and emitter contacts were deposited next by e-beam evaporation. An emitter mesa etch down to the SI InP electrically isolates the device (Figure 5.2b).

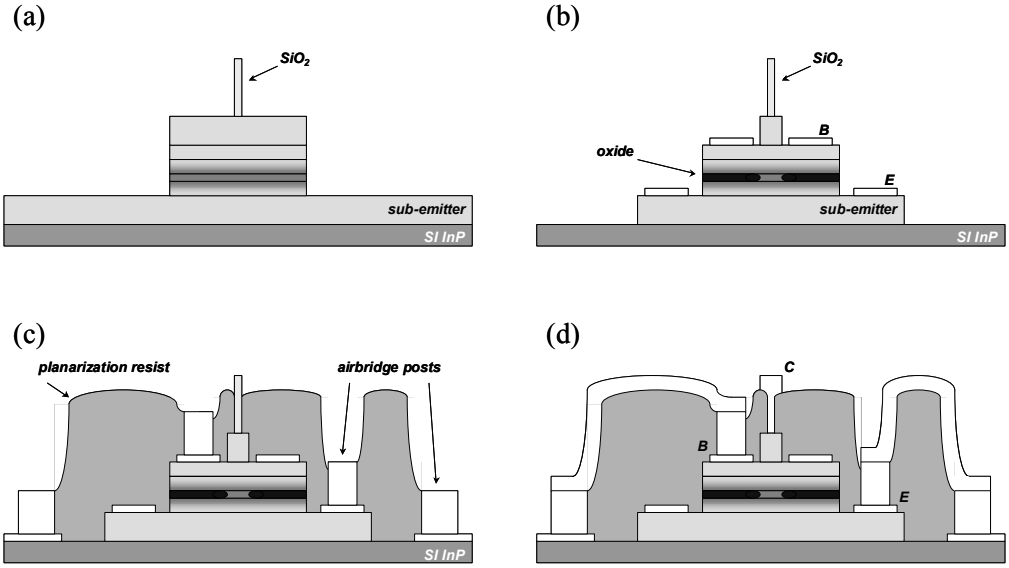


Figure 5.2 Illustration of the oxide aperture HBT fabrication process. (a) After the base mesa etch. (b) Oxidation followed by deposition of the base and emitter contacts and emitter/isolation etch. (c) After planarization, post deposition, and planarization resist etch. (d) Completed device.

A co-planar waveguide (CPW) transmission line structure and microwave probe pads are deposited on the SI InP to facilitate microwave measurements. The wafer is then planarized for subsequent airbridge/interconnect processing. After airbridge/interconnect posts are deposited by e-beam evaporation, the planarization

resist is blanket etched to expose the SiO_2 dummy collector (Figure 5.2c). Following the airbridge/interconnect lithography, the SiO_2 dummy collector is removed in buffered hydrofluoric acid to expose the collector. The airbridge/interconnect metal is deposited by e-beam evaporation, forming a Schottky contact on the collector. The fabrication is completed by opening vias for contacting the CPW lines (Figure 5.2d). Figure 5.3 shows a photograph of a completed device. A detailed description of the oxide aperture HBT fabrication process is presented in Appendix B.

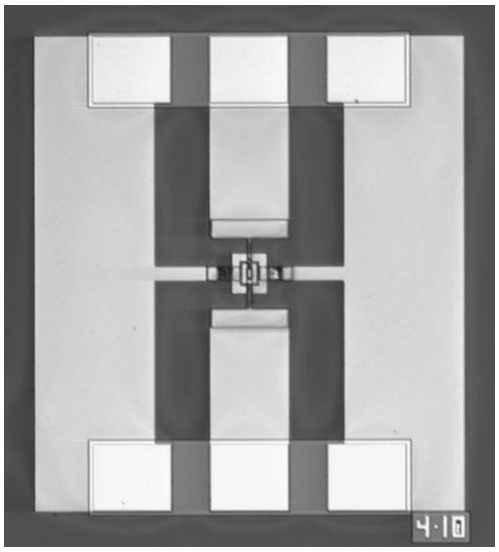


Figure 5.3 Photo of a completed oxide aperture HBT. The device here has a $4 \times 10\ \mu m^2$ collector contact.

One distinct difference in the design of the oxide aperture HBT as compared to conventional HBTs is the layout of the base mesa to the uppermost mesa: the collector mesa in the oxide aperture HBT, the emitter mesa in conventional HBTs. In conventional RF HBTs, the overall dimensions of the base mesa are reduced as much as possible in order to reduce the associated base-collector junction area and capacitance. Towards one end of the base, the mesa is commonly extended to

accommodate interconnect metallization for connecting to the transmission line (Figure 5.4a). In the case of the oxide aperture HBT, the base mesa must be similar is shape and centered on the collector mesa (Figure 5.4b). This is because at the time of this work, the only method for controlling the oxidation depth is oxidation time and temperature, which results in the oxidation depth being equidistant from the outer mesa edge. While a design like that used in a conventional HBT is desirable, the oxide aperture would not extend underneath the interconnect region, thereby not properly confining emitter current to only within the collector area, ruining the device's current gain characteristics (Figure 5.4c). The ramifications of the design used for the oxide aperture HBT on the RF performance of the device will be discussed later.

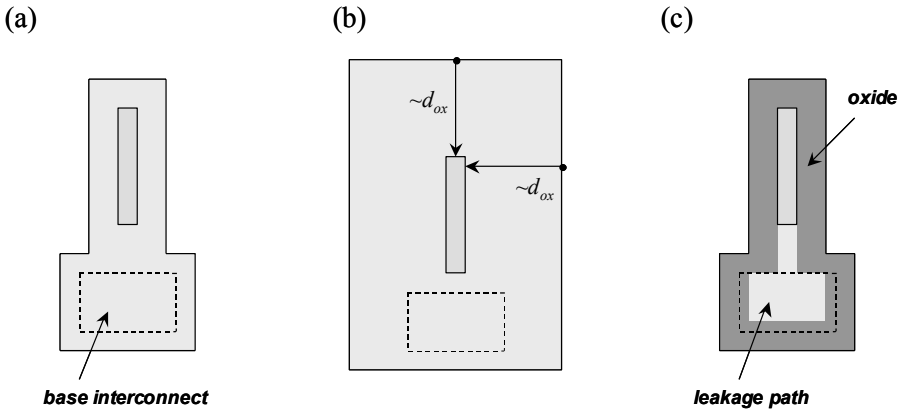


Figure 5.4 Base mesa designs for (a) a conventional RF HBT and (b) an oxide aperture HBT. (c) An oxide aperture HBT with a conventional HBT base mesa, a direct leakage path between the emitter and base would exist underneath the base interconnect.

5.3 Oxide Aperture HBT: Generation Ø

The Generation Ø oxide aperture HBTs, which were fabricated prior to the oxide diode experiments presented in Chapter 4, represent the initial attempt at producing an oxide aperture HBT. There are three major differences that distinguished Generation Ø HBTs from the subsequent generations: an $In_{0.53}Ga_{0.47}As$ base as opposed to a $GaAs_{0.49}Sb_{0.51}$ base, an abrupt heterojunction between the $AlAs_{0.56}Sb_{0.44}$ emitter and $In_{0.53}Ga_{0.47}As$ base, and a collector that is 2000 Å thick instead of 3000 Å (Figure 5.5).

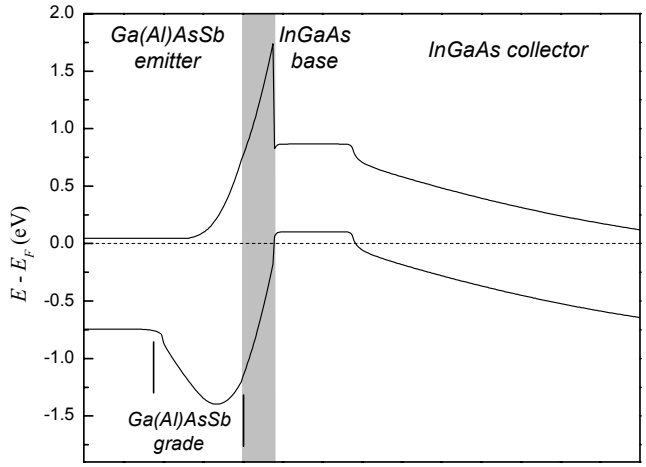


Figure 5.5 Band diagram of the Generation Ø HBT. The shaded region indicates the location of the AlAsSb/oxide aperture layer.

A Gummel plot for a HBT with an active emitter area, A_E, of $3 \times 9\ \mu m^2$ and a collector area, A_C, of $4 \times 10\ \mu m^2$ is presented in Figure 5.6. The common-emitter current gain, β, is on the order of 10^{-5}. Examination of the base-emitter diode characteristic shows an ideality factor, η, of approximately 1.7. The essentially non-

existent collector current, correspondingly low β, and high ideality factor suggest that the majority of the current in the base-emitter junction is due to recombination of emitter electrons and base holes, most probably occurring at the oxide aperture within the *pn* junction depletion region. The result is a base current nearly equivalent to the emitter current that further resulted in a non-existent collector current and current gain.

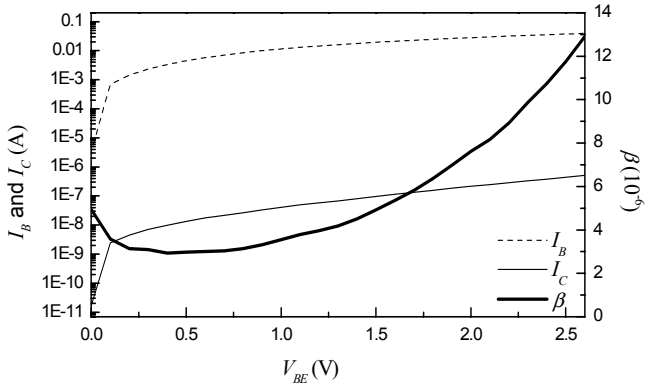


Figure 5.6 Gummel plot of a Generation Ø HBT. The emitter area (A_E) was 3×9 μm^2; the collector area (A_C), 4×10 μm^2. Note, the current gain is scaled by 10^{-6}.

The result of these experiments prompted the oxide aperture diode study presented in Chapter 4.

5.4 Oxide Aperture HBT: Generation I

The Generation I oxide aperture HBTs were the first devices fabricated with the knowledge gained from the oxide aperture diode experiments presented in Chapter 4. For this generation, the *exact same wafer* that was used to fabricate the 500 Å base-emitter grade oxide aperture diodes in Chapter 4 was used to fabricate the transistors.

The only differences between this generation of HBTs and the final generation, Generation II, is the doping level in the emitter and base regions and the thickness of the collector (Figure 5.7): the $GaAs_{0.49}Sb_{0.51}$ sub-emitter was doped 5×10^{18} cm^{-3} with Te; the linear grade from $GaAs_{0.49}Sb_{0.51}$ to $AlAs_{0.56}Sb_{0.44}$, 5×10^{17} cm^{-3} (Te); the $AlAs_{0.56}Sb_{0.44}$ emitter, 5×10^{17} cm^{-3} (Te); the base-emitter grade from $AlAs_{0.56}Sb_{0.44}$ to $GaAs_{0.49}Sb_{0.51}$, 1×10^{17} cm^{-3} (Te); and the $GaAs_{0.49}Sb_{0.51}$ base, 5×10^{18} cm^{-3} (Be). The thickness of the collector is the same as in the Generation Ø HBTs, 2000 Å.

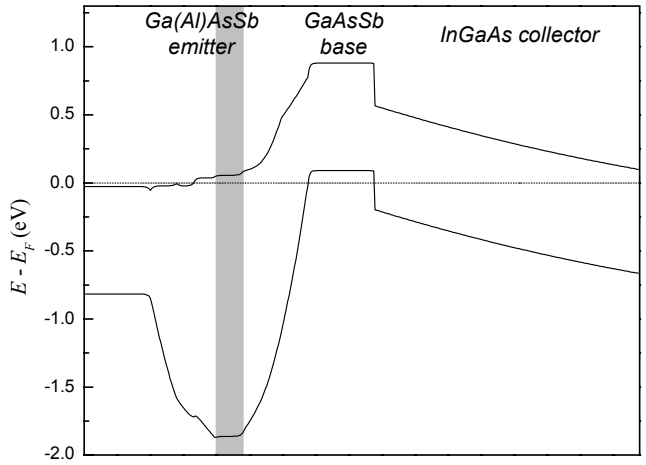


Figure 5.7 Band diagram of the Generation I HBT. The shaded region indicates the location of the AlAsSb/oxide aperture layer, bounded by two linearly graded layers.

A Gummel plot and common-emitter current-voltage characteristic of the Generation I oxide aperture HBTs is shown in Figure 5.8. These devices showed a considerably high β of approximately 90, but the ideality factors for the base current (η_B) and collector current (η_C) were surprisingly high ($\eta_{B,min} \simeq 3.34$, $\eta_{C,min} \simeq 2.95$), suggesting that the characteristics are resistively limited. These results were unexpected given that these devices were fabricated from the same wafer of

semiconductor material as the 500 Å oxide diodes from Chapter 4, which displayed an $\eta \simeq 1.01$. Additionally, the non-saturating common-emitter characteristic was unanticipated.

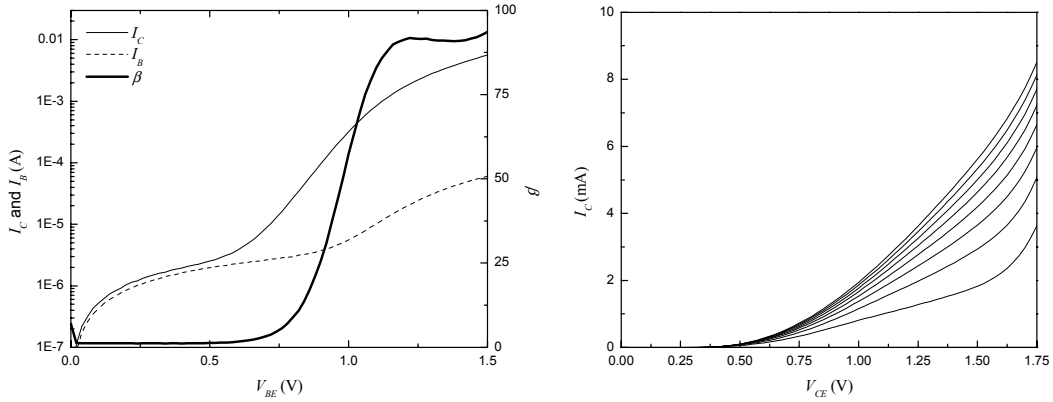


Figure 5.8 Gummel plot and common-emitter characteristic ($I_B = 0 \sim 90$ μA at 10 μA steps) of a $A_C = 4 \times 10$ μm^2 Generation I HBT.

To better understand the common-emitter characteristics observed in Figure 5.8, it would be useful to introduce two terms: the offset voltage, V_{offset}, and the knee voltage, V_{knee}. The offset voltage and knee voltage, in addition to the breakdown

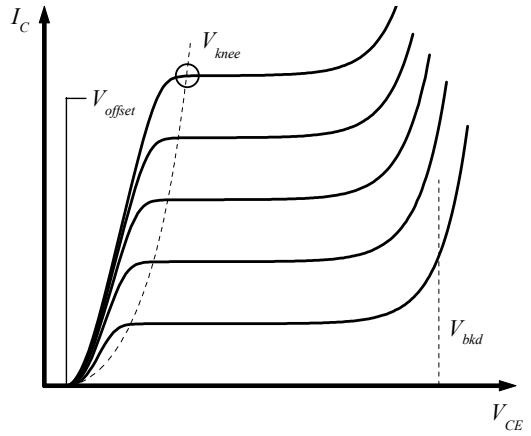


Figure 5.9 Illustration of a common-emitter characteristic showing the offset voltage (V_{offset}), the knee voltage (V_{knee}), and the breakdown voltage (V_{bkd}).

voltage (V_{bkd}), are useful in determining the voltage range over which a transistor can be operated as an amplifier (Figure 5.9). V_{offset} is defined as the collector-emitter voltage at which $I_C = 0$. V_{knee} is defined as the collector-emitter voltage at which the device shifts between forward-saturation and forward-active modes ($V_{BC} = 0$). Using an Ebers-Moll model that includes extrinsic resistances, V_{offset} and V_{knee} may be expressed as follows:

$$V_{offset} \simeq \eta_{bc} \frac{kT}{q} \ln\left(\frac{I_{bc,sat}}{\alpha_F I_{be,sat}}\right) + \left(1 - \frac{\eta_{bc}}{\eta_{be}}\right)\left(V_{BE} - I_B R_B\right) + \frac{\eta_{bc}}{\eta_{be}} I_B R_B \tag{5.1}$$

$$V_{knee} \simeq \frac{\eta_{be} kT}{q} \ln\left[\frac{I_E - \alpha_R I_C}{I_{be,sat}\left(1 - \alpha_F \alpha_R\right)}\right] - \frac{\eta_{bc} kT}{q} \ln\left[\frac{\alpha_F I_E - I_C}{I_{bc,sat}\left(1 - \alpha_F \alpha_R\right)}\right] + I_E R_E + I_C R_C \tag{5.2}$$

where k is the Boltzmann constant (8.62×10^{-5} eV/K), T is the absolute temperature of the semiconductor, and q is the electronic charge (1.602×10^{-19} C); I_{be}, $I_{be,sat}$, and η_{be} are the total current, the saturation current, and the ideality factor of the base-emitter diode, respectively; I_{bc}, $I_{bc,sat}$, and η_{bc} are the total current, the saturation current, and the ideality factor of the base-collector diode, respectively; α_F and α_R are the forward-active and reverse-active common-base current gains; V_{BE} is the applied base-emitter voltage; I_B, I_E, and I_C are the base, emitter and collector currents, respectively; and R_B, R_E, and R_C are the extrinsic base, emitter, and collector resistances, respectively. A complete presentation of the Ebers-Moll model including extrinsic resistances and the derivation of Equations (5.1) and (5.2) are presented in Appendix C.

From Equation (5.2) for V_{knee} it is clear that any emitter resistance, R_E, would lead to an increase in the knee voltage. If the emitter resistance is sufficiently high, the knee voltage could be pushed out beyond the breakdown region resulting in a characteristic like that observed in Figure 5.8 (Figure 5.10).

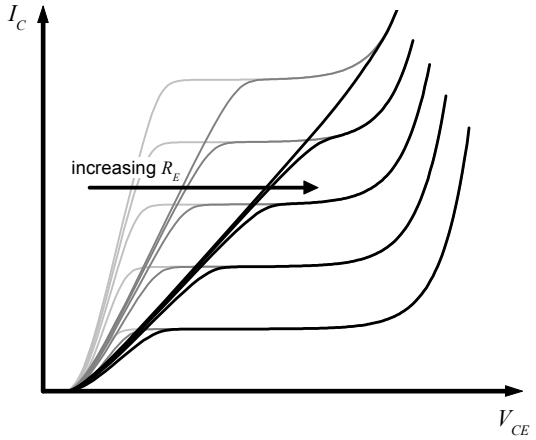


Figure 5.10 Illustration of the effect of increasing emitter resistance (R_E) on the common-emitter characteristics of an HBT.

The emitter resistance as measured by floating-collector measurements (also known as open-collector measurements) for these HBTs is approximately 85 Ω (Figure 5.11a). The oxide diodes of similar size from Chapter 4 also show correspondingly high resistance (Figure 5.11b). A collector current of 4 mA with an emitter resistance of 85 Ω alone would lead to an increase in V_{knee} of approximately 0.34 V. Additional increases from the logarithmic terms and possibly the R_C term in Equation (5.2) could easily result in the characteristic observed in Figure 5.8.

Clearly from the characteristics observed in Figure 5.8 and Figure 5.11 and the behavior suggested by Equations (5.1) and (5.2), it can be stated that the Generation I

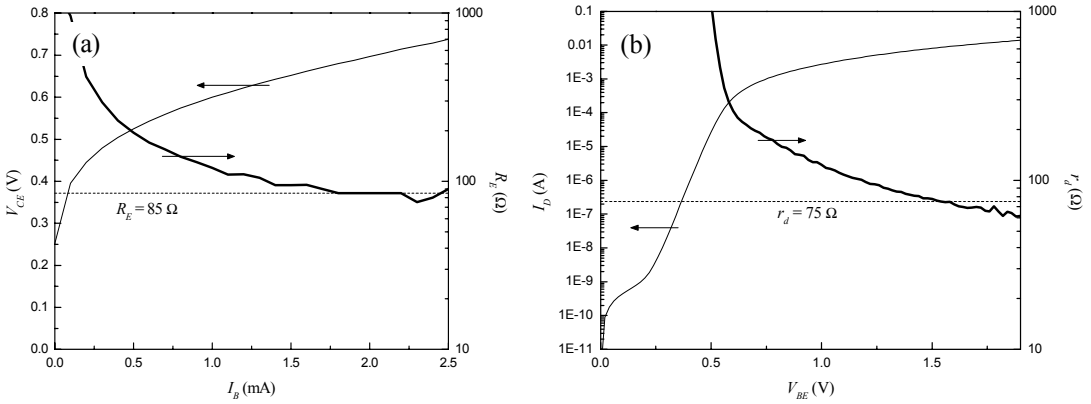


Figure 5.11 (a) Floating-collector measurement of a Generation I HBT ($A_E = 3.5 \times 9.5\ \mu m^2$, $A_C = 4 \times 10\ \mu m^2$). (b) Dynamic resistance of an oxide aperture diode with an aperture area of $4 \times 10\ \mu m^2$.

oxide aperture HBTs suffer from a large emitter resistance ($R_E = 85\ \Omega$) that results in the Gummel and common-emitter characteristics seen in Figure 5.8.

5.5 Oxide Aperture HBT: Generation II

The Generation II HBTs, the final generation of oxide aperture transistors presented in this dissertation, are nearly identical to the previous generation except for the increased doping in the emitter and base to reduce the parasitic resistances and a thicker collector (3000 Å) for an increased breakdown voltage.

Gummel and common-emitter characteristics for three sizes of Generation II HBTs are shown in Figure 5.12: a transistor with a $0.5 \times 9.5\ \mu m^2$ emitter area and $1 \times 10\ \mu m^2$ collector area (referred to as a 1×10 transistor), a transistor with $A_E = 1.5 \times 9.5\ \mu m^2$ and $A_C = 2 \times 10\ \mu m^2$ (2×10 transistor), and a transistor with $A_E = 3.5 \times 9.5\ \mu m^2$ and $A_C = 4 \times 10\ \mu m^2$ (4×10 transistor).

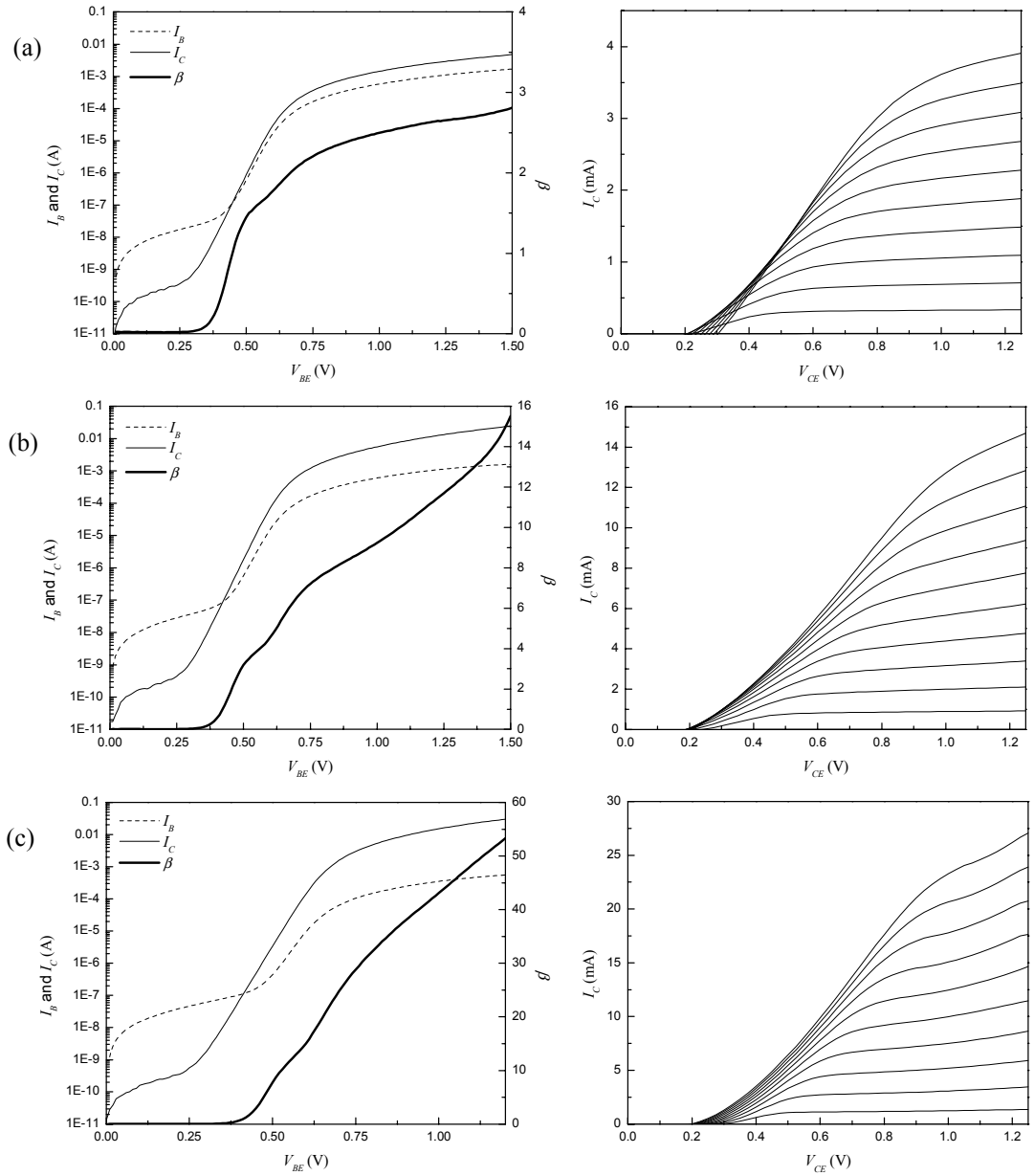


Figure 5.12 Gummel and common-emitter characteristic plots of (a) a $A_C = 1 \times 10\ \mu m^2$ ($A_E = 0.5 \times 9.5\ \mu m^2$) HBT ($I_B = 0 \sim 1.5$ mA at 150 μA steps), (b) a $A_C = 2 \times 10\ \mu m^2$ ($A_E = 1.5 \times 9.5\ \mu m^2$) HBT ($I_B = 0 \sim 1.25$ mA at 125 μA steps), and (c) a $A_C = 4 \times 10\ \mu m^2$ ($A_E = 3.5 \times 9.5\ \mu m^2$) HBT ($I_B = 0 \sim 0.5$ mA at 50 μA steps).

These devices, like the previous generation, show a considerably high gain. However, in strong contrast to the previous generations' characteristics, this

generation displays excellent ideality factors for the base and collector currents ($\eta_B = 1.18,\ \eta_C = 1$). As a result of the increased doping in the emitter and base, the knee voltage and offset voltage have decreased, as well as transistor's emitter resistance (Figure 5.13).

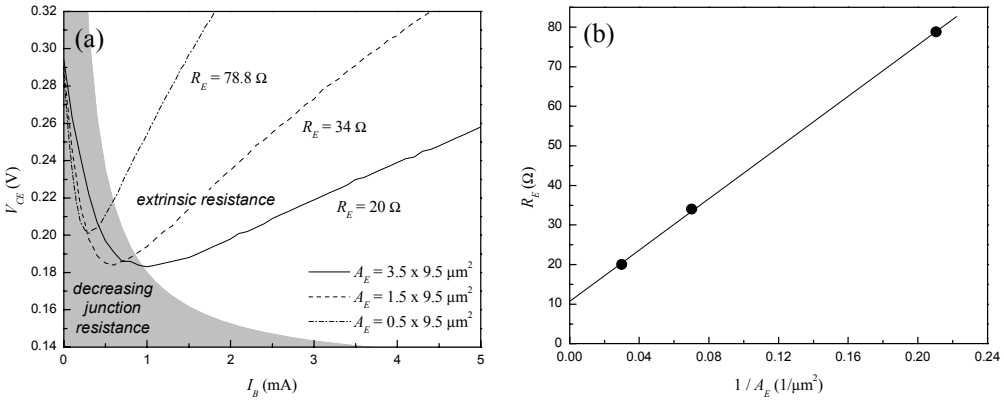


Figure 5.13 (a) Floating-collector measurements. (b) Resulting emitter resistance plotted against $1/A_E$.

Though the emitter resistance has reduced with respect to the Generation I HBTs, it is still relatively high. The fact that the emitter resistance (R_E) increases linearly with the inverse of the emitter area (A_E) indicates that the internal (vertical) resistance of the wide bandgap emitter, which scales with emitter area, dominates over the access (lateral) resistance of the sub-emitter, which is essentially independent of emitter area (Figure 5.14). This is not surprising given the poor mobility of electrons in $AlAs_{0.56}Sb_{0.44}$ ($\mu_n \simeq 40$ cm^2/Vsec at $n = 2 \times 10^{18}$ cm^{-3}).

The breakdown of these devices was lower than that observed for the Generation I HBTs even though the collectors were thicker (Figure 5.15). The lower breakdown

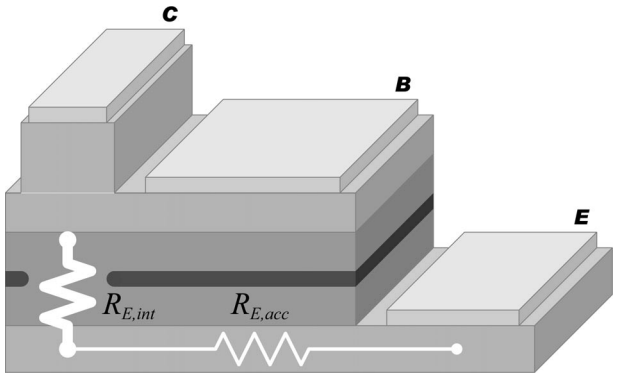


Figure 5.14 Illustration of the two resistances composing the total emitter resistances (R_E): the internal resistance ($R_{E,int}$), which scales with emitter area (A_E), and the lateral access resistance ($R_{E,acc}$), which is essentially independent of A_E.

and increase in output conductance, especially at higher current densities, is believed to be due to impact ionization in the collector and not the Early Effect.

The increase of collector current (I_C) with increased collector-emitter voltage (V_{CE}) associated with the Early Effect is a result of an increased current gain, arising from an increase in the base depletion width at the base-collector junction and the

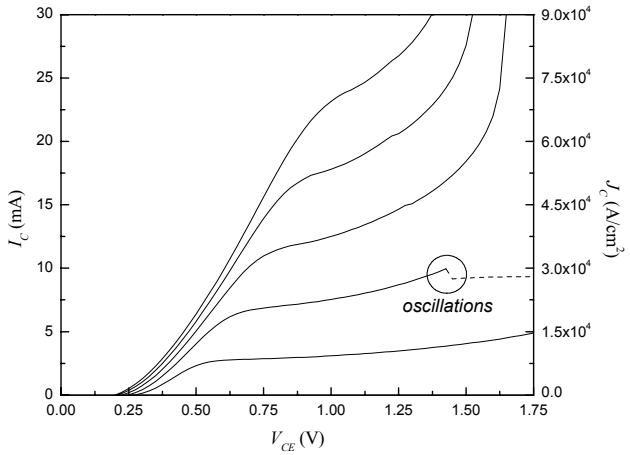


Figure 5.15 Common-emitter characteristics of a 4 × 10 HBT (I_B = 0 ~ 0.6 mA at 100 μA steps) showing breakdown at low biases for the higher collector current densities.

corresponding decrease in the neutral base width ($W_{B,neutral}$) as a consequence of the increased reverse bias across the base-collector junction (V_{BC}) (Figure 5.16a). Because the depletion width in the base is roughly proportional to $1/\sqrt{N_{base}}$ (at a fixed bias), only transistors with fairly low doping in the base suffer from the Early Effect. A figure-of-merit for the Early Effect is the Early voltage (V_A), defined as the negative value of the voltage at which the extrapolated output characteristics reach zero (Figure 5.16b):

$$V_A \simeq \frac{qN_{base}W_B^{\,2}}{\varepsilon_{base}}\left(1+\frac{N_{base}}{N_{collector}}\right) \tag{5.3}$$

N_{base} is the doping in the base, $N_{collector}$ is the doping in the collector, W_B is the total base width, and ε_{base} is the permittivity of the base material.

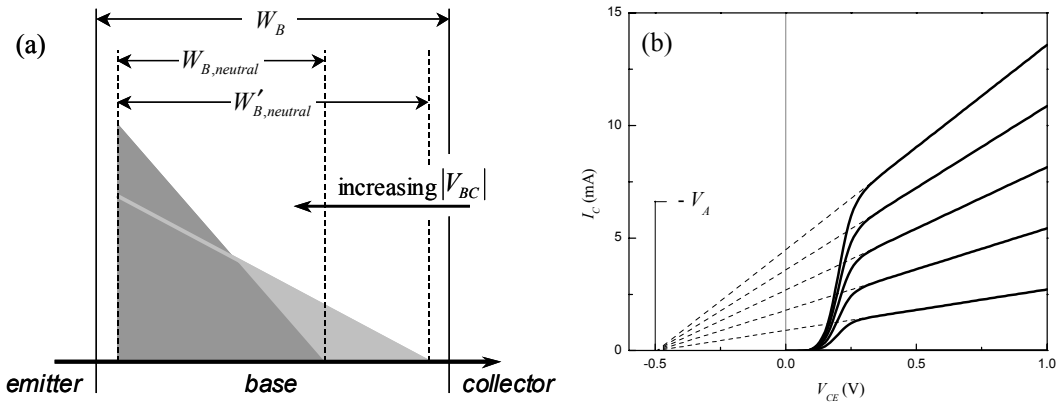


Figure 5.16 (a) Illustration of the base minority carrier profile under the Early Effect. As V_{CE} is increased, the reverse bias on the base-collector junction correspondingly increases resulting in the neutral base width decreasing from $W'_{B,neutral}$ to $W_{B,neutral}$. The resultant change in neutral base width alters the charge profile in the base (gray triangles) resulting in an increase β and I_C (the change in $W_{B,neutral}$ is exaggerated for illustrative purposes). (b) Illustration of a transistor suffering from the Early Effect (V_A = 0.5 V).

The Early voltage should be fairly constant with bias and independent of device size.[2,3] The extrapolated Early voltage of the Generation II transistors varies strongly with base current, *decreasing* in value with increasing base current, and is strongly *dependent* upon emitter area (Figure 5.17). This, in addition to the fact that these devices have a highly doped base ($N_{base} = 5 \times 10^{19}$ cm^{-3}), suggests that these transistors do not suffer from the Early Effect.

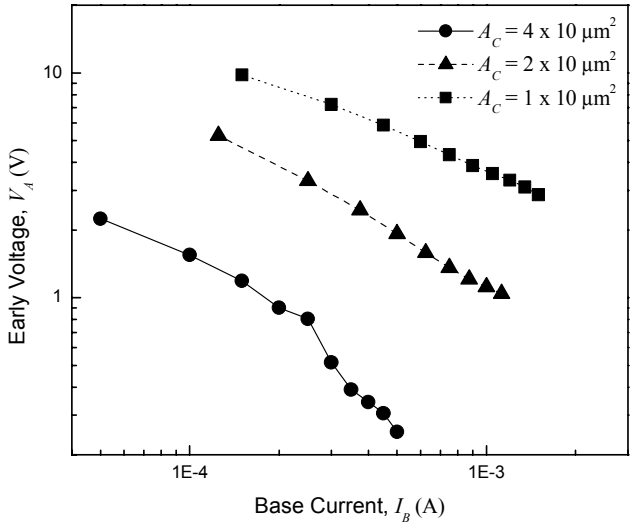


Figure 5.17 Extrapolated Early voltage (V_A) versus base current (I_B).

On the other hand, impact ionization in $In_{0.53}Ga_{0.47}As$ can occur at lower electric fields, as compared to other III-V semiconductors, due to a high ionization coefficient, α_n (Figure 5.18).[4,5] Additionally, the increased initial kinetic energy of electrons entering the collector as a result of the conduction band offset between the $GaAs_{0.49}Sb_{0.51}$ base and $In_{0.53}Ga_{0.47}As$ collector ($\Delta E_C \simeq 0.31$ eV, Figure 5.1), which acts like an electron launcher, reduces the required ionization energy ($E_{ion} \simeq 0.83$ eV)

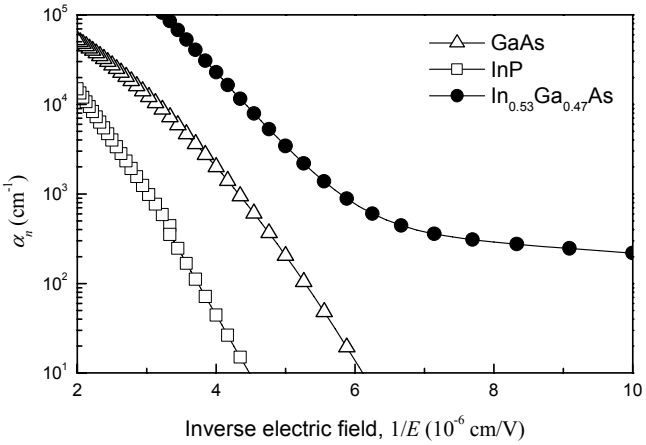


Figure 5.18 Ionization coefficient for GaAs, InP, and $In_{0.53}Ga_{0.47}As$ versus inverse electric field.[4,7]

and, consequently, electric field for impact ionization to occur, leading to increased impact ionization at lower collector-base (and therefore collector-emitter) voltages.[6]

The conclusion that the increased output conductance is due to impact ionization is also supported by the extracted Early voltages in Figure 5.17. As the device size increases, the emitter resistance decreases (Figure 5.13), resulting in a larger voltage falling across the base-collector junction for a given collector-emitter voltage, which increases the amount of impact ionization in the collector. The increase in impact ionization is reflected in an increase in the output conductance and decrease in extracted Early voltage with emitter area (Figure 5.17).

Examination of the Gummel plots (Figure 5.12) shows a reduction in β as emitter area (A_E) decreases. The best device measured ($A_E = 2.5 \times 8.5$ μm^2, $A_C = 4 \times 10$ μm^2) showed a higher β, equivalent to that measured for the Generation I transistors (Figure 5.19). The increased gain of this transistor and reduced gains of the 2×10

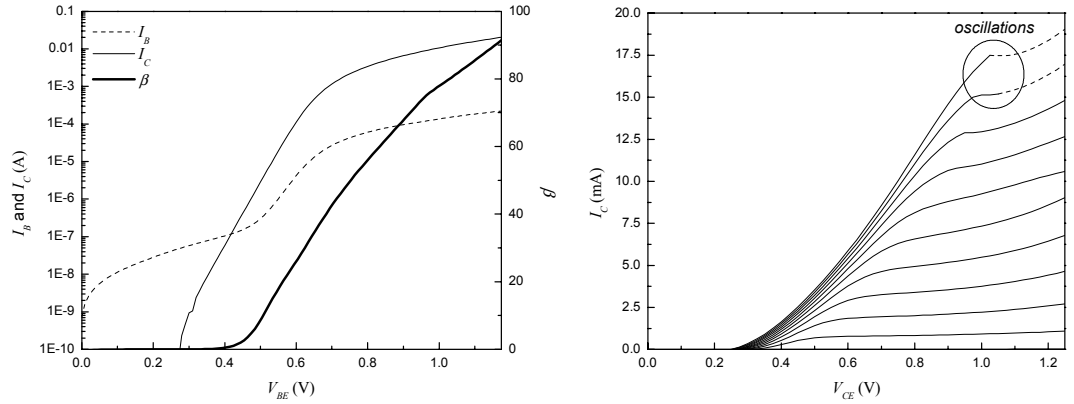


Figure 5.19 Gummel and common-emitter characteristic plots of a $A_E = 2.5 \times 8.5\ \mu m^2$, $A_C = 4 \times 10\ \mu m^2$ HBT ($I_B = 0 \sim 0.2$ mA at 20 μA steps).

and 1×10 devices, relative to the 4×10 transistor, are most probably a consequence of lateral diffusion of injected electrons in the base, as well as possibly a partially undepleted emitter.

In a device such as the oxide aperture HBT, where the collector area (A_C) is on the order of the emitter area (A_E) and the base contacts are located "within the path" of injected carriers, lateral diffusion of injected carriers outside of the collector area can

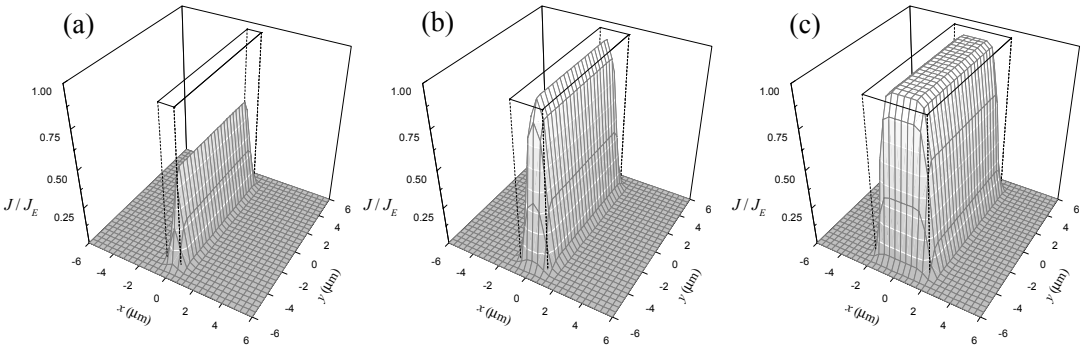


Figure 5.20 Modeled current density profiles at the base-collector junction for (a) $A_E = 0.5 \times 9.5\ \mu m^2$, $A_C = 1 \times 10\ \mu m^2$; (b) $A_E = 1.5 \times 9.5\ \mu m^2$, $A_C = 2 \times 10\ \mu m^2$; (c) $A_E = 3.5 \times 9.5\ \mu m^2$, $A_C = 4 \times 10\ \mu m^2$. The square in each plot outlines the collector area (A_C).

lead to a reduction of gain. By using a simple model for current gain based on lateral diffusion of carriers (Figure 5.20, Appendix D), it can be seen that as the areas of the emitter and collector are reduced, a greater portion of electrons diffuse outside of the collector area leading to a reduction in gain (Figure 5.21).

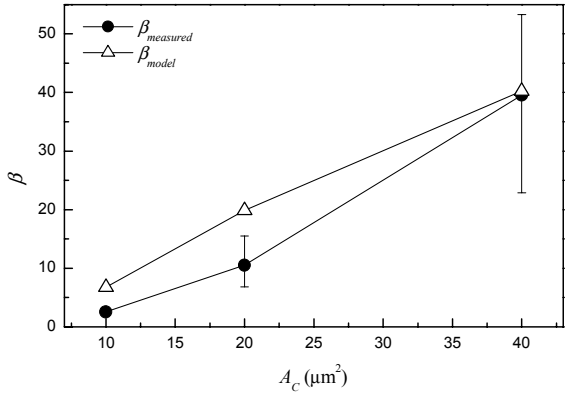


Figure 5.21 Measured and modeled current gain (β) versus collector area (A_C). The error bars on the measured β outline the practical range of gain for each device.

The validity of this model requires that the emitter current density ($J_E = I_E / A_E = (I_B + I_C) / A_E$) be constant with respect to emitter area (A_E). Figure 5.22 shows this to be true for the oxide aperture HBT.

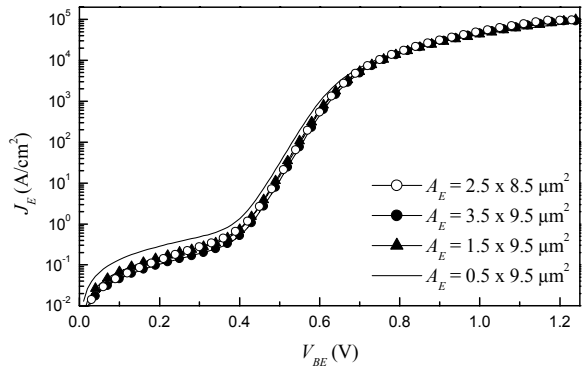


Figure 5.22 Emitter current density (J_E) for HBTs with different emitter areas (A_E)

5.6 Misaligned HBTs

Unlike conventional HBTs in which the active collector area is larger than the active emitter area, oxide aperture HBTs have active collector and emitter areas of approximately the same size (Figure 5.23). As a result, the alignment of the emitter and collector areas strongly affects the transistor's characteristics.

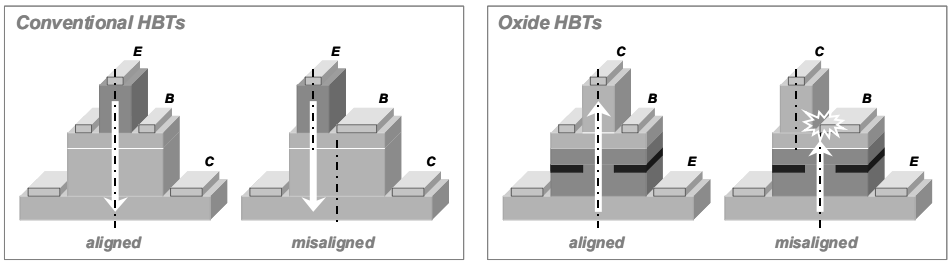


Figure 5.23 Conventional and oxide aperture HBTs: aligned and misaligned HBTs. Generally, current transport is unaffected in conventional HBTs by misalignment between emitter and collector. However, the current transport in oxide aperture HBTs is radically affected by misalignment between emitter and collector.

Simply stated, a misaligned emitter-collector results in current not being directly injected into the collector but into both the collector and the base. The result is an increase in the base current and decrease in the collector current for the same emitter current, which translates into a decreased current gain. Figure 5.24 shows examples of misaligned HBTs' Gummel and common-emitter characteristics compared to an aligned transistor.

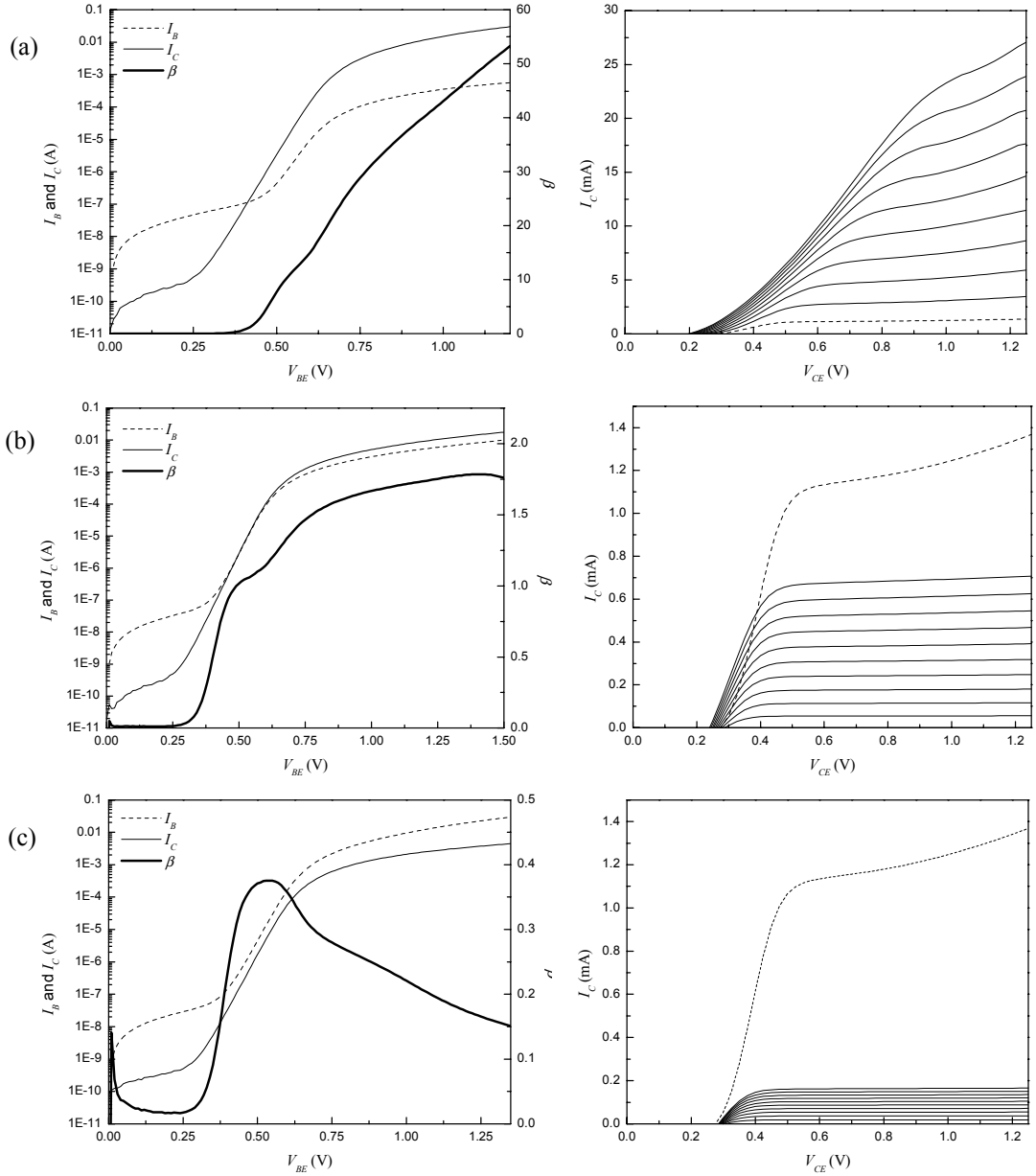


Figure 5.24 Gummel and common-emitter characteristics for misaligned HBTs ($A_E = 3.5 \times 9.5\ \mu m^2$, $A_C = 4 \times 10\ \mu m^2$) with (a) 0 μm misalignment between emitter and collector junctions, (b) a 1 μm misalignment, (c) and a 2 μm misalignment. For all characteristics $I_B = 0 \sim 0.5$ mA at 50 μA steps. For the two misaligned HBTs, the $I_B = 50$ μA curve from the 0 μm misalignment HBT (dashed line) is include for comparison.

5.7 RF Measurements

Scattering parameter (*S*-parameter) measurements were performed on the Generation II HBTs to evaluate the transistors' frequency performance. From *S*-parameter measurements, characteristics like the short-circuit current gain (h_{21}) and unilateral power gain (U) can be extracted (Figure 5.25). Subsequently, the current-gain cutoff frequency (f_τ) and the maximum frequency of oscillation (f_{max}) can be found (Figure 5.26).

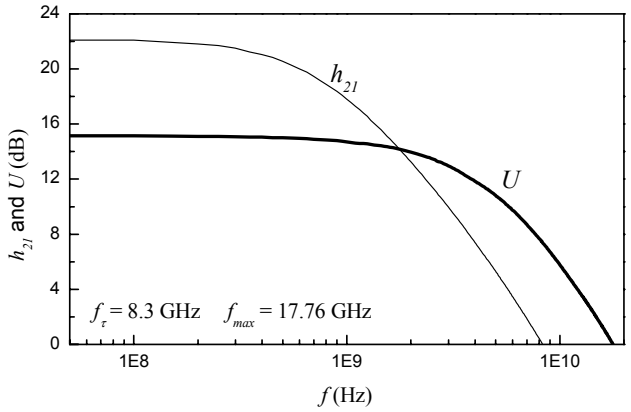


Figure 5.25 h_{21} and U from *S*-parameter measurements of a 2×10 HBT (I_C = 9.015 mA, V_{CE} = 2.0 V).

The values of $f_\tau = 8.3$ GHz and $f_{max} = 17.76$ GHz, from Figure 5.26, are much lower than expected. Calculations, using the measured emitter resistance and base resistance and assuming a fully depleted collector, suggests these devices should have an f_τ on the order of 25 GHz and $f_{max} \simeq 35$ GHz. These values were calculated using a classical hybrid-π model for a bipolar transistor (Figure 5.27).

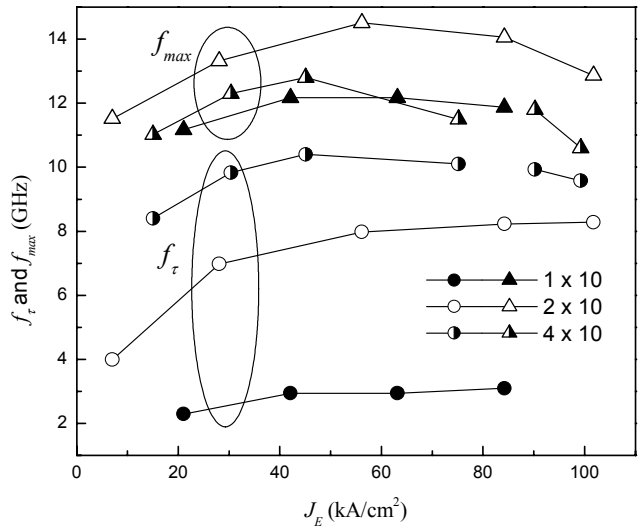


Figure 5.26 f_τ and f_{max} as a function of emitter current density (J_E) for a 1×10 (V_{CE} = 1.5 V), 2×10 (V_{CE} = 1.3 V), and 4×10 (V_{CE} = 1.25 V) HBT.

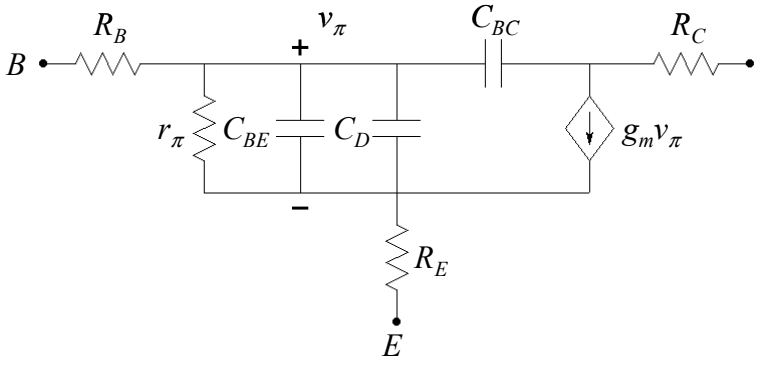


Figure 5.27 Classical hybrid-π model of a bipolar transistor.

Re-examination of the structure of the oxide aperture HBT suggests that an additional parasitic capacitance in the base-emitter junction exists as a result of the collector-up design (Figure 5.28), resulting in a modified hybrid-π model of the transistor (Figure 5.29).

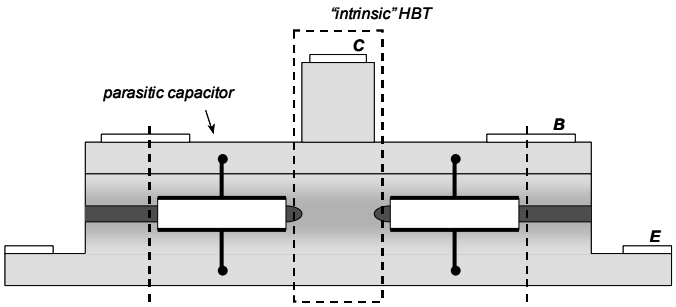


Figure 5.28 Illustration of an oxide aperture HBT indicating the location of the parasitic base-emitter capacitance.

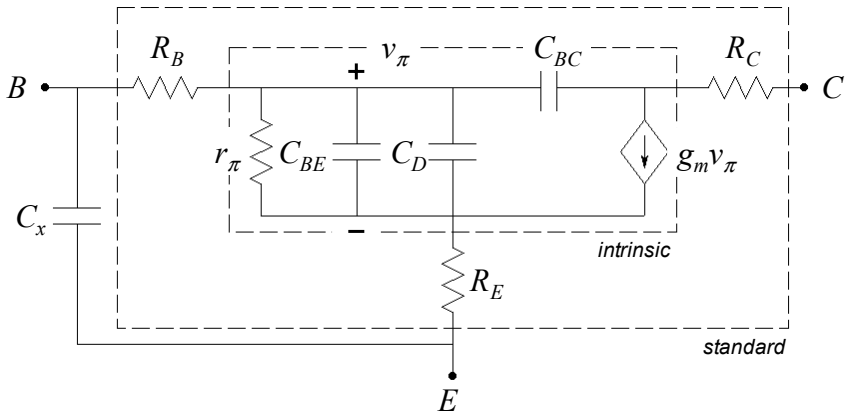


Figure 5.29 Modified hybrid-π model that includes a parasitic base-emitter capacitance, C_x.

Solving for f_τ and f_{max} of the modified model results in (Appendix E):

$$f_{\tau,x} = \frac{1}{2\pi}\left[\tau_{\tau,std} + \left(\frac{\eta V_T}{I_C} + \frac{R_B}{\beta_o} + R_E\right)C_x\right]^{-1}$$
$$\tau_{\tau,std} = \frac{\eta V_T}{I_C}\left(C_{BE} + C_{BC}\right) + \tau_B + \tau_C + \left(R_E + R_C\right)C_{BC} \tag{5.4}$$

$$f_{max,x} = f_{max,std} = \sqrt{\frac{f_{\tau,std}}{8\pi R_B C_{BC}}} \neq \sqrt{\frac{f_{\tau,x}}{8\pi R_B C_{BC}}} \tag{5.5}$$

Where $\tau_{\tau,std}$ is the time constant corresponding to the cutoff frequency of the standard model ($f_{\tau,std}$), β_o is the DC current gain of the device, and C_x is the parasitic base-emitter capacitance. The remaining variables are as defined in Chapter 3. The two key results of Equations (5.4) and (5.5) is that C_x introduces an additional time constant, which reduces f_τ while f_{max} is *unaffected* by the additional capacitance and remains related to the f_τ of the transistor *without* the parasitic capacitor.

f_τ of the oxide aperture HBT was at first expected to be fairly independent of device size. Recognizing $A_E \simeq A_C$, $f_{\tau,std}$ can be written as:

$$\begin{aligned} f_{\tau,std} &= \frac{1}{2\pi}\left[\frac{\eta V_T}{J_C \cancel{A_C}}\left(c_{be}\cancel{A_E} + c_{bc}\cancel{A_C}\right) + \tau_B + \tau_C + \left(\frac{r_e}{\cancel{A_E}} + \frac{r_c}{\cancel{A_C}}\right)c_{bc}\cancel{A_C}\right]^{-1} \\ &= \frac{1}{2\pi}\left[\frac{\eta V_T}{J_C}\left(c_{be} + c_{bc}\right) + \tau_B + \tau_C + \left(r_e + r_c\right)c_{bc}\right]^{-1} \end{aligned} \tag{5.6}$$

Where $c_{be} = C_{BE}/A_E$ and $c_{bc} = C_{BC}/A_C$ are the capacitances per unit area for the base-emitter and base-collector junctions, and $r_e \simeq R_E A_E$ and $r_c = R_C A_C$ are the area-independent representations of the emitter and collector resistance.

In actuality, f_τ is strongly dependent upon device size as a result of the parasitic base-emitter capacitance term in Equation (5.4) (Figure 5.30). Taking C_x to be equal to $\varepsilon_x/d_x \cdot A_x$, where ε_x/d_x is representative of the parallel combination of the

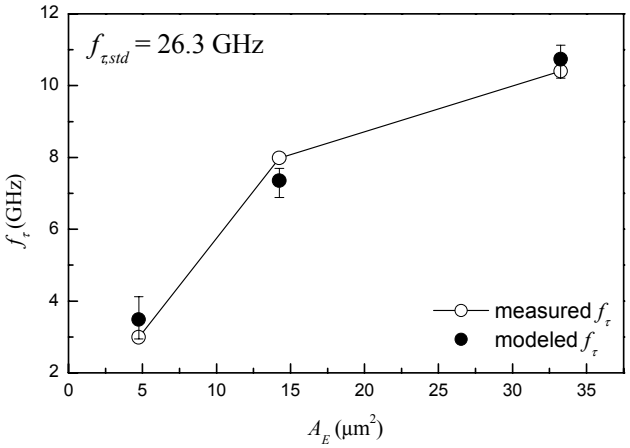


Figure 5.30 f_τ versus emitter area (A_E). $f_{\tau,std}$ is approximately 26.3 GHz and $\delta_x \simeq 6.06$ μm.

capacitors comprising C_x and A_x is the area of C_x, and assuming A_x is fixed with reference to the emitter area (Figure 5.31), $f_{\tau,x}$ can be written as a function of $A_E = l_E w_E$.

$$C_x = \frac{\varepsilon_x}{d_x} A_x = \frac{\varepsilon_x}{d_x}\left[\left(A_x + A_E\right) - A_E\right] = \frac{\varepsilon_x}{d_x}\left[\left(l_E + 2\delta_x\right)\left(w_E + 2\delta_x\right) - l_E w_E\right] \qquad (5.7)$$

$$f_{\tau,x} = \frac{1}{2\pi}\left[\tau_{\tau,std} + \left(\frac{\eta V_T}{I_C\left(A_E\right)} + \frac{R_B\left(A_E\right)}{\beta_o\left(A_E\right)} + R_E\left(A_E\right)\right) C_x\left(A_E\right)\right]^{-1} \qquad (5.8)$$

Where δ_x is the effective "width" of C_x. Applying Equation (5.8) to the measured data (Figure 5.30), allowing $\tau_{\tau,std}$ and δ_x to be the only variables, results in $f_{\tau,std} = 1/2\pi\tau_{\tau,std} \simeq 26.3$ GHz with $\delta_x \simeq 6.06$ μm.

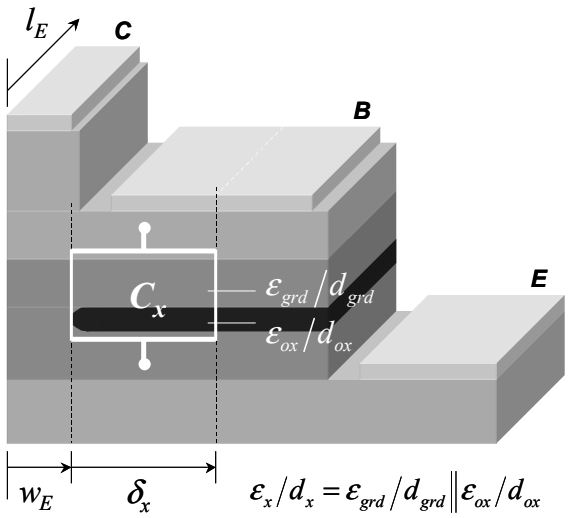


Figure 5.31 Illustration of the parasitic base-emitter capacitance, C_x.

Examination of f_τ as a function of collector-emitter voltage (V_{CE}) and collector current (I_C) shows that f_τ is essentially independent of bias (Figure 5.32). This is due to the strong dependence of f_τ on the parasitic base-emitter capacitor, C_x. Looking at Equation (5.4), assuming the C_x term dominates, f_τ should increase as I_C increases until $\eta V_T / I_C \ll (R_B/\beta_o + R_E)$, at which point f_τ "saturates" being limited by the RC_x time constant (Figure 5.32b).

On the other hand, f_{max} increases with increasing V_{CE} (Figure 5.32a and Figure 5.33). This suggests that the collector in not fully depleted, leading to a higher value for C_{BC} and a lower f_{max} than as expected. Using the extracted value of

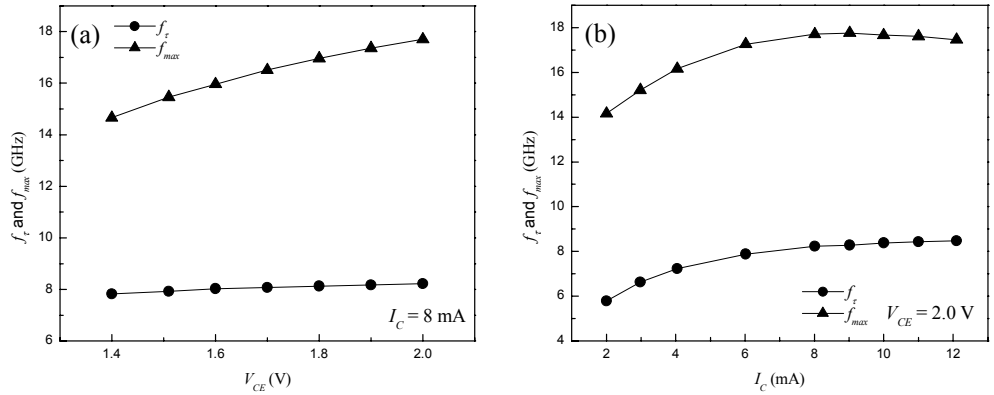


Figure 5.32 f_τ and f_{max} versus (a) collector-emitter voltage (V_{CE}) and (b) collector current (I_C) for a 2×10 HBT.

$f_{\tau,std} \simeq 26.3$ GHz from Equation (5.8) and Figure 5.30 and the measured $f_{max} \simeq 17.76$ GHz and $R_B \simeq 83\ \Omega$ suggests $C_{BC} \simeq 40$ fF ($W_{C,dep} \simeq 1000$ Å) for the 2×10 HBT.

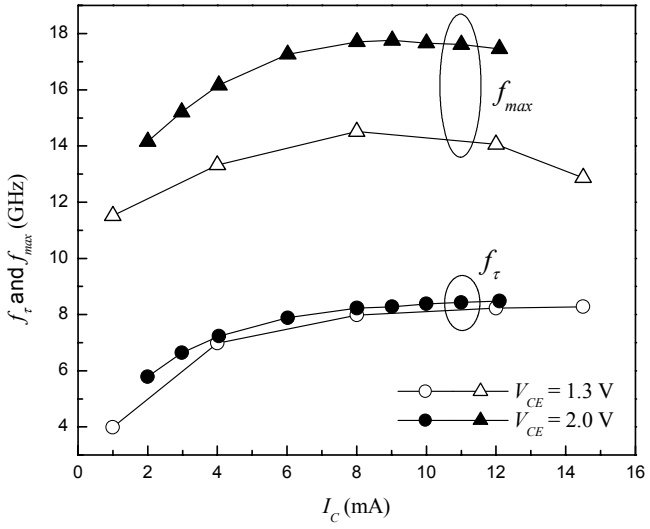


Figure 5.33 f_τ and f_{max} versus collector current (I_C) at two collector-emitter biases (V_{CE}) for a 2×10 HBT. Note that f_τ saturates to approximately the same value (~8.3 GHz) independent of V_{CE}.

5.8 High-Frequency Device Model

Proper high-frequency model extraction requires (***1***) a well-behaved, stable device from which the model parameters will be extracted and (***2***) *Y*-parameters that accurately represent the device. The oxide aperture HBTs presented in this dissertation are very stable, showing reproducible results, which involved multiple measurements spanning many weeks. The difficulty in modeling the oxide aperture HBT is in presenting an accurate representation of the device in terms of *Y*-parameters.

The *Y*-parameters derived in Appendix E, though correct for the model presented there (Figure 5.29), were derived assuming that the base-collector resistance (r_{BC}) and output resistance (r_o) were infinite, and are therefore not a completely accurate representation of the oxide aperture HBT.

The DC *Y*-parameters for that model are:

$$\mathbf{Y}^{\mathbf{x}}\Big|_{\omega\to 0} \simeq \begin{bmatrix} \left(r_\pi + R_B + \beta_o R_E\right)^{-1} & 0 \\ \dfrac{g_{mo}}{1 + g_{mo}\left(R_B/\beta_o + R_E\right)} & 0 \end{bmatrix} \tag{5.9}$$

Assuming r_{BC} is *not* infinite, it can be shown that the DC parameters become:

$$
\begin{aligned}
Y_{11}^{x}\Big|_{\omega\to 0} &\simeq \frac{r_\pi + r_{BC}}{R_B\left(r_\pi + \beta_o R_E\right) + r_{BC}\left(r_\pi + R_B + \beta_o R_E\right)} \\
Y_{12}^{x}\Big|_{\omega\to 0} &\simeq -\frac{r_\pi + \beta_o R_E}{R_B\left(r_{BC} + r_\pi + \beta_o R_E\right) + r_{BC}\left(r_\pi + \beta_o R_E\right)} \\
Y_{21}^{x}\Big|_{\omega\to 0} &\simeq \frac{g_{mo}\left(r_{BC} - R_E\right)}{R_B\left(1 + g_{mo}R_E\right) + r_{BC} + g_{mo}r_{BC}\left(\dfrac{R_B}{\beta_o} + R_E\right)} \\
Y_{22}^{x}\Big|_{\omega\to 0} &\simeq \frac{g_{mo}\left(R_B + R_E\right)}{R_B\left(1 + g_{mo}R_E\right) + r_{BC} + g_{mo}r_{BC}\left(\dfrac{R_B}{\beta_o} + R_E\right)}
\end{aligned}
\tag{5.10}
$$

Setting $r_{BC} \to \infty$, Equation (5.10) reduces to Equation (5.9).

Equation (5.10), though still not completely correct, is a more accurate representation of the oxide aperture HBT and can be used for an initial estimate of the base-collector resistance, r_{BC}. Together with the measured emitter resistance ($R_E \simeq 34\ \Omega$, Figure 5.13), base resistance ($R_B \simeq 117\ \Omega - R_E \simeq 83\ \Omega$, Figure 5.34),

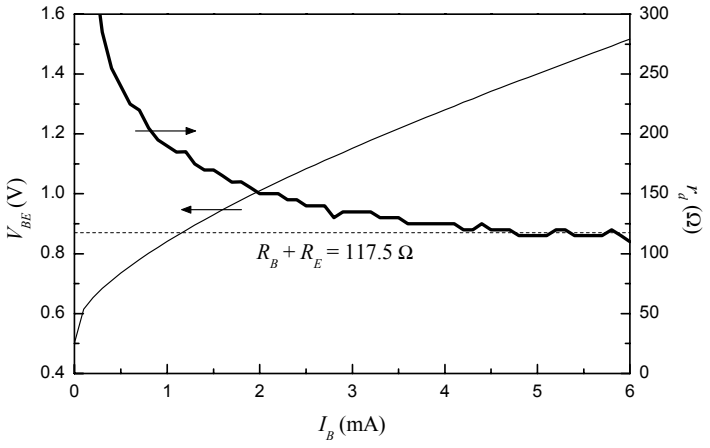


Figure 5.34 Dynamic resistance (r_d) of the base-emitter diode from a 2 × 10 HBT. At higher currents, the dynamic resistance is equivalent to the sum of the base and emitter resistances.

current gain ($\beta_o \simeq h_{21}\big|_{f\to 0} \simeq 12.7$, Figure 5.25), transconductance ($g_{mo} = \eta V_T / I_C \simeq 350$ mS), an initial estimate for r_{BC} of $4 \sim 7$ kΩ from Equation (5.10), and an initial estimate for C_{BC} of 40 fF, calculated from the results of Equation (5.8) and Figure 5.30; a model for the 2×10 HBT, using Advanced Design System (ADS) circuit simulation software,[8] was created (Figure 5.35).

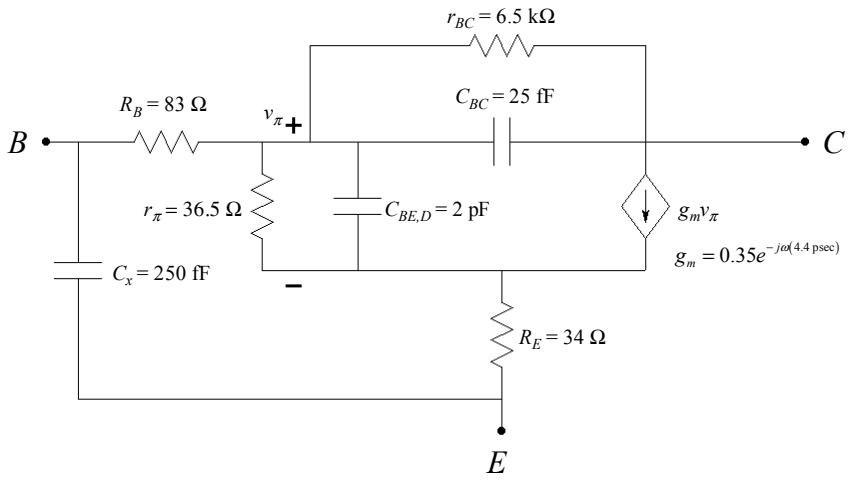


Figure 5.35 Hybrid-π model of the oxide aperture HBT simulated in ADS.

Comparison of the *S*-parameters, the short-circuit current gain (h_{21}), and the unilateral power gain (U) from an actual device with that from the model show good agreement (Figure 5.36 and Figure 5.37). In the model presented in Figure 5.35, r_{BC} is relatively low as a result of the impact ionization present in the collector. Conversely, r_o has been set equal to infinity to reflect the very low collector-emitter leakage present in the actual device ($r_o \simeq 1.33$ MΩ for $I_B = 0$ A); though this is not

physically possible, it was found that reducing r_o to as low as 10 kΩ had essentially no effect on the model, setting $r_o \to \infty$ merely simplifies the analysis.

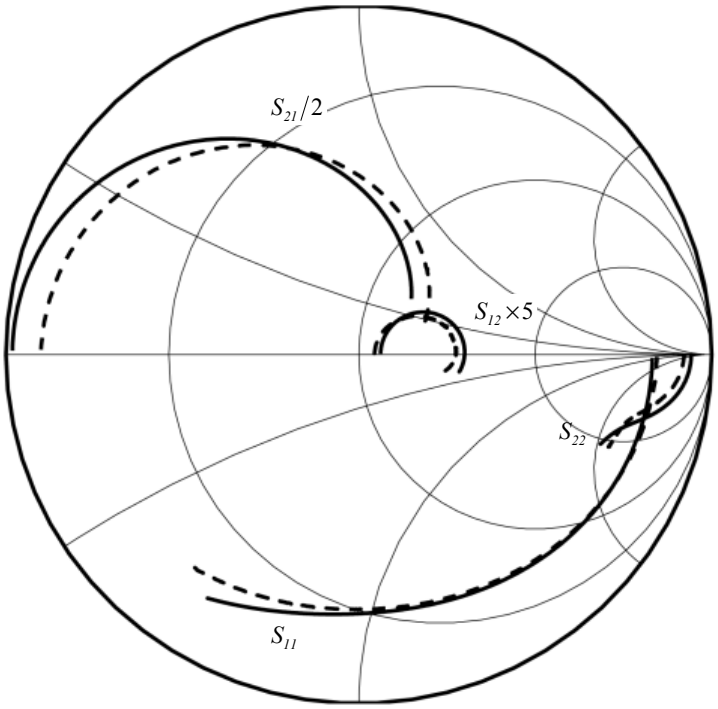


Figure 5.36 Measured *S*-parameters of a 2 × 10 HBT (dashed lines) and simulated *S*-parameters of the model presented in Figure 5.35 (solid lines). I_C = 9.015 mA, V_{CE} = 2.0 V.

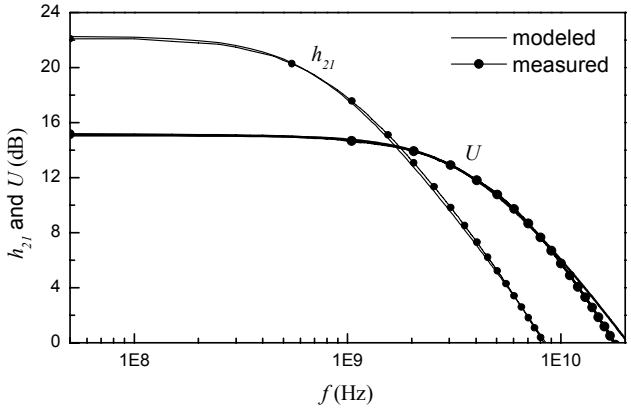


Figure 5.37 Measured and simulated h_{21} and U versus frequency for a 2 × 10 HBT and the model presented in Figure 5.35 (I_C = 9.015 mA, V_{CE} = 2.0 V).

A model of the oxide aperture HBT with the inclusion of a lateral emitter access resistance ($R_{E,acc}$) outside of the parasitic base-emitter capacitance (C_x), essentially partitioning the emitter resistance between an internal resistance and the lateral access resistance ($R_E = R_{E,int} + R_{E,acc} = 34\ \Omega$, Figure 5.14), proved to be a more accurate representation of the device (Figure 5.38~Figure 5.40). It is interesting to note that the addition of the lateral access resistance ($R_{E,acc}$) outside of the parasitic base-emitter capacitance (C_x) required a slightly higher value for C_x. Initial simulations where the base-emitter parasitic region was more correctly treated as a network of resistors and capacitors resulted in an increasingly accurate model of the oxide aperture HBT.

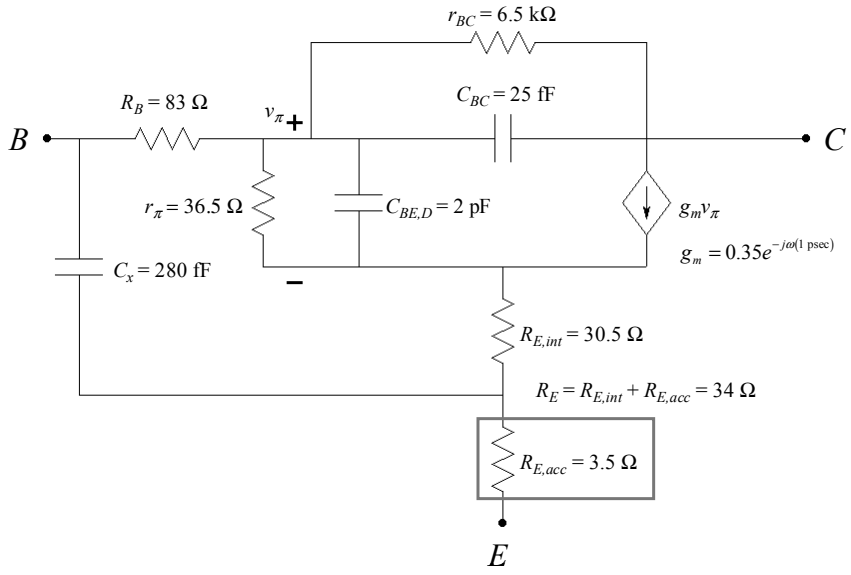


Figure 5.38 Hybrid-π model of the oxide aperture HBT with the addition of a lateral access resistance in the emitter ($R_{E,acc}$) simulated in ADS.

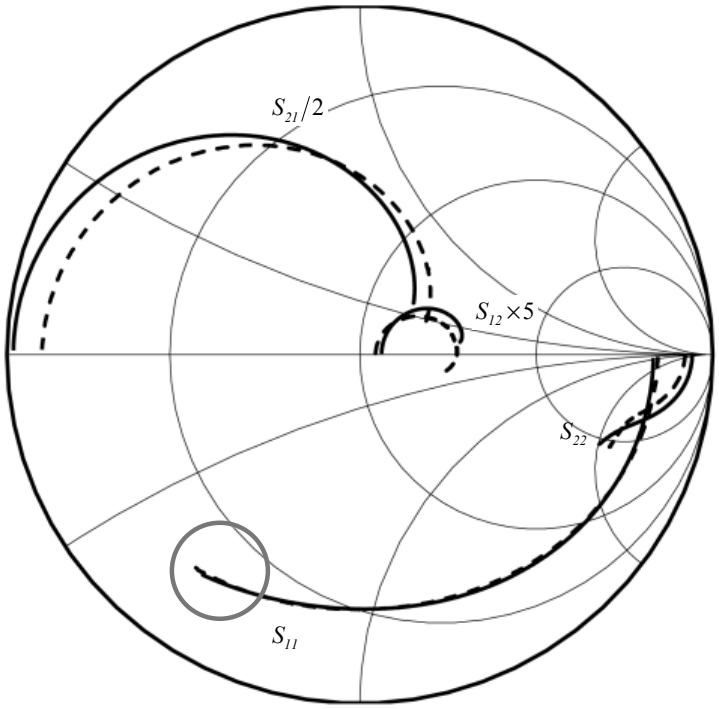


Figure 5.39 Measured *S*-parameters of a 2×10 HBT (dashed lines) and simulated *S*-parameters of the model presented in Figure 5.38 (solid lines). I_C = 9.015 mA, V_{CE} = 2.0 V. Inclusion of the lateral access resistance (RE,acc) results in a more accurate representation of the HBT (gray circle).

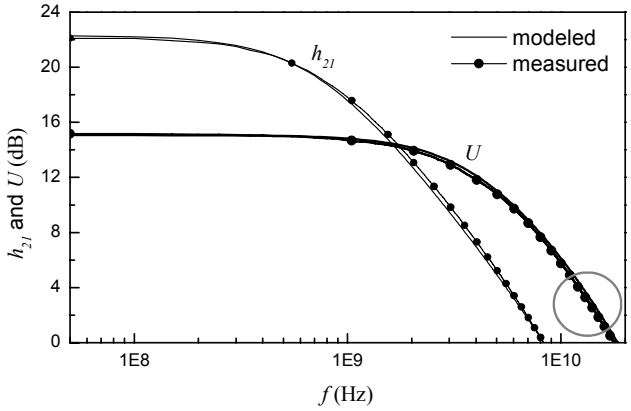


Figure 5.40 Measured and simulated h_{21} and U versus frequency for a 2×10 HBT and the model presented in Figure 5.38 (I_C = 9.015 mA, V_{CE} = 2.0 V).

Removal of C_x drastically affected the *S*-parameters of the model (Figure 5.41), which translated into a marked increase in f_τ with only a small perturbation of f_{max}, as expected from Equations (5.4) and (5.5) (Figure 5.42).

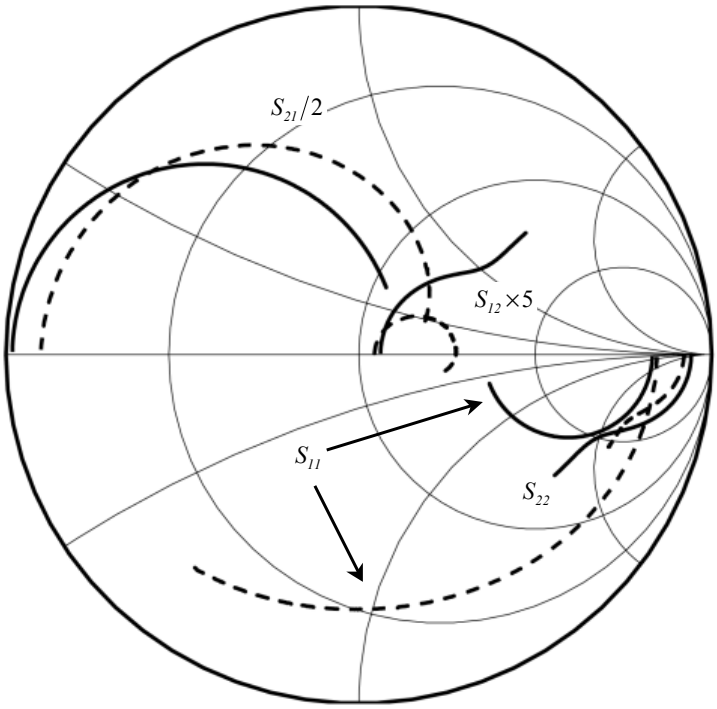


Figure 5.41 Measured *S*-parameters of a 2×10 HBT (dashed lines) and simulated *S*-parameters of the model presented in Figure 5.35 or Figure 5.38 with C_x removed (solid lines). I_C = 9.015 mA, V_{CE} = 2.0 V.

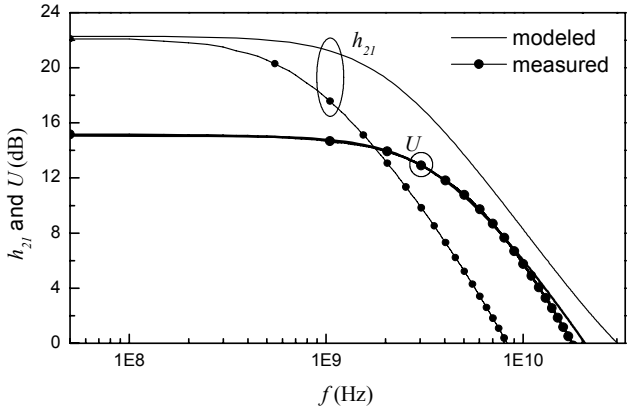


Figure 5.42 Measured and simulated h_{21} and U versus frequency for a 2 × 10 HBT and the model presented in Figure 5.35 or Figure 5.38 with C_x removed (I_C = 9.015 mA, V_{CE} = 2.0 V).

5.9 References

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[7] G. E. Stillman, "Impact ionisation coefficients in InGaAs" in *Properties of lattice-matched and strained Indium Gallium Arsenide*, edited by P. Bhattacharya (INSPEC, London, United Kingdom, 1993), pp. 76-83.

[8] Advanced Design System circuit simulation software is a product of Agilent Technologies.

CHAPTER 6

Conclusions

In this dissertation, the validity and application of the oxide aperture heterojunction bipolar transistor (HBT) design for high maximum frequency of oscillation (f_{max}) was examined. Various issues associated with fabrication of the oxide aperture HBT, such as material growth related to transistor fabrication, oxidation, junction design, and device design as related to high-frequency performance, were investigated. The work culminated with the fabrication of an oxide aperture HBT with a current-gain cutoff frequency (f_τ) on the order of 8 ~ 10 GHz and f_{max} of 12 ~ 17 GHz, with the maximum measured f_{max} being 17.76 GHz.

Two aspects concerning the design and fabrication of the oxide aperture HBT became clearly critical during the work presented in this dissertation: **(*1*)** the impact of the oxide aperture on the DC characteristics of the base-emitter junction and the necessity of a well-designed base-emitter junction for proper transistor operation and

(*2*) the effect of a parasitic base-emitter capacitance, which resulted from the collector-up design, on the high-frequency performance of the transistor.

6.1 Oxide Apertures and pn Junctions

At their present level of technology, oxides formed from the wet oxidation of aluminum-based III-V semiconductors produce surfaces with fairly high recombination velocities.[1,2] A consequence of this in the oxide aperture HBT is that the relative location of the oxide aperture to the base-emitter *pn* junction strongly effects the nature of the current conduction within the junction, which in turn impacts the DC performance of the HBT.

Placement of the oxide aperture within the depletion region of the *pn* junction resulted in a current-voltage characteristic dominated by recombination currents along the interior of the oxide aperture, evident by the increased ideality factor (η) and perimeter-dependency of the characteristic (Figure 6.1a). Moving the aperture far outside of the depletion region resulted in a characteristic no longer dominated by recombination ($\eta \rightarrow 1$), but also resulted in the region of the emitter above the oxide aperture becoming undepleted. This allowed current to flow outside of the aperture and defeated the entire purpose of the aperture, which was to channel the carriers injected from the emitter (Figure 6.1b). Therefore it became evident that there existed a critical range in which the oxide aperture must be located relative to the *pn* junction in order to completely deplete the region above the aperture, thereby properly channeling the carriers injected from the emitter, *without* introducing a

recombination center into the depletion region of the junction, hence maintaining a nearly ideal characteristic ($\eta \simeq 1$, Figure 6.1c).

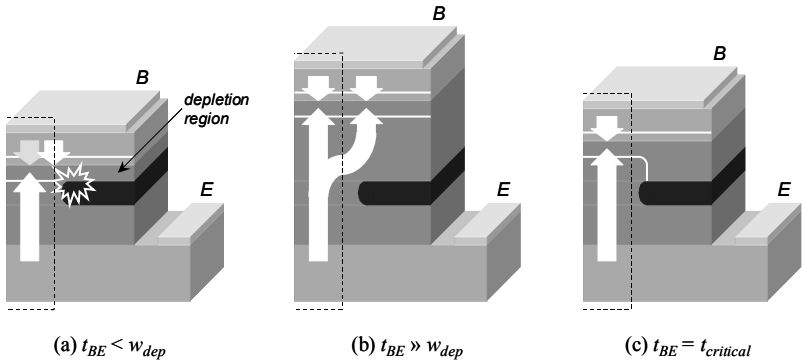

Figure 6.1 Illustration of the influence of oxide aperture to *pn* junction spacing (t_{BE}). (a) The aperture is placed within the *pn* junction depletion region ($t_{BE} < w_{dep}$), perimeter recombination dominates; (b) the aperture is placed well outside of the *pn* junction depletion region ($t_{BE} \gg w_{dep}$), the aperture no longer channels current; (c) the aperture is within the critical range ($t_{BE} = t_{critical}$), the aperture properly channels current and $\eta \rightarrow 1$.

It is important to note that this critical spacing of the oxide aperture from the base-emitter *pn* junction is not fixed but is dependent upon the relative depletion widths of the base-emitter and emitter-oxide junctions, and is therefore dependent upon the given transistor design.

6.2 The Parasitic Base-Emitter Capacitance

The intent of the oxide aperture HBT was to remove the parasitic base-collector capacitance present in conventional emitter-up designs in order to improve the frequency performance of the device. In doing so, the parasitic base-collector capacitance was exchanged for another, the parasitic base-emitter capacitance.

Like the parasitic base-collector capacitance, the parasitic base-emitter capacitance is a result of the physical geometry of the transistor, in this case the collector-up design, and is outside of the intrinsic transistor (Figure 6.2). Re-examination of a hybrid-π model of the oxide aperture HBT, which included this parasitic capacitance, showed that the f_τ measured for these devices was reduced as a direct result of an additional time constant introduced by the parasitic base-emitter capacitance.

$$f_\tau = \frac{1}{2\pi}\left[\tau_{std} + \left(\frac{\eta kT}{qI_C} + \frac{R_B}{\beta_o} + R_E\right)C_x\right]^{-1} \tag{6.1}$$

where τ_{std} is the time constant associated with f_τ of a standard HBT.

Conversely, f_{max} was found to be unaffected by the parasitic base-emitter capacitance and consequently not related to the f_τ of the device, differing from what is expected from classical transistor analysis.

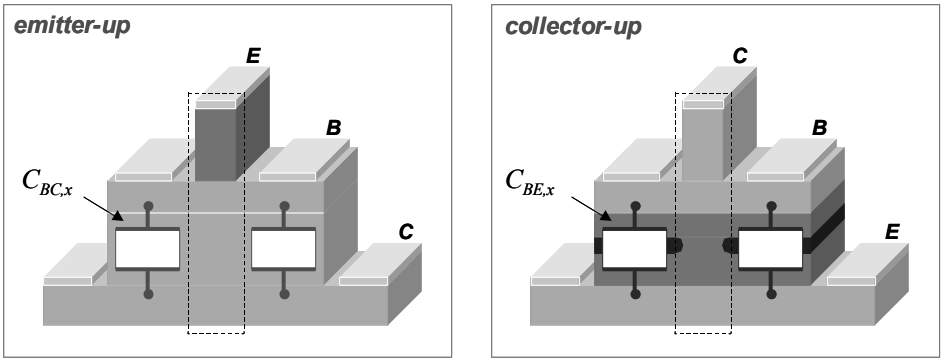

Figure 6.2 Illustration of an emitter-up HBT and a collector-up HBT showing the parasitic capacitance in each structure.

6.3 Future Work

Though a great deal of work has gone into the fabrication of the oxide aperture HBT, this dissertation simply represents a foundation for future work oriented towards optimization of the transistor for high frequency operation. Suggested areas of general research are: sub-micron scaling of the transistor for reduced base-collector capacitance and increased f_{max} and bandgap graded base layers for reduced base transit times and increased f_{τ}. Specific areas that must be examined in the next generation of transistors are **(*1*)** collector design for reduced output conductance and increased common-emitter breakdown, **(*2*)** base-emitter junction optimization for reduced emitter resistance and increased emitter efficiency, and **(*3*)** self-limiting oxidation for sub-micron scaling and reduced parasitic base-emitter capacitance.

Collector Design

The oxide aperture HBTs presented in this dissertation exhibited common-emitter

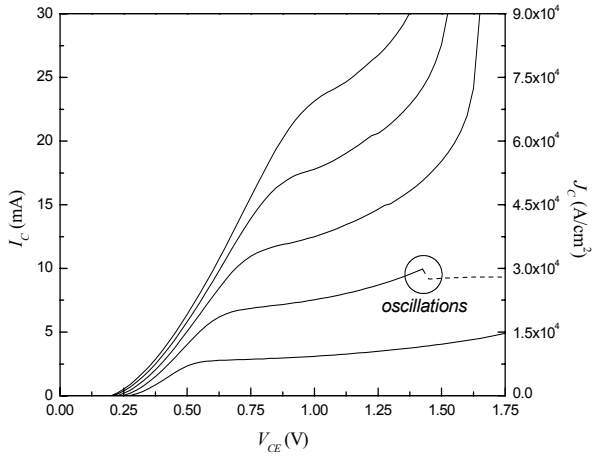

Figure 6.3 Common-emitter characteristic of a $A_C = 4 \times 10$ μm^2 oxide aperture HBT.

characteristics that displayed low output resistances and breakdown voltages (Figure 6.3). The observed characteristics were attributed to impact ionization in the $In_{0.53}Ga_{0.47}As$ collector resulting from hot electron injection from the $GaAs_{0.49}Sb_{0.51}$ base due to the considerable conduction band offset between $GaAs_{0.49}Sb_{0.51}$ and $In_{0.53}Ga_{0.47}As$ (Figure 6.4a). A simple solution to this problem is the replacement of the $In_{0.53}Ga_{0.47}As$ collector with an InP collector (Figure 6.4b).

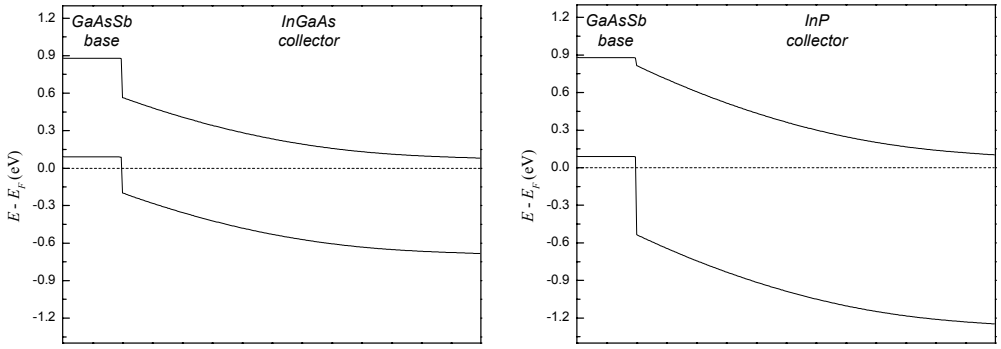

Figure 6.4 Band diagrams of (a) a GaAsSb/InGaAs base-collector junction and (b) a GaAsSb/InP base-collector junction.

InP, in addition to having a lower coefficient of ionization and higher bandgap, has a smaller conduction band offset with $GaAs_{0.49}Sb_{0.51}$ as compared to $In_{0.53}Ga_{0.47}As/GaAs_{0.49}Sb_{0.51}$. Transistors fabricated with this $GaAs_{0.49}Sb_{0.51}$/InP base-collector combination have demonstrated common-emitter breakdown voltages up to 8 V with extremely high output resistances.[3,4] It is believed that the application of an InP collector to the oxide aperture HBT would remove the problem of impact ionization in the collector and radically improve the common-emitter characteristics observed for the oxide aperture HBT.

Base-Emitter Junction Design

The final base-emitter junction design used in this dissertation (Figure 6.5), though designed to display excellent current-voltage characteristics, is by no means the optimal design. From the work presented in this dissertation, it was determined

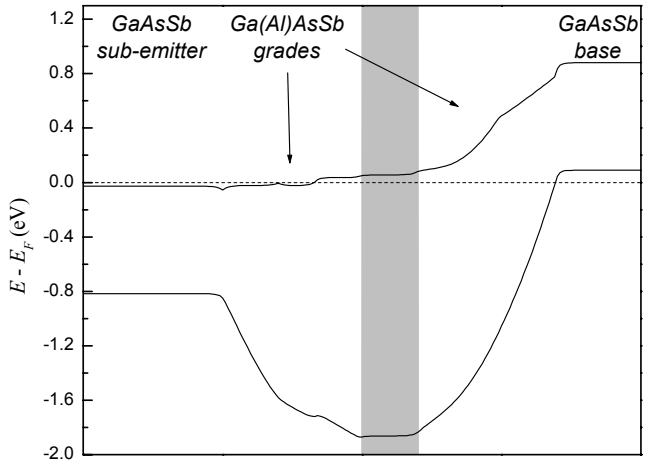

Figure 6.5 Base-emitter junction used in the Generation II HBT presented in Chapter 5. The shaded region indicates the location of the AlAsSb emitter/oxide aperture.

that the design suffered from a high emitter resistance resulting from the low mobility $AlAs_{0.56}Sb_{0.44}$ layers (the $AlAs_{0.56}Sb_{0.44}$ emitter and $Al_xGa_{1-x}AsSb$ grades). This high emitter resistance led to various problems, such as an increased knee voltage and reduced f_τ (Equation (6.1)).

In order to reduce the emitter resistance, the "amount" of $AlAs_{0.56}Sb_{0.44}$ in the emitter must be reduced. Reducing or thinning the $AlAs_{0.56}Sb_{0.44}$ containing layers requires the addition of an alternative wide bandgap material outside of the oxide aperture to maintain a heterojunction at the base-emitter junction. One possible alternative is InP.

InP, as stated previously, has a small conduction band offset with reference to $GaAs_{0.49}Sb_{0.51}$, which allows the base-emitter heterojunction to be abrupt while still maintaining a large valance band offset and an associated high emitter efficiency (Figure 6.6). The band offset between InP and $AlAs_{0.56}Sb_{0.44}$ is not as favorable, but it is believed material grading and high doping can overcome this.

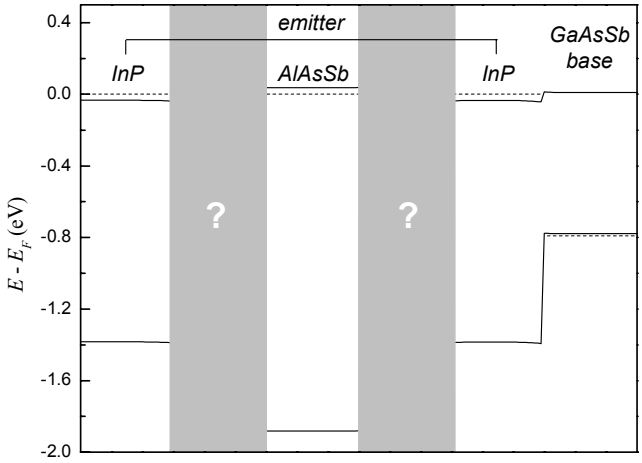

Figure 6.6 Band diagram of a GaAsSb/InP base-emitter junction under forward bias with an AlAsSb layer to form the oxide aperture. How the AlAsSb and InP layers are to be "joined" is in question.

Another alternative is to replace the $AlAs_{0.56}Sb_{0.44}$ completely with another material that can be oxidized but with a high electron mobility. There are not many alternatives lattice-matched to InP, but recent research into the oxidation of $Al_{0.48}In_{0.52}As$, strained AlAs on InP, and AlAs/InAs super-lattices lattice-matched to InP has shown some promise.[5-7]

Self-Limiting Oxidation

At present, the only means of controlling the oxidation depth of materials like $Al_xGa_{1-x}As$ and $AlAs_{0.56}Sb_{0.44}$ is time and temperature (Figure 6.7). As a result, the oxide depth is equidistant, on all sides, from the outside edge of the oxidation mesa. Additionally, the oxidation rate is very sensitive to slight changes in the oxidation environment, resulting in an error in oxidation depth of up to ± 0.25 μm.

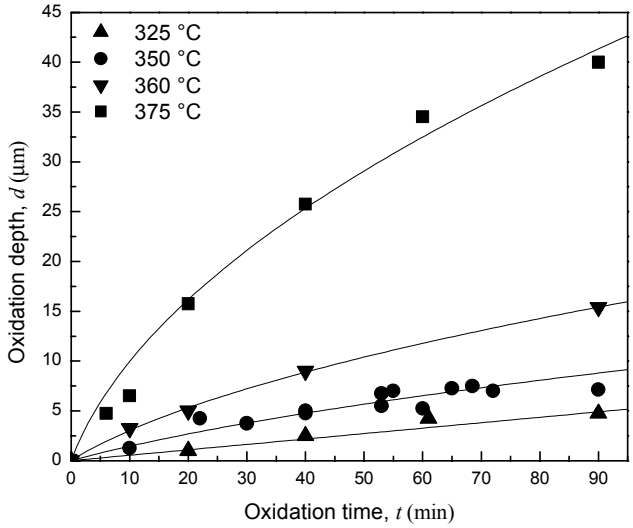

Figure 6.7 Oxidation depth of a 200 Å AlAsSb versus oxidation time for various oxidation temperatures.

In the oxide aperture HBT, the fact that the oxidation proceeds equally from all sides required the base mesa to be similar to and centered on the collector mesa, and the lack of precise control over the oxidation depth necessitated the aperture size to be above the sub-micron range (Figure 6.8a). The relatively large size of the base mesa with respect to the collector mesa led to a correspondingly large parasitic base-emitter capacitance, which resulted in the reduced observed f_τ. In order to reduce the parasitic base-emitter capacitance, in addition to simply scaling the device for high

frequency performance, a means to reproducibly self-align the oxide aperture to the collector mesa is required (Figure 6.8b).

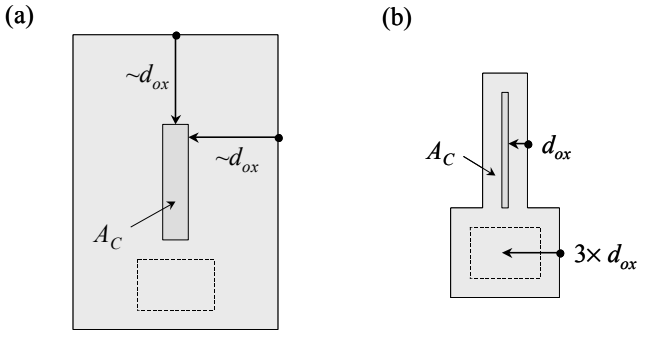

Figure 6.8 Illustrate of the base mesa for (a) the current generation of oxide aperture HBTs and (b) suggested future designs.

Experiments have shown that the oxidation of $Al_xGa_{1-x}As$ and $AlAs_{0.56}Sb_{0.44}$ results in tensibly and compressively strained overlayers, respectively,[8,9] and that by modifying the initial stress in the oxidation structure, the oxidation rate of the aluminum containing layer can be modified.[10] By engineering the layer and device structure of the oxide aperture HBT, it may be possible to retard the oxidation of $AlAs_{0.56}Sb_{0.44}$ underneath the collector, thereby creating a structure which self-aligns and self-limits the oxide aperture to the collector.

Another possibility is to alter the oxidation kinetics of the material outside of the collector area. It has been shown that low-temperature (LT) grown AlAs oxidizes up to five times faster than crystalline AlAs, which was attributed to the increased porosity of the LT AlAs layer and increased surface area of the LT AlAs grains.[11] It is believed a similar effect could be achieved with crystalline material by implanting neutral atoms (or ions of opposite polarity to the emitter doping) into the emitter

region surrounding the collector area. Here again, the oxidation rate underneath the collector would be reduced with respect to the surrounding, producing a structure which self-aligns and self-limits the oxide aperture to the collector.

6.4 References

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APPENDIX A

$AlAs_{0.56}Sb_{0.44}$ Oxidation

A fairly complete presentation on the oxidation of $AlAs_xSb_{1-x}$ can be found in the paper by Mathis *et al.*.[1] Therefore, the specific chemistry and kinetics of the oxidation of $AlAs_{0.56}Sb_{0.44}$ will not be presented here. Instead, a tabulation of the observed oxidation of $AlAs_{0.56}Sb_{0.44}$ as related to the oxide aperture diode and heterojunction bipolar transistor, in addition to extracted activation energies, is presented.

As stated in Chapter 3, oxidations were performed using a three-zone furnace; into which pre-heated water vapor was carried by nitrogen gas (Figure A.1). The water temperature and nitrogen flow rate were 90 °C and ~1198 sccm, respectively.

The oxidation of $AlAs_{0.56}Sb_{0.44}$, like $Al_xGa_{1-x}As$,[2-4] can be described using the Deal-Grove model for oxidation,[1] Equation (A.1).

$$t = \frac{x}{k_l} + \frac{x^2}{k_p} \tag{A.1}$$

t is the oxidation time, d is the oxidation depth, k_l is the linear oxidation constant, and k_p is the parabolic oxidation constant.

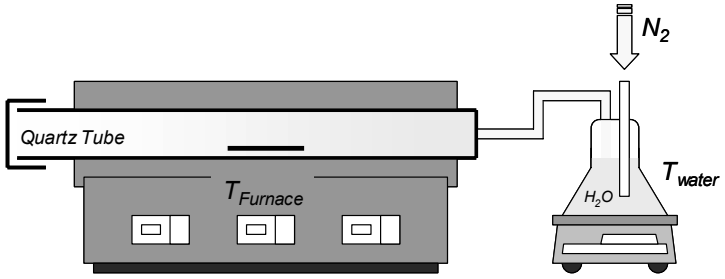

Figure A.1 Illustration of the oxidation furnace and water vapor bubbler.

Various furnace or oxidation temperatures were examined to determine the general oxidation behavior of $AlAs_{0.56}Sb_{0.44}$ versus temperature. Figure A.2 shows the oxidation depth versus oxidation time for various oxidation temperatures for two samples: one with a 300 Å and another with a 500 Å base-emitter grade (shown schematically in Figure A.3). It is interesting to note that at the lower oxidation temperatures, the oxidation characteristics are very similar.

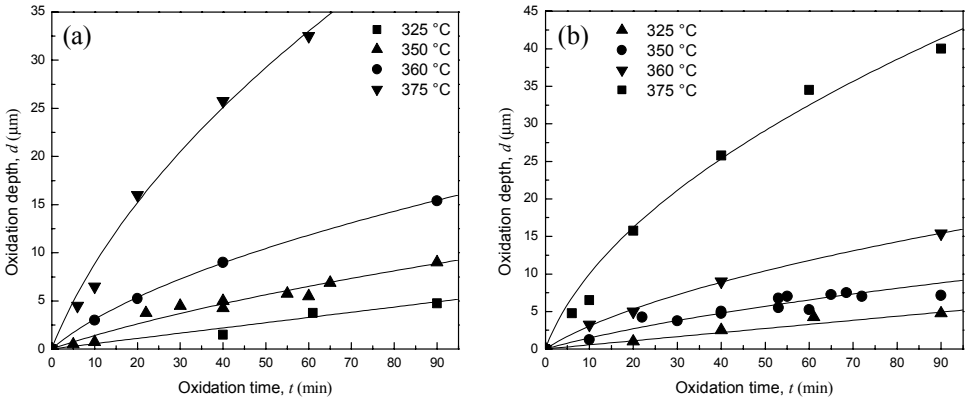

Figure A.2 Oxidation depth versus oxidation time for a sample with (a) a 500 Å emitter grade, a 200 Å AlAsSb layer, and a 300 Å base-emitter (BE) grade; and (b) a 500 Å emitter grade, a 200 Å AlAsSb layer, and a 500 Å BE grade. Furnace temperature is indicated on the plot.

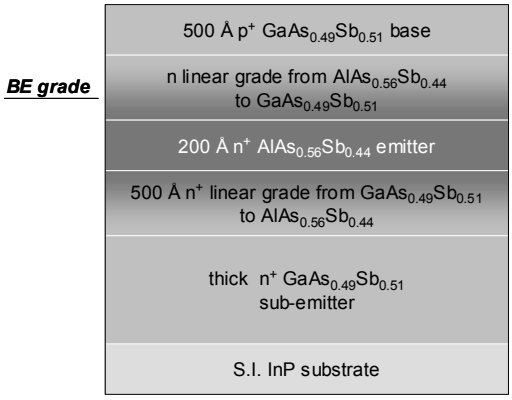

Figure A.3 Illustration of the device layer structure for the samples oxidized in Figure A.2

Two methods can be employed to determine oxidation depth. One is to simply take an optical photograph of the oxidized sample and compare it to a separate feature for which the dimension is known. This method tends to introduce a fair amount of error, as the accuracy of the oxidation depth is heavily dependent upon relative sizes of the images and the human element involved in measuring the images. A superior alternative is to use an oxidation "scale".

An oxidation scale consists of a series of mesas with varying widths; in this case the mesas vary from 1 μm to 14 μm (Figure A.4a), allowing the measurement of oxidation depths between 0.5 μm and 7 μm. As the sample with the oxidation scale is oxidized, the mesas, beginning with the 1 μm mesa, become fully oxidized. Once the oxidation of the sample is completed, the scale is examined and the oxidation depth determined by comparison of the fully oxidized mesas to the partially oxidized mesas (Figure A.4b); the oxidation depth essentially being equivalent to half the width of the last fully oxidized mesa. By varying the mesa size by 1 μm in width with each mesa, the oxidation depth could be determined to within ±0.25 μm. For oxidation depths

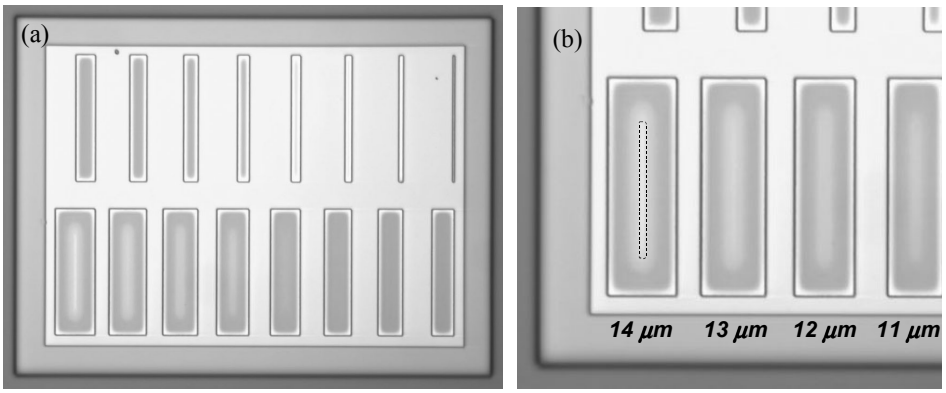

Figure A.4 (a) Photograph of an oxidation scale. (b) Examination of the scale shows that mesas up to the 13 μm width are fully oxidized, corresponding to and oxidation depth of ~6.5 μm.

greater than 7 μm, the relative oxidation depth of large mesas (~50 μm) were measured with respect to the oxidation scale and the absolute depth was determine from the ratio. The error associated with this method is greatly reduced as compared to the previous method since the oxidation depth is determined by direct measurement of a known dimension.

Arrehnius plots for the characteristics in Figure A.2 are presented in Figure A.5.

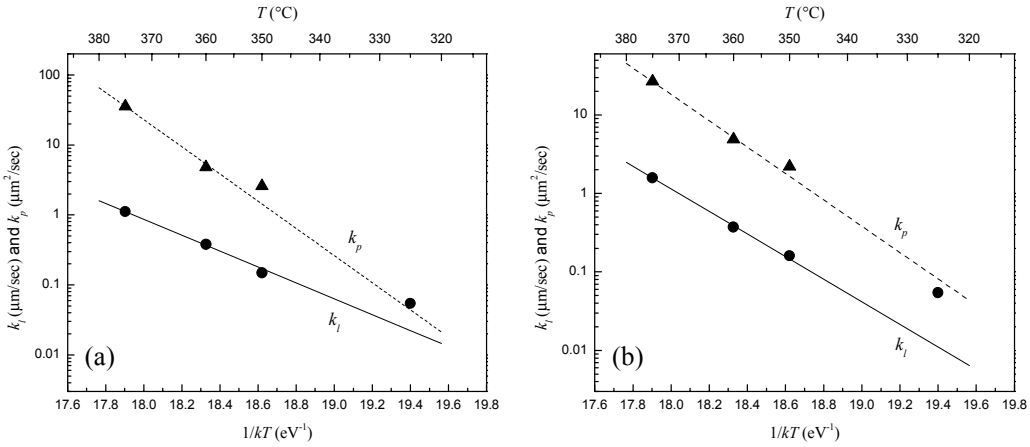

Figure A.5 (a) Arrhenius plot for the characteristics of Figure A.2a. (b) Arrhenius plot for the characteristics of Figure A.2b.

The extracted activation energies (E_A) are presented in Table A.1. It is significant to note that the determined activation energies are very sensitive to the extracted linear (k_l) and parabolic (k_p) oxidation constants.

	325 °C		350 °C		360 °C		375 °C		E_A (eV)	
	k_l	k_p	k_l	k_p	k_l	k_p	k_l	k_p	k_l	k_p
300 Å	0.055	-	0.148	2.581	0.379	4.811	1.118	35.586	2.62 ±0.15	4.47 ±0.51
500 Å	0.055	-	0.161	2.195	0.373	4.883	1.582	26.741	3.32 ±0.13	3.87 ±0.18

Table A.1 Extracted linear (k_l, μm/sec) and parabolic (k_p, μm^2/sec) rate constants and activation energies (E_A).

A.1 References

[1] S. K. Mathis, K. H. A. Lau, A. M. Andrews, E. M. Hall, G. Almuneau, E. L. Hu, and J. S. Speck, "Lateral oxidation kinetics of AlAsSb and related alloys lattice matched to InP." *Journal of Applied Physics* **89**, 2458-64 (2001).

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APPENDIX B

Process and Fabrication Notes

B.1 Oxide Aperture Diode Process

The following process was used to fabricate the diodes presented in Chapter 4. A diagram of the process flow is presented in Figure B.1. The process sheets or process traveler is presented on the pages following.

The fabrication begins with the etching of the base mesa in preparation for the oxidation of the $AlAs_{0.56}Sb_{0.44}$ emitter (Figure B.1a). The $AlAs_{0.56}Sb_{0.44}$ emitter is then oxidized to form the current aperture by wet, thermal oxidation (Figure B.1b, as described in Appendix A). After oxidation, the oxide aperture may optionally be removed by means of a selective oxide etch to form an air aperture. Often actual heterojunction bipolar transistor (HBT) material was used for the oxide diode experiments. In such cases, the collector is removed via a selective wet etch. Following the formation of the oxide aperture, the base and emitter contacts are deposited by e-beam evaporation (Figure B.1c). The emitter mesa etch, which also

serves to isolate the device electrically, is completed next (Figure B.1d). The diodes are completed with the deposition of large contact pads (Figure B.1e) and airbridges/interconnects (Figure B.1f).

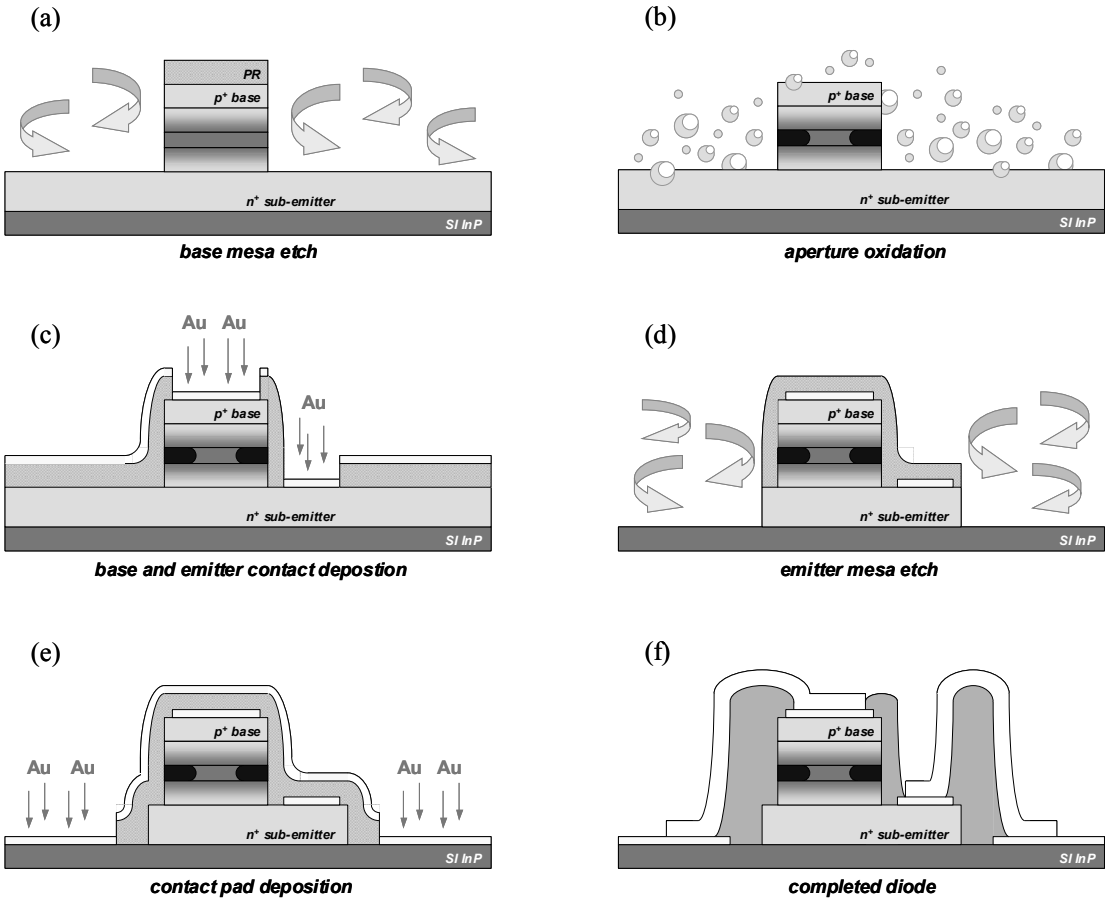

Figure B.1 Process flow for the oxide aperture diodes fabricated in this dissertation.

Diode Process

Growth:	Begin Date:
Process Ref:	End Date:

1 Base

Clean sample

ACE, ISO, DI soak	1 min each	
Nitrogen dry		
Dehydration bake	10 min @ 120 °C	

Complete ☐

Pattern base (950-0.8 PR) Base

Dehydration bake	5 min @ 200 °C (hotplate)	
Apply 950-0.8	30 sec @ 2.5 krpm	
Softbake 950-0.8	1 min @ 90 °C	
Apply CEM	30 sec @ 4 krpm	
Expose	2.25 sec @ + 33 focus	
Hardbake	2 min, 10 sec @ 100 °C	
Rinse DI	30 sec	
Develop in MF-701	45 sec ~ 1 min	

Complete ☐

Etch base (down to sub-emitter)

Oxygen descum	10 sec @ 100 W	
Etch Base	3:1:50: d = 3700 Å t = 3 min ~ 3 min 30 sec NOTE: Should observe color change (assoc. w/AlAsSb)	

The depth to etch, **d**, equals the collector + base + oxide emitter + any grades

Complete ☐

Clean sample

ACE, ISO, DI soak	1 min each	
Nitrogen dry		

Complete ☐

2 Oxidation of Emitter Aperture

Thourough clean: After standard clean

Oxygen descum	1 min @ 100 W	

Complete ☐

Oxidation

Oxidation		

Complete ☐

Clean sample			
	ACE, ISO, DI soak	1 min each	
	Nitrogen dry		
Complete			☐

3 Remove Oxide			
Oxide etch			
	Etch oxide	KOH: t = ~1.5 min	
Performed			y / n

4 Remove Collector			
Remove surface oxide			
	Oxide Removal	NH4OH:H2O (1:15) 20 sec	
Complete			☐

Etch collector (down to base)			
	Oxygen descum	10 sec @ 100 W	
	Etch Collector	Selective Etch: d = 2000 Å (collector thkns) t = ~ 1 min (**check** for EB diode)	
Complete			☐

Clean sample			
	ACE, ISO, DI soak	1 min each	
	Nitrogen dry		
Complete			☐

5 Base and Emitter Metal			
Pattern contacts (950-0.8 PR) Metal			
	Dehydration bake	5 min @ 200 °C (hotplate)	
	Apply 950-0.8	30 sec @ 2.5 krpm	
	Softbake 950-0.8	1 min @ 90 °C	
	Apply CEM	30 sec @ 4 krpm	
	Expose	1.8 sec @ + 33 focus	
	Hardbake	2 min, 10 sec @ 100 °C	
	Rinse DI	30 sec	
	Develop in MF-701	45 sec ~ 1 min	
Complete			☐

Evaporate contacts			
	Oxygen descum	10 sec @ 100 W	
	Evaporate contacts	Ti:Pt:Au:Ni (200:50:1k:100 Å)	
	Liftoff	ACE soak for ~30 min	
Complete			☐

Clean sample			
	ACE, ISO, DI soak	1 min each	
	Nitrogen dry		
Complete			☐

6 Emitter

Pattern emitter (950-0.8 PR) Emitter

Dehydration bake	5 min @ 200 °C (hotplate)	
Apply 950-0.8	30 sec @ 2.5 krpm	
Softbake 950-0.8	1 min @ 90 °C	
Apply CEM	30 sec @ 4 krpm	
Expose	2.25 sec @ + 33 focus	
Hardbake	2 min, 10 sec @ 100 °C	
Rinse DI	30 sec	
Develop in MF-701	~ 1 min	

Complete ☐

Etch emitter (down to SI InP)

Oxygen descum	10 sec @ 100 W	
Etch Emitter	3:1:50: d = 2500 Å (sub-e thkns) NOTE: Should observe color change (assoc. w/GaAsSb)	

Complete ☐

Clean sample

ACE, ISO, DI soak	1 min each	
Nitrogen dry		

Complete ☐

7 Contacts

Pattern contacts (950-0.8 PR) Contacts

Dehydration bake	5 min @ 200 °C (hotplate)	
Apply 950-0.8	30 sec @ 2.5 krpm	
Softbake 950-0.8	1 min @ 90 °C	
Apply CEM	30 sec @ 4 krpm	
Expose	2.25 sec @ + 33 focus	
Hardbake	2 min, 10 sec @ 100 °C	
Rinse DI	30 sec	
Develop in MF-701	~ 1 min	

Complete ☐

Evaporate AC pads

Oxygen descum	10 sec @ 100 W	
Evaporate contacts	Ti:Pt:Au:Pt (200:50:2.5k:50Å)	
Liftoff	ACE soak for ~30 min	

Complete ☐

Clean sample

ACE, ISO, DI soak	1 min each	
Nitrogen dry		

Complete ☐

8 Posts

PMGI SF11 application

Dehydration bake	5 min @ 200 °C (hotplate)	

Apply SF11	40 sec @ 5 krpm	
Softbake	2 min @ 200 °C (hotplate)	
Cool down	30 sec	
Apply SF11	40 sec @ 5 krpm	
Softbake	3 min @ 200 °C (hotplate)	

Complete ☐

Pattern posts (4210 PR) Posts

Apply 4210	30 sec @ 5 krpm	
Softbake 4210	1 min @ 90 °C	
Expose	0.64 sec @ + 33 focus	
Develop in AZ400K (1:4)	45 sec ~ 1 min	

This should give a thickness of about 2 μm

Complete ☐

Pattern posts (SF11)

Deep UV Expose	2 min (3500 mJ/cm2)	
Develop in SAL 101	~ 1 min	

Repeat if necessary

Complete ☐

Remove 4210 PR mask

ACE, ISO, DI soak	1 min each	
Nitrogen dry		
Oxygen descum	30 sec @ 100 W	

Complete ☐

Reflow PMGI SF11

Reflow bake	19 min @ 200 °C (hotplate)	

Complete ☐

Clean sample

ACE, ISO, DI soak	1 min each	
Nitrogen dry		

Complete ☐

9 Airbridge

Pattern airbridge (4210 PR) Airbridge

Dehydration bake	5 min @ 200 °C (hotplate)	
Apply 4210	30 sec @ 5 krpm	
Softbake 4210	1 min @ 90 °C	
Expose	0.64 sec @ + 33 focus	
Develop in AZ400K (1:4)	45 sec ~ 1 min	

Complete ☐

Evaporate airbridge

Oxygen descum	10 sec @ 100 W	
Evaporate contacts	Ti:Pt:Au (200:50:17250 Å)	
Liftoff	ACE soak (gently)	

Complete ☐

Clean sample

ACE, ISO, DI soak	1 min each	
Nitrogen dry		

Complete ☐

10 Contact Vias

Pattern contact vias (4330 PR) Vias

Apply 4330	30 sec @ 5 krpm	
Softbake 4330	2 min @ 90 °C	
Expose	1 sec @ + 33 focus	
Develop in AZ400K (1:4)	45 sec ~ 1 min	

This should give a thickness of about 3 μm

Complete ☐

Pattern posts (SF11)

Deep UV Expose	2 min (3500 mJ/cm2)	
Develop in SAL 101	~ 1 min	

Repeat if necessary

Complete ☐

Remove 4330 PR mask

ACE, ISO, DI soak	1 min each	
Nitrogen dry		
Oxygen descum	30 sec @ 100 W	

Complete ☐

Process Notes:

Definitions of Etchs:

3:1:50

H3PO4:H2O2:H2O (3:1:50) by vol.
rate = 872.7 Å/min = 14.6 Å/sec for InGaAs
rate = 6222 Å/min = 103.7 Å/sec for GaAsSb

Oxide Dip

NH4OH:H2O (1:15) by vol.

Selective Etch

1 M citric acid:H2O2 (2:1) by vol.
rate = 2000 Å/min = 34 Å/sec for InGaAs
rate = 10 Å/min = for GaAsSb

BHF Etchs

BHF:H2O (1:10) by vol.
rate = 26.4 Å/sec for SiO2
Straight BHF
rate = 302 Å/min for SiN

KOH Etch

KOH:H2O (1:12) by vol.
rate = 4 μm/min for AlxOy

SF6:Ar:O2
SF6:Ar:O2 (5:10:3) sccm, P = 20 mTorr, V = 250 V rate = 370 Å/min for SiO2 rate = 1140 Å/min for SiN

CF4:O2 in RIE3
CF4:O2 (3:12) sccm, P = 20 mTorr, V = 250 V

CF4:O2 in Descummer
CF4:O2 (1:5)→(90:450 mTorr), 300 W rate = 0.24 μm/min

B.2 Oxide Aperture Heterojunction Bipolar Transistor Process

The following process was used to fabricate the HBTs presented in Chapter 5. A diagram of the process flow is presented in Figure B.2. The process sheets or process traveler is presented on the pages following.

The fabrication begins with the deposition of a SiO_2 dummy collector (Figure B.2a). The deposition of a metal collector at this stage would result in the formation of an ohmic collector due to the eventual high temperature oxidation step. The desire of a Schottky collector necessitates the use of a dummy collector. Following the deposition of the dummy collector, the base mesa is etched to facilitate the oxidation of the $AlAs_{0.56}Sb_{0.44}$ emitter (Figure B.2b). The $AlAs_{0.56}Sb_{0.44}$ emitter is then oxidized to form the current aperture by wet, thermal oxidation (Figure B.2c). After oxidation, the oxide aperture may optionally be removed by means of a selective oxide etch to form an air aperture. Following the formation of the oxide aperture, the

collector mesa is defined by means of a selective wet etch (Figure B.2d), after which the base and emitter contacts are deposited by e-beam evaporation (Figure B.2e). The emitter mesa etch, which also serves to isolate the device electrically, is performed next (Figure B.2f).

A co-planar waveguide (CPW) transmission line is deposited in order to facilitate RF measurements (Figure B.2g). The wafer is then planarized for subsequent interconnect processing. Interconnect posts are then deposited and the planarization resist is blanket etched to expose the SiO_2 dummy collector (Figure B.2h). Lithography to define the interconnect lines is completed, the SiO_2 dummy collector is removed by means of a short BHF dip, and the interconnect metal is deposited and lifted-off (Figure B.2i). Opening up vias for contacting the CPW transmission lines completes the process.

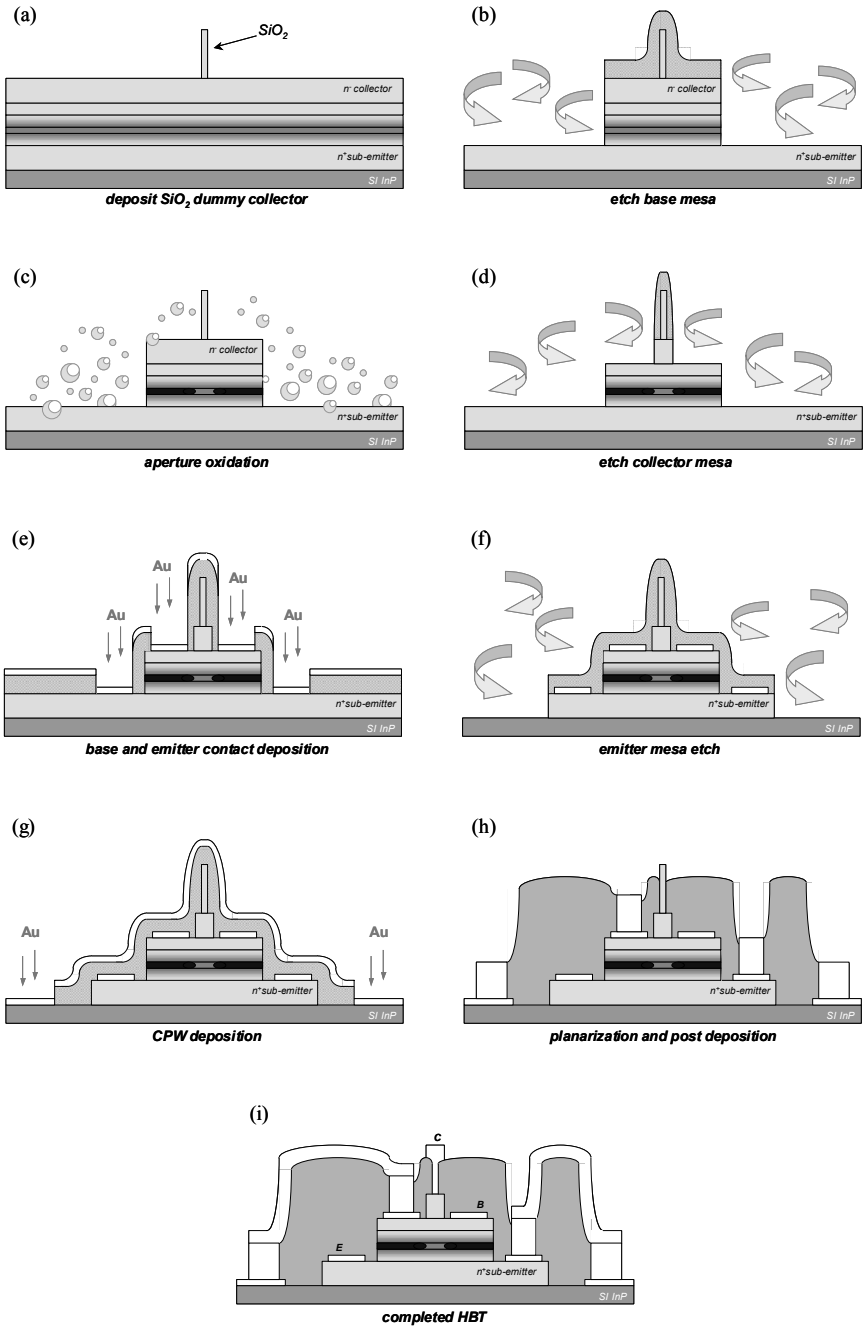

Figure B.2 Process flow for the oxide aperture HBTs fabricated in this dissertation.

HBT Process

Growth:	Begin Date:
Process Ref:	End Date:

Notes:

1 Dummy Collector

Clean sample

ACE, ISO, DI soak	1 min each	
Nitrogen dry		
Dehydration bake	10 min @ 120 °C (oven)	

Complete ☐

Pattern dummy collector contact

2 layer resist process using SF11 and 4110 gives ~ 2 μm

Dehydration bake	5 min @ 200 °C (hotplate)	
Apply SF11	40 sec @ 5 krpm	
Softbake SF11	2 min @ 200 °C (hotplate)	
Cool down	30 sec	
Apply 4110	30 sec @ 5 krpm	
Softbake 4110	1.5 min @ 90 °C	
Expose	0.32 sec @ +33 focus	
Develop in AZ400K (1:4)	45 sec ~ 1 min	
Deep UV expose	2 min	
Develop in SAL 101	1 min	

Repeat deep UV expose and develop if necessary

Complete ☐

Evaporate SiO2

Using E-Beam #2

Descum	20 sec @ 100 W, 300 mT	
Oxide dip	15 sec	
Evaporate SiO2	1000 Å: < 1 Å/sec > 1000 Å: ~ 5 Å/sec total thickness = 1 μm	
Liftoff	~10 min slow soak in ACE	
Deep UV expose	2 min	
Develop in SAL 101	1 min	

Repeat deep UV expose and develop if necessary

Complete ☐

2 Base Mesa

Pattern base mesa

Dehydration bake	5 min @ 200 °C (hotplate)	
Apply 950-0.8	30 sec @ 2.5 krpm	
Softbake 950-0.8	1 min @ 90 °C	
Apply CEM	30 sec @ 4 krpm	
Expose	1.8 sec @ +33 focus	

Hardbake	2 min 10 sec @ 100 °C	
DI rinse	30 sec	
Develop in MF-701	45 sec ~ 1 min	

Complete ☐

Etch base

Etch base down to sub-emitter

Descum	10 sec @ 100 W, 300 mT	
Etch base	3:1:50 color of samples darkens twice: @ base, @ AlAsSb t = 3 min ~ 3 min 30 sec	

Complete ☐

Clean sample

ACE, ISO, DI soak	1 min each	
Nitrogen dry		

Complete ☐

3 Oxidation of Emitter Aperture

Thourough clean

ACE, ISO, DI soak	1 min each	
Nitrogen dry		
Deep UV expose	2 min	
Develop in SAL 101	1 min	
Descum	1 min @ 100 W, 300 mT	

Complete ☐

Oxidation

Oxidation		

Complete ☐

4 Remove Oxide

Oxide etch

Optional step	KOH t = ~ 1.5 min	

Performed ☐

5 Collector Mesa

Surface oxide removal

Oxide dip	15 sec	

Complete ☐

Pattern collector mesa

Dehydration bake	5 min @ 200 °C (hotplate)	
Apply 950-0.8	30 sec @ 2.5 krpm	
Softbake 950-0.8	1 min @ 90 °C	
Apply CEM	30 sec @ 4 krpm	

	Expose	1.8 sec @ +33 focus	
	Hardbake	2 min 10 sec @ 100 °C	
	DI rinse	30 sec	
	Develop in MF-701	45 sec ~ 1 min	
Complete			☐

Etch collector

Etch collector down to base

	Descum	10 sec @ 100 W, 300 mT	
	Etch collector	Selective Etch t = 1.5 min	
Complete			☐

Clean sample

	ACE, ISO, DI soak	1 min each	
	Nitrogen dry		
Complete			☐

6 Base/Emitter Contacts

Pattern contacts

	Dehydration bake	5 min @ 200 °C (hotplate)	
	Apply 950-0.8	30 sec @ 2.5 krpm	
	Softbake 950-0.8	1 min @ 90 °C	
	Apply CEM	30 sec @ 4 krpm	
	Expose	1.8 sec @ +33 focus	
	Hardbake	2 min 10 sec @ 100 °C	
	DI rinse	30 sec	
	Develop in MF-701	45 sec ~ 1 min	
Complete			☐

Evaporate contacts

	Descum	10 sec @ 100 W, 300 mT	
	Evaporate contacts	Ti:Pt:Au (150:50:1000 Å)	
	Liftoff	Slow soak in ACE	
Complete			☐

7 Emitter Mesa

Pattern emitter mesa

	Dehydration bake	5 min @ 200 °C (hotplate)	
	Apply 950-0.8	30 sec @ 2.5 krpm	
	Softbake 950-0.8	1 min @ 90 °C	
	Apply CEM	30 sec @ 4 krpm	
	Expose	1.8 sec @ +33 focus	
	Hardbake	2 min 10 sec @ 100 °C	
	DI rinse	30 sec	
	Develop in MF-701	45 sec ~ 1 min	
Complete			☐

Etch emitter (down to SI InP)

Etch emitter

	Descum	10 sec @ 100 W, 300 mT	
	Etch emitter	3:1:50	

	Should see color change associated w/ GaAsSb/InP	

Complete ☐

8 AC Pads

Pattern AC pads

Dehydration bake	5 min @ 200 °C (hotplate)	
Apply 950-0.8	30 sec @ 2.5 krpm	
Softbake 950-0.8	1 min @ 90 °C	
Apply CEM	30 sec @ 4 krpm	
Expose	1.8 sec @ +33 focus	
Hardbake	2 min 10 sec @ 100 °C	
DI rinse	30 sec	
Develop in MF-701	45 sec ~ 1 min	

Complete ☐

Evaporate pads

Descum	10 sec @ 100 W, 300 mT	
Evaporate contacts	Ti:Pt:Au (200:50:2500 Å)	
Liftoff	Slow soak in ACE	

Complete ☐

9 Probe Pads

Pattern pads

Dehydration bake	5 min @ 200 °C (hotplate)	
Apply 950-0.8	30 sec @ 2.5 krpm	
Softbake 950-0.8	1 min @ 90 °C	
Apply CEM	30 sec @ 4 krpm	
Expose	1.8 sec @ +33 focus	
Hardbake	2 min 10 sec @ 100 °C	
DI rinse	30 sec	
Develop in MF-701	45 sec ~ 1 min	

Complete ☐

Evaporate pads

Descum	10 sec @ 100 W, 300 mT	
Evaporate contacts	Ti:Pt:Au (200:50:7000 Å)	
Liftoff	Slow soak in ACE	

Complete ☐

10 Posts and Etchback

Pattern posts

Dehydration bake	5 min @ 200 °C (hotplate)	
Apply SF11	40 sec @ 5 krpm	
Softbake SF11	2 min @ 200 °C (hotplate)	
Cool down	30 sec	
Apply SF11	40 sec @ 5 krpm	
Reflow bake	20 min @ 275 °C (oven)	
Apply 4110	30 sec @ 5 krpm	
Softbake 4110	1.5 min @ 90 °C	
Expose	0.32 sec @ +33 focus	
Develop in AZ400K (1:4)	45 sec ~ 1 min	

Deep UV expose	2 min	
Develop in SAL 101	1 min	

Repeat deep UV expose and develop if necessary

Complete ☐

Evaporate pads

Descum	10 sec @ 100 W, 300 mT	
Evaporate contacts	Ti:Pt:Au:Ni (100:50:5k:150 Å)	
Liftoff	Slow soak in ACE	

Complete ☐

Etch back

Using Oxygen Descummer

Clean	O2 300 mTorr, 300 W, 10 min	
Etch SF11	O2 300 mTorr, 300 W, 2.5 min watch dummy collector	
Clean	O2 300 mTorr, 300 W, 10 min	

Complete ☐

SF11 Reflow

Reflow bake	5 min @ 250 °C (oven)	

Complete ☐

11 Airbridge

Pattern airbridge

Dehydration bake	5 min @ 200 °C (hotplate)	
Apply 4210	30 sec @ 5 krpm	
Softbake 4210	1.5 min @ 90 °C	
Expose	0.64 sec @ +33 focus	
Develop in AZ400K (1:4)	45 sec ~ 1 min	

Complete ☐

Dummy contact removal

Etch SiO2	BHF Etch: t = ~3 min	

Complete ☐

Evaporate bridge

Descum	10 sec @ 100 W, 300 mT	
Evaporate contacts	Ti:Pt:Au (150:50:15k Å)	
Liftoff	Slow soak in ACE (gently)	

Complete ☐

12 Contact Vias

Pattern vias

Dehydration bake	5 min @ 200 °C (hotplate)	
Apply 4330	30 sec @ 5 krpm	
Softbake 4330	1.5 min @ 90 °C	
Expose	1 sec @ +33 focus	

Develop in AZ400K (1:4)	45 sec ~ 1 min	
Deep UV expose	2 min	
Develop in SAL 101	1 min	

Repeat deep UV expose and develop if necessary

Complete ☐

Clean sample

ACE, ISO, DI soak	1 min each	
Nitrogen dry		
Dehydration bake	10 min @ 120 °C (oven)	

Complete ☐

Process Notes

3:1:50

H3PO4:H2O2:H2O (3:1:50) by vol.
rate = 872.7 Å/min = 14.6 Å/sec for InGaAs
rate = 6222 Å/min = 103.7 Å/sec for GaAsSb

Oxide Dip

NH4OH:H2O (1:15) by vol.

Selective Etch

1 M citric acid:H2O2 (2:1) by vol.
rate = 2000 Å/min = 34 Å/sec for InGaAs
rate = 10 Å/min = for GaAsSb

BHF Etchs

BHF:H2O (1:10) by vol.
rate = 26.4 Å/sec for SiO2
Straight BHF
rate = 302 Å/min for SiN

KOH Etch

KOH:H2O (1:12) by vol.
rate = 4 μm/min for AlxOy

SF6:Ar:O2

SF6:Ar:O2 (5:10:3) sccm, P = 20 mTorr, V = 250 V
rate = 370 Å/min for SiO2
rate = 1140 Å/min for SiN

CF4:O2 in RIE3

CF4:O2 (3:12) sccm, P = 20 mTorr, V = 250 V

CF4:O2 in Descummer

CF4:O2 (1:5)→(90:450 mTorr), 300 W
rate = 0.24 μm/min

APPENDIX C

Ebers-Moll Bipolar Transistor Model

The "classical" and ideal Ebers-Moll model of a bipolar transistor consists of two *pn* diodes that represent the two junctions within the transistor and two dependent current sources that handle current injection from one junction into the other, which the diodes cannot characterize (Figure C.1). Though simple, the Ebers-Moll model is very versatile, capable of modeling a bipolar transistor under any DC bias condition (e.g., common-emitter, common-base, forward/reverse-active, forward/reverse-

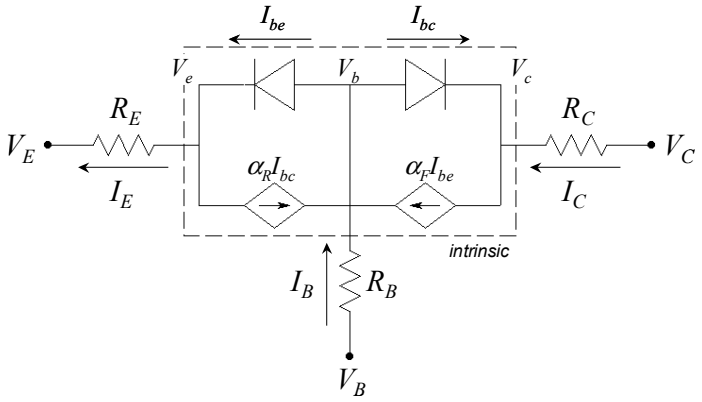

Figure C.1 The Ebers-Moll model of a bipolar transistor, including external resistances.

saturation). Non-idealities, such as extrinsic resistances or the Early Effect, may be added through additional elements.[1] Figure C.1 shows the Ebers-Moll model including extrinsic resistances. Equations (C.1) to (C.3) represent the classical form of the currents present in the Ebers-Moll model.

$$I_E = I_{be} - \alpha_R I_{bc} = I_{be,sat}\left(e^{qV_{be}/\eta_{be}kT} - 1\right) - \alpha_R I_{bc,sat}\left(e^{qV_{bc}/\eta_{bc}kT} - 1\right) \qquad \text{(C.1)}$$

$$I_C = \alpha_F I_{be} - I_{bc} = \alpha_F I_{be,sat}\left(e^{qV_{be}/\eta_{be}kT} - 1\right) - I_{bc,sat}\left(e^{qV_{bc}/\eta_{bc}kT} - 1\right) \qquad \text{(C.2)}$$

$$I_B = I_E - I_C \qquad \text{(C.3)}$$

Where I_{be}, $I_{be,sat}$, and η_{be} are the total current, the saturation current, and the ideality factor of the base-emitter diode, respectively; I_{bc}, $I_{bc,sat}$, and η_{bc} are the total current, the saturation current, and the ideality factor of the base-collector diode, respectively; α_F and α_R are the forward-active and reverse-active common-base current gains; and V_{be} and V_{bc} are the internal base-emitter and base-collector voltages:

$$V_{be} = V_b - V_e \qquad V_{bc} = V_b - V_c$$

By using Kirchoff's voltage law, the internal voltages, V_{be} and V_{bc}, may be written in terms of the external voltages, V_{BE} and V_{BC}, allowing Equations (C.1) and (C.2) to be re-written in terms of these external voltages:

$$V_{be} = V_{BE} - I_B R_B - I_E R_E \qquad V_{bc} = V_{BC} - I_B R_B + I_C R_C$$

$$I_E = I_{be,sat}\left(e^{q(V_{BE} - I_B R_B - I_E R_E)/\eta_{be}kT} - 1\right) - \alpha_R I_{bc,sat}\left(e^{q(V_{BC} - I_B R_B + I_C R_C)/\eta_{bc}kT} - 1\right) \qquad \text{(C.4)}$$

$$I_C = \alpha_F I_{be,sat}\left(e^{q(V_{BE} - I_B R_B - I_E R_E)/\eta_{be}kT} - 1\right) - I_{bc,sat}\left(e^{q(V_{BC} - I_B R_B + I_C R_C)/\eta_{bc}kT} - 1\right) \qquad \text{(C.5)}$$

Equations (C.4) and (C.5), with Equation (C.3), now allow for the theoretical examination of HBTs incorporating the influence of extrinsic resistances (i.e. emitter resistance, R_E; base resistance, R_B; and collector resistance, R_C). Particular useful applications are the derivation of Gummel, common-emitter, and common-base characteristics under the influence of external resistances; as well as the offset voltage (V_{offset}) and knee voltage (V_{knee}) of the common-emitter characteristic presented in Chapter 5 (Figure C.2).

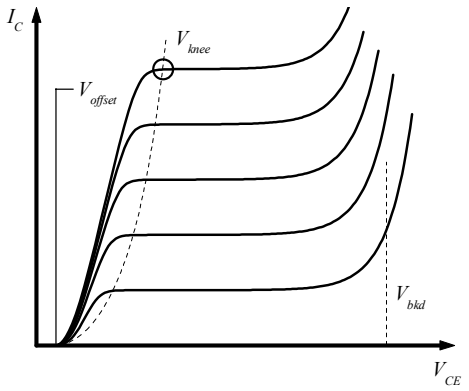

Figure C.2 Illustration of the offset voltage, V_{offset}, and knee voltage, V_{knee}, of a common-emitter characteristic.

C.1 The Offset Voltage

The offset voltage, V_{offset}, is defined as the collector-emitter voltage at which $I_C = 0$. Setting Equation (C.5) equal to zero, letting $I_E = I_B$ (Kirchoff's current law), and $V_{BC} = V_{BE} - V_{CE}$ (Kirchoff's voltage law) results in:

$$0 = \alpha_F I_{be,sat}\left(e^{q(V_{BE}-I_BR_B-I_BR_E)/\eta_{be}kT}-1\right) - I_{bc,sat}\left(e^{q(V_{BE}-V_{CE}-I_BR_B)/\eta_{bc}kT}-1\right) \qquad \text{(C.6)}$$

$I_C = 0$ requires both the base-emitter and base-collector diodes to be forward biased. Under most conditions this results in both of the exponents in Equation (C.6) being much greater than one, allowing Equation (C.6) to be approximated as:

$$0 \simeq \alpha_F I_{be,sat} e^{q(V_{BE}-I_B R_B - I_B R_E)/\eta_{be} kT} - I_{bc,sat} e^{q(V_{BE}-V_{CE}-I_B R_E)/\eta_{be} kT} \tag{C.7}$$

Algebraic manipulation of Equation (C.7) results in the offset voltage (V_{offset}).

$$V_{offset} = V_{CE}\big|_{I_C=0} \simeq \eta_{bc} \frac{kT}{q} \ln\left(\frac{I_{bc,sat}}{\alpha_F I_{be,sat}}\right) + \left(1 - \frac{\eta_{bc}}{\eta_{be}}\right)(V_{BE} - I_B R_B) + \frac{\eta_{bc}}{\eta_{be}} I_B R_E \tag{C.8}$$

C.2 The Knee Voltage

The knee voltage, V_{knee}, is defined as the collector-emitter voltage at which the device shifts between forward-saturation and forward-active modes ($V_{BC} = 0$). To be able to solve for V_{knee} analytically, it is assumed that the exponents in Equations (C.4) and (C.5) are much greater than one. Applying Kirchoff's voltage law ($V_{BE} = V_{CE} + \cancel{V_{BC}}$) and solving Equation (C.4) for I_{be} results in:

$$\begin{aligned} I_{be} &\simeq I_E + \alpha_R I_{bc,sat} e^{q(-I_B R_B + I_C R_C)/\eta_{bc} kT} \\ &\simeq I_E + \alpha_R I_{bc} \end{aligned} \tag{C.9}$$

Plugging Equation (C.9) into Equation (C.5):

$$\begin{aligned} I_C &\simeq \alpha_F \left(I_E + \alpha_R I_{bc}\right) - I_{bc} \\ &\simeq \alpha_F I_E - \left(1 - \alpha_F \alpha_R\right) I_{bc} \end{aligned} \tag{C.10}$$

Solving Equation (C.10) for both I_{bc} and $I_B R_B$:

$$I_{bc} \simeq \frac{\alpha_F I_E - I_C}{1-\alpha_F \alpha_R} \tag{C.11}$$

$$I_B R_B \simeq I_C R_C - \eta_{bc} \frac{kT}{q} \ln\left[\frac{\alpha_F I_E - I_C}{I_{bc,sat}\left(1-\alpha_F \alpha_R\right)}\right] \tag{C.12}$$

Inserting Equation (C.11) back into Equation (C.9) and solving for V_{CE}:

$$V_{CE} \simeq \eta_{be} \frac{kT}{q} \ln\left[\frac{I_E - \alpha_R I_C}{I_{be,sat}\left(1-\alpha_F \alpha_R\right)}\right] + I_B R_B + I_E R_E \tag{C.13}$$

Replacing $I_B R_B$ in Equation (C.13) with Equation (C.12) results in an expression for V_{knee}:

$$\begin{aligned} V_{knee} &= V_{CE}\big|_{V_{BC}=0} \\ &\simeq \frac{\eta_{be} kT}{q} \ln\left[\frac{I_E - \alpha_R I_C}{I_{be,sat}\left(1-\alpha_F \alpha_R\right)}\right] - \frac{\eta_{bc} kT}{q} \ln\left[\frac{\alpha_F I_E - I_C}{I_{bc,sat}\left(1-\alpha_F \alpha_R\right)}\right] + I_E R_E + I_C R_C \end{aligned} \tag{C.14}$$

It should be noted that both the equation for the offset voltage (Equation (C.8)) and the knee voltage (Equation (C.14)) are in terms of experimentally determinable values; making the equations useful for not only theoretical, but also experimental study.

C.3 References

[1] S. M. Sze, *Physics of Semiconductor Devices*, 2 ed. (John Wiley & Sons, Inc., New York, 1981).

APPENDIX D

Gain-Diffusion Model

Presented here is a simple model proposed as an explanation for the common-emitter current gain (β) behavior as seen in the various sized heterojunction bipolar transistors (HBTs) presented in Chapter 5 (Figure D.1).

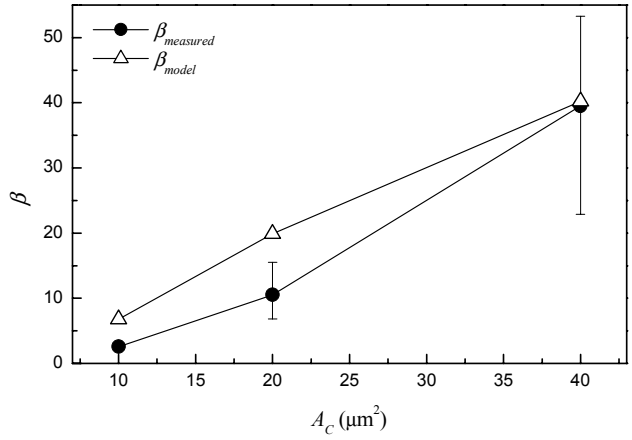

Figure D.1 Common-emitter current gain (β) versus collector area (A_C).

D.1 Gain-Diffusion Model

The following model for the common-emitter current gain (β) is based upon two key assumptions: **(*1*)** the current characteristics of the transistor are ideal (i.e., non-ideal effects such as recombination in the space-charge region or along the perimeter of the active areas is ignored) and **(*2*)** that only the current at the base-collector junction that is *within* the collector area (A_C) contributes to collector current (I_C). From the work presented in Chapter 4, the first assumption, at least with respect to the base-emitter junction, is very reasonable.

The emitter current (I_E) is the total current flowing through the emitter junction area (A_E) and may be written as:

$$I_E = \iint_{A_E} J(x,y)\Big|_{z=0}\, dxdy \tag{D.1}$$

where A_E is the emitter junction area and $J(x,y)$ is a position *dependent* current density flowing perpendicular the emitter area. If the emitter-base junction is defined as being located in the *xy*-plane at $z=0$, then $J(x,y)\Big|_{z=0}$ is the current density at the emitter-base junction. Application of assumption **(*1*)** results in $J(x,y)$ being uniform across the entire emitter junction allowing Equation (D.1) to be rewritten as:

$$I_E = \iint_{A_E} \overbrace{J(x,y)\Big|_{z=0}}^{J_E}\, dxdy = J_E A_E \tag{D.2}$$

where J_E is the position *independent* current density at the emitter (Figure D.2a).

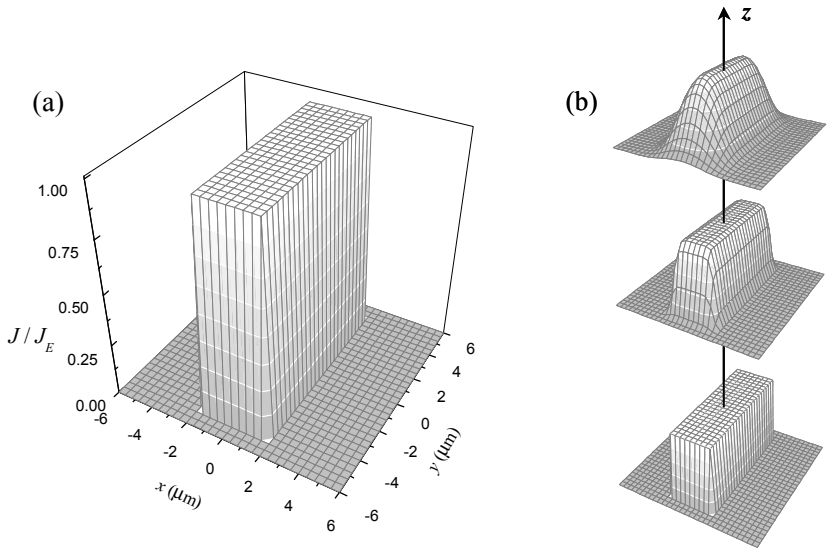

Figure D.2 (a) Current profile at the emitter-base junction ($z = 0$). The magnitude of the profile is uniform across the entire junction. (b) Illustration of the current profile as it transits the base, including the effect of lateral diffusion.

As the carriers comprising the emitter current transit the base, they begin to diffuse laterally, perpendicular to the direction of current flow (Figure D.2b). Applying assumption ***(2)***, the resultant collector current (I_C) is:

$$I_C = \iint_{A_C} J(x,y)\Big|_{z=w_B}\, dxdy \tag{D.3}$$

where A_C is the collector junction area and the base-collector junction has been defined as being located in the *xy*-plane at $z = w_B$, with w_B being the thickness or width of the base layer. Ignoring for the moment the exact form of $J(x,y)\Big|_{z=w_B}$, the common-emitter current gain (β) can be expressed in terms of Equations (D.2) and (D.3), realizing $I_B = I_E - I_C$ (Kirchoff's current law):

$$\beta = \frac{I_C}{I_B} = \frac{I_C}{I_E - I_C} = \frac{\iint_{A_C} J(x,y)\big|_{z=w_B}\, dxdy}{J_E A_E - \iint_{A_C} J(x,y)\big|_{z=w_B}\, dxdy} \tag{D.4}$$

To be able to solve Equation (D.4), even numerically, the form of $J(x,y)\big|_{z=w_B}$ must be known. In this case, it is assumed that the lateral motion of carriers is solely due to diffusion, which can be described using Fick's second law:

$$\frac{\partial n}{\partial t} = D\nabla^2 n \tag{D.5}$$

where n is the concentration of carriers, D is the diffusion coefficient (assumed here to be isotropic), and $\nabla^2 = \nabla \bullet \nabla = \partial^2/\partial x^2 + \partial^2/\partial y^2 + \partial^2/\partial z^2$ where ∇ is the Dell operator. The solution of Equation (D.5) in two-dimensions, applied to a uniform initial distribution centered on the origin, can be shown to be:[1]

$$n(x,y) = \frac{n_o}{4}\left[\operatorname{erf}\left(\frac{x - x_o/2}{2\sqrt{Dt}}\right) - \operatorname{erf}\left(\frac{x + x_o/2}{2\sqrt{Dt}}\right)\right] \left[\operatorname{erf}\left(\frac{y - y_o/2}{2\sqrt{Dt}}\right) - \operatorname{erf}\left(\frac{y + y_o/2}{2\sqrt{Dt}}\right)\right] \tag{D.6}$$

where n_o is the initial value of the carrier distribution, x_o and y_o are the widths in x and y of the initial profile, and t is time. In terms of current, Equation (D.6) becomes:

$$\begin{aligned} J(x,y) &= -qn(x,y)v_z \\ &= \frac{J_o}{4}\left[\operatorname{erf}\left(\frac{x - x_o/2}{2\sqrt{Dt}}\right) - \operatorname{erf}\left(\frac{x + x_o/2}{2\sqrt{Dt}}\right)\right] \left[\operatorname{erf}\left(\frac{y - y_o/2}{2\sqrt{Dt}}\right) - \operatorname{erf}\left(\frac{y + y_o/2}{2\sqrt{Dt}}\right)\right] \end{aligned} \tag{D.7}$$

where q is the electron charge (1.602×10^{-19} C), v_z is the velocity of the carriers in the z-direction (assumed to be constant), and J_o is the initial value of the current profile. Equation (D.7) applied to the present problem, taking the current profile at the emitter-base junction ($z = 0$) as the initial condition, becomes:

$$J(x,y) = \frac{J_E}{4}\left[\operatorname{erf}\left(\frac{x - w_E/2}{2\sqrt{Dt}}\right) - \operatorname{erf}\left(\frac{x + w_E/2}{2\sqrt{Dt}}\right)\right] \left[\operatorname{erf}\left(\frac{y - l_E/2}{2\sqrt{Dt}}\right) - \operatorname{erf}\left(\frac{y + l_E/2}{2\sqrt{Dt}}\right)\right] \tag{D.8}$$

w_E and l_E are the width and length of the emitter junction, respectively.

Realizing that the time taken for the carriers to transit from $z = 0$ to $z = w_B$ is equivalent to the base transit time, τ_B, Equation (D.4) can be rewritten in terms of the emitter area ($A_E = w_E l_E$) and the collector area (A_C):

$$\beta = \frac{I_C}{J_E A_E - I_C} = \frac{I_C / J_E}{A_E - I_C / J_E} \tag{D.9}$$

where

$$\begin{aligned} \frac{I_C}{J_E} &= \frac{1}{J_E}\iint_{A_C} J(x,y)\Big|_{t=\tau_B}\, dxdy \\ &= \frac{1}{4}\iint_{A_C}\left[\operatorname{erf}\left(\frac{x - w_E/2}{2\sqrt{D\tau_B}}\right) - \operatorname{erf}\left(\frac{x + w_E/2}{2\sqrt{D\tau_B}}\right)\right] \\ &\qquad \left[\operatorname{erf}\left(\frac{y - l_E/2}{2\sqrt{D\tau_B}}\right) - \operatorname{erf}\left(\frac{y + l_E/2}{2\sqrt{D\tau_B}}\right)\right] dxdy \end{aligned} \tag{D.10}$$

In their present form, Equations (D.9) and (D.10) can be easily solved numerically. Evaluating Equation (D.10) analytically is very difficult and ultimately unnecessary since it does not offer any additional insight into the problem.

In the case of the oxide aperture HBT, neither the diffusion constant (D) nor the base transit time was known (τ_B). Therefore, Equations (D.9) and (D.10) were applied to the $A_C = 4 \times 10\ \mu m^2$ HBT and evaluated, setting β equal to its measured value, to determine the $\sqrt{D\tau_B}$ term. Given that the layer structures for all the HBTs considered were equivalent, β was then determined for the $A_C = 2 \times 10\ \mu m^2$ and $A_C = 1 \times 10\ \mu m^2$ HBTs assuming $\sqrt{D\tau_B}$ to be constant (Figure D.1). The associated current profiles at the base-collector junction ($z = w_B$) are shown in Figure D.3.

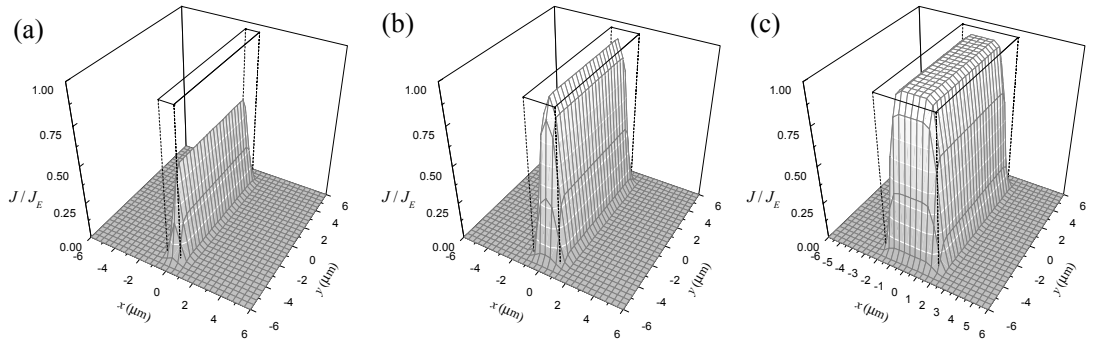

Figure D.3 Current profiles at the base-collector junction for (a) a $A_C = 1 \times 10\ \mu m^2$, (b) a $A_C = 2 \times 10\ \mu m^2$, and (c) a $A_C = 4 \times 10\ \mu m^2$ HBT. The square outline indicates the relative size of the collector area (A_C).

It is important to note that this model was derived assuming that the lateral motion of carriers is due solely to diffusion. In reality, the lateral motion of carriers is also affected by the potential distribution within the base. In a device with a relatively low

base resistance, the potential distribution should be fairly uniform, with the resulting error in the model being fairly small.

D.2 References

[1] S. K. Ghandhi, "The mathematics of diffusion" in *VLSI fabrication principles: silicon and gallium arsenide*, edited by S. K. Ghandhi (John Wiley & Sons, Inc., New York, 1994), pp. 801-17.

APPENDIX E

Derivation of f_τ and f_{max} with a Parasitic Input Capacitor

The classical form of the current-gain cutoff frequency (f_τ), originally given by Equation 3.1, is presented here again in an expanded form:

$$f_\tau = \frac{1}{2\pi\tau_\tau} = \frac{1}{2\pi}\left[\frac{\eta V_T}{I_C}\left(C_{BE}+C_{BC}\right)+\tau_B+\tau_C+\left(R_E+R_C\right)C_{BC}\right]^{-1} \qquad \text{(E.1)}$$

$$\tau_B = \frac{W_B{}^2}{2D_n} \qquad \tau_C = \frac{W_C}{2v_{sat}} \qquad \text{(E.2)}$$

$V_T = kT/q$ is the thermal voltage, where k is the Boltzmann constant (8.62×10^{-5} eV/K), T is the absolute temperature of the semiconductor in Kelvin, and q is the electronic charge (1.602×10^{-19} C); I_C is the collector current; C_{BE} and C_{BC} are the base-emitter and base-collector junction/depletion capacitances, respectively. τ_B and τ_C are the base and collector transit times, respectively, where W_B is the width of

the neutral base layer, D_n is the electron diffusion constant in the neutral base, W_C is the width of the depleted collector, and v_{sat} is the saturation velocity of electrons in the depleted collector; and R_E and R_C are the extrinsic emitter and collector resistances, respectively.

Equation (E.1) is derived using the model presented in Figure E.1.[1] The various elements of the model are defined as follows: R_B, R_E, and R_C are the total resistances (extrinsic and intrinsic) of the base, emitter, and collector, respectively; $g_m = g_{mo} e^{-j\omega(\tau_B+\tau_C)}$ is the transconductance, where $g_{mo} = \eta V_T / I_C$ is the DC transconductance and τ_C is the collector transit time as defined in Equation (E.2); r_π is related to the dynamic resistance of the base-emitter junction and is equal to β_o / g_{mo}, where β_o is the DC common-emitter current gain; C_{BE} is the base-emitter junction/depletion capacitance and $C_D = g_{mo}(\tau_B + \tau_C)$ is a diffusion capacitance associated with charge transport through the base and collector; and C_{BC} is the junction/depletion capacitance of the base-collector junction. In most situations, this

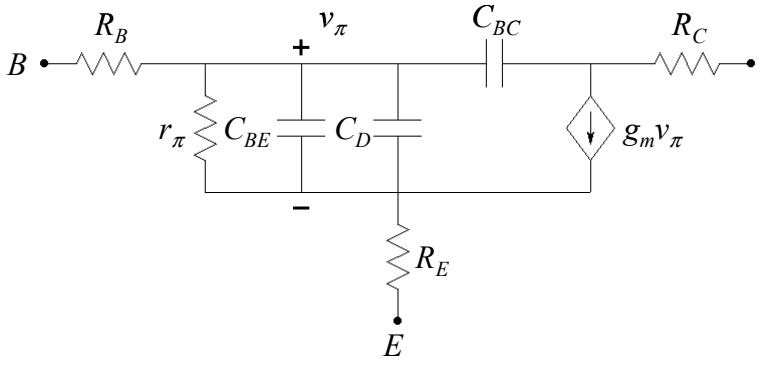

Figure E.1 A standard hybrid-π model of a bipolar transistor.[1]

model is more than sufficient to describe the frequency performance of a bipolar transistor.

In the case of the oxide aperture heterojunction bipolar transistor (HBT), an additional parasitic capacitance in the base-emitter junction exists as a result of the collector-up design (Figure E.2). A parasitic capacitor/resistor network, similar to a

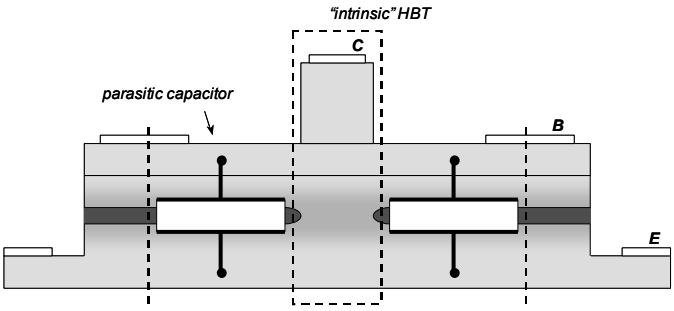

Figure E.2 Illustration of an oxide aperture HBT indicating the parasitic capacitance in the base-emitter junction.

lossy transmission line, would more accurately model the extrinsic portion of the base-emitter junction (Figure E.3); but to make the problem of solving for f_τ under the influence of a parasitic capacitance tractable, a single capacitor is used and the resistances outside of the parasitic capacitor are assumed to be negligible. The

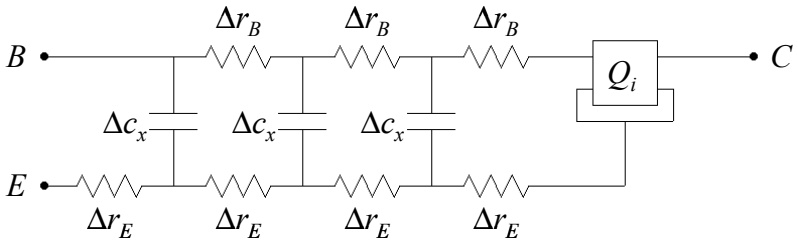

Figure E.3 Illustration of an intrinsic HBT (Q_i) with the suggested capacitor/resistor network (lossy transmission line) within the base-emitter access region. Δr_B, Δr_E, and Δc_x represent the differential components of the line.

resultant hybrid-π model of the oxide aperture HBT, including the parasitic capacitance (C_x), is presented in Figure E.4.

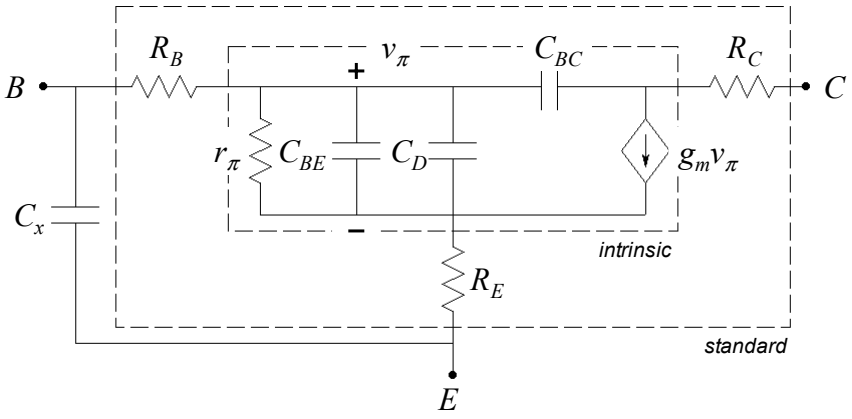

Figure E.4 Hybrid-π model of the oxide aperture HBT including the parasitic base-emitter capacitor, C_x.

E.1 Derivation of f_τ

f_τ is defined as the frequency at which the magnitude of the short-circuit current gain (h_{21}) drops to unity. h_{21} in terms of the two-port *Y*-parameters of an HBT is:

$$h_{21} = \left.\frac{i_2}{i_1}\right|_{v_2=0} = \left.\frac{i_2/v_1}{i_1/v_1}\right|_{v_2=0} = \frac{i_2/v_1|_{v_2=0}}{i_1/v_1|_{v_2=0}} = \frac{Y_{21}}{Y_{11}} \tag{E.3}$$

Though the equation for h_{21} is simple, directly deriving the expressions for Y_{21} and Y_{11} of even a standard HBT is fairly involved. For this reason an "inside-out" derivation of the *Y*-parameters is used, in which the parameters of the entire model are developed starting with the innermost, intrinsic model of the device and adding layers of complexity.

The *Y*-parameters of the intrinsic transistor ($\mathbf{Y^i}$) in Figure E.4 are simple enough to derive:

$$\begin{aligned} Y_{11}^i &= \left.\frac{i_1}{v_1}\right|_{v_2=0} = \frac{1}{r_\pi} + j\omega\left(C_{BE} + C_D + C_{BC}\right) \\ Y_{12}^i &= \left.\frac{i_1}{v_2}\right|_{v_1=0} = -j\omega C_{BC} \\ Y_{21}^i &= \left.\frac{i_2}{v_1}\right|_{v_2=0} = g_m - j\omega C_{BC} \\ Y_{22}^i &= \left.\frac{i_2}{v_2}\right|_{v_1=0} = j\omega C_{BC} \end{aligned} \tag{E.4}$$

$$\mathbf{Y^i} = \begin{bmatrix} Y_{11}^i & Y_{12}^i \\ Y_{21}^i & Y_{22}^i \end{bmatrix} \tag{E.5}$$

Examination of the standard transistor model, representing the intrinsic model as a two-port network (Figure E.5), allows the *Z*-parameters of the standard model ($\mathbf{Z^{std}}$) to be written as:

$$\begin{aligned} Z_{11}^{std} &= Z_{11}^i + R_B + R_E \\ Z_{12}^{std} &= Z_{12}^i + R_E \\ Z_{21}^{std} &= Z_{21}^i + R_E \\ Z_{22}^{std} &= Z_{22}^i + R_E + R_C \end{aligned} \tag{E.6}$$

$$\mathbf{Z^{std}} = \begin{bmatrix} Z_{11}^{std} & Z_{12}^{std} \\ Z_{21}^{std} & Z_{22}^{std} \end{bmatrix} \tag{E.7}$$

with:

$$\mathbf{Z^i} = \begin{bmatrix} Z_{11}^i & Z_{12}^i \\ Z_{21}^i & Z_{22}^i \end{bmatrix} = \begin{bmatrix} \frac{Y_{22}^i}{\Delta Y^i} & \frac{-Y_{12}^i}{\Delta Y^i} \\ \frac{-Y_{21}^i}{\Delta Y^i} & \frac{Y_{11}^i}{\Delta Y^i} \end{bmatrix} = \frac{1}{\Delta Y^i} \begin{bmatrix} Y_{22}^i & -Y_{12}^i \\ -Y_{21}^i & Y_{11}^i \end{bmatrix} \tag{E.8}$$

$$\Delta Y^i = Y_{11}^i Y_{22}^i - Y_{12}^i Y_{21}^i \tag{E.9}$$

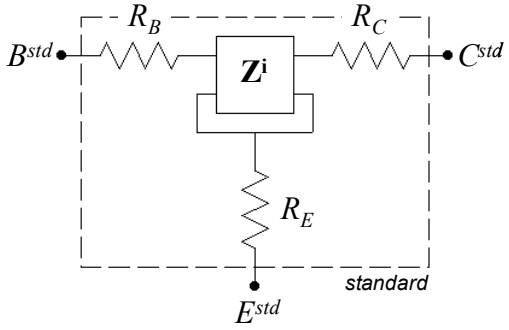

Figure E.5 The standard transistor model, representing the intrinsic transistor as a two-port network.

Repeating the procedure, representing the standard transistor model as a two-port network (Figure E.6), results in the *Y*-parameters of the overall oxide aperture transistor model (Y^x):

$$\begin{aligned} Y_{11}^x &= Y_{11}^{std} + j\omega C_x \\ Y_{12}^x &= Y_{12}^{std} \\ Y_{21}^x &= Y_{21}^{std} \\ Y_{22}^x &= Y_{22}^{std} \end{aligned} \tag{E.10}$$

$$\mathbf{Y^x} = \begin{bmatrix} Y_{11}^x & Y_{12}^x \\ Y_{21}^x & Y_{22}^x \end{bmatrix} \tag{E.11}$$

with:

$$\mathbf{Y^{std}} = \begin{bmatrix} Y_{11}^{std} & Y_{12}^{std} \\ Y_{21}^{std} & Y_{22}^{std} \end{bmatrix} = \begin{bmatrix} \dfrac{Z_{22}^{std}}{\Delta Z^{std}} & \dfrac{-Z_{12}^{std}}{\Delta Z^{std}} \\ \dfrac{-Z_{21}^{std}}{\Delta Z^{std}} & \dfrac{Z_{11}^{std}}{\Delta Z^{std}} \end{bmatrix} = \frac{1}{\Delta Z^{std}} \begin{bmatrix} Z_{22}^{std} & -Z_{12}^{std} \\ -Z_{21}^{std} & Z_{11}^{std} \end{bmatrix} \tag{E.12}$$

$$\Delta Z^{std} = Z_{11}^{std} Z_{22}^{std} - Z_{12}^{std} Z_{21}^{std} \tag{E.13}$$

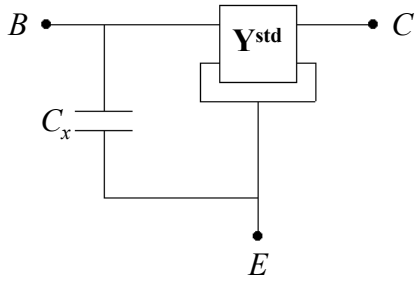

Figure E.6 The oxide aperture transistor model, representing the standard transistor as a two-port network.

With the *Y*-parameters of the oxide aperture transistor, h_{21} for the device can be evaluated.

$$h_{21} = \frac{Y_{21}^{x}}{Y_{11}^{x}} = \frac{-Z_{21}^{std} / \Delta Z^{std}}{Z_{22}^{std} / \Delta Z^{std} + j\omega C_x} = \frac{-Z_{21}^{std}}{Z_{22}^{std} + j\omega C_x \Delta Z^{std}} \tag{E.14}$$

Evaluating ΔZ^{std}:

$$\begin{aligned} \Delta Z^{std} &= Z_{11}^{std} Z_{22}^{std} - Z_{12}^{std} Z_{21}^{std} \\ &= \left(Z_{11}^{i} + R_B + R_E\right)\left(Z_{22}^{i} + R_E + R_C\right) - \left(Z_{12}^{i} + R_E\right)\left(Z_{21}^{i} + R_E\right) \\ &= \left(\frac{Y_{22}^{i}}{\Delta Y^{i}} + R_B + R_E\right)\left(\frac{Y_{11}^{i}}{\Delta Y^{i}} + R_E + R_C\right) - \left(\frac{-Y_{12}^{i}}{\Delta Y^{i}} + R_E\right)\left(\frac{-Y_{21}^{i}}{\Delta Y^{i}} + R_E\right) \\ &= \frac{1}{\Delta Y^{i}}\Big[1 + \left(R_B + R_E\right)Y_{11}^{i} + \left(R_E + R_C\right)Y_{22}^{i} \\ &\qquad + R_E\left(Y_{12}^{i} + Y_{21}^{i}\right) + \left(R_B R_E + R_B R_C + R_E R_C\right)\Delta Y^{i}\Big] \end{aligned}$$

$$\Delta Z^{std} = \frac{\zeta^{std}}{\Delta Y^i} \tag{E.15}$$

The numerator has been equated to ζ^{std} for convenience.

Plugging Equation (E.15) back into Equation (E.14) and evaluating Z_{21}^{std} and Z_{22}^{std} results in:

$$\begin{aligned} h_{21} &= \frac{\left(Y_{21}^i - R_E \Delta Y^i\right) / \Delta Y^i}{\left[Y_{11}^i + \left(R_E + R_C\right)\Delta Y^i\right] / \Delta Y^i + j\omega C_x \zeta^{std} / \Delta Y^i} \\ &= \frac{Y_{21}^i - R_E \Delta Y^i}{Y_{11}^i + \left(R_E + R_C\right)\Delta Y^i + j\omega C_x \zeta^{std}} \end{aligned} \tag{E.16}$$

Evaluating ΔY^i:

$$\begin{aligned} \Delta Y^i &= Y_{11}^i Y_{22}^i - Y_{12}^i Y_{21}^i \\ &= \left[\frac{1}{r_\pi} + j\omega\left(C_{BE} + C_D + C_{BC}\right)\right]\left[j\omega C_{BC}\right] - \left[-j\omega C_{BC}\right]\left[g_m - j\omega C_{BC}\right] \\ &= j\omega C_{BC}\left[\frac{1}{r_\pi} + g_{mo} e^{-j\omega(\tau_B + \tau_C)} + j\omega\left(C_{BE} + C_D\right)\right] \end{aligned}$$

Assuming the frequency range over which we are concerned in is much less than $1/\left(\tau_B + \tau_C\right)$ allows $e^{-j\omega(\tau_B + \tau_C)}$ to be approximated by $\left[1 - j\omega\left(\tau_B + \tau_C\right)\right]$. Therefore:

$$\Delta Y^i \simeq j\omega C_{BC}\left[\frac{1}{r_\pi} + g_{mo} + j\omega\left(C_{BE} + C_D - g_{mo}\tau_B - g_{mo}\tau_B\right)\right]$$

Ignoring terms ω^2 and higher:

$$\Delta Y^i \simeq j\omega C_{BC}\left(\frac{1}{r_\pi}+g_{mo}\right)$$
$$\simeq j\omega C_{BC}\left(\frac{g_{mo}}{\beta_o}+g_{mo}\right)\simeq j\omega g_{mo}C_{BC}\left(\frac{1}{\beta_o}+1\right)$$

For most transistors $\beta_o \gg 1$, resulting in:

$$\Delta Y^i \simeq j\omega g_{mo}C_{BC} \tag{E.17}$$

Plugging ΔY^i back into Equation (E.16) and replacing the intrinsic *Y*-parameters:

$$h_{21}=\frac{g_m - j\omega C_{BC} - j\omega g_{mo}R_E C_{BC}}{\frac{1}{r_\pi}+j\omega\left(C_{BE}+C_D+C_{BC}\right)+j\omega g_{mo}\left(R_E+R_C\right)C_{BC}+j\omega C_x\zeta^{std}}$$

$$\text{with } \zeta^{std}=1+\frac{R_B+R_E}{r_\pi}+j\omega\left(R_B+R_E\right)\left(C_{BE}+C_D+C_{BC}\right)$$
$$+j\omega\left(R_E+R_C\right)C_{BC}+R_E g_m - j\omega 2R_E C_{BC}$$
$$+j\omega g_{mo}\left(R_B R_E+R_B R_C+R_E R_C\right)C_{BC}$$

Setting $g_m = g_{mo}e^{-j\omega(\tau_B+\tau_C)} \simeq g_{mo}\left[1-j\omega\left(\tau_B+\tau_C\right)\right]$, $r_\pi = \beta_o / g_{mo}$, and ignoring terms ω^2 and higher results in:

$$h_{21}\simeq\frac{g_{mo}-j\omega\left[\left(1+g_{mo}R_E\right)C_{BC}+g_{mo}\tau_B+g_{mo}\tau_C\right]}{\frac{g_{mo}}{\beta_o}+j\omega\left[C_{BE}+C_D+C_{BC}+g_{mo}\left(R_E+R_C\right)C_{BC}+\left(1+\frac{g_{mo}}{\beta_o}\left(R_B+R_E\right)+g_{mo}R_E\right)C_x\right]}$$
$$\simeq\frac{1-j\omega\left[\left(1/g_{mo}+R_E\right)C_{BC}+\tau_B+\tau_C\right]}{\frac{1}{\beta_o}+j\omega\left[\frac{1}{g_{mo}}\left(C_{BE}+C_D+C_{BC}\right)+\left(R_E+R_C\right)C_{BC}+\left(\frac{1}{g_{mo}}+\frac{R_B}{\beta_o}+R_E\left(1+\frac{1}{\beta_o}\right)\right)C_x\right]}$$

For $\beta_o \gg 1$:

$$h_{21} \simeq \frac{1 - j\omega\left[\left(1/g_{mo} + R_E\right)C_{BC} + \tau_B + \tau_C\right]}{j\omega\left[\frac{1}{g_{mo}}\left(C_{BE} + C_D + C_{BC}\right) + \left(R_E + R_C\right)C_{BC} + \left(\frac{1}{g_{mo}} + \frac{R_B}{\beta_o} + R_E\right)C_x\right]}$$

Setting the frequency "coefficients" to:

$$\begin{aligned} \tau_z &= \left(1/g_{mo} + R_E\right)C_{BC} + \tau_B + \tau_C \\ \tau_p &= \frac{1}{g_{mo}}\left(C_{BE} + C_D + C_{BC}\right) + \left(R_E + R_C\right)C_{BC} + \left(\frac{1}{g_{mo}} + \frac{R_B}{\beta_o} + R_E\right)C_x \end{aligned} \tag{E.18}$$

allows h_{21} to be written as:

$$h_{21} \simeq \frac{1 - j\omega\tau_z}{j\omega\tau_p} \tag{E.19}$$

Solving for the magnitude of h_{21} and setting it equal to unity:

$$\left|h_{21}\right\|_{\omega=\omega_\tau} \simeq \frac{\sqrt{1 + \left(\omega_\tau\tau_z\right)^2}}{\omega_\tau\tau_p} = 1$$

Assuming $1/\tau_z \gg \omega_\tau$ results in:

$$\begin{aligned} \frac{1}{\omega_\tau} = \tau_p &= \frac{1}{g_{mo}}\left(C_{BE} + C_D + C_{BC}\right) + \left(R_E + R_C\right)C_{BC} + \left(\frac{1}{g_{mo}} + \frac{R_B}{\beta_o} + R_E\right)C_x \\ &= \frac{1}{g_{mo}}\left(C_{BE} + g_{mo}\tau_B + g_{mo}\tau_C + C_{BC}\right) + \left(R_E + R_C\right)C_{BC} + \left(\frac{1}{g_{mo}} + \frac{R_B}{\beta_o} + R_E\right)C_x \\ &= \frac{1}{g_{mo}}\left(C_{BE} + C_{BC}\right) + \tau_B + \tau_C + \left(R_E + R_C\right)C_{BC} + \left(\frac{1}{g_{mo}} + \frac{R_B}{\beta_o} + R_E\right)C_x \end{aligned}$$

$$\frac{1}{\omega_\tau} = \frac{\eta V_T}{I_C}\left(C_{BE} + C_{BC}\right) + \tau_B + \tau_C + \left(R_E + R_C\right)C_{BC} + \left(\frac{\eta V_T}{I_C} + \frac{R_B}{\beta_o} + R_E\right)C_x \tag{E.20}$$

Recognizing that $\tau_p \gg \tau_z$, the assumption of $1/\tau_z \gg \omega_\tau$ in the derivation of Equation (E.20) was reasonable.

Recalling the form of the current-gain cutoff frequency for a standard HBT (Equation (E.1)), Equation (E.20) may be rewritten as:

$$f_{\tau,x} = \frac{1}{2\pi}\left[\tau_{\tau,std} + \left(\frac{\eta V_T}{I_C} + \frac{R_B}{\beta_o} + R_E\right)C_x\right]^{-1}$$
$$\tau_{\tau,std} = \frac{\eta V_T}{I_C}\left(C_{BE} + C_{BC}\right) + \tau_B + \tau_C + \left(R_E + R_C\right)C_{BC} \qquad \text{(E.21)}$$

Equation (E.21) is the current-gain cutoff frequency for a transistor with a parasitic base-emitter capacitor ($f_{\tau,x}$) as shown in Figure E.4. Setting $C_x = 0$ reduces Equation (E.21) to Equation (E.1), as expected.

Method of Time Constants

The preceding derivation of f_τ, based on the *Y*-parameters of the device, though correct is somewhat excessive. In situations where the derivation of *Y*-parameters are not required or desired, it is more convenient to determine f_τ by means of the Method of Time Constants (MoTC). Under the MoTC, gain (voltage or current) is approximated by:

$$A \simeq \frac{A\big|_{\omega=0}}{1 + j\omega\tau_p} \qquad \text{(E.22)}$$

where A is the overall gain, $A\big|_{\omega=0}$ is the associated DC gain, and τ_p is a time constant equivalent to the summation of the first order RC time constants within the device/circuit/system.

Applying the MoTC to the oxide aperture HBT (Figure E.4), the short-circuit current gain (h_{21}) is given by:

$$h_{21} \simeq \frac{\beta_o}{1 + j\omega\tau_p} \tag{E.23}$$

$$\begin{aligned}\tau_p &= \tau_{BE,D} + \tau_{BC} + \tau_x \\ &= \beta_0\left(\frac{\eta V_T}{I_C}C_{BE} + \tau_B + \tau_C\right) + \beta_o\left(\frac{\eta V_T}{I_C} + R_E + R_C\right)C_{BC} + \beta_o\left(\frac{\eta V_T}{I_C} + \frac{R_B}{\beta_o} + R_E\right)C_x\end{aligned} \tag{E.24}$$

where $\tau_{BE,D}$, τ_{BC}, and τ_x are the RC time constants associated with C_{BE} and C_D, C_{BC}, and C_x, respectively.

Solving Equation (E.23) for f_τ of the oxide aperture HBT results in:

$$\begin{aligned}f_{\tau,x} &= \frac{1}{2\pi}\frac{\beta_o}{\tau_p} \\ &= \frac{1}{2\pi}\left[\frac{\eta V_T}{I_C}\left(C_{BE} + C_{BC}\right) + \tau_B + \tau_C + \left(R_E + R_C\right)C_{BC} + \left(\frac{\eta V_T}{I_C} + \frac{R_B}{\beta_o} + R_E\right)C_x\right]^{-1}\end{aligned} \tag{E.25}$$

Recognizing the relative terms, Equation (E.25) may be rewritten as:

$$\begin{aligned}f_{\tau,x} &= \frac{1}{2\pi}\left[\tau_{\tau,std} + \left(\frac{\eta V_T}{I_C} + \frac{R_B}{\beta_o} + R_E\right)C_x\right]^{-1} \\ \tau_{\tau,std} &= \frac{\eta V_T}{I_C}\left(C_{BE} + C_{BC}\right) + \tau_B + \tau_C + \left(R_E + R_C\right)C_{BC}\end{aligned} \tag{E.26}$$

which is equivalent to Equation (E.21) from the preceding derivation.

One conceptual advantage of the MoTC is that it permits the immediate recognition of the RC_x time constant as an additional delay term within f_τ.

E.2 Derivation of f_{max}

One definition for f_{max} is the frequency at which the magnitude of the unilateral power gain (U) drops to unity. U in terms of the two-port Y-parameters of an HBT is given by Equation (E.27).[1]

$$U = \frac{\left|Y_{21} - Y_{12}\right|^2}{4\left[\mathrm{Re}\left(Y_{11}\right)\mathrm{Re}\left(Y_{22}\right) - \mathrm{Re}\left(Y_{12}\right)\mathrm{Re}\left(Y_{21}\right)\right]} \tag{E.27}$$

For a standard HBT, Equation (E.27) results in:

$$U_{std} = \frac{\left|Y_{21}^{std} - Y_{12}^{std}\right|^2}{4\left[\mathrm{Re}\left(Y_{11}^{std}\right)\mathrm{Re}\left(Y_{22}^{std}\right) - \mathrm{Re}\left(Y_{12}^{std}\right)\mathrm{Re}\left(Y_{21}^{std}\right)\right]} \simeq \frac{\omega_{\tau,std}{}^2}{4R_B C_{BC}\omega^2} \tag{E.28}$$

Solving for f_{max} ($U^{std} = 1$):

$$f_{max,std} = \sqrt{\frac{f_{\tau,std}}{8\pi R_B C_{BC}}} \tag{E.29}$$

To determine f_{max} for a transistor with a parasitic input capacitor (Figure E.4), Equation (E.27) is applied to $\mathbf{Y^x}$.

$$U_x = \frac{\left|Y_{21}^x - Y_{12}^x\right|^2}{4\left[\mathrm{Re}\left(Y_{11}^x\right)\mathrm{Re}\left(Y_{22}^x\right) - \mathrm{Re}\left(Y_{12}^x\right)\mathrm{Re}\left(Y_{21}^x\right)\right]} \tag{E.30}$$

Recognizing that $\mathbf{Y^x}$ is equal to $\mathbf{Y^{std}}$ with the exception of $Y_{11}^{x} = Y_{11}^{std} + j\omega C_x$, U_x becomes:

$$U_x = \frac{\left|Y_{21}^{std} - Y_{12}^{std}\right|^2}{4\left[\mathrm{Re}\left(Y_{11}^{std} + j\omega C_x\right)\mathrm{Re}\left(Y_{22}^{std}\right) - \mathrm{Re}\left(Y_{12}^{std}\right)\mathrm{Re}\left(Y_{21}^{std}\right)\right]}$$

$$\mathrm{Re}\left(Y_{11}^{std} + j\omega C_x\right) = \mathrm{Re}\left(Y_{11}^{std}\right)$$

therefore:

$$U_x = \frac{\left|Y_{21}^{std} - Y_{12}^{std}\right|^2}{4\left[\mathrm{Re}\left(Y_{11}^{std}\right)\mathrm{Re}\left(Y_{22}^{std}\right) - \mathrm{Re}\left(Y_{12}^{std}\right)\mathrm{Re}\left(Y_{21}^{std}\right)\right]} = U_{std} \qquad \text{(E.31)}$$

Solving for f_{max} ($U^x = U^{std} = 1$):

$$f_{max,x} = f_{max,std} = \sqrt{\frac{f_{\tau,std}}{8\pi R_B C_{BC}}} \qquad \text{(E.32)}$$

Equation (E.32) is the maximum frequency of oscillation for a transistor with a parasitic base-emitter capacitor ($f_{max,x}$) shown in Figure E.4 and is *identical* to f_{max} for a standard HBT.

The implications of Equations (E.21) and (E.32) are profound. Equation (E.21) states that the parasitic input capacitor (C_x) enters into f_τ as an additional "charging" time constant, resulting in a reduced f_τ; but Equation (E.32), which commonly relates f_τ to f_{max} of a transistor, asserts f_{max} is *not* proportional to the f_τ of the device as presented in Equation (E.21) but to the f_τ of the device without the parasitic input capacitor, Equation (E.1). In other words, C_x has no effect on f_{max}.

E.3 Y-parameters of an HBT with a Parasitic Capacitor

For completeness, the *Y*-parameters of the HBT model with parasitic capacitor (Figure E.4) are presented here:

$$\begin{aligned}
Y_{11}^{x} &\simeq \frac{1}{\zeta^{std}}\left[\frac{1}{r_\pi}-\omega^2\left(R_E+R_C\right)C_{BE}C_{BC}\right] \\
&\quad + j\omega\left[\frac{1}{\zeta^{std}}\left(g_{mo}\left(R_E+R_C\right)C_{BC}+C_{BE}+C_D+C_{BC}\right)+C_x\right] \\
Y_{12}^{x} &\simeq -\frac{\omega^2 R_E C_{BE}C_{BC}}{\zeta^{std}} - j\omega\frac{\left(1+g_{mo}R_E\right)C_{BC}}{\zeta^{std}} \\
Y_{21}^{x} &\simeq \frac{g_{mo}+\omega^2 R_E C_{BE}C_{BC}}{\zeta^{std}} - j\omega\frac{C_D+\left(1+g_{mo}R_E\right)C_{BC}}{\zeta^{std}} \\
Y_{22}^{x} &\simeq -\frac{\omega^2\left(R_B+R_C\right)C_{BE}C_{BC}}{\zeta^{std}} + j\omega\frac{\left[1+g_{mo}\left(R_B+R_C\right)\right]C_{BC}}{\zeta^{std}}
\end{aligned} \tag{E.33}$$

$$\begin{aligned}
\zeta^{std} = 1+g_{mo}\left(\frac{R_B}{\beta_o}+R_E\right) + j\omega\big[& R_B\left(C_{BE}+C_D+C_{BC}\right)+R_E C_\pi \\
& +R_C C_{BC}+g_{mo}\left(R_B R_E+R_E R_C\right)C_{BC}\big]
\end{aligned} \tag{E.34}$$

At low frequencies ($\omega \to 0$), the *Y*-parameters reduce to:

$$\mathbf{Y}^{\mathbf{x}}\Big|_{\omega\to 0} \simeq \begin{bmatrix} \left(r_\pi+R_B+\beta_o R_E\right)^{-1} & 0 \\ \dfrac{g_{mo}}{1+g_{mo}\left(R_B/\beta_o+R_E\right)} & 0 \end{bmatrix} \tag{E.35}$$

It is important to note that the *Y*-parameters developed here were derived assuming that the resistance between the base and collector (r_{BC}) and the output resistance (r_o) were infinite. The addition of these two resistances would result in a more accurate and complete model, especially at low frequency, making the

Y-parameters more useful for model extraction; but the error resulting from the exclusion of these resistances in the derivation of f_τ and f_{max} is negligible.

E.4 References

[1] W. Liu, *Handbook of III-V heterojunction bipolar transistors* (John Wiley & Sons, Inc., New York, 1998).