UNIVERSITY OF CALIFORNIA
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A Technology Incorporating Selective Area Regrowth for High Uniformity, Low Phase Noise, Single-Level Metal High Electron Mobility Transistors (HEMTs)

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

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in

Electrical and Computer Engineering

by

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December 1996

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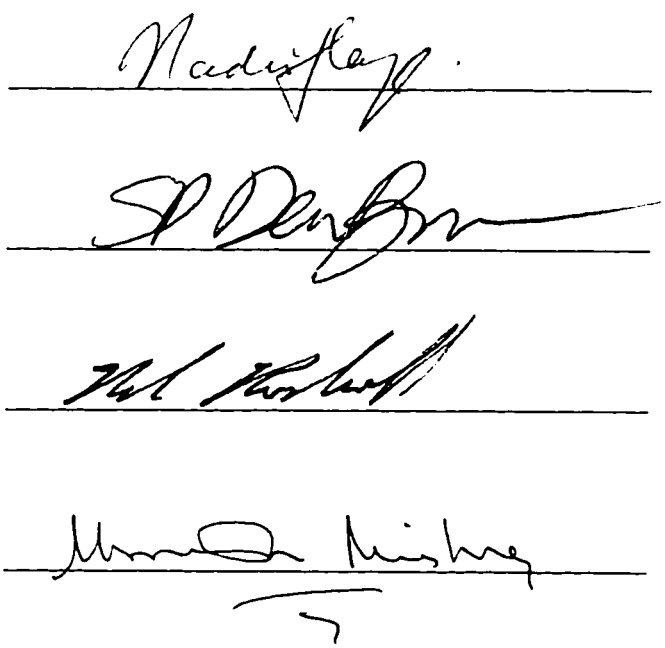

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Bugünümü borçlu olduğum sevgili Anneciğime, Babacığıma ve yaşamımın son 5.5 yılını paylaştığım sevgili eşim Zarina'ya...

To my dearest parents, Nezihi and Seniha Kızıloğlu, to whom I owe where I am today, and to my dearest wife, Zarina, for being with me for the last 5.5 years of my life...

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1. K. Kiziloglu, B.P. Keller, P.M. Chavarkar, X. Cao, S.P. DenBaars, U.K. Mishra, "Selective area growth as an enabling technology for high-uniformity single-level metal HEMTs," presented at the 38th Electronic Materials Conference held in Santa Barbara, CA, June 26-28, 1996.

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Fields of Study

Studies in electromagnetics and microwave modeling
Professors Nadir Dağlı and George L. Matthaei

Studies in compound semiconductor devices, fabrication and modeling
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Abstract

A Technology Incorporating Selective Area Regrowth for High Uniformity, Low Phase Noise, Single-Level Metal High Electron Mobility Transistors (HEMTs)

by

Kürşad Kızıloğlu

A reproducible, uniform, and reliable FET technology for various high frequency and low noise applications including receivers, transmitters, microwave and opto-electronic integrated circuits is crucial. The rapid developments in materials technologies have made it possible to investigate the fabrication of FETs, where processing and growth are continuously interleaved throughout the fabrication of devices. In this work, we report on the fabrication of a HEMT, where selective growth is employed twice to arrive at the final device: once to achieve low resistance ohmic contacts, and second time to achieve a stable epitaxial surface passivation.

We first develop a technology for non-alloyed ohmic contacts with highly doped regrowth of GaInAs on various GaInAs channel devices including AlInAs/GaInAs/InP HEMTs. For the regrowths done on HEMTs with Si doping in the AlInAs donor layer, we find that, if the doping concentration in the regrown GaInAs is low ($n = 1.5 \cdot 10^{18}$ cm^{-3}), and HF solutions are employed in the processing steps, there exist instabilities in the contacts at higher temperatures. This is attributed to the passivation of Si dopant atoms in AlInAs by fluorine. However, we achieve temperature stable ohmic contacts with a contact resistance of 0.1 $\Omega \cdot mm$ regardless of the samples' exposure to HF when higher doping ($n = 7 \cdot 10^{18}$ cm^{-3}) is incorporated in the regrowth process.

Based on the regrowth technology with which we have achieved non-alloyed, low resistance highly doped source and drain contacts, we demonstrate the feasibility of HEMTs with epitaxial surface passivation. We examine the merits and drawbacks of epitaxially passivating our devices by overgrowing both InP by MOCVD, and AlInAs by MOCVD and MBE. The implementation of epitaxial overgrowth coupled with the regrown contacts enable the following: (i) fabrication of devices with a single level of metalization for all the source, drain, and gate contacts, (ii) elimination of recess etching as lower access region

resistance is guaranteed by the overgrowth in the access regions, and (iii) devices with suppressed low-frequency and phase noise characteristics. We report on the dc, microwave, low-frequency and phase noise characteristics of these epitaxially passivated HEMTs with regrown contacts, and compare their performance to existing data in the literature.

Table of Contents

Introduction

A reproducible, uniform, and reliable FET technology for various high frequency and low noise applications including receivers, transmitters, opto-electronic integrated circuits (OEICs) and microwave monolithic integrated circuits (MMICs) is crucial. In this dissertation, we report on the realization of InP based FETs that utilize developments in materials technologies, whereby processing and growth are continuously interleaved throughout the fabrication of the devices. The final devices employ selective regrowth twice: once to achieve low resistance ohmic contacts, and second time to achieve a stable epitaxial surface passivation. The implementation of epitaxial overgrowth coupled with the regrown contacts enable: (i) fabrication of devices with a single level of metalization for all the source, drain, and gate contacts, (ii) elimination of recess etching, and (iii) devices with suppressed low-frequency and phase noise characteristics.

It is recognized that ohmic contacts play an important role in the high frequency and low noise transistors as the need to reduce device parasitics and further improve device characteristics becomes more pressing. Among the various methods for establishing ohmic contacts to semiconductor devices are:

(i) standard ohmic contacts achieved by deposition of metal on the semiconductor and subsequent alloying.

(ii) ion implantation of dopant species (such as Si for n-type ohmic contacts) in the source and drain regions. This step is followed by a high temperature annealing process to activate the implanted dopants. Finally as is done in (i), metal is deposited and alloyed to create the ohmic contact.

(iii) non-alloyed contacts to highly doped regrown regions in the source and drain areas.

We thus start in Chapter 1 by giving a background on the methods used to characterize ohmic contacts. We briefly talk about the physics of metal-semiconductor junctions and introduce a circuit theory based formulation methodology to tackle contacts in which current conduction takes place in two layers instead of a single one. We then use this methodology and a theoretical approach based on the physics of ohmic contacts to analyze an implementation of regrown contacts achieved with GaInAs regrowth on InP channel devices.

As mentioned above, one possible means of achieving ohmic contacts is the implantation of donor species into areas where contacts are desired. However, because implantation requires high temperature anneal steps for dopant activation, in Chapter 2 we characterize the effects of high temperature treatment on AlInAs/GaInAs/InP HEMT structures. We perform a series of annealing experiments and investigate the effects of these high temperature anneals on the mobility and the sheet carrier concentration of the electrons. We conclude the chapter by discussing the viability of implanted contacts for various applications.

In the rest of the dissertation, we concentrate our efforts in investigating highly doped regrown GaInAs contacts on InP based FETs. Regrown contacts have inherent advantages over other contact schemes in that (i) they enable non-alloyed contacts, which improves device stability and reliability, (ii) single level metal fabrication of FETs is possible, where the gate, source and drain metalizations are carried out at the same time, and perhaps most importantly, (iii) they create an enabling technology, which makes it possible to achieve good ohmic contacts to semiconductor devices regardless of the channel material. In Chapter 3, we thus investigate "homojunction regrowth" where highly doped GaInAs is regrown on GaInAs channel devices. We report on the instabilities encountered in the contacts for lower doping concentrations used in the regrown GaInAs when HF is employed in the processing steps. However, we present low resistance and temperature stable ohmic contacts regardless of the sample's exposure to HF when higher doping is incorporated in the regrowth process.

Based on the regrowth technology for achieving non-alloyed, low resistance highly n^+ doped source and drain contacts, we then demonstrate in Chapter 4, the feasibility of HEMTs with epitaxial surface passivation. We give fabrication details and show dc, microwave, low-frequency noise and phase noise measurement results on HEMTs with regrown contacts that have a single level of metalization for all the source, drain and gate terminals, and because of surface epitaxial passivation, that require no recess etching. We conclude the chapter by comparing our devices with the state-of-the-art.

Three appendices follow an overall summary and notes on possible directions for future work. Appendix 1 gives general processing details and is followed by Appendix 2 on electron beam lithography at UCSB. Appendix 3 lists the manufacturer's safety data sheets on the particular E-beam resists used.

Chapter 1

Ohmic Contacts and Contact Resistance of Regrown GaInAs on InP

Ohmic contacts are the terminals through which the semiconductor devices communicate with the outside world electrically. Good ohmic contacts should be stable with respect to both time and temperature, and should have low resistance associated with them to make it possible to access the intrinsic devices without losing much of the original information that is sent or received from the device. They continue to play an important role in today's high frequency and low noise transistors as well, as the need to reduce device parasitics and further improve device characteristics becomes more pressing. There are various methods for establishing ohmic contacts to semiconductor devices:

(i) standard ohmic contacts achieved by deposition of metal on the semiconductor and subsequent alloying.

(ii) ion implantation of dopant species (such as Si for n-type ohmic contacts) in the source and drain regions. This step is followed by a high temperature annealing process to activate the implanted dopants. Finally as is done in (i), metal is deposited and alloyed to create the ohmic contact.

(iii)non-alloyed contacts to highly doped epitaxially regrown regions in the source and drain areas.

In this chapter we give a background on the methods that are used to characterize ohmic contacts and report contacts achieved by regrowth of n^+-GaInAs on n-InP channel devices.

1.1. Definitions, Models and Measurement Methods

Figure 1.1 shows a schematic of ohmic contacts on a lateral device. The total resistance R between the two terminals is given by

$$R = 2R_C + R_S \frac{L}{w}, \qquad (1.1)$$

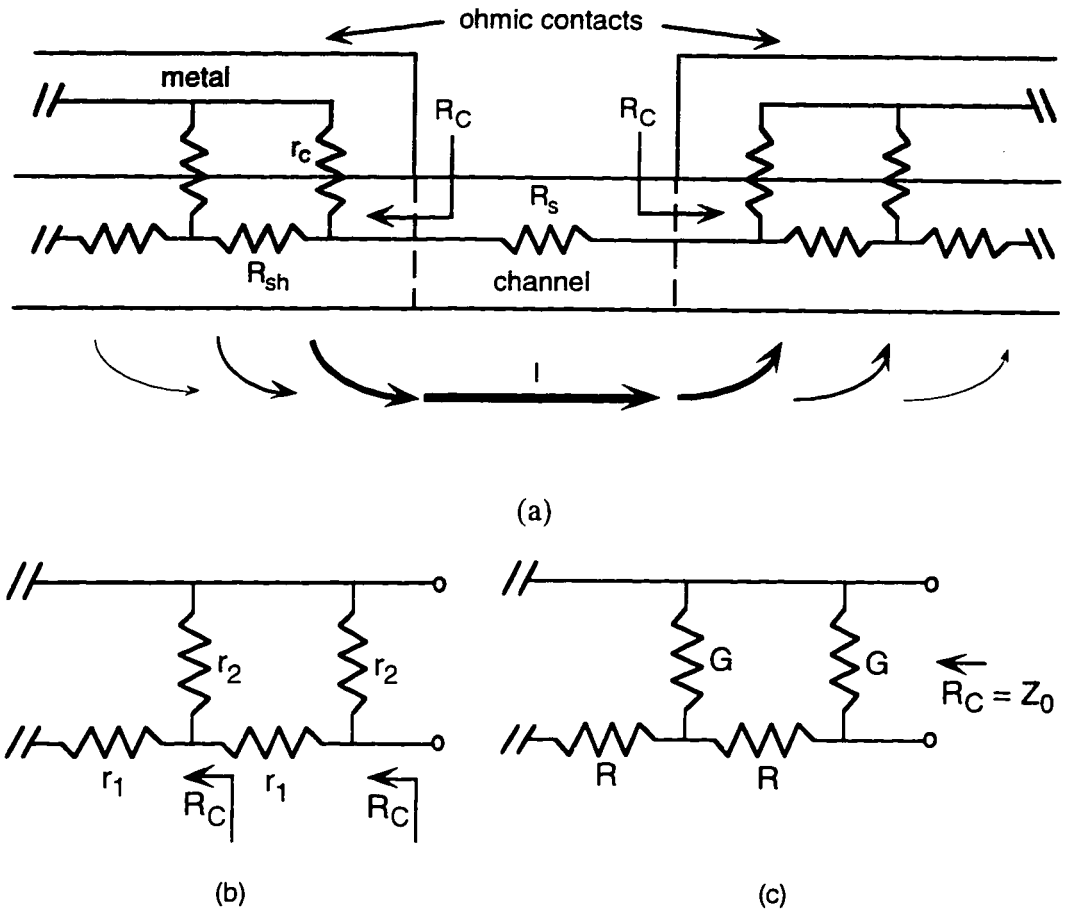

Figure 1.1. (a) Schematic cross section of a conductive channel with ohmic contacts at the ends. The current decreases exponentially as it moves away from the edges of the metalization. (b) Resistor network model for the contact resistance. (c) Transmission line model for the contact resistance.

where R_C (Ω) is the contact resistance of the ohmic contact, R_S (Ω/sq) is the sheet resistance of the channel material, L is the separation, and w is the width of the contacts. The parameter shown in the figure as r_c ($\Omega \cdot cm^2$) is the specific contact resistivity and is the basic parameter that characterizes the contact between the metal and the semiconductor. It is possible to model the current conduction underneath the contacts with a resistor network as shown in Figure 1.1 (b). The current drops exponentially as it moves further into the contacts. A relevant parameter is the transfer length, L_t, under the contact, where the current has dropped to 1/e of its initial value at the edge. For modern microwave devices this value is about a micron or less. Since the dimensions of the pads provided for ohmic contacts on device mask layouts are on the order of tens of microns, the

resistor network can be assumed to be a semi-infinite one for all practical purposes [1].

We can calculate the relationships among the various resistance parameters by the models shown in Figure 1.1. In Figure 1.1 (b), the resistors r_1 and r_2 are given in terms of the device parameters as

$$r_1 = \frac{R_{sh}}{w}\,dx \text{ and } r_2 = \frac{r_c}{w\,dx}. \tag{1.2}$$

Utilizing the fact that we have a semi-infinite network, we can write

$$(r_1 + R_C) \,//\, r_2 = R_C, \tag{1.3}$$

and obtain

$$R_C^2 + r_1 R_C - r_1 r_2 = 0. \tag{1.4}$$

If we now insert the values for r_1 and r_2 from (1.2) into (1.4), let dx go to zero, and solve for R_C, we get

$$R_C = \frac{\sqrt{r_c R_{sh}}}{w}, \text{ or } r_c = \frac{\left(R_C\, w\right)^2}{R_{sh}}. \tag{1.5}$$

We can arrive at the same result from a transmission line point of view as well [3]. In this case, the resistance per unit length, R, and the conductance per unit length, G as shown in Figure 1.1 (c) are given by

$$R = R_{sh} / w \text{ and } G = w / r_c. \tag{1.6}$$

The well known transmission line equations for the characteristic impedance Z_0 and the propagation constant γ are

[1] The succeding analysis is modified slightly for cases where the contacts have finite lengths [1, 2].

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \text{ and } \gamma = \sqrt{(R + j\omega L)(G + j\omega C)}, \tag{1.7}$$

where L and C are the inductance and the capacitance per unit length. In our case, since we have a purely resistive "transmission line", $L = C = 0$. Substituting the values of R and G from (1.6) into (1.7), and remembering that the input impedance of an infinite transmission line is its characteristic impedance, we obtain

$$Z_0 = R_C = \frac{\sqrt{r_c R_{sh}}}{w} \text{ and } \gamma = \frac{1}{L_t} = \sqrt{\frac{R_{sh}}{r_c}}, \tag{1.8}$$

which is the same result as obtained in (1.5).

To measure the contact and sheet resistances experimentally, a test pattern comprising of ohmic contacts with varying separations on isolated bars is used as shown in Figure 1.2 (a). To obtain the contact and sheet resistances of the structure, the measured resistance values are plotted with respect to the contact separation as shown in Figure 1.2 (b). From a linear fit, R_C and R_S can be quickly extracted as shown. The x-intercept L_x, is related to the transfer length, L_t. From (1.1), L_x can be written as

$$L_x = \frac{2 R_C w}{R_S}. \tag{1.9}$$

By substituting R_C in terms of r_c, and r_c in terms of L_t from (1.8), we obtain

$$L_x = \frac{2 R_{sh}}{R_S} L_t. \tag{1.10}$$

Normally the sheet resistance under the contact, R_{sh}, and the sheet resistance of the channel, R_S are different from each other as the contact is formed by alloying, implantation of dopants, or regrowth of highly doped material. Therefore additional measurements would be required if the values of r_c, R_{sh}, or L_t were desired. However, for practical considerations, $R_{sh} = R_S$ is generally assumed [2].

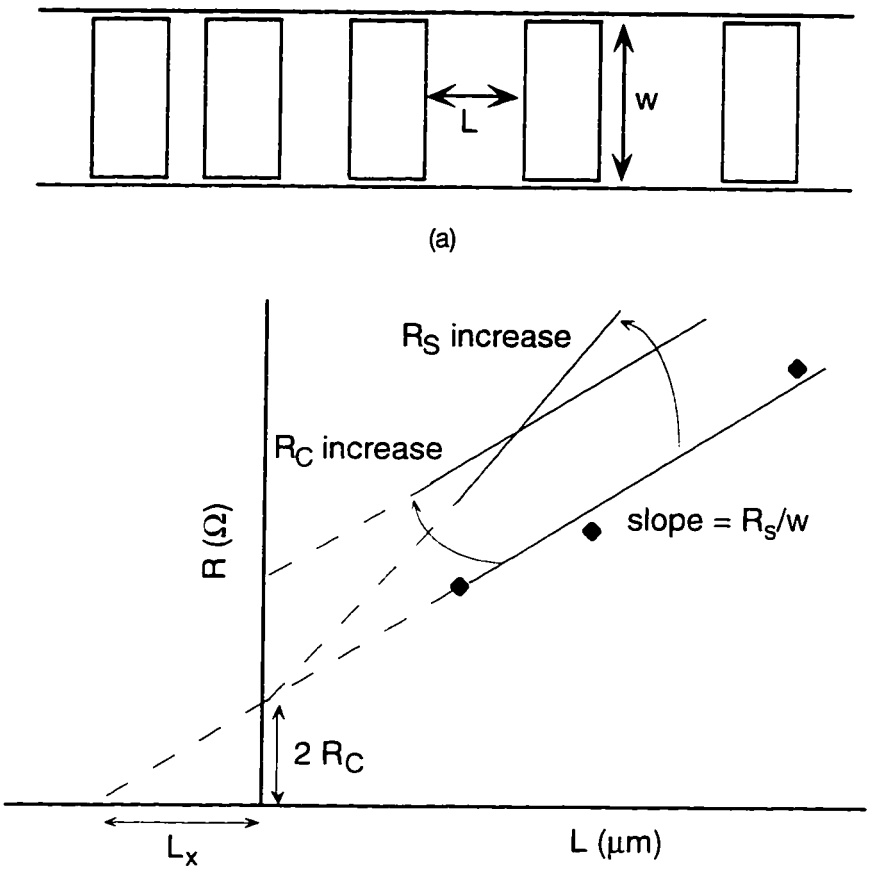

Figure 1.2. (a) Pattern used for contact and sheet resistance measurements. (b) The fitted line graphs from which the R_C and R_S can be extracted.

Figure 1.2 (b) also shows graphically that an increased slope in the fitted line will point out to an effective increase in the sheet resistance of the channel, and a parallel upward shift will be interpreted as an increase in the ohmic contact resistance.

1.2. A Two-Layer TLM Method

We now present a method that we have developed for analyzing a contact resistance scheme, where current conduction takes place in two layers under the contact as shown in Figure 1.3 (a). This contact scheme is encountered, for example, when a highly doped low bandgap material is regrown on a conductive channel or an ohmic contact region of higher doping is achieved on the original

conductive channel either by metalization and alloying or dopant implantation and activation. The contact resistance R_C of the semi-infinite resistor network is, by definition, the input resistance of the 2-port between the nodes 1 and 0. We note that the two-ports defined by the nodes 1, 2, 0, and the nodes 1', 2', 0 are identical. Representing the networks in terms of their impedance parameters, we can write

$$[\,Z\,] = [\,Z'\,]. \tag{1.11}$$

The impedance parameters relate the currents flowing into the network to the voltages at the terminals and are given by

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = [Z] \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \text{ where } [Z] = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}. \tag{1.12}$$

Figure 1.3 (b) depicts the circuit diagram of the network with the semi-infinite ladder replaced by its equivalent two-port representation. We note that the resistors R_{S1}, R_{S2}, and r_c are in cascade connection with the original network, which naturally leads to representation in *ABCD* parameters. With the current and voltage directions as shown in Figure 1.3 (b), the *ABCD* parameters of a two-port network are defined as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}, \tag{1.13}$$

and they are related to the *Z* parameters through [4]

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \dfrac{z_{11}}{z_{21}} & \dfrac{z_{11}\,z_{22} - z_{12}\,z_{21}}{z_{21}} \\ \dfrac{1}{z_{21}} & \dfrac{z_{22}}{z_{21}} \end{bmatrix}. \tag{1.14}$$

The ABCD matrices for a series and a parallel resistor R are easily computed to be $\begin{bmatrix} 1 & R \\ 0 & 1 \end{bmatrix}$ and $\begin{bmatrix} 1 & 0 \\ \dfrac{1}{R} & 1 \end{bmatrix}$ respectively. The *ABCD* parameters of the final network before the parallel r_{ci} connection is thus given by the matrix product

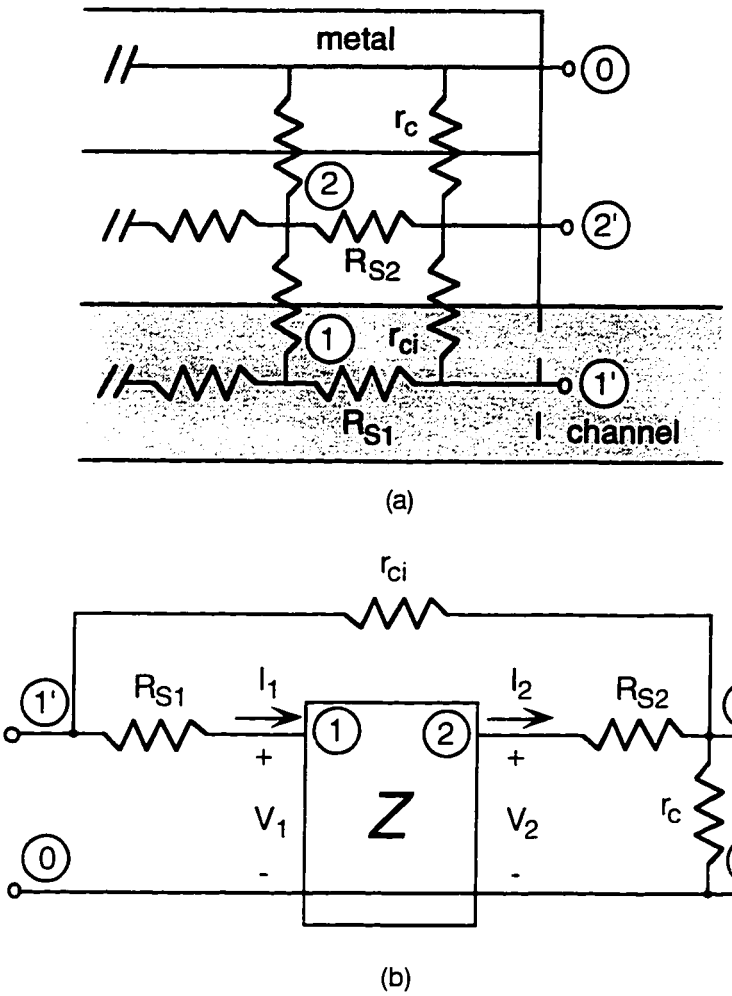

Figure 1.3. (a) A 2-port resistor network model for analyzing a two-layer conduction scheme under the ohmic contact. (b) Equivalent circuit diagram for the resistor network.

$$\begin{bmatrix} A^* & B^* \\ C^* & D^* \end{bmatrix} = \begin{bmatrix} 1 & R_{S1} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} 1 & R_{S2} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{r_c} & 1 \end{bmatrix}. \tag{1.15}$$

The easiest way to connect the resistor r_{ci} in parallel is by utilizing Y parameter representation, which relates the currents at the network terminals to the voltages. Thus, we first convert the $A^*B^*C^*D^*$ matrix to its equivalent Y parameter representation, [Y^*] [4], and then compute the Y parameters of the final two port as

$$[Y'] = [Y^*] + \frac{1}{r_{ci}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}, \tag{1.16}$$

where the second term is the Y parameter matrix for the resistor, r_{ci}. We end the matrix manipulation by converting the matrix Y' to Z', its equivalent Z parameter representation. The equality (1.11) represents four coupled nonlinear equations in eight variables. Given any four variables, the remaining four unknowns can be solved numerically. For example, if R_{S1}, R_{S2}, r_c, and R_C (= z_{11}) are given, we can solve for r_{ci}, z_{12}, z_{21}, and z_{22}. Clearly, the resistances have to be entered into the equations for a small incremental length, dx. Thus, instead of the symbolic representation in Figure 1.3 (b), the resistances are entered as

$$r_{ci} \leftarrow \frac{r_{ci}}{dx\, w},\ r_c \leftarrow \frac{r_c}{dx\, w},\ R_{S2} \leftarrow R_{S2}\frac{dx}{w}, \text{ and } R_{S1} \leftarrow R_{S1}\frac{dx}{w}. \tag{1.17}$$

1.3. Physics of Ohmic Contacts

A metal-semiconductor contact is considered ohmic if it can support the required current across the interface without appreciable voltage drop [5]. In compound semiconductors, the metal-semiconductor Schottky barrier height is typically determined by Fermi-level pinning as shown in Figure 1.4.

The electron transport across the metal-semiconductor interface occurs in two main regimes: thermionic and field emission [6, 7]. The particular regime of

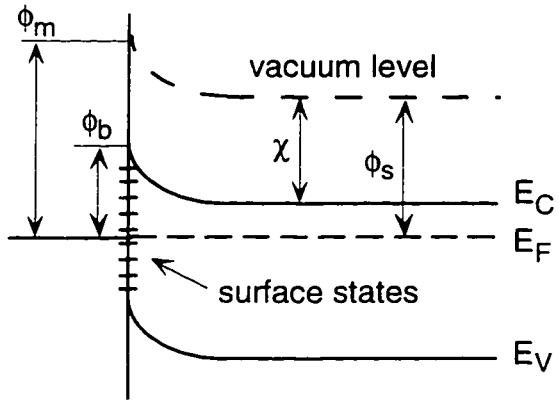

Figure 1.4. Schematic band diagram of a metal-semiconductor junction. ϕ_m and ϕ_s are the metal and the semiconductor workfunctions, χ is the electron affinity of the semiconductor, and ϕ_b is the Schottky barrier height.

operation depends on the relative magnitudes of the thermal energy of the electrons, kT, where k is Boltzman's constant and T is the temperature, and a characteristic tunneling energy E_{00} defined by

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{m^* \varepsilon}}, \tag{1.18}$$

where q is the electronic charge, $\hbar$ is Planck's constant divided by 2π, N_D is the concentration of donors, m^* is the effective mass of the tunneling electrons, and ε is the dielectric constant of the semiconductor. The electrons can traverse the potential barrier if they have sufficiently high thermal energy or they can tunnel through it if it is sufficiently thin. In an intermediate case, the electrons have enough thermal energy to reach the thinner part of the barrier, and then tunnel there. It is the tunneling action that enables ohmic contacts from metal-semiconductor junctions. Qualitatively, the three regimes are described as follows:

$$\begin{aligned}
&\frac{kT}{E_{00}} >> 1 && \text{thermionic emission} \\
&\frac{kT}{E_{00}} \approx 1 && \text{thermionic-field emission} \\
&\frac{kT}{E_{00}} << 1 && \text{field emission (tunneling)}
\end{aligned} \tag{1.19}$$

The specific contact resistivity associated with a junction is given by

$$r_c = \frac{1}{\left.\frac{\partial J}{\partial V}\right|_{V \to 0}}. \tag{1.20}$$

Applying (1.20) to the equations of current for electron transport across the metal-semiconductor interface, we obtain the following set of functional dependencies for the specific contact resistance [7]:

$$r_c \propto \begin{cases} \exp\left[\dfrac{\phi_b}{\sqrt{N_D}}\right] & \text{FE} \\ \exp\left[\dfrac{\phi_b}{\sqrt{N_D}\coth\left(\dfrac{E_{00}}{kT}\right)}\right] & \text{TFE.} \\ \exp\left[\dfrac{\phi_b}{kT}\right] & \text{TE} \end{cases} \tag{1.21}$$

The dependence of r_c on N_D is graphically summarized in Figure 1.5 [7].

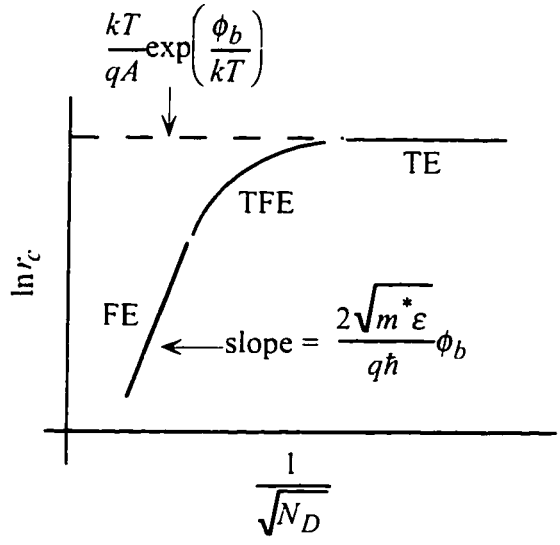

Figure 1.5. Theoretical dependence of the specific contact resistance on the doping concentration.

1.4. Implementation of Regrown Contacts: Regrowth of GaInAs on InP

As an alternative to standard ohmic contacts achieved by deposition of metal on the semiconductor and subsequent alloying, non-alloyed contacts to highly doped regrown regions have been reported in the literature [8-10]. Non-alloyed ohmic contacts offer various advantages over alloyed contacts [11]. It is also possible to fabricate the source, drain and gate regions all with the same level of metalization since the alloying step is eliminated. This ease in the process

should improve reliability, uniformity and yield in device processing, which are parameters of great importance in, for example, the case of integrated circuits.

To demonstrate the feasibility of regrown contacts and establish the process basis, we characterize the regrowth of n^+-GaInAs on InP channel devices. We fabricate TLM patterns with both top and side regrowth as shown schematically in Figure 1.6. The basic structure consists of an Fe doped InP buffer grown on a semi-insulating InP substrate, which is followed by a 0.5 μm thick channel of Si doped InP ($n = 2.4 \cdot 10^{17}$ cm^{-3}). The structure in Figure 1.6 (a) is achieved as follows: $Ga_{0.47}In_{0.53}As$ doped with Si ($n = 1.24 \cdot 10^{18}$ cm^{-3}) is regrown on the original sample after the sample has been exposed to air, photoresist spinning and removal steps to simulate actual device processing conditions. Both the growth and the regrowth are done by MOCVD [12]. The sample is then patterned with a TLM mask by photolithography and metal liftoff. Standard AuGe/Ni/Au metalization scheme is used. The contact pads of the TLM patterns are 100 μm in length and 200 μm in width, and have spacings that vary from 3 μm to 30 μm. Finally, using the contact metal as the mask, the unmasked regrown areas are partially etched by reactive ion etching ($CH_4/H_2/Ar$ gases with flows of 4/20/10 sccm, at a pressure of 75-125 mTorr, and a self dc bias of -500 V). Etching is completed by a 3:1:50 H_3PO_4:H_2O_2:H_2O solution, which etches away the regrown GaInAs and stops at the InP channel.

To get the structure in Figure 1.6 (b), first the TLM mask is used to pattern a 2000 Å thick SiO_2, deposited by plasma enhanced chemical vapor deposition (PECVD). The InP channel is subsequently etched by RIE all the way to the buffer with conditions similar to above. The etching is completed by a wet etching step in a 3:1 HCl:H_2O solution. Highly doped $Ga_{0.47}In_{0.53}As$ is then selectively regrown in these regions in the MOCVD reactor. Afterwards, metal contacts are deposited on the regrown regions through the realignment of

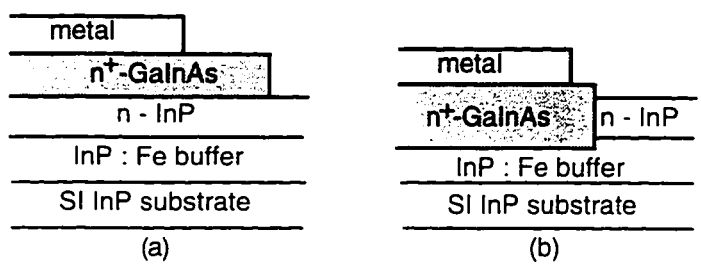

Figure 1.6. (a) Schematic representation of (a) the top regrowth and (b) the side regrowth.

the TLM mask, photolithography, and subsequent metal liftoff. In both structures (a) and (b), adjacent TLM bars are isolated from one another by mesa etching.

In both cases, prior to regrowth, the wafer is treated with buffered HF to remove any nascent surface oxide. Also to test whether residual carbon compounds at the surface may have any effect on the electrical characteristics of the regrowth interface, some of the samples are placed in a UV ozone photoreactor to reduce the amount of residual carbon that might be present at the surface [13]. Along with some samples kept as non-annealed control samples, the process is completed by annealing the contacts using a strip annealer at 350°C, 400°C, and 450°C.

1.4.1. Measurements of Contact Resistance

Once the structures have been fabricated, the room temperature contact resistances are measured by using a four probe measurement technique, in which the current is passed through two of the probes, and the potential difference is measured across the other two. This way, the effect of uncertainties in the definition of probe resistances is eliminated. For each data point, at least three different TLM patterns are measured and the average value is recorded. Figure 1.7 shows the variation of these contact resistances with respect to annealing temperature as measured at 300 K. The optimum annealing temperature for these structures appears to be around 400°C.

One of the main contributions to the contact resistance is from the regrown GaInAs to n-InP interface. To understand the effect of this interface better, we measure the contact resistances of annealed metal contacts on the regrown areas at low temperatures. Figure 1.8 shows the variations in these contact resistances with respect to the measurement temperature. Because of limited instrumental capabilities of the low temperature measurement system, these resistances were measured with two probes. The error bars on the graphs thus represent the uncertainties in defining the probe resistance. We see a temperature dependence in the contact resistance particularly in the top regrowth case.

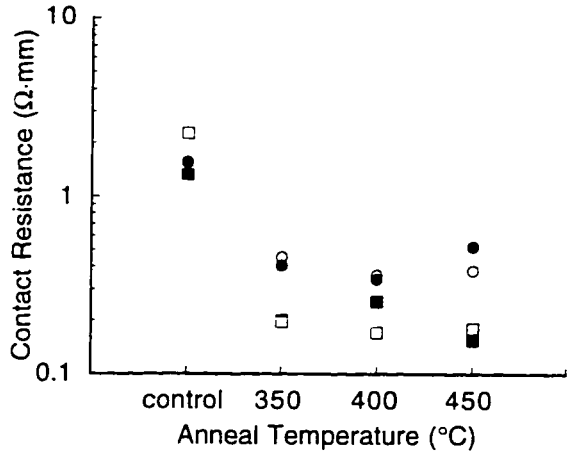

Figure 1.7. Variation of the contact resistance with respect to annealing temperature for samples with top (circles) and side (squares) regrowth. UV ozone treatment of the samples before regrowth does not seem to have an appreciable effect on the resistance (solid markers show samples without any ozone treatment, unfilled markers show those with ozone treatment prior to regrowth).

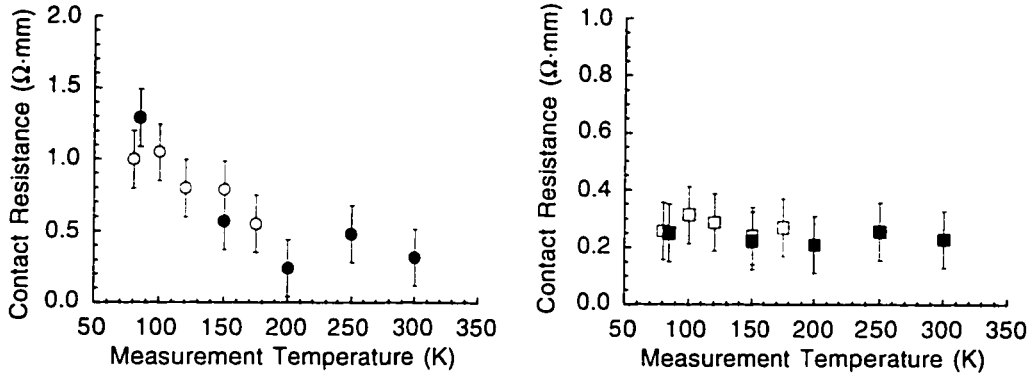

Figure 1.8. The variation of the contact resistance for (a) the top regrowth, and (b) the side regrowth with respect to the measurement temperature (solid markers show samples without any ozone treatment, unfilled markers show those with ozone treatment prior to regrowth).

1.4.2. Experimental and Theoretical Calculation of the Interface Resistance

We notice that the case of top regrowth presents a two-layer conduction problem underneath the ohmic contact and can thus solve for the specific contact resistance associated with the GaInAs/InP interface, r_{ci}, by using the method

outlined in Section 1.2. In this case, the known variables are the metal to regrowth specific contact resistivity, r_c, the sheet resistance of the regrown GaInAs, R_{S2}, the sheet resistance of the InP channel, R_{S1}, and the measured contact resistance of the whole structure, R_C. The unknown variable is the specific contact resistivity of the regrowth to channel interface, r_{c1}. We determine the first three parameters from separate TLM measurements made on n^+-GaInAs and n-InP on semi-insulating InP substrates, where the growth and doping conditions of these layers are the same as those used for the actual experiments. For our structures these values are: $r_c = 1.07 \cdot 10^{-7}$ $\Omega \cdot cm^2$, $R_{S1} = 220$ Ω/sq and $R_{S2} = 21$ Ω/sq. From the four coupled nonlinear equations that we arrive as a result of the matrix manipulations, we calculate the numerical solutions using Mathematica [14]. We will refer to these solutions as "experimental values" henceforth.

We also approach the problem theoretically by assuming an abrupt heterojunction interface between the regrown GaInAs and the n-InP channel by using the concepts outlined in Section 1.3, and model the measured resistivity by the effect of the conduction band barrier at this interface[2]. As we apply thermionic emission and thermionic field emission theories to electron transport across the GaInAs/InP barrier, we also check for the variation of the barrier height with respect to temperature by solving Poisson's equation at various temperatures [15][3]. Figure 1.9 shows a sampling of these calculations. We note that the barrier height decreases by about 15 meV as the temperature moves down to 100K from 300K. Finally, we compare the r_{c1} values extracted from the experiments and those calculated by the theory in Figure 1.10. We note that the thermionic emission theory grossly overestimates the resistance below 200K. *In this region, the resistance is well approximated by the thermionic field emission theory.*

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[2] Although the methodology outlined in Section 3 is for a metal to semiconductor Schottky barrier interface, it should remain applicable to our case as well since the regrown GaInAs is doped highly degenerately.

[3] In [15], the Fermi-Dirac integrals for the distribution of the electrons are approximated accurately by short series as outlined in [16, 17]. We have also solved the Poisson equation for this system using Joyce-Dixon approximation [18, 19], but found that the ratio of the electron concentration in the notch to the effective density of states (n/N_C) goes above 10 around $T = 250$ K, thereby limiting the range of applicability of this approximation to temperatures above this value.

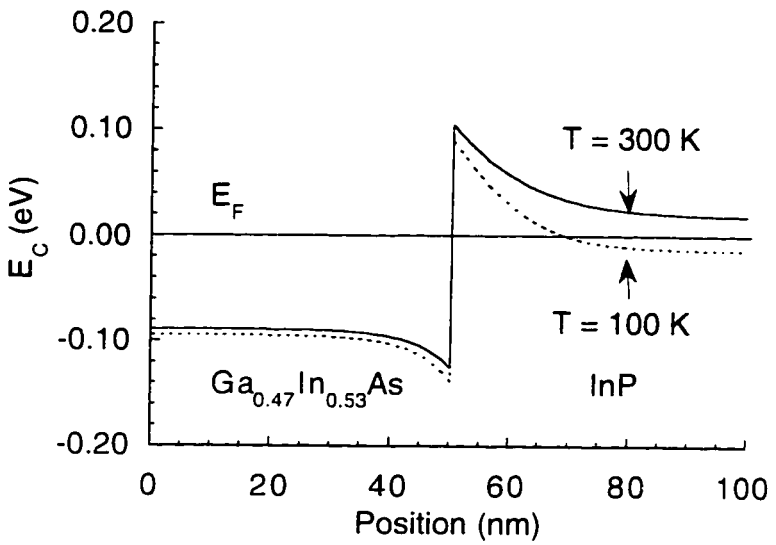

Figure 1.9. Calculated conduction band edge for an abrupt GaInAs/InP heterointerface at T = 100 K and 300 K.

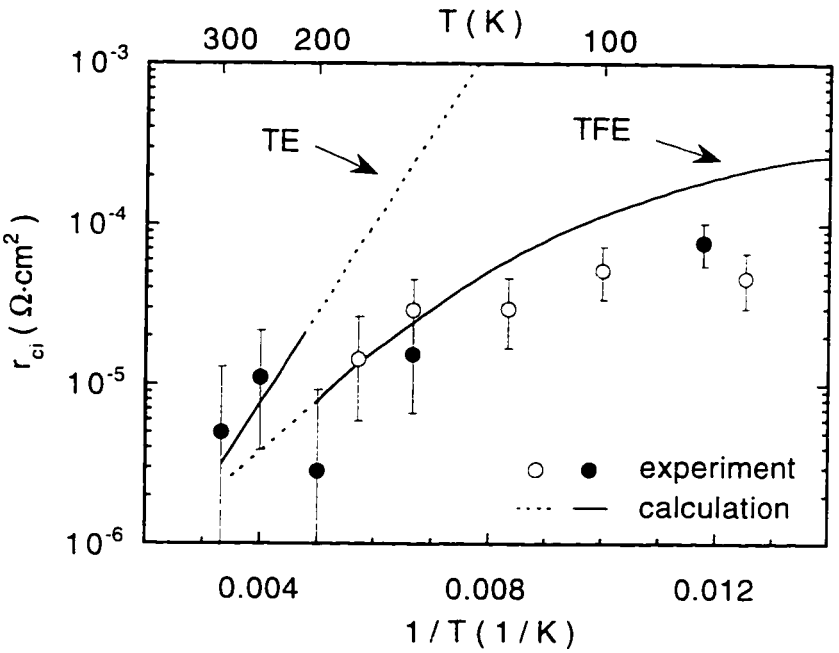

Figure 1.10. A comparison between the theoretical and the experimental values (obtained by circuit analysis) for the specific contact resistivity, r_{ci}, for the top regrowth. The solid lines indicate the regions where the calculations are valid according to [6, 7] (solid markers show samples without any ozone treatment, unfilled markers show those with ozone treatment prior to regrowth).

1.5. Summary

We have reviewed the existing methods that are used to characterize ohmic contacts and introduced a new one to analyze contacts into which the current conduction takes place in two layers. We have also established a regrowth process in which n^+-GaInAs was grown on n-InP channel devices. By measuring the contact resistance at various temperatures on annealed samples, we modeled the variation of the interfacial specific contact resistivity by thermionic field emission and thermionic emission theories as applied to the electron transport across the heterojunction barrier. Using the 2-layer TLM method, we also solved for the contact resistivity based on experimental measurements and showed good agreement between theoretical predictions and the experimental data.

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Chapter 2

Effects of Rapid Thermal Annealing on Bulk AlInAs/InP and AlInAs/GaInAs/InP HEMT Structures with Planar Si Doping

AlInAs/GaInAs/InP high electron mobility transistors (HEMT) have proven to be one of the best candidates for low-noise microwave and millimeter wave applications [1]. Two of the main factors influencing the performance of these devices are the total two-dimensional electron gas concentration (2DEG) and the corresponding mobility. Improvements in the high-frequency performance of these devices can be achieved by the reduction of external parasitics through self-aligned gate technology in which the source and drain ohmic regions are fabricated by ion implantation. The HEMT structure then has to be annealed to activate the implanted ions. The key concerns are what happens to the device structure and its electrical properties during the high temperature anneals, and particularly how the sheet carrier concentration and the mobility are affected.

Previous studies have investigated layer interdiffusion characteristics of AlGaAs/GaAs quantum well heterostructures [2], and GaInAs/AlInAs quantum wells [3] under annealing with SiO_2 capping. The effects of rapid thermal annealing on the integrity of GaInAs/AlInAs interfaces [4], pseudomorphic AlGaAs/InGaAs/GaAs HEMTs [5], selectively doped GaAs/*n*-AlGaAs heterostructures [6], and modulation-doped AlGaAs/GaAs heterostructures [7] have also been studied.

In this chapter, we investigate the effects of high temperature rapid thermal annealing(RTA) processes on carrier concentration and mobility of bulk AlInAs and lattice-matched AlInAs/GaInAs/InP HEMT structures with planar Si doping. We observe both deterioration in the mobility of the HEMT samples and loss of charge with annealing. We show that the influencing factors for these observations are the surface and the heterointerface. We note particularly that the bulk AlInAs stays stable even at high annealing temperatures such as 900°C.

2.1. Experiments

The cross sections of the planar doped AlInAs and the AlInAs/GaInAs/InP HEMT structures are shown in Figure 2.1. The planar-doped AlInAs structure simulates the donor region of the HEMT and is employed to

investigate the effects of RTA processes on the bulk AlInAs region only, separate from the effects on the AlInAs/GaInAs heterointerface. These structures were grown by MBE, lattice-matched to semi-insulating InP substrate. The room temperature net carrier concentration (n_s) and mobility (μ) of the bulk AlInAs were $5.4 \cdot 10^{12}$ cm^{-2} and 840 $cm^2/V \cdot sec$ respectively. The HEMT structure had a net carrier concentration and mobility of $3.1 \cdot 10^{12}$ cm^{-2} and 8500 $cm^2/V \cdot sec$ at 300K and $3.0 \cdot 10^{12}$ cm^{-2} and 26,500 $cm^2/V \cdot sec$ at 15K respectively. The HEMT samples were rapid thermal annealed for 5 s at 700°C, 800°C, and 900°C in a forming gas ambient (10% H_2, 90% N_2) in an AG Associates Heatpulse 410 rapid thermal annealer. The choices for the capping material to prevent As desorption were Si_3N_4 (n = 2.05 : 1000 Å), SiO_2 (n = 1.47 : 1000 Å) and GaAs pieces in close proximity. The Si_3N_4 and the SiO_2 caps were deposited by a plasma enhanced chemical vapor deposition (PECVD) system; the thicknesses and the refractive indices of the films were measured by an ellipsometer. The indices obtained show that the composition of the dielectric films are very close to being stoichiometric. The temperature dependence of the mobility and the sheet carrier concentration of the samples were measured by a Van der Pauw technique.

2.2. Results and Discussions

Figure 2.2 depicts a schematic diagram of possible effects of high temperature anneals on the device structure, such as diffusion of the donor Si atoms and the intermixing of the AlInAs/GaInAs heterointerface, and their resulting influence on the electrical properties of the structure, such as μ and n_s.

GaInAs	Contact $n = 5 \times 10^{18}$ cm^{-3}	70 Å
AlInAs	Schottky	200 Å
AlInAs	Donor $n = 1 \times 10^{19}$ cm^{-3}	33 Å
AlInAs	Spacer	15 Å
GaInAs	Channel	400 Å
AlInAs / GaInAs	4-Period Superlattice	400 Å
AlInAs	Buffer	2500 Å
InP	Semi Insulating Substrate	

(a)

GaInAs	Cap	15 Å
AlInAs		1000 Å
	δ - doping	
AlInAs		4000 Å
InP	Semi Insulating Substrate	

(b)

Figure 2.1. (a) AlInAs/GaInAs/InP HEMT and (b) δ-doped bulk AlInAs structures used in this study.

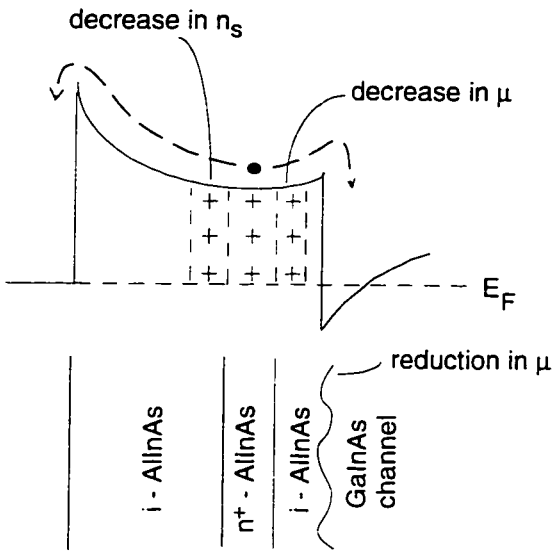

Figure 2.2. Possible effects of high temperature anneals on the device structure and its electrical properties.

We now discuss these effects starting with the mobility and the carrier concentration characteristics after the 700°C and 800°C anneals. We continue with the 900°C anneals in a separate section as these characteristics differ significantly from the previous ones.

2.2.1. 700°C and 800°C Anneals

2.2.1.1. Discussions on the Mobility

Anneals carried out on samples with Si_3N_4 capping or GaAs pieces in close proximity result in similar mobility versus temperature characteristics. In both of these methods, a slight reduction in mobility is observed as the annealing temperature increases. Figure 2.3 shows the mobility versus temperature measurements for the samples annealed with GaAs in proximity and SiO_2 capping. *We suggest that the reduction in the mobilities is due to the enhanced diffusion of the Si donor atoms towards the 2 DEG channel, which increases the coulombic scattering between the carriers and the ionized donors.*

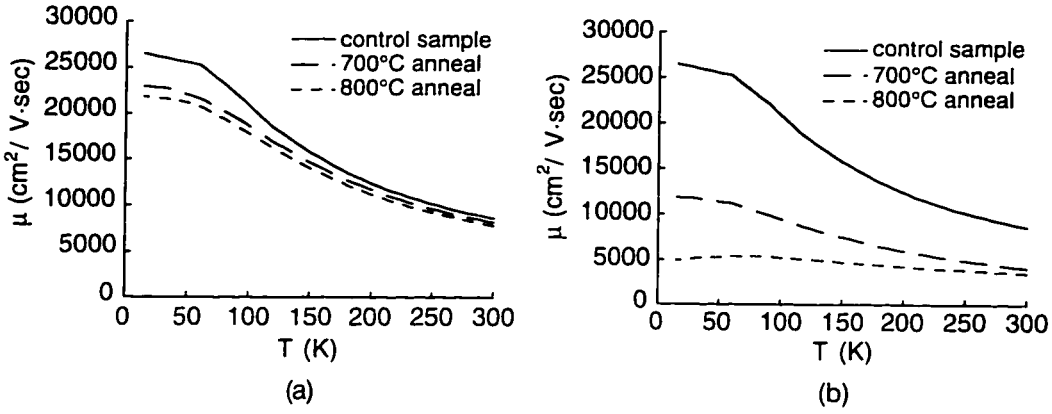

Figure 2.3. Comparison of mobility vs. temperature between (a) proximity and (b) SiO_2 capped anneals.

We also observe in Figure 2.3 that the reduction in mobilities of the samples annealed with SiO_2 capping is more pronounced than that of the samples annealed with proximity GaAs. We note that the reduction in the low temperature mobilities is as high as 80% as compared to their original value. This further reduction in mobility in the SiO_2 capped samples may be attributed to the diffusion of Ga and In atoms into the oxide, which results in vacancies and the intermixing of the AlInAs/GaInAs interface. To check this phenomenon, secondary ion mass spectroscopy (SIMS) profiling was carried out on samples that had been annealed using Si_3N_4 and SiO_2 caps. Since the mobility versus temperature behavior is very similar for the anneals done with proximity GaAs and Si_3N_4 capping, we only compare the SIMS data between samples annealed using SiO_2 and Si_3N_4.

Prior to profiling, the Si_3N_4 and SiO_2 caps were removed in solutions of concentrated HF and buffered oxide etch respectively. The outdiffusion of Ga and In atoms for the SiO_2 capped anneals is apparent from Figure 2.4, which shows the SIMS profiles for Ga and In atoms for the samples annealed at 800°C with Si_3N_4 and SiO_2 capping. The layer interdiffusion phenomenon has previously been used for wavelength modification of quantum wells [2, 3]. The outdiffusion of Ga atoms in rapid thermal annealing processes with SiO_2 encapsulation has been also previously shown to occur in bulk GaAs [8].

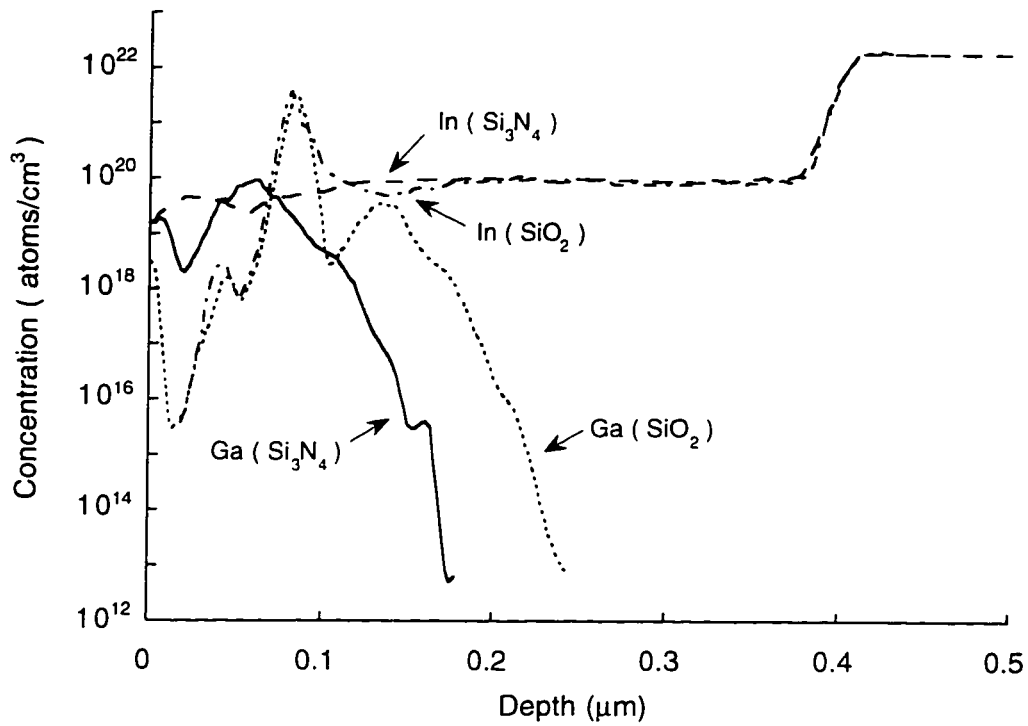

Figure 2.4. Normalized SIMS profiles showing a comparison of Ga and In concentrations in HEMT samples with SiO_2 and Si_3N_4 capped anneals at 800°C.

2.2.1.2. Discussions on the Carrier Concentration

Figure 2.5 shows the carrier concentration (n_s) versus temperature for 700°C and 800°C anneals done with Si_3N_4 and SiO_2 cappings, and GaAs in close proximity. A decrease in n_s with increasing annealing temperatures is observed. There may be a few possible reasons for this reduction in the charge concentration:

(i) Electron capture by defects that could possibly be generated during the high temperature anneals.

(ii) Possible amphoteric behavior of Si in AlInAs similar to as observed before in AlGaAs [7].

(iii)Preferential vacancy enhanced diffusion of the Si donor atoms towards the surface, which would both reduce the efficiency of electron transfer to the channel and also could form electrically inactive Si complexes.

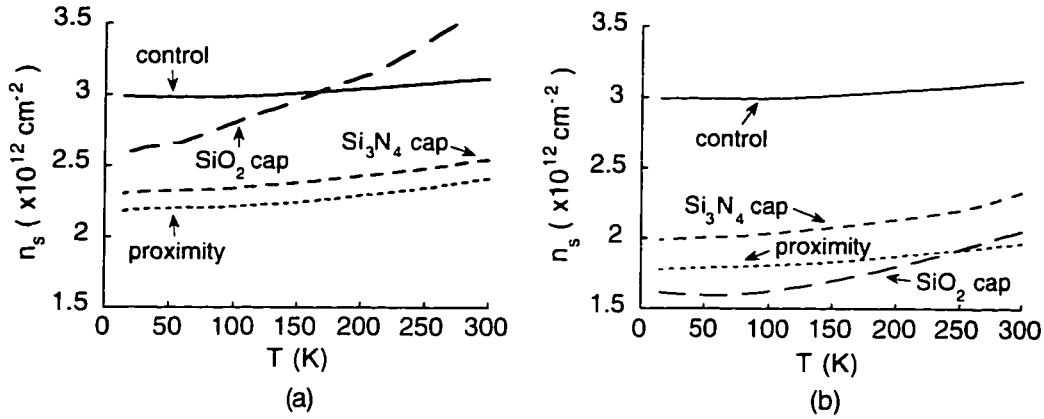

Figure 2.5. Carrier concentrations vs. temperature for samples annealed with SiO_2 and Si_3N_4 caps, and proximity GaAs, at annealing temperatures of (a) 700°C and (b) 800°C.

To determine the dominant cause of the reduction of sheet carrier concentration, the δ-doped bulk AlInAs samples shown in Figure 2.1 (b) were subjected to the same annealing temperatures and conditions as the HEMT samples. Figure 2.6 shows the measurement results for anneals done with Si_3N_4 encapsulation. We note that the electron concentrations are maintained to within experimental errors, and the mobility actually increases with the annealing temperature. Cathodoluminescence (CL) studies of bulk AlInAs samples also show a much higher intensity for AlInAs at 900°C than at 700°C indicating an improvement in the bulk AlInAs quality. The CL spectra are shown in Figure 2.7. These findings suggest that electron capture by defects is not the reason for the loss of carriers with annealing since the bulk AlInAs stays stable during annealing. Amphoteric behavior of Si in AlInAs is also ruled out since, to within experimental errors, the 2 DEG carrier concentration does not vary with respect to annealing. Previous work has shown that the AlInAs/GaInAs interface preserves its quality during anneals of up to 800°C [4]. *We therefore believe that surface enhanced diffusion of the Si donor atoms is the dominant mechanism for the loss of charge in the HEMT structures.* As depicted in Figure 2.2, and evidenced by the reduction in mobility as discussed in Section 2.2.1.1, there appears to be a diffusion of the donor atoms towards the channel as well. However, the surface enhanced diffusion seems to dominate, resulting in an overall decrease in the measured sheet carrier concentration.

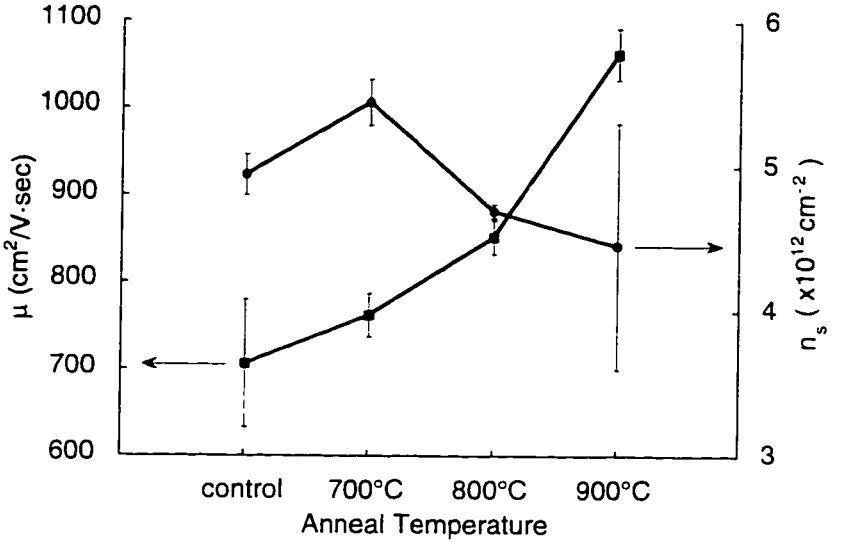

Figure 2.6. Room temperature mobility and carrier concentration values for the δ-doped bulk AlInAs sample for different annealing temperatures. Si_3N_4 capping was used during the annealing. Error bars show experimental variations in the measurements.

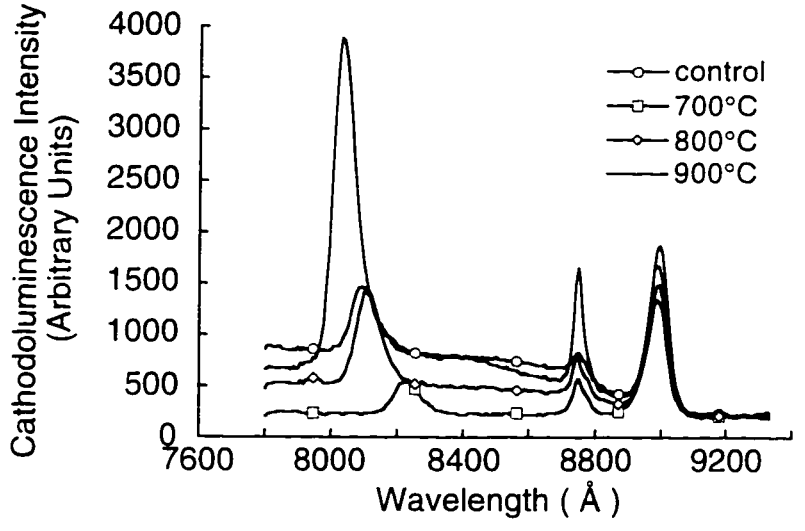

Figure 2.7. CL spectra of bulk AlInAs for samples after 700°C, 800°C, and 900°C anneals.

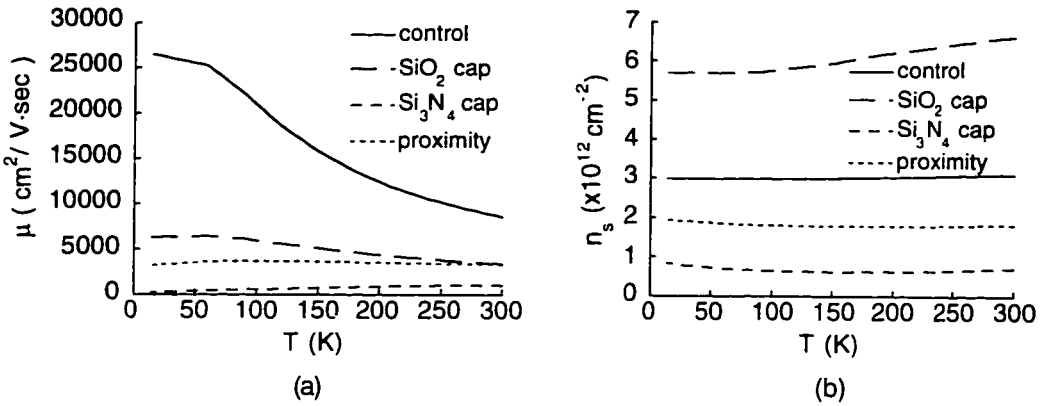

Figure 2.8. (a) Mobility and (b) sheet carrier concentration measurements vs. temperature for 900°C anneals.

2.2.2. 900°C Anneals

Figure 2.8 shows mobility and sheet carrier concentration data for samples annealed at 900°C using Si_3N_4 and SiO_2 caps, and GaAs in close proximity. We note that the mobility for the samples show a considerable reduction for all three methods of annealing. Another point of observation is that the mobility becomes virtually independent of the measurement temperature. The carrier concentration drops to about $1.7 \cdot 10^{12}$ and $6 \cdot 10^{11}$ cm^{-2} for the proximity and Si_3N_4 anneals, but actually increases to $6 \cdot 10^{12}$ cm^{-2} for the anneal with SiO_2 cap. *The dramatic reduction in the mobilities and its temperature independence is believed to be caused by severe layer mixing at the AlInAs/GaInAs interface, and a loss of the crystalline properties of the structure, which occurs only at or above 900°C.*

The increase in the sheet charge concentration for the SiO_2 anneal is due to the doping of the ternary materials by Si back-diffusing from the SiO_2 cap [3]. We observe this behavior also by the SIMS measurements as shown in Figure 2.9. Here, we see that there is a definite increase in the surface Si concentration in the sample annealed with a SiO_2 cap at 900°C compared to the sample annealed with a Si_3N_4 cap at 800°C. We should note that SIMS data of Si distribution for an anneal done with a Si_3N_4 cap at 700°C look similar to the 800°C anneal. We also expect the Si distribution in the samples annealed using Si_3N_4 caps to be qualitatively close to the non-annealed sample. In this regard, SIMS measurements done on similar heterostructures with bulk doping of AlInAs were reported to show no extensive movement of Si dopants under similar annealing conditions [9].

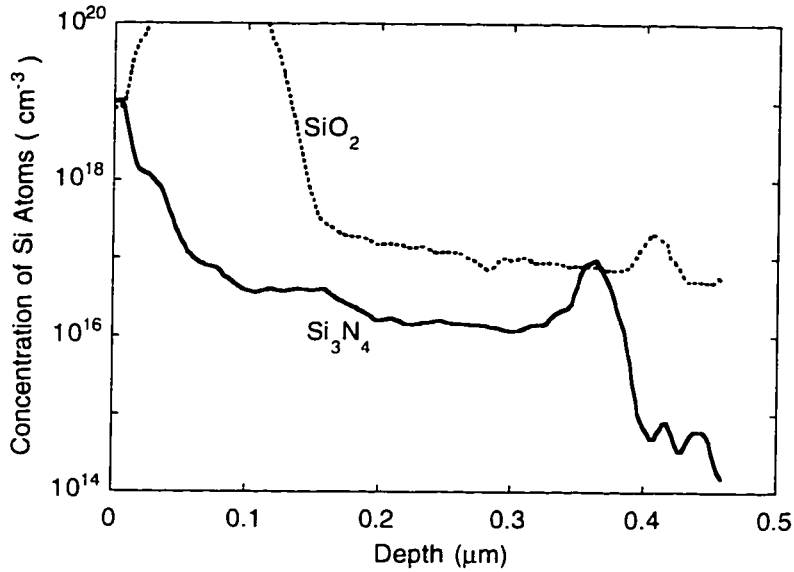

Figure 2.9. Normalized SIMS profiles for Si for anneals done with Si_3N_4 cap (at 800°C) and SiO_2 cap (at 900°C).

2.3. Summary

This study shows that the heterostructure integrity of the AlInAs/GaInAs interface is destroyed after a 900°C anneal even though the material quality of bulk AlInAs improves at this temperature. Also, a loss of carriers to surface states by vacancy enhanced diffusion in samples annealed at 700°C and 800°C are observed. The mobility in these samples also degrades with increasing annealing temperature due to diffusion of the donor Si atoms towards the 2 DEG channel. For the particular case of anneals with SiO_2 encapsulation, the reduction in mobility is more pronounced due to the outdiffusion of Ga and In atoms into the oxide thereby creating vacancies and resulting in interface intermixing.

The reduction in mobility and charge loss are more significant at low temperatures. We therefore conclude that ohmic contact formation by dopant implantation and activation is not a viable method particularly for applications which require stable device characteristics not only at room temperatures, but at cryogenic temperatures as well.

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Chapter 3

Regrowth of n^+ GaInAs on GaInAs Channel Devices

Obtaining reliable and low resistance ohmic contacts is one of the enabling factors in reducing device parasitics and achieving high frequency and low noise transistors. We previously stated that possible approaches that can be taken to realize low resistance contacts in high performance HEMTs are: (a) ion implantation, (b) capping with a highly doped low bandgap material, and (c) highly doped epitaxial regrowth of contacts. The ion implantation method requires a high temperature, post-implantation anneal to activate the implanted dopants. However, as has been observed in Chapter 2, this annealing step gives rise to problems of mechanical, electrical and metallurgical stability of the underlying structure [1] and therefore is not a very desirable technology for reliable contacts. The second method has been investigated by some researchers [2], but since it provides a tunneling contact, its applications are limited to materials with small bandgaps and high doping incorporability. Regrown ohmic contacts, however, have the potential to enable low resistance, non-alloyed, and reliable contacts to the channels of FETs for various material systems [3-5]. For power applications, JHEMT structures incorporating regrown source and drain contacts have been shown to have higher breakdown voltages compared to control devices fabricated with alloyed ohmic contacts [4]. In Chapter 1, we presented initial technological and theoretical work on the regrowth of GaInAs on InP channel devices. In this chapter, we advance the state-of-the-art by investigating highly doped regrown GaInAs ohmic contacts to various FET structures with GaInAs channels and report on a technology with which we have achieved temperature stable regrown contacts with contact resistances of 0.1 Ω·mm.

3.1. Fabrication of the TLM Patterns

To characterize the ohmic contact resistance of the regrown contacts, we use transmission line patterns as shown in Figure 1.2. The TLM pads have dimensions of 100 x 200 μm^2, and seven separations ranging from 3 to 30 μm. The process to fabricate the structures starts with PECVD SiO_2 deposition on the samples and photolithography to define the pads. We then etch the TLM patterns in the oxide by either a CF_4 plasma or an SF_6 / Ar RIE and do a short clean-up in a diluted buffered HF acid solution (BHF). We subsequently etch the desired amount of the semiconductor in a 3:1:50 solution of H_3PO_4:H_2O_2:H_2O. We then

dip the samples in BHF, and after rinsing with water, transfer them into the MOCVD reactor immediately for regrowth. The samples themselves are grown by MBE.

Before the regrowth starts, the samples are kept at 200°C for 5 minutes with H_2 flow, and then baked at 450°C under tertiary butylarsine (TBA) overpressure. Regrowth takes place at 620°C with TBA, trimethylgallium (TMG) and trimethylindium (TMIn) precursors. Disilane (Si_2H_6) is used for Si doping of the regrown GaInAs. The growth occurs selectively on the etched surfaces over the masked areas since the operating pressure is kept at 0.1 atm.

In the standard process, after the regrowth is done, we remove the SiO_2 mask by dipping the samples in BHF [1]. We then metalize the contacts by photolithography and liftoff (AuGe/Ni/Au is used), and complete the process by mesa etching of the TLM bars.

3.2. Initial Regrowth Studies on FET and HEMT Structures

To establish the regrowth technology, we carry out our first study of GaInAs homojunction regrowth on a simple doped channel structure that

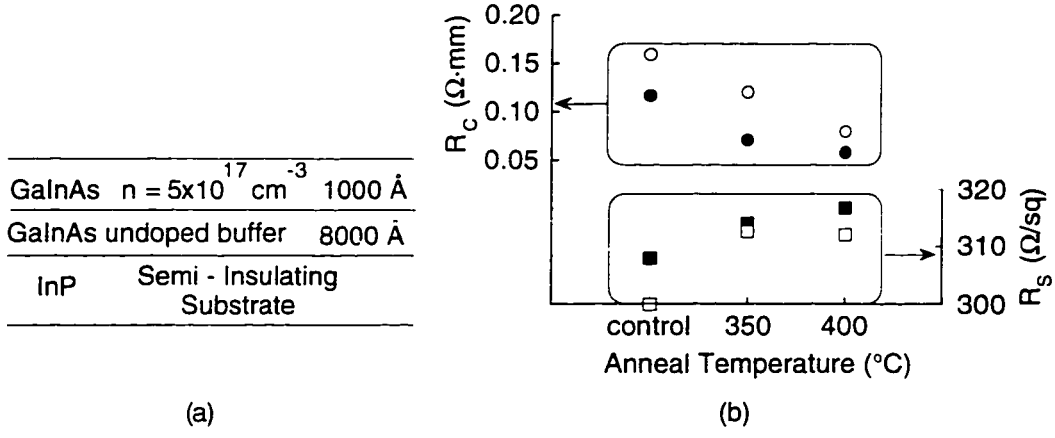


Figure 3.1. (a) The GaInAs doped-channel structure and (b) the contact (R_C) and sheet (R_S) resistances for regrown contacts on this structure vs. annealing temperature. Solid markers depict top regrowth, open markers depict side regrowth.

[1] A modified procedure to ensure stable contacts is discussed later in the chapter.

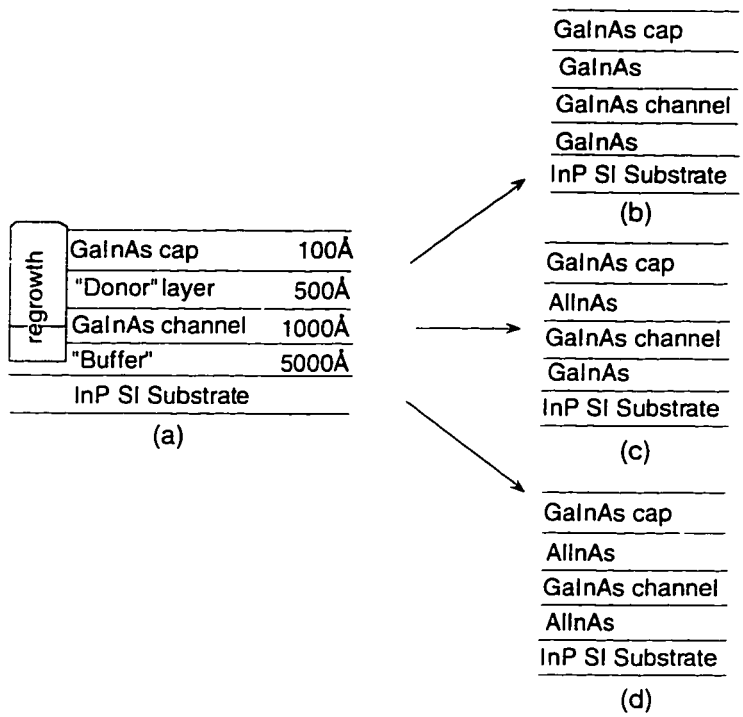


Figure 3.2. Layer schematics used to investigate the effects of implementing regrowth on AlInAs containing HEMT structures. The dashed line in the "regrowth" area show the possibilities of starting the regrowth either from the GaInAs channel, or from the AlInAs buffer. The figures represent the following:

(a) the structure on which regrowth is desired.
(b) the starting "all GaInAs" structure.
(c) top GaInAs layer is replaced by AlInAs.
(d) GaInAs buffer is replaced by AlInAs.

comprises of an 8000 Å thick $Ga_{0.47}In_{0.53}As$ buffer layer grown lattice matched on semi-insulating InP substrate, on top of which is a 1000 Å thick GaInAs "channel" region with $n = 5 \cdot 10^{17}$ cm^{-3} doping. We examine both top and side regrown contacts on this device structure similar to what is done in Chapter 1. Figure 3.1 shows the contact (R_C) and sheet resistances (R_S) of these regrown contacts with respect to the annealing temperature. The annealing is carried out on a strip annealer under forming gas atmosphere. We observe low resistance regrown ohmic contacts from this "homojunction" regrowth. Our goal is to implement this regrowth technology in high-performance HEMTs. Thus, we next carry out a set of experiments that guides us in that direction. Figure 3.2 shows the evolution of the structures that we use to do the transition from the structure of Figure 3.1 to a

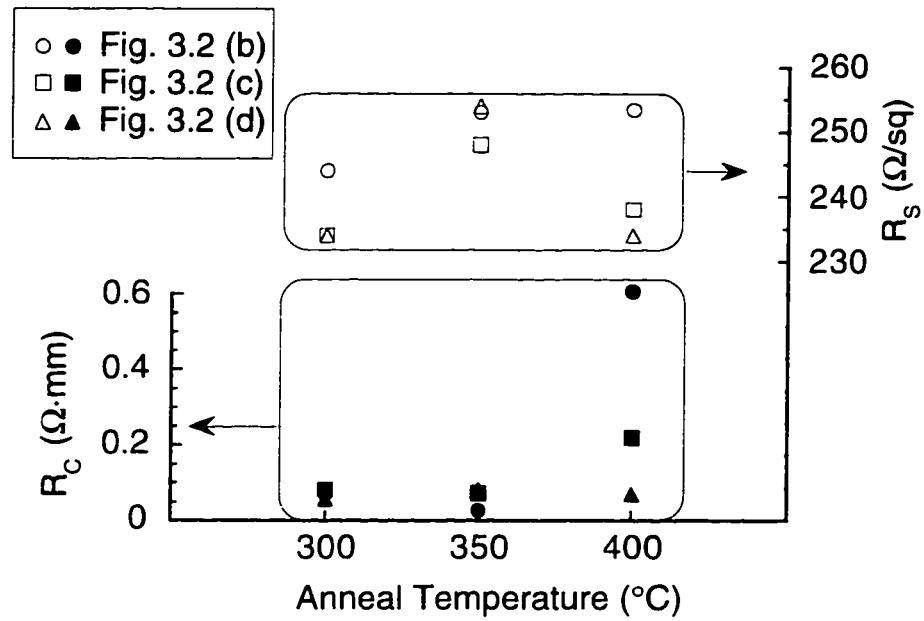


Figure 3.3. Contact and sheet resistances for the structures shown in Figure 3.2. Open markers depict the R_S, solid markers depict the R_C values. Low resistance regrowth is achieved on all structures.

standard HEMT structure. Notice that going from (b) to (d), we incorporate an AlInAs layer at each step, eventually arriving at (d) that mimics a HEMT structure. Because the process is an ex-situ etch and regrowth process, the reason for this experiment is to find out whether the incorporation of Al containing layers in the underlying structure for regrowth presents problems for the regrowth itself. Clearly, when we etch into the sample as shown in Figure 3.2 (a), we expose the AlInAs donor layer on the side. This might result in the creation of interface traps and charge depletion from the channel thereby yielding a high contact resistance. If the etch is done into the buffer, then the regrowth has to be initiated on an exposed and oxidized AlInAs surface. Note that in all of these structures, the GaInAs channel is doped to $n = 5 \cdot 10^{17}$ cm^{-3}. Figure 3.3 shows the extracted contact and sheet resistances from TLM measurements for the n^+ GaInAs regrowths done on these structures. *For all cases, we achieve low contact resistances, and the samples are thermally stable up to annealing temperatures of 400°C.*

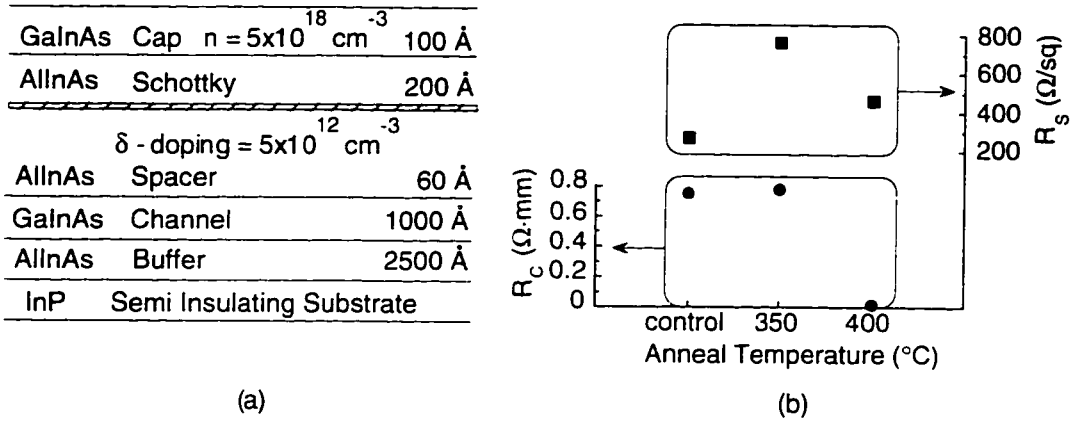


Figure 3.4. (a) The HEMT structure used and (b) the effects of annealing on the TLM resistances for regrown contacts on it. Note the jump in the R_S when sample is annealed.

Having established the basis of the process, we experiment with regrowth on an actual HEMT sample with a δ-doping ($n_s = 5 \cdot 10^{12}$ cm^{-2}) in the AlInAs carrier supply layer. Similar to the previous structures, we keep the channel thickness at 1000 Å. Figure 3.4 shows the effects of annealing on these contacts. We note a significant increase in the extracted sheet resistance when the structure is annealed. This result is somewhat surprising because in all previous regrowths on structures mimicking HEMTs, the contacts have shown thermal stability. The current structure, however, has two differences from the previous ones: (i) the GaInAs channel is undoped, and (ii) the AlInAs layer has Si doping in it. To address the question of whether lack of doping in the GaInAs channel is detrimental to low resistance contact regrowth, we design two doped-channel HEMT structures. Figure 3.5 shows the effect of annealing on the TLM resistances for regrown contacts on these structures. Note that we try both δ-doping and uniform doping in the GaInAs channel, and design the doping concentrations in the channel and the AlInAs donor layers such that approximately two thirds of the charge comes from the AlInAs layer. *Observing the fact that the extracted sheet resistances for all three structures again increase substantially with annealing, we can conclude that doping in the GaInAs channel itself is not a determining factor for the temperature instability of these contacts.* In a separate experiment, we also look at the uniformly doped sample more closely, and heat it up with 50°C increments starting from 150°C. The deterioration in the TLM resistances actually seem to be starting around 250°C.

GaInAs	Cap $n = 5x10^{18}$ cm^{-3}	140 Å
AlInAs	Schottky	200 Å
	δ - doping = $5x10^{12}$ cm^{-3}	
AlInAs	Spacer	60 Å
GaInAs	Channel	200 Å
AlInAs	Buffer	2500 Å
InP	Semi Insulating Substrate	

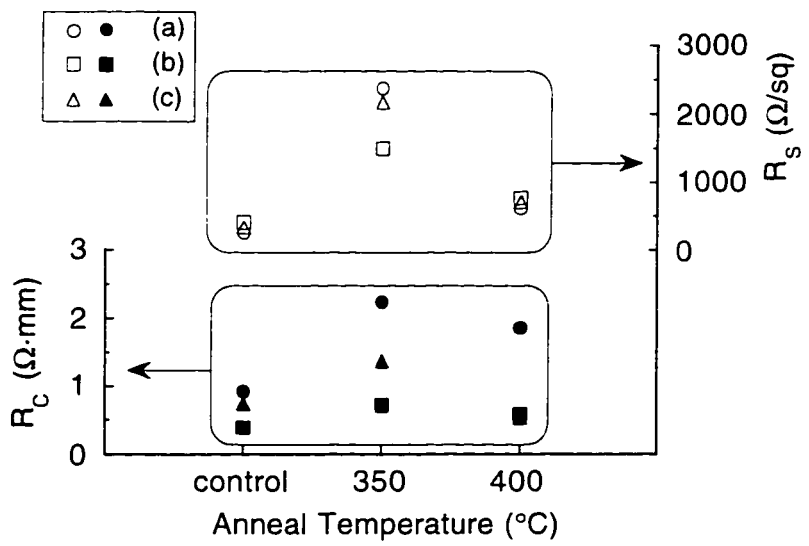
(a)

GaInAs	Cap $n = 5x10^{18}$ cm^{-3}	100 Å
AlInAs	Schottky	200 Å
	δ - doping = $3.5x10^{12}$ cm^{-3}	
AlInAs	Spacer	60 Å
	δ - doping = $1.5x10^{12}$ cm^{-3}	150 Å
GaInAs	Channel	50 Å
AlInAs	Buffer	2500 Å
InP	Semi Insulating Substrate	

(b)

GaInAs	Cap $n = 5x10^{18}$ cm^{-3}	100 Å
AlInAs	Schottky	200 Å
	δ - doping = $3.5x10^{12}$ cm^{-3}	
AlInAs	Spacer	60 Å
GaInAs	Channel $n = 5x10^{17}$ cm^{-3}	200 Å
AlInAs	Buffer	2500 Å
InP	Semi Insulating Substrate	

(c)



(d)

Figure 3.5. (d) Effects of annealing on the TLM resistances for regrowths on (a) regular, (b) δ-doped, and (c) uniformly doped channel HEMTs.

The next question is then whether the Si doping in the AlInAs donor layer is related to the temperature instabilities. Recent studies have shown that atomic hydrogen can form bonds with Si in AlInAs and passivate it, resulting in the loss of free carriers in the sample [6-8]. These studies also indicate, however, that when these samples are annealed for a brief period in inert atmospheres at temperatures around 450-500°C, the doping is reactivated. Since hydrogen and hydrogen containing gases are used in the MOCVD process, it is a possibility that the donors in our structures are passivated as well. We check the validity of this hypothesis as follows: we start with two HEMT samples, one standard and one with uniform doping in the channel. After regrowth before further processing, we anneal some pieces with a rapid thermal annealer (RTA) at 450°C for 5 minutes under N_2 gas. We then continue with the rest of the process, and carry out the TLM measurements, which are shown in Figure 3.6. Surprisingly, we see the same trend in the TLM resistances of all of these samples with respect to annealing temperatures. As can be observed, both at 350°C and 400°C, and both in the RTA annealed and the control samples, there are substantial increases in the resistances. *We can thus rule out the possibility of hydrogen passivation of Si in AlInAs as a culprit for the deterioration of the resistances with annealing.*

3.3. Effects of Fluorine on the Regrown Contacts

It is worthwhile to note that some researchers have attributed temperature instabilities in AlInAs/GaInAs HEMT structures to fluorine passivation effects of

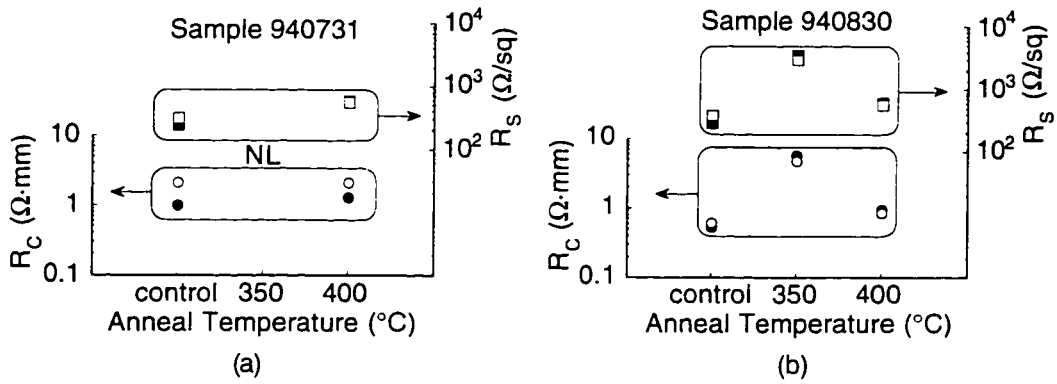


Figure 3.6. Effects of annealing in the RTA at 450°C for 5 min. after the regrowth on the TLM resistances. In (a) is shown the standard, and in (b) the doped-channel HEMT. Open markers show the data for the RTA annealed samples, and solid markers depict no RTA anneal. The IV curves for 350°C annealed sample in (a) were very nonlinear (NL); thus no data points were extracted.

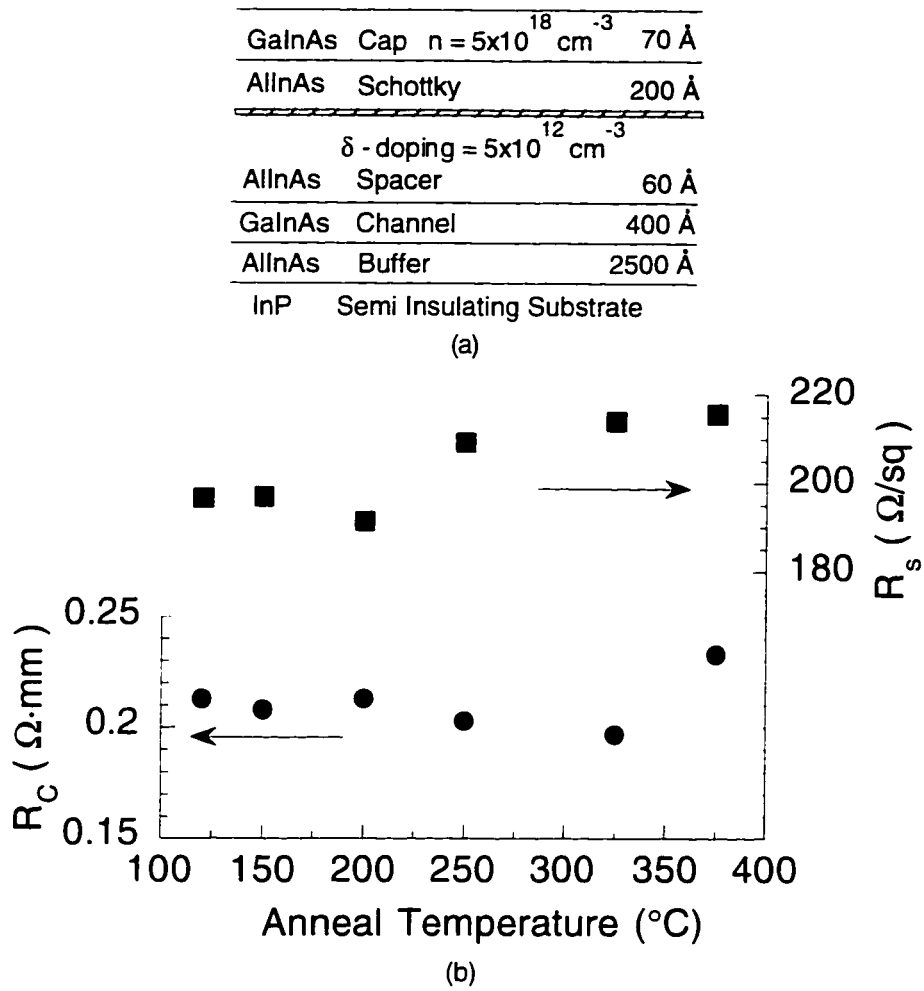


Figure 3.7. (b) The extracted TLM resistances for regrowth on a standard HEMT as shown in (a) A modified process that minimizes fluorine exposure was used.

Si dopants in AlInAs [9]. These researchers have confirmed the detrimental fluorine effects by dipping Si doped AlInAs samples in HF acid, and observing an order of magnitude decrease in the carrier concentration after an anneal at 450°C. They have also shown that the carrier concentration in AlInAs/GaInAs HEMT samples start decreasing significantly after anneals at 300°C. They have verified the existence of fluorine in the Si-doped AlInAs layers by SIMS measurements. To check if fluorine passivation could be a problem for our system as well, we devise a new set of experiments with the goal of minimizing the usage of BHF. In particular, instead of the standard process that we have been employing, we do the following: etch the isolation mesa first, deposit oxide, pattern the oxide, etch the semiconductor, skip BHF dip and immediately transfer the samples to the

MOCVD reactor for regrowth. After regrowth, without removing the oxide mask, do lithography for liftoff and finally metalization. Since we do the mesa isolation first, at this stage the samples are ready for measurement. Figure 3.7 shows the resistance measurements for regrown contacts fabricated using this modified process on a standard HEMT sample. *We notice that the sheet resistance is now stable with respect to the annealing temperature.*

To further pinpoint the effects of fluorine in our structures, we design the following set of controlled experiments. We do the processing steps similar to above, starting with mesa isolation and leaving the oxide mask in place after regrowth.

(a) A standard regrowth with two samples, in which one of the samples is subjected to BHF predip before loading into the MOCVD reactor for regrowth, and the other is not.

(b) A regrowth experiment similar to (a), with the pregrowth bake time at 450°C 30 minutes instead of 10 minutes to find out whether the prebake time affects fluorine incorporation.

(c) An atmospheric pressure regrowth with two samples, where no BHF predip is done and one of the samples is etched into the channel while the other is etched through the channel and into the buffer for regrowth, essentially as a sanity check to assure that the etch depth or growing on the AlInAs buffer is not a critical factor in determining the outcome of the regrowth. The atmospheric pressure regrowth enables a higher doping incorporation in the regrown GaInAs compared to the low pressure regrowth as shown in Figure 3.8. In our case, we have always worked with a doping of about $1.5 \cdot 10^{18}$ cm^{-3} for the low pressure regrowth and have now achieved a doping of about $7 \cdot 10^{18}$ cm^{-3} for the atmospheric pressure regrowth. The drawback of operating at atmospheric pressure, however, is the decrease in the selectivity of the regrowth, as observed in Figure 3.9 [2].

Upon measurement of the contact resistances, we find that the prebake time or etching into or through the channel for regrowth does not change the results significantly. However, we do see other dramatic trends, which are shown in Figure 3.10. We observe two points here: (i) in none of the cases does the sheet resistance show severe deterioration with respect to temperature and (ii) the

[2] Normally one should be able to achieve a higher doping by simply increasing the disilane flow rate or its concentration in the source tank. However, because of the current configuration of our MOCVD system, we are limited in both of these aspects.

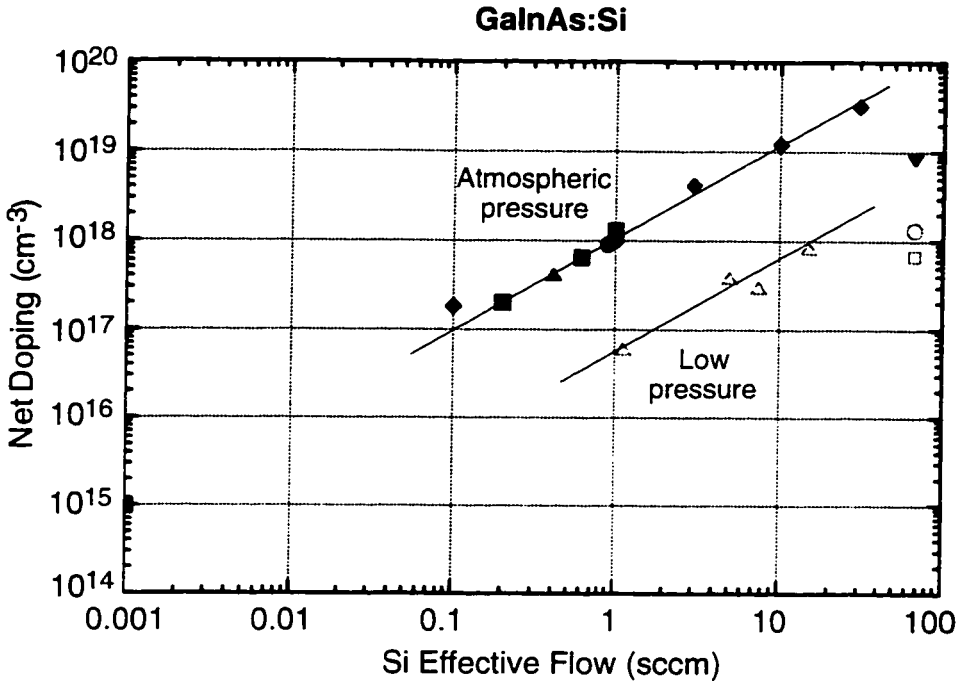
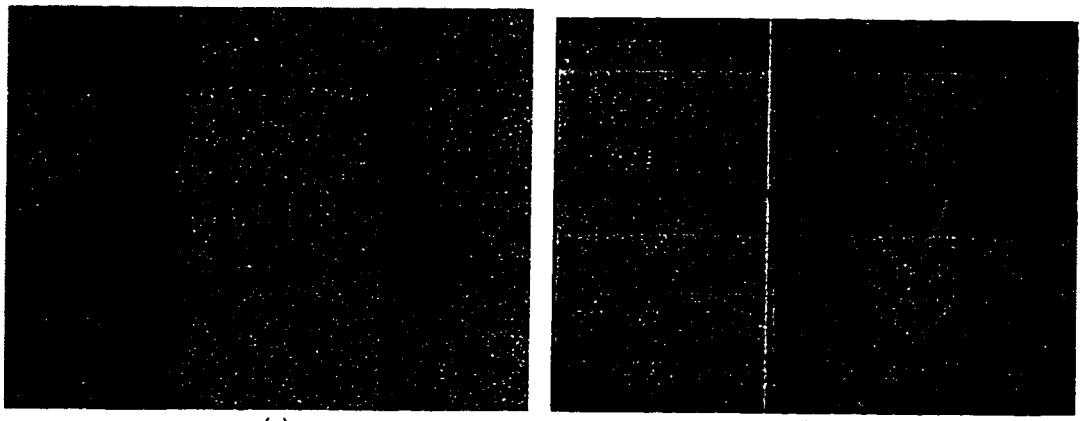


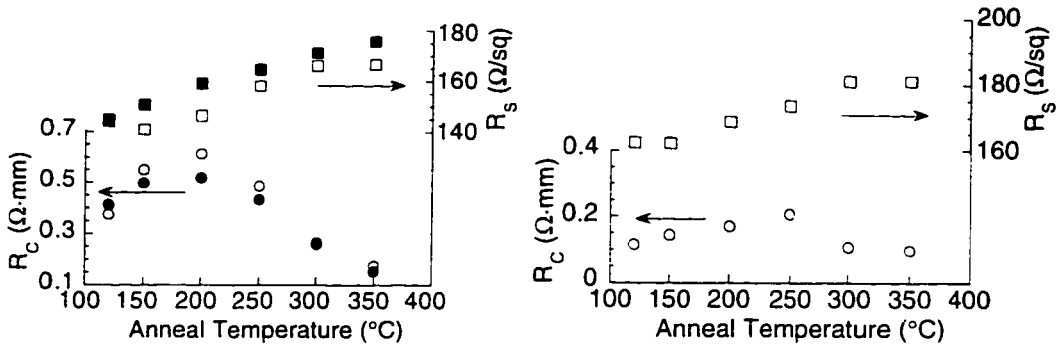
Figure 3.8. Empirically obtained Si doping incorporation curves for GaInAs with respect to flow of 200 ppm of Si_2H_6 in H_2 gas (courtesy Dr. B.P. Keller and the UCSB MOCVD Group).

contact resistance for the atmospheric pressure regrowth (higher doping in the regrowth) is much smaller than the lower pressure one (lower doping). The temperature stability in the R_S in both of the samples with and without BHF predip is somewhat surprising. At this stage, the only difference between the standard process of the previous experiments and the modified process with the BHF predip in this last one is that we have not yet removed the oxide mask from the surface of our samples in this experiment. To see whether the exposure of the sample surface after the completion of regrowth to BHF is the culprit for the deterioration of the TLM resistances as shown in Figures 3.4-6, we carry out the following experiment: we dip one sample from the low pressure regrowth run, and one from the atmospheric pressure regrowth in BHF for 2 minutes to remove the oxide mask. We then heat both of these samples and extract their R_C and R_S from TLM measurements. Figure 3.11 shows these parameters. The striking points are that (i) although with respect to heating, the R_S in the low pressure regrowth stays stable, it shows a sudden jump compared to its value before removal of the oxide mask on the surface and (ii) the R_S of the atmospheric pressure regrowth sample stays stable at its control value after blanket BHF dipping and also with respect



(a) (b)

Figure 3.9. Optical photographs of (a) low pressure and (b) atmospheric pressure regrowth. Selectivity of the regrowth is reduced in the latter case.



(a) (b)

Figure 3.10. TLM resistances for (a) the low pressure and (b) the atmospheric pressure regrowth. Circles show the R_C, and squares the R_S values. Solid markers depict BHF dipping of the sample prior to regrowth, open markers depict no BHF dip.

toannealing.

We note that for our regrowth technology to be applicable to actual FETs, the samples have to withstand HF treatment since the oxide mask has to be removed for further processing of the device. *We observe that the samples that have the higher doping in the regrowth are not affected by HF treatment whereas those with the lower doping are.* It appears from our experiments that for the

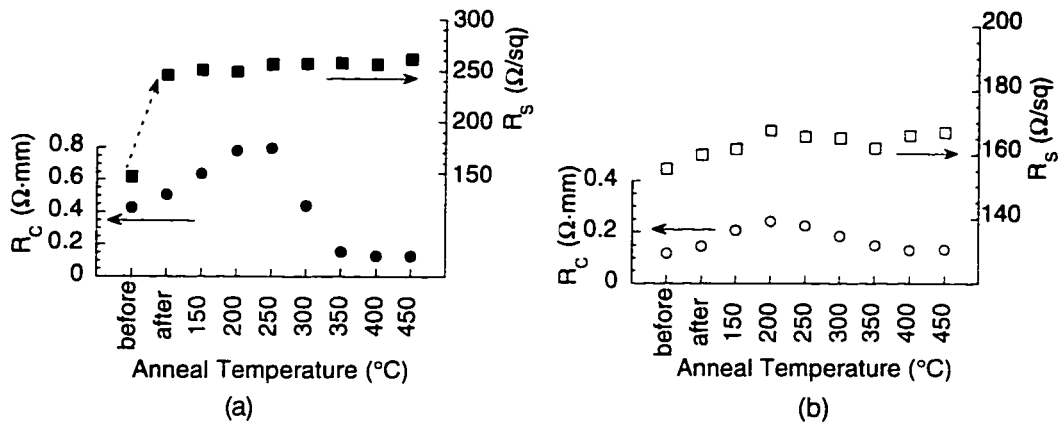


Figure 3.11. The effect of blanket BHF dip on (a) the low pressure regrowth and (b) the atmospheric pressure regrowth sample. Note the jump in the sheet resistance in (a) after the exposure of the surface to BHF. Solid markers depict BHF dipping of the sample prior to regrowth, open markers depict no BHF dip.

samples that have lower doping in the regrowth, exposure to HF creates thermal instabilities and higher contact resistances. At this point, the exact mechanisms of reactions between the samples and HF are not clear to us. However, sufficiently high doping in the regrowth seems to compensate these parasitic effects. We also feel that we have not yet reached the lower limit on the contact resistance, and that with higher doping in the regrown GaInAs on the order of 10^{19} cm^{-3}, we should be able to obtain an R_C value lower than the 0.1 Ω·mm achieved with a doping of about $7 \cdot 10^{18}$ cm^{-3}.

3.4. Summary

We have demonstrated a viable regrown contact technology to achieve low contact resistances for high frequency devices. These contacts are reliable and thermally stable. We obtained a non-alloyed contact resistance of 0.1 Ω·mm for $n \approx 7 \cdot 10^{18}$ cm^{-3} doped GaInAs selectively regrown on AlInAs/GaInAs HEMT structures. We have shown that exposure to HF has detrimental effects on the thermal stability of the regrowth structures when the doping in the regrowth is on the order of 10^{18} cm^{-3}, but that these effects are compensated with a sufficiently high doping in the regrowth. We believe that doping in the regrowth of the order of 10^{19} cm^{-3} will enable us to obtain yet lower contact resistances than those achieved so far.

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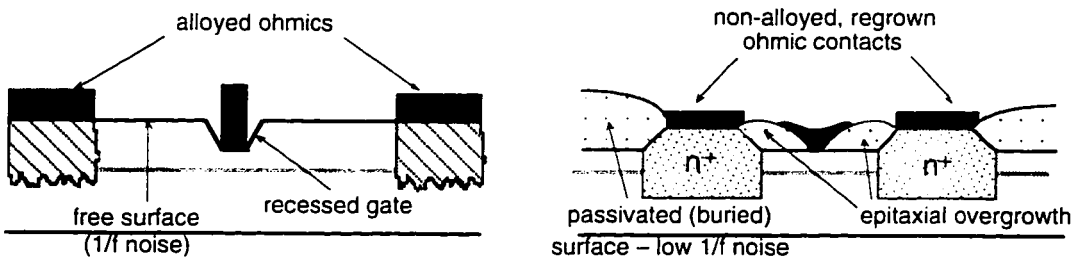
Chapter 4

Fabrication of the HEMT

Developments in materials technologies presented in the previous chapters allow realizing FETs, where processing and growth are continuously interleaved throughout the fabrication of the devices. Having established a technique for low resistance non-alloyed regrown ohmic contacts, in this chapter we report on the fabrication of a HEMT that not only incorporates the regrown contacts for its source and drain terminals, but also makes use of the regrowth technique to create a surface epitaxially passivated device with an "effective gate recess". Surface passivation to improve transistor characteristics has been an issue of interest to a great many researchers [1, 2]. One would like to avoid free surfaces near the active channels in III-V semiconductors because (i) traps associated with the surface can result in frequency dispersion of device characteristics and (ii) free surfaces can yield to degraded low frequency noise (such as 1/f noise) behavior, which is known to arise from the variations in the occupancy of bulk and surface trap centers [3]. Generation-recombination noise shows itself also in the low frequency noise spectrum as bulges superimposed on the 1/f spectra [4].

4.1. Device Proposal and Design

Figure 4.1 shows a schematic comparison between a standard HEMT and the proposed device. There are two distinct differences in the proposed device over the standard HEMT: (i) non-alloyed, low resistance, regrown ohmic contacts



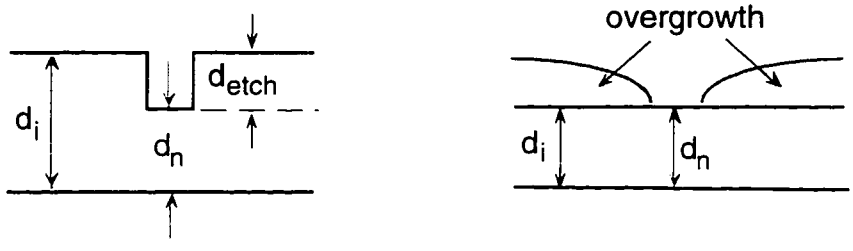
(a) Conventional device (b) Proposed ideal device

Figure 4.1. A schematic comparison between (a) a conventional device and (b) the proposed ideal device.

are employed instead of the alloyed ohmic contacts enabling the fabrication of the device with a single level of metalization for all the source, drain and gate contacts, and (ii) no recess etching is done in the traditional sense, but rather a "buried channel" device is formed by overgrowth of epitaxial passivation outside of the gate area. The proposed device is expected to be better than the standard one from a uniformity and reliability point of view as not only the ohmic contact formation is improved but there is a tighter control on the threshold voltage definition of the device as well, as explained below.

The minimum recess etching of the gate region is necessary to assure that sufficient charge can be provided to the channel under the gate from the access region between the source and the gate terminals even under positive bias of the gate. The initial thickness of the cap can be adjusted to provide for a lower access resistance and the threshold voltage can be controlled independently by additional recess etching. Figure 4.2 shows the possible ways a "recess" can be defined. The threshold voltage depends on the gate to 2 DEG separation, d_n. [5]. For a desired threshold voltage (or equivalently d_n), $d_n = d_i - d_{etch}$ is conventionally achieved by etching a recess (Figure 4.2 (a)). If $d_n = d_i$ is designed however (Figure 4.2 (b)), then overgrowth of epitaxial passivation outside of the gate region will provide for the lower access region resistance compared to the resistance under the gate. The threshold voltage is subject to nonuniformities across the wafer with recess etching, unless a very tight control on the etching process is held. However, with the overgrowth method, the threshold voltage is set by the original MBE growth, which provides for very uniform layer thicknesses across the wafer.

Figure 4.3 (a) depicts the layer design used to implement the devices. The structure is grown lattice matched to a semi-insulating InP substrate by MBE. On



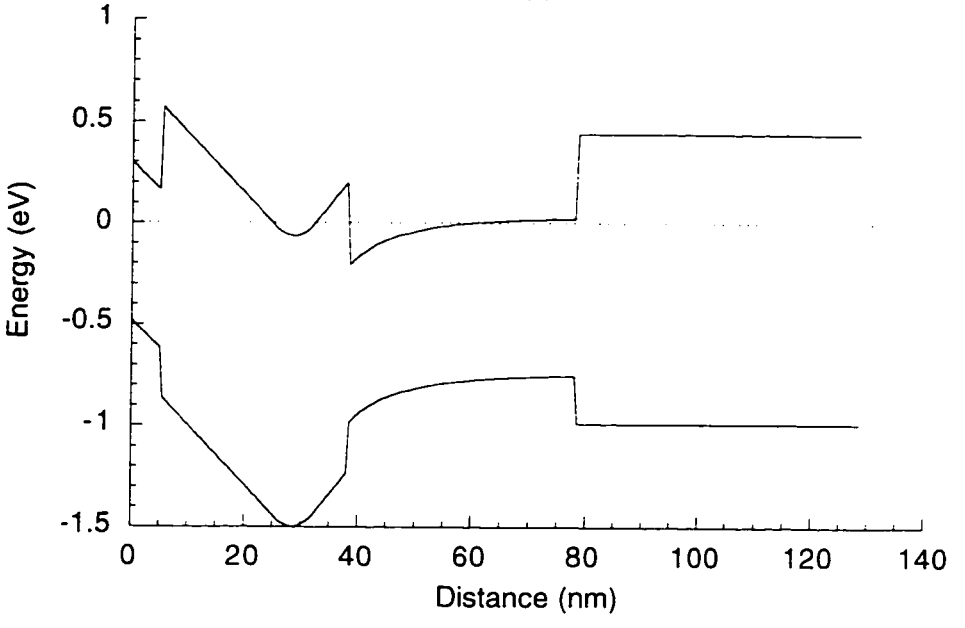
(a) d_n achieved by recess etching

(b) Lower access resistance achieved by overgrowth

Figure 4.2. The desired thickness, d_n, for a particular V_{th} design can be achieved either by recess etching, or if d_n is set by the initial donor region thickness, d_i. overgrowth outside of the gate region prevents g_m compression for positive gate biases [6].

GaInAs	Cap		50Å
AlInAs	Schottky		200Å
AlInAs	Donor	$n = 8x10^{18}$ cm^{-3}	70Å
AlInAs	Spacer		60Å
GaInAs	Channel		400Å
AlInAs	Buffer		2500Å
InP	Semi Insulating Substrate		

(a)



(b)

Figure 4.3 (a) The HEMT design to be used in epitaxial surface passivation experiments. (b) Band diagram at equilibrium for this layer structure.

top of the 2500 Å buffer and the 400 Å channel, a 60 Å spacer is allocated to ensure good electron mobility as has been established by previous HEMT runs at UCSB [7]. A thin uniformly doped donor region is designed to hold about $5 \cdot 10^{12}$ cm^{-2} charge, which yields a sheet carrier concentration (n_s) of about $3 \cdot 10^{12}$ cm^{-2} in the channel. Uniform doping was chosen over planar doping because higher mobilities have been reported with uniformly doped HEMTs than planar doped ones for thin spacers [5, 8]. The GaInAs cap is kept at a thickness of 50 Å and is undoped. The cap is designed to be totally depleted as the gate metal is placed directly on the surface in the completed device. Since low contact resistance to the

channel is provided through the n^+ regrown regions, there is no need to dope the cap as is conventionally done [9, 10] [1]. Figure 4.3 (b) shows the corresponding band diagram at equilibrium plotted using Bandprof [12] assuming a 0.3 V Schottky barrier height on the GaInAs surface. The simulated sheet charge in the channel and the donor regions come out to be $2.8 \cdot 10^{12}$ cm^{-2} and $6.9 \cdot 10^{11}$ cm^{-2} respectively. Based on this layer design two samples were grown independently at two different times: 951003B by Mark Mondry, and 951108 by Prashant Chavarkar. Table 4.1 lists their measured sheet charges (n_s) and mobilities (μ).

Sample	n_s (10^{12} cm^{-2})	μ ($cm^2/V \cdot s$)
951003B	2.0	12,000
951108	2.8	8,300 [2]

Table 4.1. Measured sheet carrier concentrations and mobilities for the MBE samples to be used in succeeding experiments.

4.2. Initial Process Idea

Figure 4.4 shows the initially proposed process flow to fabricate the epitaxially surface passivated HEMTs with regrown contacts. The structure first goes through the standard contact regrowth process as in Chapter 3. A submicron gate is then written, and using evaporation and liftoff, a SiO_2 dummy gate is placed onto the surface. Overgrowth of epitaxial passivation then takes place in all unmasked areas of the sample. To place the contacts, source and drain lithography is carried out and the epitaxial passivant is etched down to the previously regrown contact epi. After drain and source metalization are deposited, a gate level lithography is carried out. The process is finally finished with mesa isolation.

The etching through the overgrown passivant and stopping at the surface of the contact regrowth for contact metalization are one of the critical stages in this process as the contact regrowth is terminated by grading to InAs to enable

[1] Some researchers have reported other merits of having an undoped cap compared to a doped one, such as improved gate leakage characteristics and lower output conductance [11].

[2] The smaller mobility observed for this sample is probably an artifact of the measurement method, where, to get a quick reading, the Van der Pauw measurement was taken on a small square sample with four In dots placed on its corners instead of the standard rigorous VdP pattern definition and etching, which was done for measuring the sample 951003B.

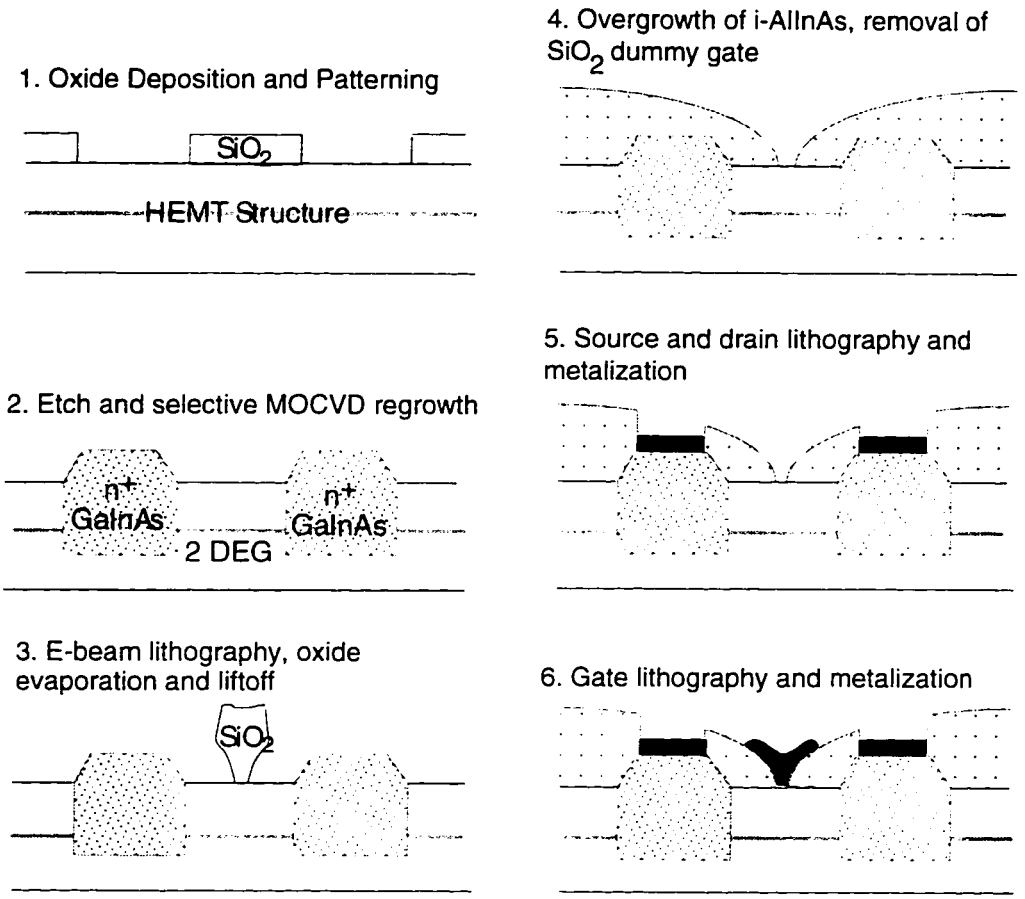


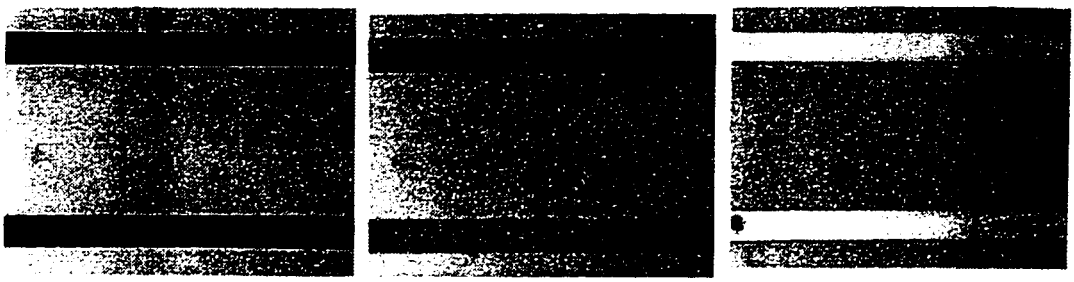
Figure 4.4. Initially proposed process flow for the fabrication of the surface passivated HEMT.

lower contact resistance. We therefore investigated the feasibility of a thin layer of InP as an etch-stop layer on the contact regrowth, over which i-AlInAs could be grown for surface passivation. We grew the test structure shown in Figure 4.5 by MOCVD and then carried out an etch test on this sample with a 3:1:50 solution of H_3PO_4:H_2O_2:H_2O after a 10 s 1:10 NH_4OH:H_2O predip and rinse. Figure 4.6 shows the progress of the etch with respect to time. As evident, the InP cap is not able to provide for a selective etch stop layer against the phosphoric acid solution because it is likely that the InP grown on InAs is lattice mismatched and relaxed [13].

AlInAs	undoped	5000Å
InP	undoped	60Å
InAs		10Å
GaInAs → InAs grading		50Å
GaInAs		7500Å
InP	Buffer	
InP	Semi Insulating Substrate	

$n \approx 8 \times 10^{18}\ cm^{-3}$

Figure 4.5. Test structure Z951006C to check the InP etch stop layer on the GaInAs/InAs regrowth.



(a) (b) (c)

Figure 4.6. The etch progress of mesa bars on sample Z951006C in a 3:1:50 H_3PO_4:H_2O_2:H_2O solution. Initial thickness of the resist mask was 9500 Å. It is clear that the InP cap does not provide for a selective etch stop against the phosphoric acid solution.

(a) After 4 min. of etch, t = 14,300 Å (t_{etch} = 4800 Å). The top AlInAs is almost gone.
(b) After 5 min. of etch, t = 15,600 Å (t_{etch} = 6100 Å). The structure has etched through the InP.
(c) After 8 min. of etch, t = 19,600 Å (t_{etch} = 10,100 Å). The etched, bright appearing surface is the GaInAs channel.

4.3. Improved Process Idea

As the etchback idea was not feasible, an alternate process scheme was devised in which the contact areas were covered with dummy oxide masks as well during the surface passivation run [14]. Since E-Beam lithography is used to write the patterns for sacrificial oxide gates, it is a straightforward task to write the

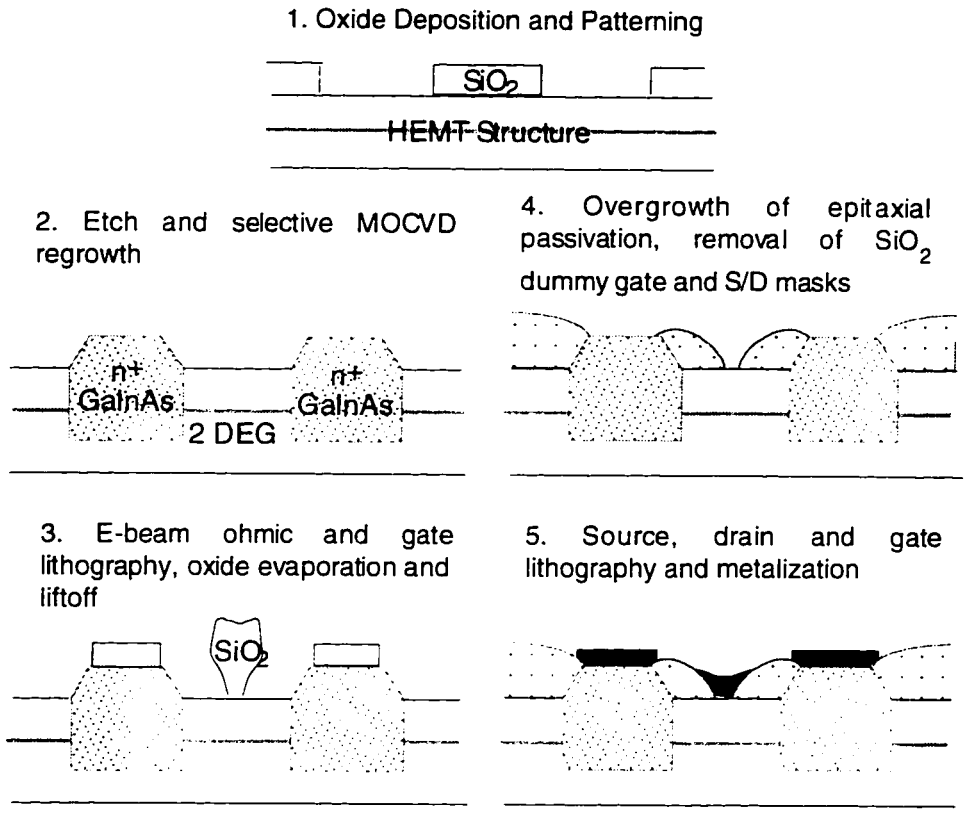


Figure 4.7. Improved process flow sequence with the source and drain contact regrowth areas covered during the insulator overgrowth.

source and drain areas concurrently for subsequent oxide evaporation and liftoff [3]. The modified process flow sequence is hence depicted in Figure 4.7.

The overgrowth of the epitaxial passivant can be carried out either by MBE or by MOCVD. Figure 4.8 compares these two overgrowth schemes. It is evident that the E-Beam lithography to put down the dummy oxide gate is one of the most critical lithography steps in this process sequence, particularly for the MBE overgrowth of the insulator. Contrasted to MOCVD growth, MBE growth is not selective as it is essentially an ultra-high vacuum deposition system. For MBE overgrowth, the top portion of the T-gate determines the projected

[3] We do pay a penalty for including the large contact areas in the E-Beam lithography: time! For each of the chip sites, the write takes 1.5 - 2 minutes. For a typical small sample with about 150 devices on it, the total wafer exposure time is about 5 - 6 hours.

gatelength. We have previously established an in-situ etch and MBE regrowth scheme and have found out that the mask profile is also crucial in achieving a successful liftoff of the polycrystalline material on the mask [15, 16]. For selective MOCVD overgrowth, however, the bottom footprint of the dummy oxide determines the lithographic dimension for the gatelength, and the actual shape of the oxide is not critical. Therefore, MOCVD overgrowth is expected to be a more versatile system from a processing standpoint as long as the same material quality can be obtained from the MOCVD system as from the MBE system.

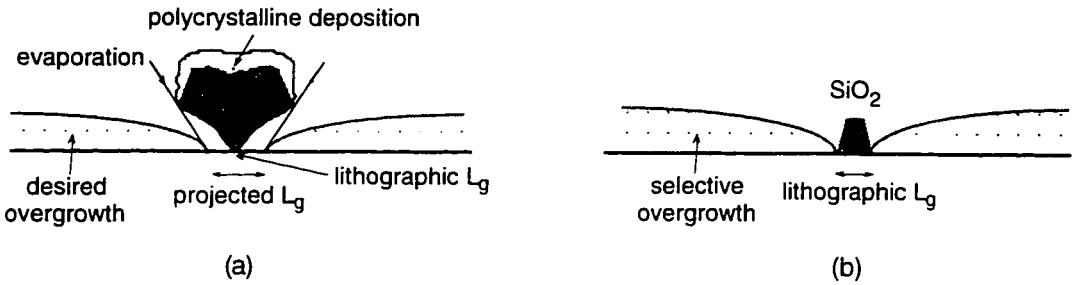


Figure 4.8. Schematic depictions of (a) MBE "overgrowth" and (b) selective MOCVD overgrowth.

4.4. Overgrowth of AlInAs by MOCVD

The first overgrowth experiment we designed was the growth of i-AlInAs by MOCVD. As the underlying HEMT structure, we used the MBE grown sample 950810 (shown in Figure 4.9), on which the MOCVD contact regrowth R951002D had been performed [4].

GaInAs	Cap	$n = 5x10^{18}$ cm^{-3}	140Å
AlInAs	Schottky	δ-doping	200Å
AlInAs	Spacer	$n_S = 5x10^{12}$ cm^{-2}	60Å
GaInAs	Channel		400Å
AlInAs	Buffer		2500Å
InP	Semi Insulating Substrate		

Figure 4.9. Sample 950810 used for initial tests of AlInAs overgrowth by MOCVD.

[4] At the time of this experiment, this MBE sample was the only one with the contact regrowth carried out and ready for the next step. Overgrowth experiments on the MBE samples specifically designed for this purpose (namely, 951003B and 951108) are reported in Sections 4.5 and 4.6.

The overgrowth was performed on the sample through the process flow as outlined in Figure 4.7, the details of which are given as follows:

(i) Exposure and development of the E-Beam resist.
(ii) Slight O_2 plasma (10 s, 300 mTorr, 50 W) for resist descum.
(iii) Loading into the E-Beam evaporator, evaporation of SiO_2, and subsequent liftoff.
(iv) Pre-growth surface dip in 1:10 $NH_4OH:H_2O$ solution for 10 s, water rinse for 2 min.
(v) Selective MOCVD regrowth (run R951206E) carried out at 650°C, 76 torr (0.1 atm), aiming for a 650 Å of unintentionally doped AlInAs capped by 100 Å of undoped GaInAs.

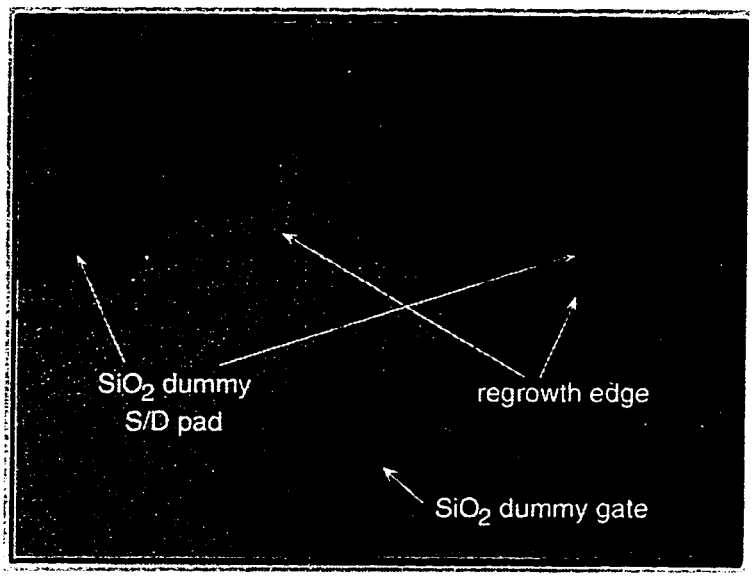
4.4.1. Dummy Oxide Gate Issues

Figure 4.10 shows a typical alignment and cross-section of an oxide gate before overgrowth has been performed. Figure 4.11 depicts an oxide gate after the overgrowth. The sticking of the gate to the surface of the wafer appears to be poor. Examining the process flow outlined above, we note that after the O_2 plasma descum, the surface of the sample is likely to be left with irregular clusters of gallium and arsenic oxides. In this particular run, no surface oxide cleaning dip was done before the evaporation of the dielectric, thereby resulting in possibly poor sticking of the dielectric to the wafer surface. Then either the high temperature of the MOCVD reactor, or the NH_4OH dip before the overgrowth may have caused the dielectric to lift off of the surface. To check the first hypothesis, the following experiment was performed:

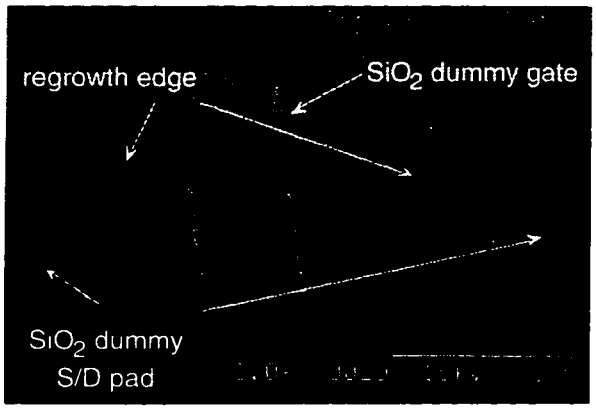
(i) On a blank GaAs piece, gate finger patterns were exposed by E-beam and developed.
(ii) Half of the sample was dipped in a 1:10 BHF: H_2O solution for 5 s, and then rinsed in water for 2 min.; the other half was left on the side.
(iii) SiO_2 was evaporated and lifted off on both pieces.
(iv) Both pieces were annealed in the RTA to simulate the temperature profile of the MOCVD reactor: 250°C for 5 min., 450°C for 10 min., and 650°C for 5 min.

Subsequent inspection under the microscope showed that none of the gates had been affected by the high temperature steps. This thus rules out the effect of temperature on the sticking of the oxide to the semiconductor surface. The following experiment however, reveals that it is the NH_4OH dip that etched the

irregular nascent oxide under the SiO_2 dielectric, and hence lifted the dielectric off. On two separate pieces, E-Beam lithography was done to put down the gate patterns in the E-Beam resist. Before SiO_2 evaporation however, a 5 s, 1:10 $BHF:H_2O$ dip was performed on one of the samples followed by a 2 min. rinse in water (BHF was preferred as NH_4OH delaminates PMMA). After evaporating the dielectric, both samples were subjected to a 10 s 1:10 $NH_4OH:H_2O$ dip. As a result, all the gates on the sample which had been loaded to the evaporator



(a)

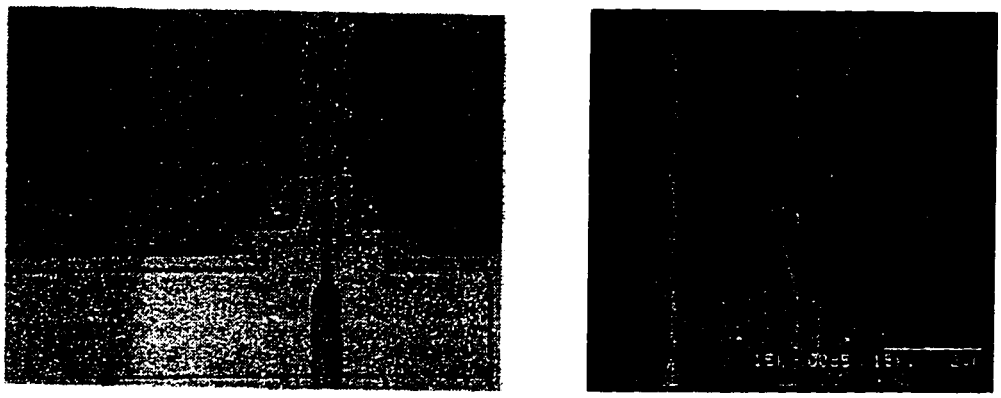


(b)

(c)

Figure 4.10. E-Beam registration and alignment for the dummy oxide gate. (a) Alignment as seen by optical microscope (magnification: ~1740). The darker areas are the evaporated SiO_2, the light areas are the source and drain regrowth regions. (b) An SEM view of the alignment. (c) The cross section of a 0.3 μm gate. See Appendix 2 for a discussion about the profile of the gate.

without surface conditioning peeled off, whereas the gates on the sample with the BHF surface pretreatment before evaporation remained intact. Essentially, by etching the irregular nascent oxide on the surface by the BHF solution, and subsequently growing a smooth layer of oxide by the water rinse, a clean surface was provided for the evaporated SiO_2 to stick to. From this point on in all the succeeding experiments, BHF surface treatment was used before the SiO_2 evaporation thereby ensuring good sticking to the surface and masking for the subsequent overgrowth process.

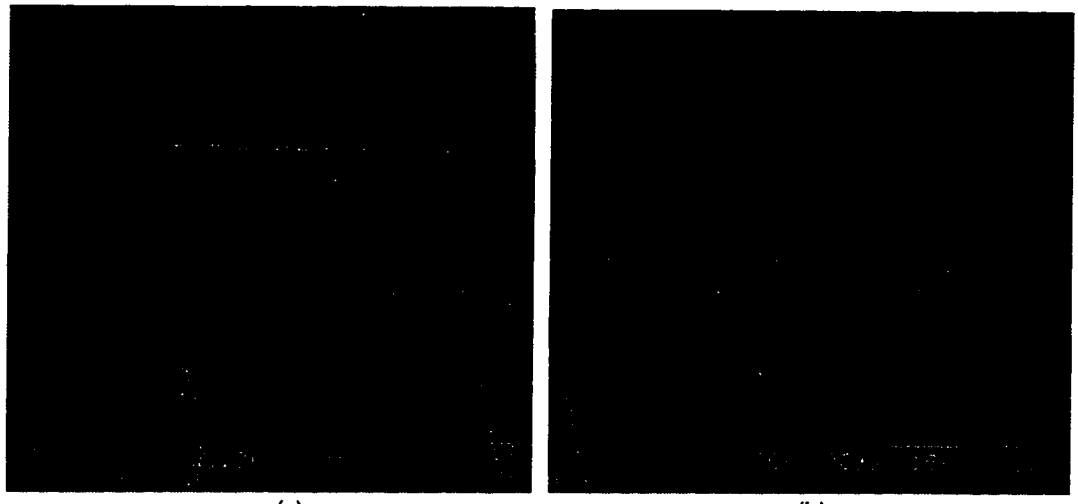


(a) (b)

Figure 4.11. (a) Appearance of the dummy oxide gates after MOCVD overgrowth of AlInAs (magnification: ~790). (b) The AlInAs step is clearly visible in this SEM micrograph after the dummy gate is removed. Instead of an expected 0.3 μm, the gate footprint turned out to be ~0.8 μm.

4.4.2. Completion of the Process and Results

The process on the sample 950810 was completed despite the problem of bad gate footprint definition. Another layer of E-Beam gates (aligned to the footprint defined by the dummy oxide, and wide enough to cover it) were written along with source and drain pads, and the sample was metalized with Ti/Pt/Au. The devices were isolated through mesa etching and completed. While writing the gate metal overlay, a notch was made at the gatefeed, so that the gate finger could be undercut during mesa isolation. This was necessary because of the mask that was used to pattern the source and drain regrowths, which also had a pad for the gate. The gate metal essentially sat on a regrown area as well. This area had to be isolated from the rest of the device so as not to create a short to the 2DEG in the channel. Figure 4.12 depicts SEM micrographs that show this gate finger isolation.



(a) (b)

Figure 4.12. (a) SEM micrograph of the finished device showing the gate feed along with the source and drain contacts after mesa isolation. (b) A close-up of the isolated gatefeed finger.

Dc measurements of the devices, however, revealed short circuits between the gate, drain and source terminals. There could be two possible reasons for this observation: (i) the mesa isolation etch was not complete (although the SEM micrographs of Figure 4.12 clearly point to the opposite) providing a leakage conduction path underneath the gate pad through the buffer, or (ii) the overgrown AlInAs was conductive. To check the first conjecture, the gate to source diodes on a few devices were measured and showed short circuits. Next, with a dc pin probe, the metal gatefeeds were carefully broken one at a time and the gate to source current was measured again. While the measurement was still a short after breaking one feed, the current level dropped four orders of magnitude after both feeds were broken signifying that the gate to source pad isolation was satisfactory. These IV characteristics are depicted in Figure 4.13 (a). To check on the second conjecture, a semi-insulating (SI) InP piece which was put into the MOCVD reactor along with the actual device samples for AlInAs overgrowth was probed on its surface with two dc pin probes positioned a couple of microns away from each other. This measurement gives us an approximate but direct measure of how conductive the overgrown epitaxial material is. Figure 4.13 (b) shows the IV characteristics along with a reference measurement done on a SI InP substrate surface. The five orders of magnitude higher current levels seen in the AlInAs sample compared to the SI InP are testimony to a very conductive epi. Although somewhat surprising at first, this result is not completely unexpected. Researchers have shown that large

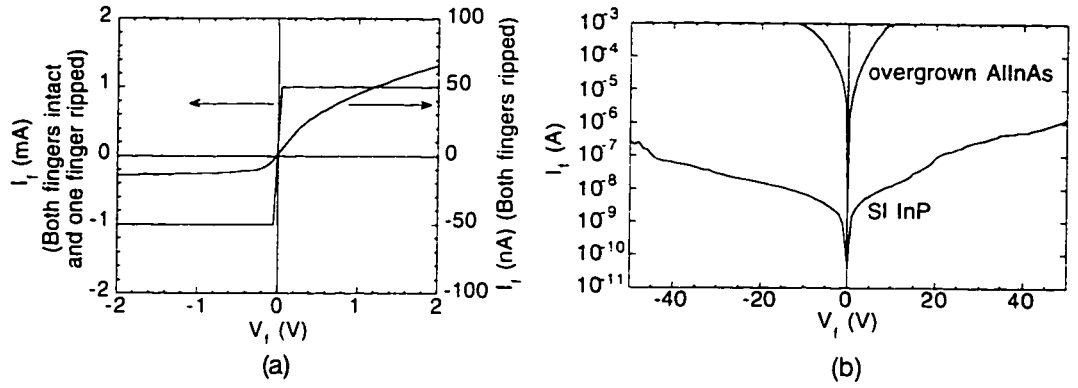


Figure 4.13. (a) IV characteristics between the gate and the source terminals with the gatefeeds intact and ripped. Note different scales in y-axes. (b) Surface probe currents of overgrown AlInAs and SI InP. Note the five orders of magnitude higher current level for the AlInAs growth.

amounts of oxygen can be incorporated as a deep level donor in MOCVD grown AlInAs [17, 18], and can give rise to electron concentrations in excess of 10^{17} cm^{-3}. It appears that here at UCSB we are suffering from similar problems.

4.5. Overgrowth of InP by MOCVD

4.5.1. Design and Process

MOCVD grown InP presents itself as an alternative overgrowth passivation layer since growing undoped AlInAs by our MOCVD system seems problematic. Placement of an InP passivation layer on AlInAs will however, create a quantum well because of the conduction band offset between these two materials. To avoid a 2 DEG on the surface, InP can be doped slightly p-type. Figure 4.14 depicts the simulated band diagram and the distribution of electrons for a 500 Å p^--InP overgrowth ($p = 5 \cdot 10^{16}$ cm^{-3}) on the structure shown in Figure 4.3 (a). Since the total sheet charge of electrons in the InP overgrowth comes out to be on the order of 10^{11} cm^{-2}, this scheme should provide for an effectively resistive surface passivation. Note that the top GaInAs cap still has to be removed before the overgrowth to prevent the formation of a GaInAs quantum well on the surface.

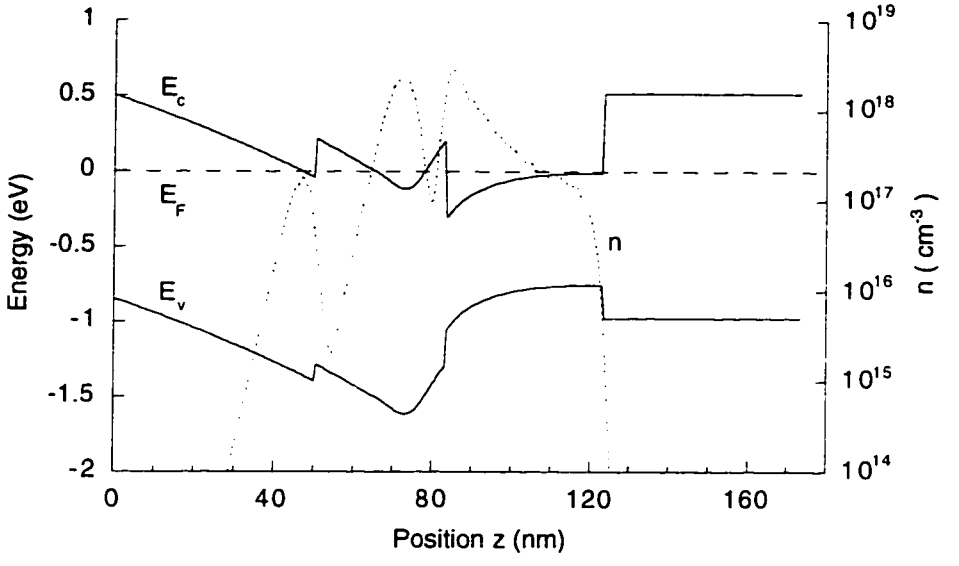


Figure 4.14. The band diagram for p^-–InP overgrowth (p = $5 \cdot 10^{16}$ cm^{-3}) on the HEMT structure shown in Figure 4.3 (a) along with the distribution of electrons throughout the structure. Schrödinger's Equation was also solved self consistently for the whole region. The integrated total charge density in the overgrowth and the channel regions are $1.1 \cdot 10^{11}$ cm^{-2} and $2.6 \cdot 10^{12}$ cm^{-2} respectively.

Sample 951108 (with contact regrowth R951206C) was used to fabricate devices with InP overgrowth. In standard fashion, dummy gate and source/drain patterns were written by E-Beam lithography. After SiO_2 evaporation and liftoff, the top GaInAs cap was removed from the sample by a 1:10 $NH_4OH:H_2O$ surface dip followed by a 3 s 3:1:50 $H_3PO_4:H_2O_2:H_2O$ etch (the etch rate of GaInAs/AlInAs ternaries in this solution is ~20 Å/s). The sample was then quickly loaded into the MOCVD reactor for the InP overgrowth. It was held in the reactor under TBA overpressure at 200°C for 5 min. and 450°C for 10 min. Finally the growth was carried out at 620°C and 0.1 atm using diethylzinc as the precursor for p-doping (run number: R960130D).

Figure 4.15 shows the structure after the InP overgrowth both with the dummy oxide still on and removed. The surface of the InP growth looks rather rough on the areas where the underlying AlInAs layer was exposed, but smooth where the underlying material was the previously regrown GaInAs. Since the etching of the GaInAs cap on the HEMT structure was done ex-situ, the AlInAs Schottky layer was exposed to air and inevitably oxidized, although the transfer time from the etching hood to the MOCVD reactor was minimal. We recall from

Chapter 3 however, that no electrical or surface morphological problems were encountered when GaInAs was regrown on exposed AlInAs buffer. The currently observed surface roughness may possibly arise from growing a binary (InP) under TBP overpressure on an oxidized ternary (AlInAs) surface, which should be kept under TBA overpressure to avoid As desorption from the surface [5].

After the overgrowth was performed and the dummy oxide was stripped, another level of E-beam lithography was employed to write and deposit the overlay metals for the device terminals. The process was concluded by isolating the devices with a mesa etch. Figure 4.16 shows cross sections from the finished device.

4.5.2. Device Results (Dc and Microwave)

Figure 4.17 shows the pertinent dc characteristics of a 300 μm (chip 14.2) and a 400 μm (chip 12.4) wide device. The devices have a full channel current of about 280 mA/mm, with a maximum g_m of about 220 mS/mm. They have leaky gate characteristics, however, and do not exhibit a hard pinchoff as evidenced by

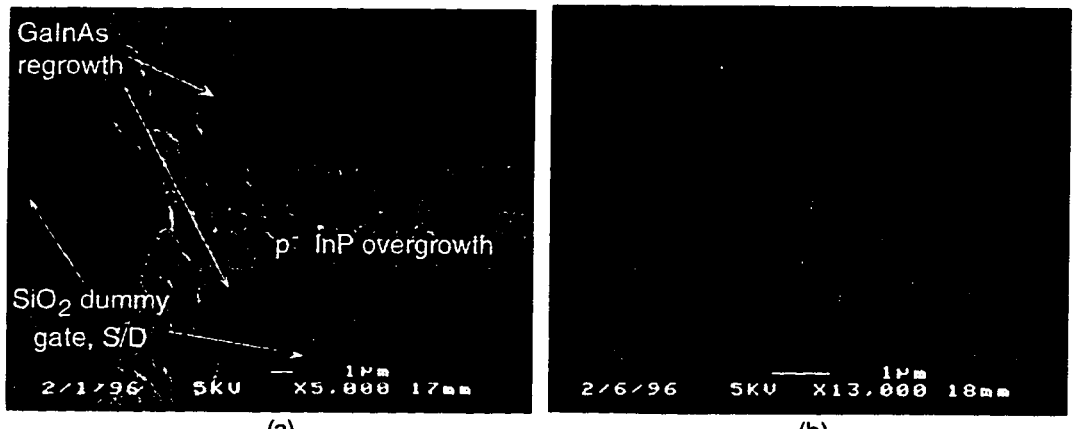


Figure 4.15. (a) SEM micrograph of the HEMT sample with overgrown p^- – InP. The gate and source/drain dummy oxides are still on the sample. (b) A closer look at the overgrowth with the oxide gate removed. The footprint of the gate is ~0.35 μm.

[5] To ascertain that the rough surface was indeed a materials and ex-situ processing problem rather than a fortuitous artifact, the entire InP overgrowth process was repeated one more time with the MBE sample 951003 (contact regrowth R951206B, overgrowth R960307A). As a result a similarly rough surface was obtained for this run as well on the areas, where the underlying material was the exposed AlInAs.

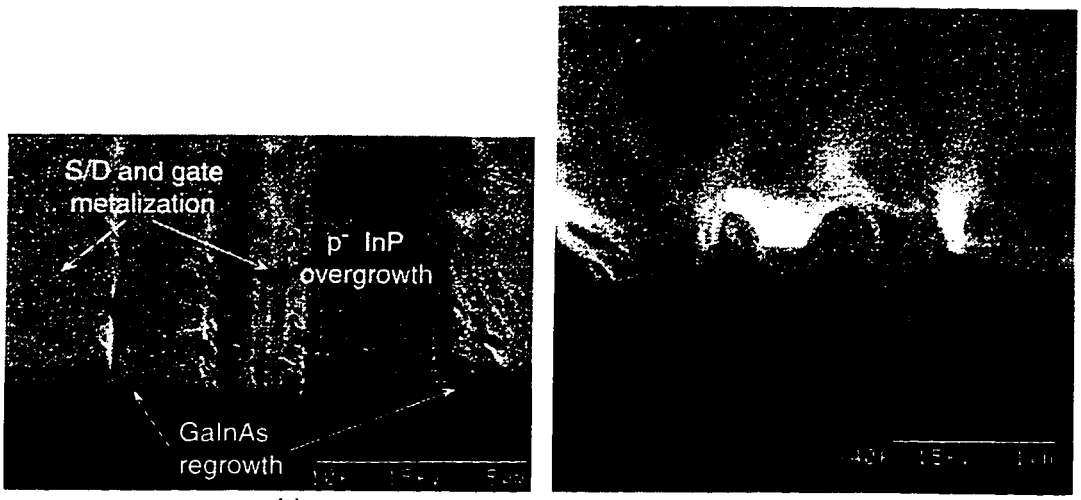


Figure 4.16. SEM cross-sectional views of the completed device. In (a) the source/drain contact regrowth and metalization can also be seen.

the I_D vs. V_{GS} curves. The dc characteristics of these devices were also measured at various low temperatures. Figure 4.18 depicts the behavior of these devices at the measurement temperature of 100K. The g_m is now as high as 350 mS/mm, the increase in which is mainly due to the increase of the 2DEG mobility at low temperatures. The other noticeable difference in the low temperature curves contrasted to the room temperature measurements is the hundred-fold decrease in the reverse leakage current in the gate. This behavior is also observable in the I_D vs. V_{GS} curves in terms of a sharp cut off around V_{GS} = -0.9V. From these observations, it is possible to conclude that the ohmic metalization on the source and drain terminals, which overlaps with the p⁻-InP overgrowth creates a leaky Schottky junction to the overgrowth. Thus at room temperature, where electrons are thermally more energetic than at low temperatures, there is a leakage path between the gate-source and the gate-drain terminals through the InP overgrowth.

Figure 4.19 shows the evolution of the drain currents and the transconductances with respect to the measurement temperature in a comparative fashion. In addition to the previous observations, we also note that the gate voltage at which the g_m peaks moves towards more positive values. The transconductance of a HEMT collapses at positive voltages for mainly three reasons: (i) Under forward bias, the access region of the device can no longer provide for a sufficient amount of charge supply for the gate region effectively creating a high resistance path between the source and the gate. (ii) The donor

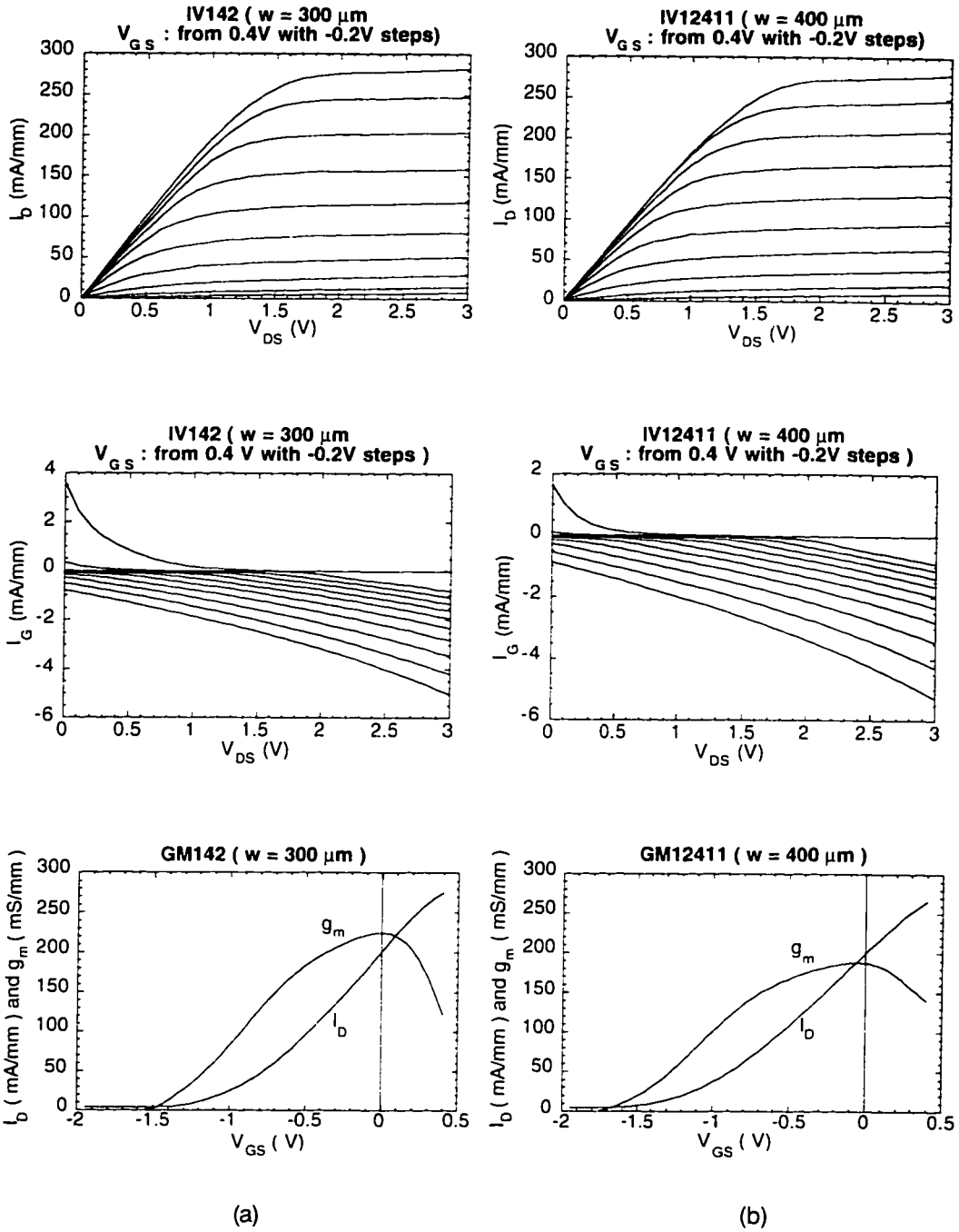


Figure 4.17. I_D vs. V_{DS}, I_G vs. V_{DS} and g_m and I_D vs. V_{GS} characteristics of a (a) 300 μm (chip 14.2) and a (b) 400 μm (chip 12.4) device. The current and transconductance values have been normalized to 1 mm for both devices.

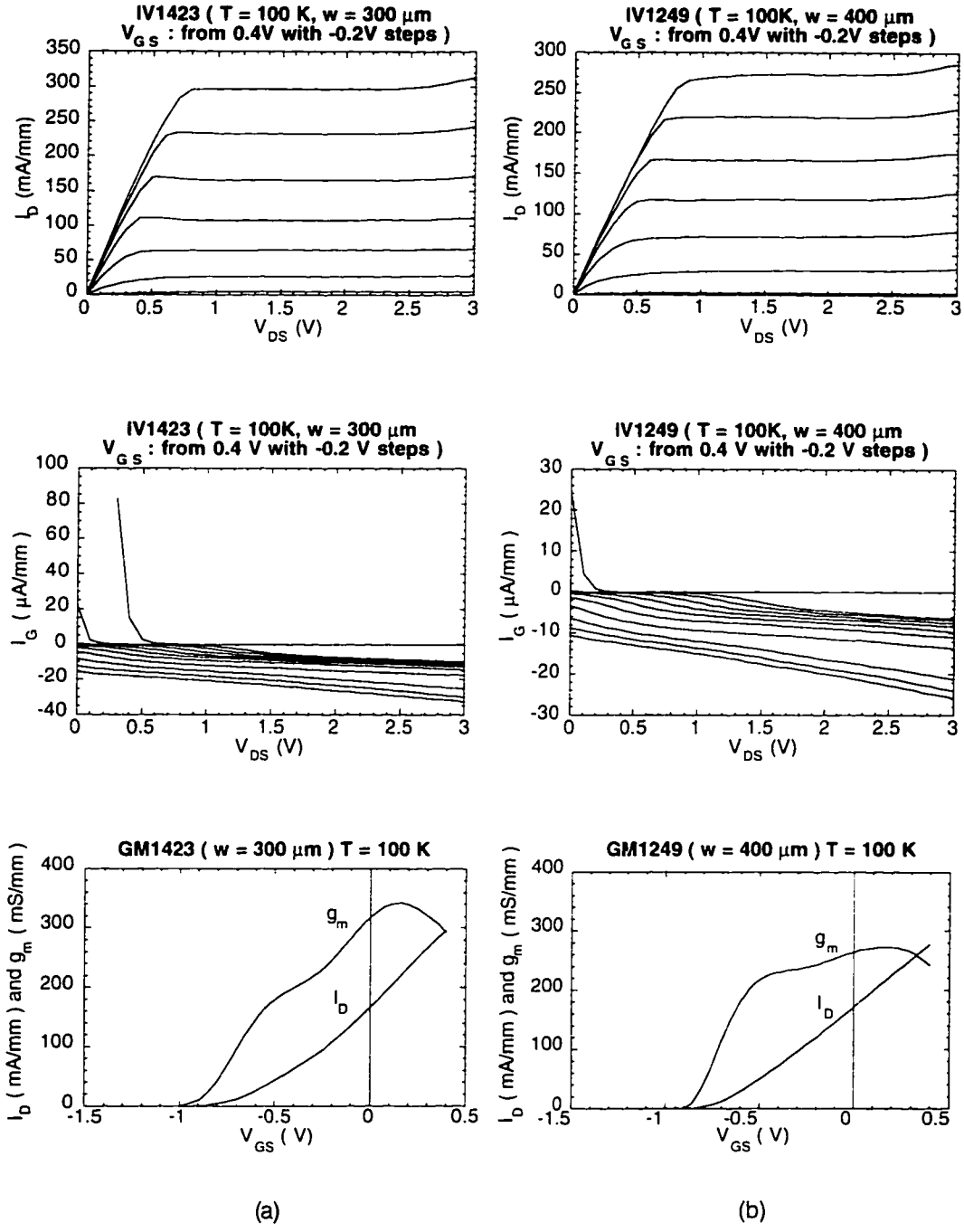


Figure 4.18. I_D vs. V_{DS}, I_G vs. V_{DS} and g_m and I_D vs. V_{GS} characteristics of the (a) 300 μm (chip 14.2) and (b) 400 μm (chip 12.4) device at 100K. The current and transconductance values have been normalized to 1 mm for both devices. Note that the ordinate for the middle graphs have the units of μA/mm.

region (AlInAs) starts conducting, creating a parasitic MESFET operation. (iii) The gate diode turns on. In our case, because we have an effectively better Schottky diode at low temperatures, we seem to be pushing the g_m collapse to further positive voltages.

S-parameter measurements were also carried out on these devices using the HP 8510B Automatic Network Analyzer between 0.045 - 40 GHz. Extracting the frequencies of merit from these measurements, we find that the 300 μm device (chip 14.2) has $f_T \approx 18$ GHz, $f_{max} \approx 50$ GHz (at $V_{DS} = 2$ V, $V_{GS} = -0.6$ V, $I_D = 113$ mA/mm), and the 400 μm device (chip 12.4) has $f_T \approx 20$ GHz, $f_{max} \approx 45$ GHz (at $V_{DS} = 2$ V, $V_{GS} = -0.6$ V, $I_D = 93$ mA/mm).

4.6. Overgrowth of AlInAs by MBE

The next experiment with the process of epitaxial surface passivation is the overgrowth of undoped AlInAs by MBE. The process flow in this case is the same as for the MOCVD overgrowth except for two key differences: (i) the profiles of the dummy oxide gate, and source/drain covers have more stringent requirements on them as regards the cross sectional aspect ratios, and (ii) the removal of the GaInAs cap is done in-situ by a chlorine RIE system connected to the MBE chamber. For this experiment, the sample 951108 was used as the underlying material with n^+ contact regrowth on it (R951206C). An in-situ etch depth of about 70 Å was targeted to remove the top GaInAs layer. A 700 Å of undoped AlInAs growth was aimed. Two MBE regrowth runs were performed to grow the AlInAs, one at standard (510°C), and one at low growth temperature (340°C). After the overgrowth, the polycrystalline deposits on the dummy oxide mask were lifted off by removing the oxide in a BHF:H_2O solution, with the help of an ultrasound vibrator. Figure 4.20 shows an optical microscope photograph of a typical pattern of surface passivation after liftoff. Although the gate footprint of the T-shaped dummy oxide profile was about 0.3 μm, the eventual gate footprint came out to be about 0.9 μm because of the shadowing effect of the wider top region as depicted in Figure 4.8 (a). The process was concluded by the standard procedure of second E-beam alignment and lithography, gate metalization, and device mesa isolation.

Figure 4.21 shows the dc characteristics of a typical device from the run done at standard temperature. Maximum g_m is about 170 mS/mm, and full channel current is about 210 mA/mm. Contrasted to the InP overgrown samples, these

devices have sharp pinchoff characteristics along with low gate leakage, which signifies that the overgrown undoped AlInAs layer is sufficiently resistive.

S-parameter characterization on this device has yielded f_T = 25 GHz, $f_{max} \approx$ 70 GHz at a bias of V_{DS} = 2 V, V_{GS} = -0.4 V, I_D = 70 mA/mm.

4.7. Phase Noise and Low Frequency (Baseband) Noise Performance

Phase noise and low frequency noise measurements were carried out on both the MOCVD p⁻-InP and the MBE i-AlInAs overgrown devices. The HP 3048A Phase Noise Measurement System was used for both set of tests. For phase noise measurements, the devices were embedded in an oscillator circuit with a dielectric resonator (loaded Q = 1250) oscillating at 4.025 GHz [19]. Figure 4.22 shows the circuit diagram for the oscillator and the block diagram of the HP 3048

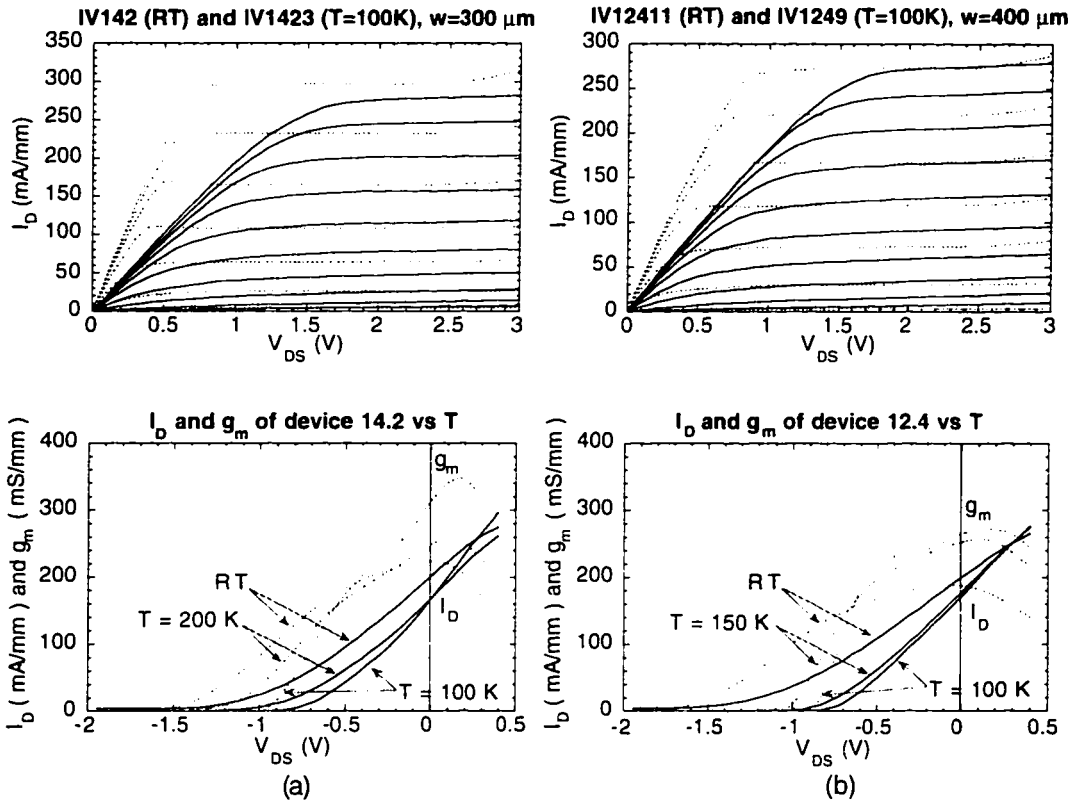


Figure 4.19. A comparative look at the temperature evolution of the dc characteristics for (a) the 300 μm (chip 14.2) and (b) the 400 μm (chip 12.4) devices. The dashed curves in the I_D vs. V_{DS} graphs correspond to the 100K measurements.

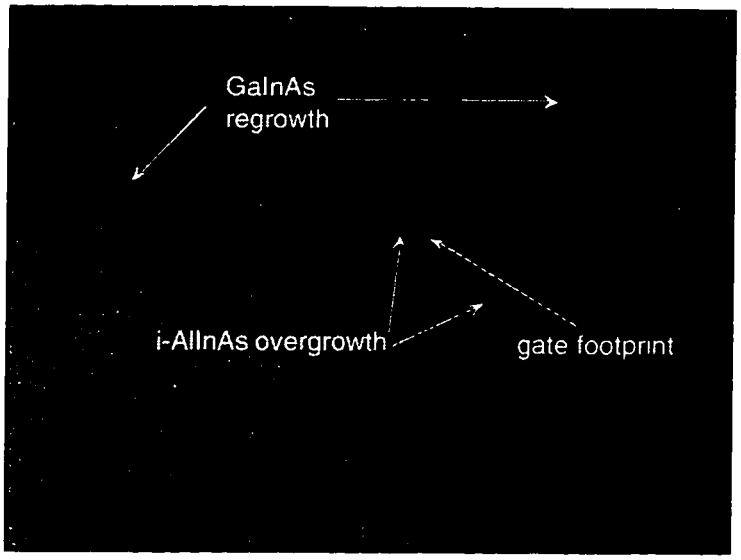


Figure 4.20. Optical microscope picture (magnification: ~1160) of the gate footprint after MBE AlInAs overgrowth and liftoff. The gate length is ~0.9 μm.

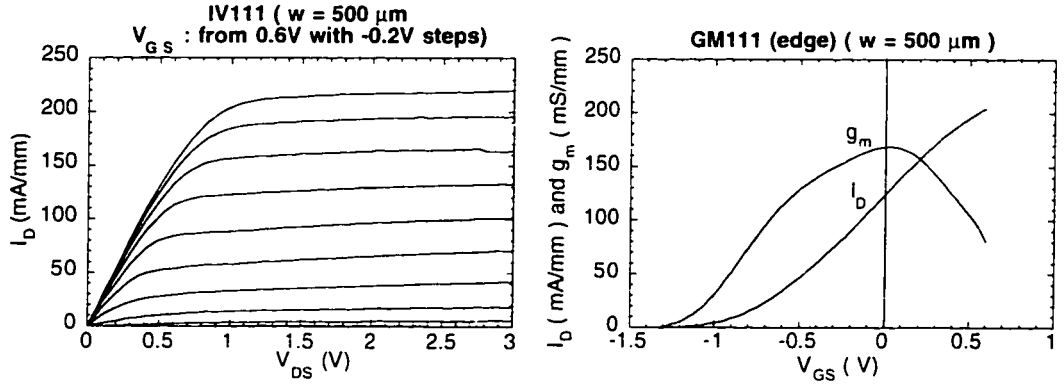


Figure 4.21. Dc characteristics of a 500 μm (chip 11.1) device with standard temperature AlInAs overgrowth.

measurement system configured for phase noise measurements. The system uses a phase detector technique to downconvert and display the signal spectrum, which is modulated by the DUT. We choose the respective heterodyning frequency and the passband in the HP 11729C Carrier Noise Test Set based on the oscillator frequency so that the downconverted IF frequency falls in the range of 350-500

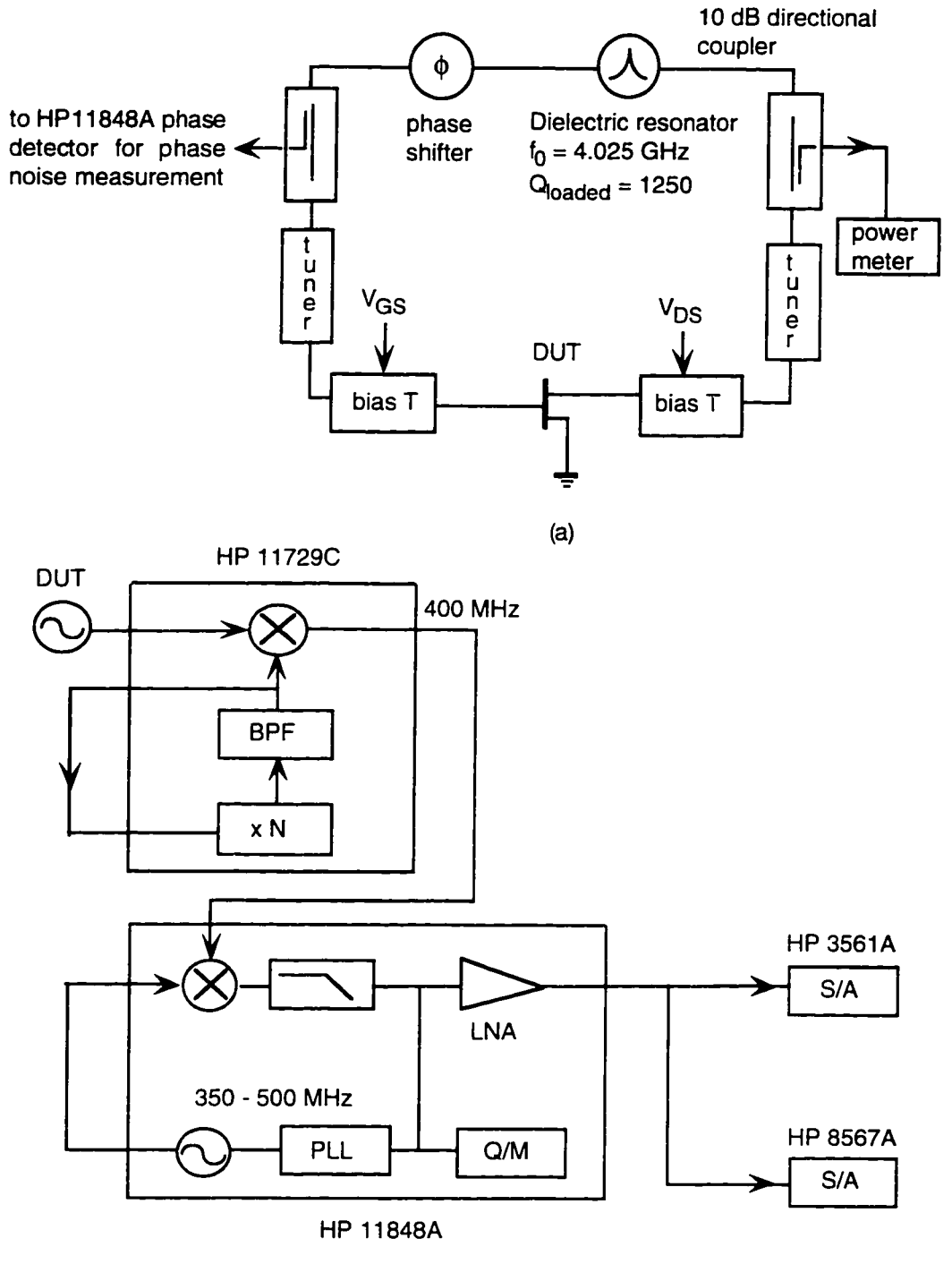


Figure 4.22. (a) DUT embedded oscillator circuit for phase noise measurements. (b) HP 3048A Phase Noise Measurement System block diagram.

MHz, which is the local oscillator frequency range in the HP 11848A, Phase Noise Interface. At this stage the IF signal is phaselocked and amplified. The signal is then directed to the Dynamic Signal Analyzer (FFT Display) HP 3561A, which can display the frequencies between 0.01 Hz - 100 kHz. For larger offset frequencies, the HP 8567A Spectrum Analyzer is used.

4.7.1. Measurements on Devices with MOCVD InP Passivation

Figure 4.23 (a) depicts the measured phase noise on device 12.4 (w = 400 μm, L_g = 0.4 μm) on the sample R951206C, with MOCVD overgrown p$^-$-InP passivation (run no. R960130D). Single sideband noise power densities of -40 dBc/Hz at 100 Hz offset, -67 dBc/Hz at 1 kHz offset, and -95 dBc/Hz at 10 kHz offset from the carrier are obtained. To provide for a general comparison, phase noise values from a collection of reference oscillators are also summarized in Table 4.2 [6]. Figure 4.23 (b) shows the phase noise measurement on device 15.1 (w = 500 μm, L_g = 0.4 μm) on the same sample. This device is noisier with single sideband noise power density readings of -33 dBc/Hz at 100 Hz offset, -62 dBc/Hz at 1 kHz offset, and -90 dBc/Hz at 10 kHz offset from the carrier.

The baseband low frequency noise behavior of the devices were measured by directly feeding the DUT output into the LNA input in the HP 11848 Phase Noise Interface. Figure 4.24 shows the instrumentation and the equivalent circuit diagram for baseband measurements. The input to the LNA in the HP 11848 has a maximum peak voltage rating of 1 V, and a frequency range of dc - 40 MHz. Therefore, a Stanford Research Systems SR 560 Low Noise Preamplifier was used to provide for a high impedance dc block by selecting a gain setting of unity and a passband of 1 Hz - 1 MHz. The bias to the devices was applied through a large inductance of 2.8 H. The measured noise density is expressed in dBv/Hz.

Figure 4.25 shows low frequency drain noise measurements from the two devices with MOCVD InP passivation. We observe that the measured noise voltage spectrum has a slope of -8.3 dB/decade, signifying a frequency variation in the form of $1/f^{0.83}$, slower than an absolute $1/f$ dependence. Variations of the low

[6] The resonating elements, the circuitry and the frequencies of oscillation are varied in these references. The reported phase noise figures contain not only the upconverted intrinsic baseband noise of the devices, but also the contributions of the particular circuitry used. The listings should therefore be consulted for general reference only, and not for individual comparisons.

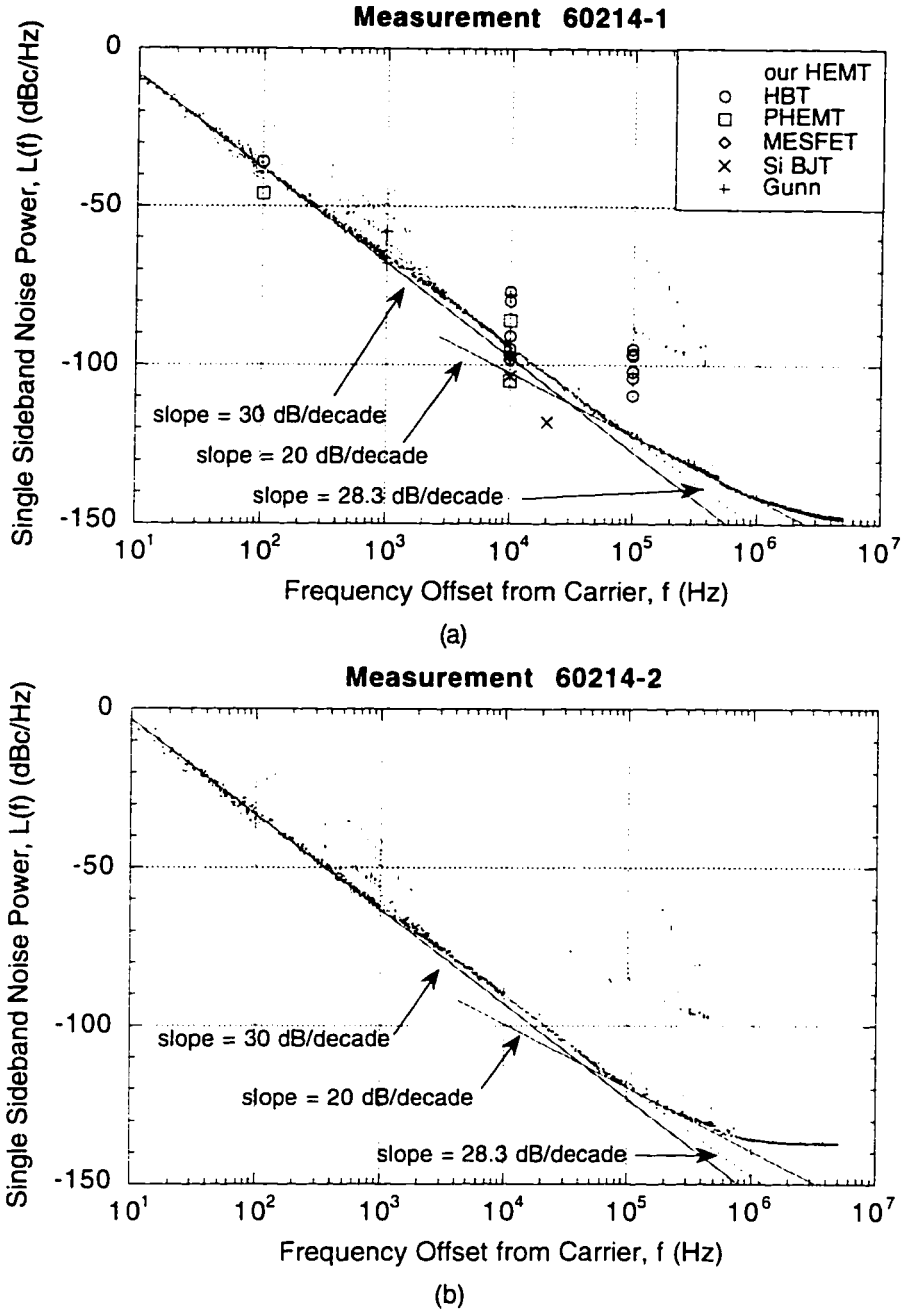


Figure 4.23. Phase noise measurements of the sample R9510206C, (a) chip 12.4, at the bias conditions of V_{GS} = -0.6 V, V_{DS} = 2.0 V, I_D = 25 mA (w = 400 μm, L_g = 0.4 μm) and P_b = -8.62 dBm along with reference values for oscillators from Table 4.2, and (b) chip 15.1 at the bias conditions of V_{GS} = -0.5 V, V_{DS} = 2.0 V, I_D = 30 mA (w = 500 μm, L_g = 0.4 μm) and P_b = -7.35 dBm. The dotted line in both graphs represents the best fit to the data, and has a slope of -28.3 dB/decade.

Device	f_0 (GHz)	f_m (kHz)	$L(f_m)$ (dBc/Hz)	$L(f_m)$ @ 4 GHz	Note	Year	Ref. No.
InP HBT	40	100	-84	-104	VCO	1995	[20]
InP HBT	62	100	-78	-102	VCO	1995	[20]
InP HBT	95	100	-82	-109.5	DRO	1995	[20]
GaInP/GaAs HBT	7.8	10	-85	-90.8	YTO	1994	[21]
GaAs HBT	4	10	-95	-95	DRO	1986	[22]
GaAs HBT	15.5	10	-65	-76.8		1988	[23]
GaAs HBT	29	100	-80	-97	VCO	1988	[24]
GaAs HBT	12.3	10	-70	-79.8	DRO	1989	[25]
GaAs HBT	15.6	100	-85	-96.5	VCO	1992	[26]
GaAs/GaInAs PHEMT	5.6	0.1	-43	-45.9		1995	[27]
GaAs HBT	5.6	0.1	-33	-36.9		1995	[27]
GaAs HBT	20	100	-81	-95	VCO	1995	[3]
Si diodes	7.6	10	-131	-136.6	Hi Q	1995	[28]
GaAs MESFET	4	10	-97	-97	Q=160	1993	[29]
GaAs/GaInAs PHEMT	4	10	-86	-86	Q=160	1993	[29]
GaAs/GaInAs PHEMT	4	10	-105	-105	Q=160, T=110 K	1993	[29]
Si BJT	18	20	-105	-118	YTO	1985	[30]
Si BJT	6	10	-100	-103.5	DRO	1981	[31]
GaAs MESFET	6	10	-95	-98.5	DRO	1981	[31]
Gunn	10	1	-50	-58		1992	[32]
Gunn	10	10	-70	-78		1992	[32]
Gunn	10	1	-60	-68		1978	[33]
Gunn	10	10	-90	-98		1978	[33]

Table 4.2. A collection of references with various phase noise performances. These data are plotted as reference in Figure 4.23 (a) as well. f_0 refers to the oscillator center frequency and f_m, to the offset frequency. $L(f_m)$ is the single sideband noise spectral density. To convert the published data to noise power with respect to our oscillator frequency of f_c = 4.025 GHz, 20 log (f_{pub}/f_0) is subtracted from the reported phase noise measurements (a small frequency modulation is assumed) [34]. Some VCOs are tuned by bias, whereas others utilize varactor tuning.

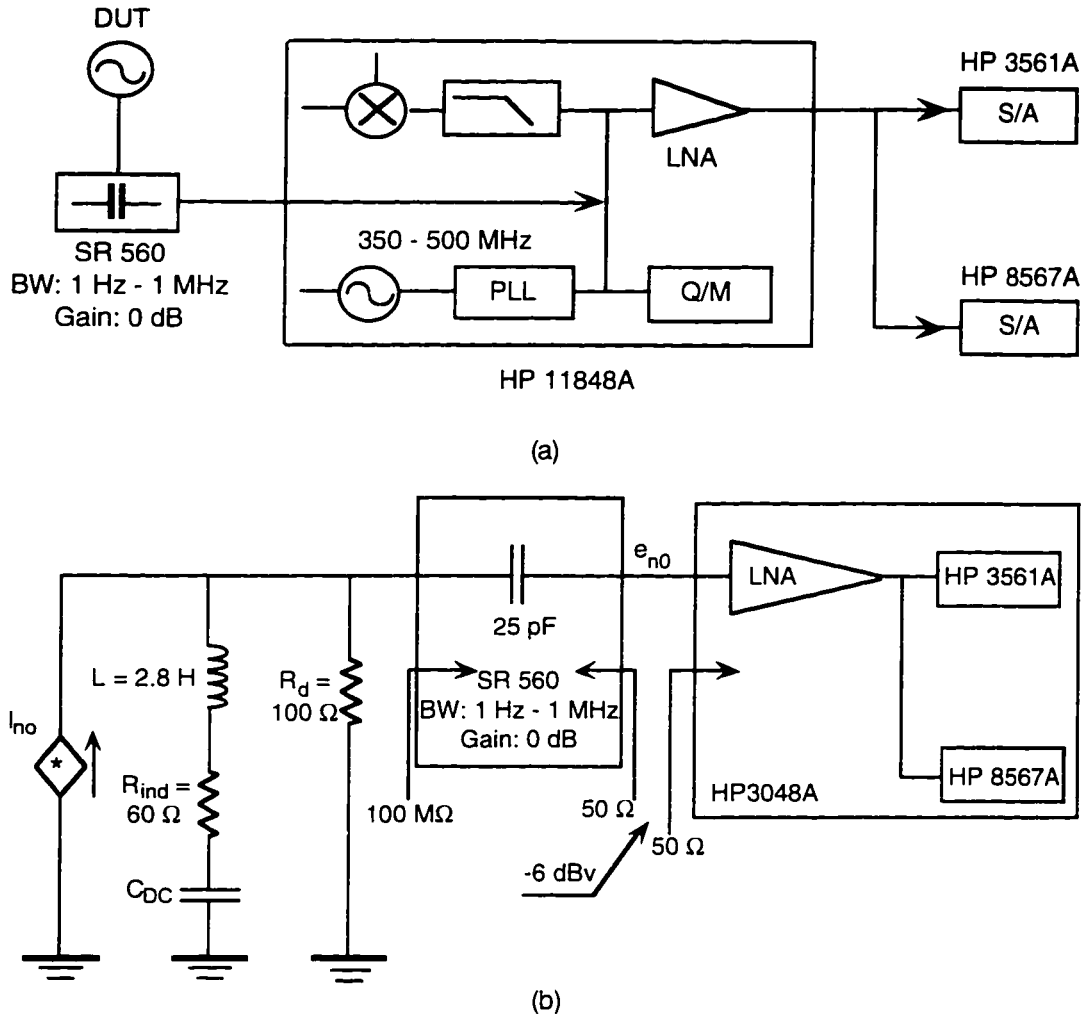


Figure 4.24. (a) Instrumentation diagram for making low frequency baseband noise measurements. (b) Circuit diagram for the low frequency noise measurements.

frequency noise spectrum in the form of $1/f^{\alpha}$, with α in the range of 0.6 to 1.0 has previously been observed by other researchers as well [4]. The slope of -8.3 dB/decade corroborates to the -28.3 dB/decade slope that is observed in Figure 4.23 in the phase noise measurements in that it signifies a frequency independent upconversion factor, K_{FM}, as has been observed before in HBTs [35], and MESFETs and HEMTs [36]. The following relationship between the phase noise spectrum, $L(f)$, and the input referred baseband noise spectrum, $S_v(f)$, clarifies this observation [35, 37]:

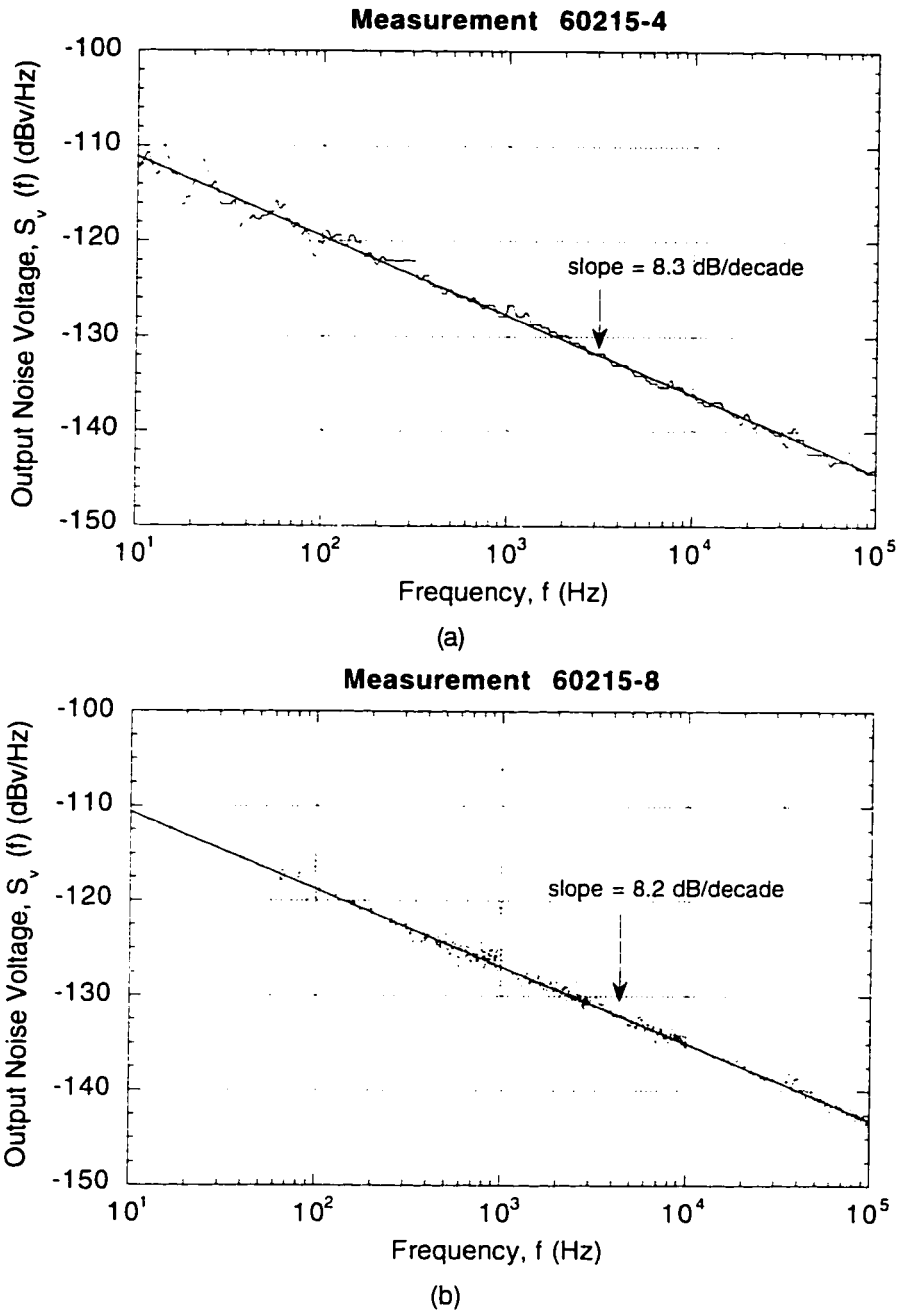


Figure 4.25. Low frequency output (drain) noise measurements on sample R951206C (with MOCVD InP overgrowth), (a) chip 12.4 (w = 400 μm, L_g = 0.4 μm), at the bias conditions of V_{GS} = -0.6 V, V_{DS} = 2.0 V, I_D = 26 mA (the spurs have been eliminated) and (b) chip 15.1 (w = 500 μm, L_g = 0.4 μm) at the bias conditions of V_{GS} = -0.5 V, V_{DS} = 2.0 V, I_D = 35 mA.

$$L(f) = 10 \log \left(\frac{S_v(f) K_{FM}^{\ 2}}{2f^2} \right). \tag{4.1}$$

The upconversion factor for the devices can be estimated using (4.1). First, the output baseband noise voltage spectrum, $S_{ov}(f)$, has to be referred to the input voltage noise spectrum, $S_{iv}(f)$, through [4]

$$S_{iv}(f) = S_{ov}(f) - 20 \log G + 6 \text{ dB}, \tag{4.2}$$

where

$$G = \frac{g_m R_L R_{DS}}{R_L + R_{DS}} \tag{4.3}$$

is the gain of the device, and the 6 dB term accounts for the voltage division between the output of the DUT and the input of the LNA. From Figure 4.17 (b), we see that at V_{GS} = -0.6 V and V_{DS} = 2.0 V, g_m = 160 mS/mm and g_0 = 5 mS/mm or R_{DS} = 200 Ω·mm. Recalling that w = 400 μm for the device 12.4, and R_L = 100 Ω, the device gain is calculated to be G = 5.3 ≡ 14.5 dB. Assuming no dispersion in the g_m and R_{DS} with respect to frequency, the baseband gate noise spectrum can thus be approximated as 8.5 dB lower than what is plotted in Figure 4.25 (a). Similarly for the device 15.1 (w = 500 μm) at V_{GS} = -0.5 V and V_{DS} = 2.0 V, g_m = 175 mS/mm and g_0 = 5.2 mS/mm. Its gain is then calculated to be G = 6.9 ≡ 16.8 dB. Figure 4.26 shows the input referred baseband noise spectral densities for these two devices. An interesting observation is that the noise spectral density for the 500 μm device is about 1 dB lower than that of the 400 μm device. This difference is essentially the same as the ratio of the widths of the two devices, 10 log (500 μm / 400 μm) = 0.9 dB. This observation is reassuring since the gate noise spectral density in FETs is inversely proportional to the gate width [38]. Finally the upconversion coefficient K_{FM}, for the device 12.4 (w = 400 μm) is calculated to be 6.9 MHz/V, and for the device 15.1 (w = 500 μm), 12 MHz/V.

There is a range of data on the low frequency noise performance of various FETs in the literature. We document in Table 4.3 pertinent figures of merit for a list of publications, from lattice matched GaInAs/InP HEMTs to GaAs MESFETs for reference purposes. It should be kept in mind, however, that an accurate comparison should be made among devices with similar characteristics and parameters.

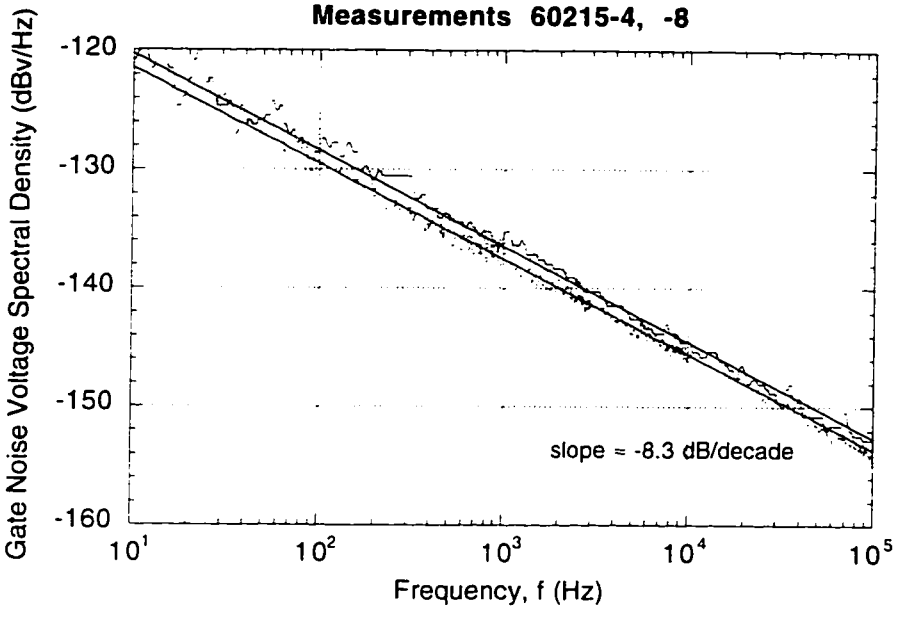


Figure 4.26. Input referred noise spectral densities for devices 12.4 (w = 400 μm) (upper, connected points), and 15.1 (w = 500 μm) (lower, scattered points). The straight lines represent the best fits to the data, and have slopes of -8.3 dB/decade.

4.7.2. Measurements on Devices with MBE AlInAs Passivation

Figure 4.27 shows phase noise measurements for the sample R951206C-edge, device 11.1, which is passivated by undoped AlInAs grown at standard temperature by MBE. It appears that the phase noise is lower at biases for which I_D is closer to I_{DSS}. The operating current has been reported to determine the upconversion factor of the low frequency noise to phase noise [27]. In our case, we see that for the lowest phase noise measurement, the slope of the curve is -28.5 dB/decade, the same as what was observed for the MOCVD passivated samples. The slopes of the middle and the top noise curves in Figure 4.27 (b) are -29.1 and -30 dB/decade respectively.

4.8. Summary

Based on the regrowth technology for achieving non-alloyed, low resistance highly n^+ doped source and drain contacts, we have demonstrated the

Device/ Reference	I_{DSS} (mA/mm)	g_m (mS/mm)	L (μm)	w (μm)	V_{DS} (V)	V_{GS} (V)	I_{DS} (mA/mm)	$\|e_n\|^2$ (dBV/Hz)
This work (12.4)	270	160	0.35	400	2.0	-0.6	65	-136.5
GaInAs/InP HEMT (x=0.65) (x=0.53) [4]	500 530	510 450	0.7 0.7	150 150	1.5 1.5	for max g_m	240 220	-133.3 -131.2
GaInAs/InP HEMT [39]	400	~700	0.15	50		0.0	170	-134.0
GaAs HEMT [40]			0.25	150		-0.4	149	-134.2
GaAs SL-HEMT [29]	255	550	0.8	200	2.0			-139.5
GaAs MESFET [38]	160		0.8	400	2.6	-0.7	35	-137.7
GaAs MESFET [36]	90		0.5	300	3.0	0.0		-138.4

Table 4.3. A collection of references with low frequency noise performances of various FETs. The e_n's are quoted for f = 1 kHz and are normalized to a device width of 400 μm.

feasibility of HEMTs with epitaxial surface passivation. The implementation of epitaxial overgrowth coupled with the regrown contacts enabled the following: (i) fabrication of devices with a single level of metalization for all the source, drain, and gate contacts, (ii) elimination of recess etching as lower access region resistance is guaranteed by the reduced surface depletion due to the overgrowth in the access regions, and (iii) devices with reasonably low low-frequency and phase noise characteristics. In particular, for the MOCVD InP passivated devices with gatelengths of 0.5 μm, g_m values of 220 mS/mm were obtained, along with a full channel current density of 280 mA/mm. The f_T and f_{max} for these devices were around 20 and 50 GHz respectively. For the MBE AlInAs passivated devices with $L_g \approx 0.9$ μm, we obtained g_m = 170 mS/mm with $I_{D,\,full}$ = 210 mA/mm. The frequencies of merit for these devices were f_T = 25 GHz and f_{max} =70 GHz.

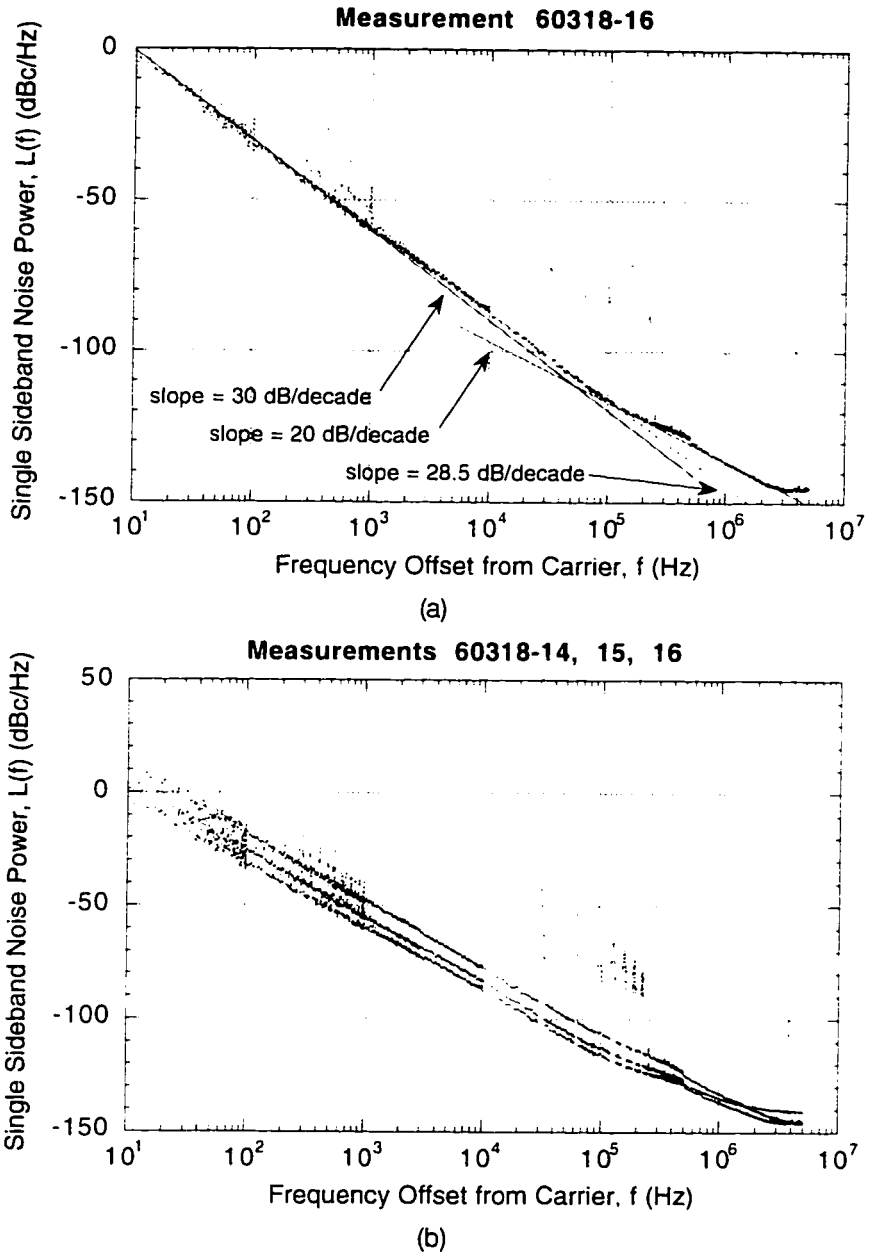


Figure 4.27. (a) Phase noise spectrum of the device 11.1 (w = 500 µm, L_g = 0.9 µm) from sample R951206C-edge at V_{GS} = 0 V. (b) Phase noise spectra for the same device at three different bias points:

Measurement	V_{GS} (V)	I_D (mA)	V_{DS}	P_b (dB)
60318-14 (top)	-0.4	18	1.5	-12
60318-15 (middle)	-0.2	25	2.0	-10
60318-16 (lower)	0	42	2.0	-12

We attribute the somewhat low current densities to as yet unoptimized process parameters such as etch depth variations before overgrowth and interface states at the overgrowth interface. With an optimized process, however, HEMTs fabricated with surface passivation overgrowth will offer higher current levels compared to HEMTs with recessed gates made from the same underlying material because the access region in the overgrown HEMT will continue to provide the necessary charge for carrying current at more positive gate biases.

The low frequency noise exhibited by all of these devices followed frequency relationships that varied from $1/f^{0.83}$ to $1/f$ depending on the device parameters and the bias applied. A low single sideband noise power density of -95 dBc/Hz at 10 kHz offset from the carrier frequency of 4.025 GHz was obtained from a device (w = 400 μm, L_g = 0.4 μm) passivated with MOCVD overgrown InP. For the same device, a baseband gate noise spectral density of -136.5 dBv/Hz was obtained. The devices had frequency independent upconversion factors. The phase noise and the low frequency noise performance of these devices compare favorably to the data published in the literature. Further control experiments have to be carried out to conclusively demonstrate the impact of epitaxial passivation on noise characteristics.

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Summary and Suggestions for Future Work

In this dissertation, we have introduced a new approach for making FETs by utilizing developments in materials technologies, whereby processing and growth are continuously interleaved. The realized InP based HEMTs should offer a reproducible, uniform, and reliable technology for various high frequency and low noise applications such as receivers, transmitters, OEICs and MMICs. Selective regrowth was used twice to achieve the devices: once to make low resistance ohmic contacts, and second time to passivate the surface epitaxially. The implementation of epitaxial overgrowth coupled with the regrown contacts has enabled the following: (i) fabrication of devices with a single level of metalization for all the source, drain, and gate contacts, (ii) elimination of gate recess etching, and (iii) devices with suppressed low-frequency and phase noise characteristics.

Having recognized that ohmic contacts play an important role in today's high frequency and low noise transistors, we started our work by searching for a reliable, stable and versatile ohmic contact technology. An alternative that was considered early on was a contact scheme created by implantation of donor species. However, the species have to be activated through high temperature anneals, which brought forward the questions of what would happen to the device structure and its electrical parameters such as mobility (μ) and sheet carrier concentration (n_s) of electrons. We performed a series of annealing experiments on AlInAs/GaInAs/InP HEMT structures and observed reductions in both μ and n_s. These reductions were more significant when the devices were measured at low temperatures. We thus concluded that ohmic contact formation by dopant implantation and activation is not a viable method particularly for applications which require stable device characteristics not only at room temperatures, but at cryogenic temperatures as well.

We therefore concentrated our efforts in investigating highly doped regrown contacts on InP based FETs. Regrown contacts have inherent advantages over other contact schemes in that (i) they enable non-alloyed contacts, which improves device stability and reliability, (ii) single level metal fabrication of FETs is possible, where the gate, source and drain metalizations are carried out at the same time, and perhaps most importantly, (iii) they create an enabling technology, which makes it possible to achieve good ohmic contacts to semiconductor devices regardless of the channel material. We thus developed a

technology for non-alloyed ohmic contacts with highly doped regrowth of GaInAs on various GaInAs channel devices including AlInAs/GaInAs/InP HEMTs. For the regrowths done on HEMTs with Si doping in the AlInAs donor layer, we found that, if the doping concentration in the regrown GaInAs is low ($n = 1.5 \cdot 10^{18}$ cm^{-3}), and HF solutions are employed in the processing steps, there exist instabilities in the contacts at higher temperatures. We attributed this to the passivation of Si dopant atoms in AlInAs by fluorine. However, we achieved temperature stable ohmic contacts with a contact resistance of 0.1 $\Omega \cdot mm$ regardless of the samples' exposure to HF when higher doping ($n = 7 \cdot 10^{18}$ cm^{-3}) was incorporated in the regrowth process.

Based upon this regrowth technology for achieving non-alloyed, low resistance n^+ doped source and drain contacts, we then demonstrated the feasibility of HEMTs with epitaxial surface passivation, where we studied the overgrowth of InP by MOCVD and AlInAs by MOCVD and MBE. There are advantages in avoiding free surfaces near the III-V active channels: (i) traps associated with the surface can result in frequency dispersion of device characteristics and (ii) free surfaces can yield to degraded low frequency noise (such as 1/f noise) behavior, which is known to arise from the variations in the occupancy of bulk and surface trap centers. Therefore, we also examined low frequency and phase noise characteristics of the fabricated devices and found that they compared favorably with the existing data in the literature.

The demonstrated work should lead to many exciting possibilities in both device physics and fabrication methods. Different materials (regular or low temperature grown InP, AlInAs, or GaAlInAs), doping types (n or p) and concentrations can be experimented with for achieving an optimum epitaxial passivation design. Effects of each of these parameters on low frequency noise characteristics can be examined in order to be able to point to various sources of noise in the transistors. The effects of the passivation on breakdown characteristics can be investigated. The regrowth for contacts can be applied to other semiconductor devices, such as HBTs, or devices in other material systems, such as GaN, where a traditional contact scheme is highly resistive.

On the materials and processing side, further work can be undertaken to grow oxygen free AlInAs in the MOCVD system and to achieve a more repeatable etch and regrowth technology for the MBE system. Studies can be performed to achieve higher doping concentrations for MOCVD regrown contacts with improved selectivity of growth over masked areas.

Appendix 1

Process Notes

The device fabrication sequence was summarized in Chapter 4 (see Figure 4.7). The detailed process sequence follows:

(i) *SiO_2 deposition*

1. Obtain wafer from MBE. Cleave a small piece from the wafer and perform a Van der Pauw measurement for electron mobility and sheet charge data.
2. Clean sample: 2 min. each in acetone and isopropyl alcohol (IPA), blow dry.
3. Put sample in PECVD chamber for SiO_2 deposition. Enclose a Si sample to monitor thickness.
   - After chamber pumpdown, wait for ~ 10 min. for sample dehydration.
   - Use the SiO20 recipe to deposit a thickness of 2000 Å. The parameters are:
     T = 250°C, P = 0.9 Torr, SiH_4 flow: 100 sccm, N_2O flow: 300 sccm, rf power = 20 W (constant power operation, corresponding dc voltage = 13-15 V)
4. Measure thickness and index on the monitor Si piece with the Ellipsometer.

(ii) *Image reversal lithography*

1. Spin HMDS at 6 Krpm.
2. Spin 5214E at 6 Krpm, 40 s.
3. Soft bake at 100°C on hot plate for 1 min.
4. To remove resist edge bead, use a square mask, expose twice, two sides at a time, 1.5 min. each.
5. Develop in 1:4 AZ 400K:H_2O, for 1 min.
6. Expose image for 12 s, at 7.5 mW/cm^2.
7. Post-exposure bake at 110°C on hot plate for 1 min.
8. Flood expose for 1 min.
9. Develop in 2:11 AZ 400K:H_2O for 40-50 s.
10. Oxygen plasma ash at 300 mTorr, 100 W, 15 s.

(iii) *SiO_2 RIE etch*

1. Clean the RIE chamber before deposition:
   - O_2 flow at 25 sccm, P = 100 mTorr, dc self bias = -500 V, rf power = 175 W, for 10-20 min.

2. Place the sample and the Si monitor piece inside the chamber. Align the laser and the detector off of the Si piece for maximum readout. Etch with:
   - $SF_6/Ar/O_2$ 10/10/1 sccm, P = 25 mTorr, dc self bias = -100 V, rf power = 30 W, for required duration.

   The etch time is determined by monitoring the detector output during etch and by allocating for some overtime to account for possible etch nonuniformities across the actual wafer. Figure A.1.1 shows a typical readout profile. In this particular case, the etch seems to have completely gone through the SiO_2 layer by 7.5 min. An additional 2 min. were allocated, which brought the overall etch time to 9.5 min.
3. Etch clean with 1:10 BHF:H_2O for 10 s, rinse with DI water for 2 min.
4. Iterative cycles of acetone soak and O_2 plasma ash (300 mTorr, 100 W, 1-2 min.) until the resist is completely cleared.

(iv). Wet etch for regrowth

1. Etch clean for 10 s in 1:10 $NH_4OH:H_2O$, rinse in DI water for 2 min.
2. Etch in 3:1:50 $H_3PO_4:H_2O_2:H_20$ solution for 15-30 s, stirring the solution at 80-120 rpm. The goal here is to etch to about the middle of the GaInAs in the channel for run-to-run consistency. The colors of the layers are also monitored as they are being etched. The following color variations are typically observed with respect to etch time:

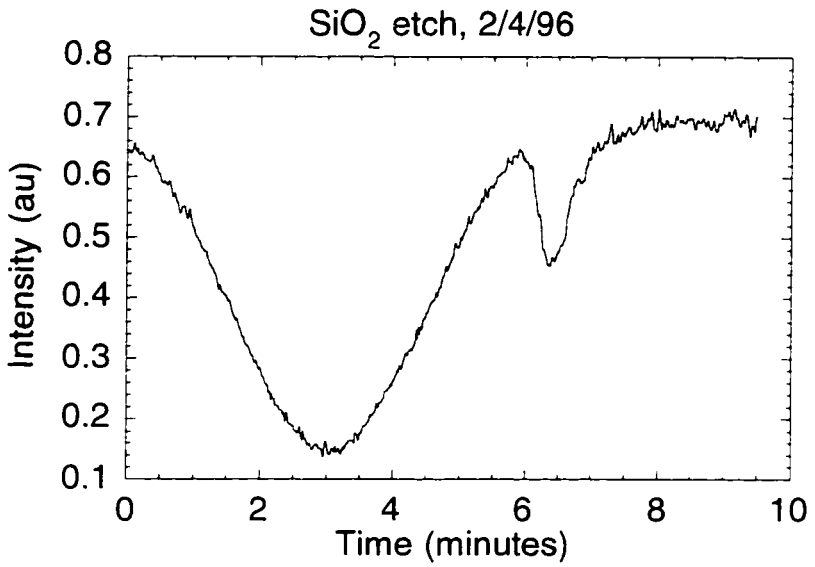

Figure A.1.1. Optical detector readout during RIE etching from a Si monitor piece with SiO_2 on top (initial t = 1950 Å, n = 1.447). The Si surface appears at 7.5 min. after which the etching is continued for another 2 min.

- ~3 s: dark purple (GaInAs cap etched, AlInAs Schottky layer appears).
- 10-15 s: gray (AlInAs donor layer is etched through, the GaInAs channel appears).
- 20-30 s: bright gray (in the middle of the GaInAs channel).

3. Rinse in DI water for 1 min., blow dry.

(v). MOCVD regrowth

1. Immediately carry the sample to the MOCVD room and load it in the reactor along with a blank InP piece for thickness and carrier concentration measurements.
2. Carry out atmospheric pressure regrowth for n^+ GaInAs contacts as described in Chapter 3. A regrowth thickness of 3000-4000 Å seems to give optimal results (growth rate ≈ 12 Å/s for the particular mask used – the larger the masked to unmasked area ratio, the faster the growth rate). GaInAs is graded to InAs to achieve low contact resistance over ~75 Å (10 s growth time) and capped with an InAs layer of 10-15 Å.

(vi). E-Beam lithography for gate, source and drain oxides

1. Due to atmospheric pressure regrowth, there is polycrystalline GaInAs deposition across the masked SiO_2 surface as well. Etch and clear the areas surrounding the E-beam registration crosses (see Section A.2.5 for details).
2. Perform E-beam lithography as described in Appendix 2.
3. Descum resist by oxygen plasma at 300 mTorr, 50 W, for 10 s.

(vii). SiO_2 evaporation and liftoff

1. Surface oxide clean in 1:10 BHF:H_2O for 5 s, rinse in DI water for 2 min. (NH_4OH solutions are not used as they delaminate E-beam resists).
2. Load the sample in the E-Beam evaporator immediately. Evaporate 3000-5000 Å of SiO_2, at a rate of 3-4 Å/s with a quartz cylinder as the target. It is necessary to do a slow and uniform evaporation for optimum results.
3. Liftoff in very gently boiling methylene chloride (CH_2Cl_2) at 35-40°C.
4. Soak in acetone to clean any resist residue. Rinse in IPA, blow dry.

(viii). Overgrowth of the epitaxial passivation

1. Etch clean in 1:10 NH_4OH:H_2O for 10 s, rinse in DI water for 2 min.
2. (a) For MOCVD overgrowth of InP, etch the GaInAs cap away in a 3:1:50 H_3PO_4:H_2O_2:H_2O solution for 3-5 s, rinse with DI water. Load it in the reactor immediately.

(b) For MBE overgrowth, the cap is etched in situ. Hand the sample over to MBE system for etch and overgrowth of GaInAs.

3. Remove/liftoff (MOCVD/MBE) the SiO_2 mask in 1:10 BHF:H_2O solution for 1-2 min., rinse in DI water for 2 min.

(ix). E-beam lithography and metalization

1. Perform E-beam lithography registering and aligning to the previous gate level. The footprint should be wide enough (~1 μm) to cover the gate opening.
2. Descum resist by oxygen plasma at 300 mTorr, 50 W, for 10 s.
3. Surface oxide clean in 1:10 BHF:H_2O for 5 s, DI rinse for 2 min.
4. Load sample in the E-beam evaporator immediately. Evaporate 500 Å Ti, 500 Å Pt, 3000 Å Au with rates of 3-5 Å/s.
5. Liftoff in very gently boiling methylene chloride (CH_2Cl_2) at 35-40°C.
6. Soak in acetone to clean any resist residue. Rinse in IPA, blow dry.

(x) Isolation mesa lithography

1. Clean and dehydration bake sample at 120°C oven for 10 min.
2. Spin HMDS at 6 Krpm. Spin AZ 4110 at 6 Krpm for 40 s.
3. Soft bake at 100°C hot plate for 1 min.
4. Expose twice for edge bead removal using the square mask, 1.5 min. each.
5. Develop in 1:4 AZ 400K:H_2O for 50 s.
6. Align and expose image for 12-14 s at 7.5 mW/cm^2.
7. Develop in 1:4 AZ 400K:H_2O for 50 s.
8. Oxygen plasma descum at 300 mTorr, 100 W for 15 s.

(xi) Isolation mesa etch

1. Hard bake resist at 120°C oven for 10 min.
2. Etch clean in 1:10 NH_4OH:H_2O for 10 s, rinse in DI water for 2 min.
3. Figure A.1.2 shows the cross section of the layers to be etched before mesa

overgrown InP or AlInAs	500-1000 Å
polycrystalline GaInAs	3000-4000 Å
SiO_2 mask	2000 Å
Device epi layers	3300 Å

InP substrate

Figure A.1.2. Cross section of the layers outside of the active device area before mesa isolation. The polycrystalline GaInAs is due to the regrowth performed at atmospheric pressure.

isolation. For devices with MOCVD overgrowth, the top InP has to be removed first:

- 1 min. 3:1 $HCl:H_2O$ at -3 – -1°C, stirring the solution at 120 rpm.

The following is the same etch sequence for devices with both InP and AlInAs overgrowth:

4. 3-4 min. etch in 3:1:50 $H_3PO_4:H_2O_2:H_2O$ solution, stirring at 120 rpm. Etch until the SiO_2 appears from underneath. Rinse with DI water.
5. Remove SiO_2 mask in 1:10 $BHF:H_2O$ until clear (3-4 min.). Rinse with DI water.
6. Etch the epitaxial material in 3:1:50 $H_3PO_4:H_2O_2:H_2O$ solution, stirring at 120 rpm for 3-4 min. While etching the following color changes are observed:
   - 3-5 s: dark purple (GaInAs cap etched, AlInAs Schottky layer appears).
   - 10-15 s: gray (AlInAs donor layer is etched through, the GaInAs channel appears).
   - 40-50 s: purplish (GaInAs channel is etched, the AlInAs buffer appears).
7. Check isolation between devices. The isolation resistance should be on the order of MΩ. Also check device gate pad to source and drain isolation.
8. Remove resist in acetone, rinse with IPA, blow dry. Assure gate feed undercut by SEM inspection (see Figure 4.12).

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Appendix 2

Electron-Beam Lithography at UCSB

A.2.1. E-Beam System

Compared to optical lithography, E-beam lithography offers many advantages: excellent level-to-level registration, very high resolution and easy pattern modifiability because of direct-write capability. Some disadvantages are increased equipment complexity and the extended time it may take to finish an exposure since each pattern has to be written individually. Although for simple gate pattern direct write this may not be of much concern, the exposure time does increase significantly if larger areas such as contact pads are included in the exposure pattern, as evidenced earlier in Chapter 4.

For our experiments, we have used the IBM Vector Scan 1 (VS-1) E-Beam Lithography System, which first started its operation in 1976 at IBM Almaden Research Laboratory in San Jose. The system was donated to UCSB in 1990 and was operational shortly thereafter. Figure A.2.1 shows the block diagram of the VS-1 System. The electron beam is deflected onto the workpiece by the deflection amplifier according to the instructions that come from the pattern generator and the digital to analog converter. Before it hits the sample surface, the electron beam passes through complex "optics", where it is aligned and focused. Figure A.2.2 shows the schematic of the electron column. The technical system parameters are summarized in Table A.2.1.

Source	ZrO/W thermal field emission (25 kV)
Resolution	d_p ~ 10-45 nm (I_b ~ 1-25 nA), $J \sim 10^3 - 10^4$ A/cm^2
Deflection Aberrations	d_p ~ 13 nm at 200 μm deflection (400 μm field)
Chip Size	Up to 40 x 40 mm^2 (400 μm subfield)
Noise	60 Hz: << 10 nm Low frequency mechanical: ~10-20 nm High frequency: < 4 nm (200 μm field)
Writing Speed	0.2-10 MHz (limited to 5 MHz by pattern generation and deflection hardware)
Overlay Accuracy	60 nm (3σ)
Proximity Correction	Selective dose assignment based on N-Gaussian Model

Table A.2.1. FELS-3 system specifications.

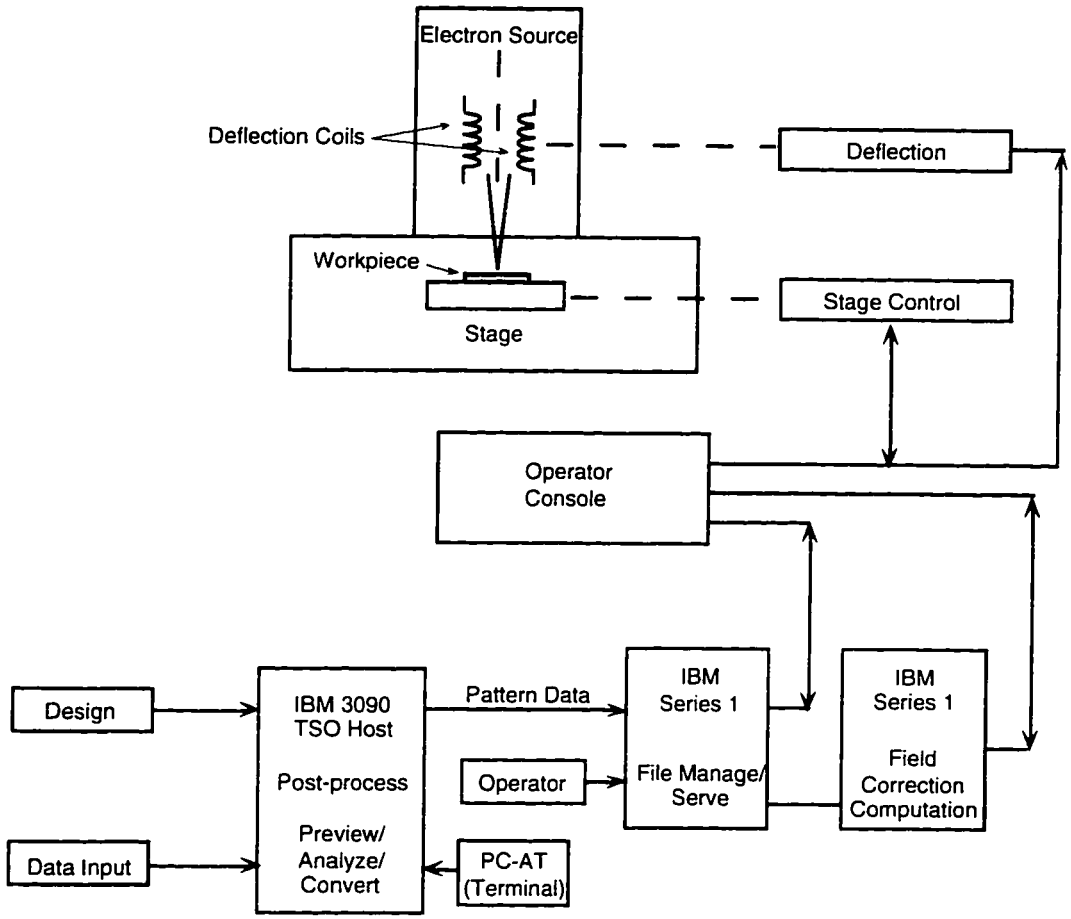


Figure A.2.1. Block diagram of the IBM Vector Scan 1 (VS-1) Electron Beam Lithography System.

A.2.2. E-Beam Pattern Preparation and Exposure Parameters

The IBM VS-1 system post-processor, Glives, accepts layouts in the GL-1 format. Masks can be prepared with any layout tool as long the patterns can be saved in the GDS format. The GDS data are then converted to the GL-1 format through a computer program. The Glives post-processor adjusts exposure parameters to correct for proximity effects based on the N-Gaussian model [1]. For our exposures, the following set of Gaussian parameters were used: α = 0.115, β = 2, η = 0.619

The total charge (dosage) per unit area that is deposited on the resist through exposure is given by

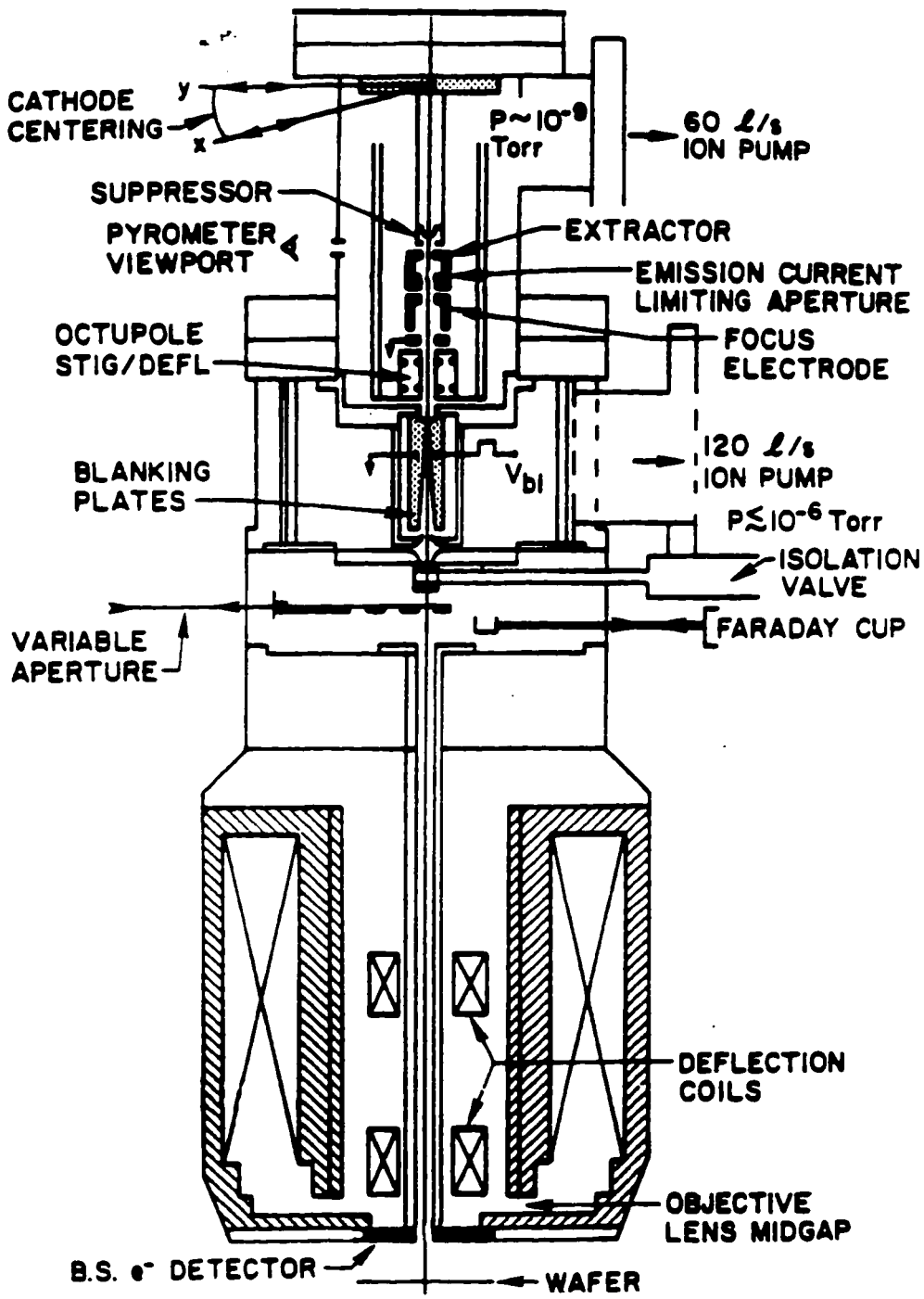


Figure A.2.2. The electron optics for the IBM VS-1 E-Beam Writer.

$$\text{Dose}\left(\frac{\mu C}{cm^2}\right) = 0.1\frac{I_b\,(\text{nA})}{f(\text{MHz})\,bs^2\,(\mu\text{m})}, \qquad \text{(A.2.1)}$$

where I_b is the electron beam current measured by the Faraday Cup, f is the pattern generator clock frequency, bs is the beam-step size, i.e., the amount the beam moves electronically between each pixel that is written, and in parentheses are given the units of each variable as they are entered into the equation. For example, if I_b = 1 nA, f = 1 MHz, and a field size of 1/20 μm/bs is used, the total base dosage per unit area will be

$$\text{Dose} = 0.1\frac{1}{1\,(0.05)^2} = 40\mu\text{m/cm}^2.$$

For direct write of gate level lithography, gate fingers with L_g = 0.1 μm were designed using a 1/20 μm/bs resolution. Exposure with the base dose of 40-50 μC/cm^2 (f = 1 - 0.8 MHz) yielded patterns with gatelengths in the range of 0.15-0.35 μm. The particular choice for the post-proximity Gaussian parameters as stated above enhances the base dosage in the gate fingers by another factor of ~3.5 compared to larger areas such as pads, whose overall dose remains close to the base dose after the proximity correction.

A.2.3. E-Beam Lithography Process

A tri-level resist process was developed using the positive radiation sensitive resist PMMA (poly-methyl-methacrylate) and its copolymer PMMA/MAA (poly[methylmethacrylate-co-methacrylic acid]). Table A.2.2 gives the trade product description. The MSDS for these resists are shown in Appendix 3. The resist is prepared for exposure as follows:

1. Spin PMMA at 4000 rpm. Hot plate bake at 180°C for 90 s. (t ≈ 2000 Å)
2. Spin PMAA at 6200 rpm. Hot plate bake at 180°C for 90 s. (t ≈ 5000 Å)
3. Spin PMMA at 6200 rpm. Hot plate bake at 180°C for 90 s. (t ≈ 1500 Å)

After exposure, the resist is processed through the following steps:

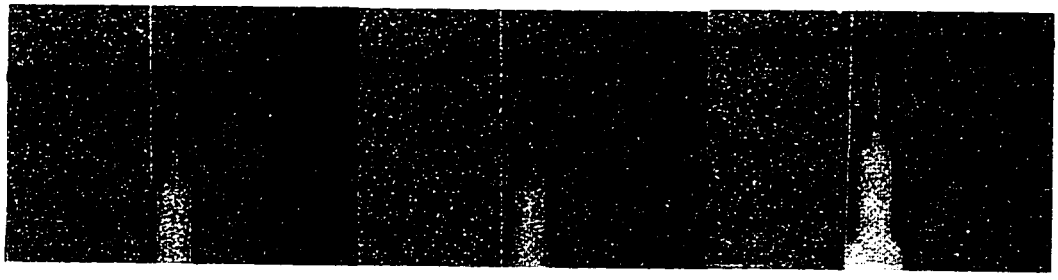
1. O_2 plasma ash, 300 mTorr, 100 W, 30 s.
2. Develop in 1:2 EGMEA[1]:Ethanol, at 21°C for 150 s.
3. IPA rinse for 30-45 s.

[1] $CH_3CO_2(CH_2)_2OC_2H_5$, Ethylene Glycol Monoethyl Ether Acetate; also known as (ethyl) cellosolve acetate, 2-ethoxy ethyl acetate, or ethyl glycol acetate.

Prod. No.	Description
M130505	Nano 495 PMMA A 5.5% (molecular weight 495, 5.5% solids in Anisole)
M410010	Nano MMA(17.5)MAA EL 10% (dissolved in ethyl lactate)[2]
Manufacturer:	Microlithography Chemical Corporation, 294 Pleasant Street, Watertown, MA 02172-2401. Tel: (617) 926 3322, Fax: (617) 926 2919.

Table A.2.2. Product descriptions for the E-Beam resists.

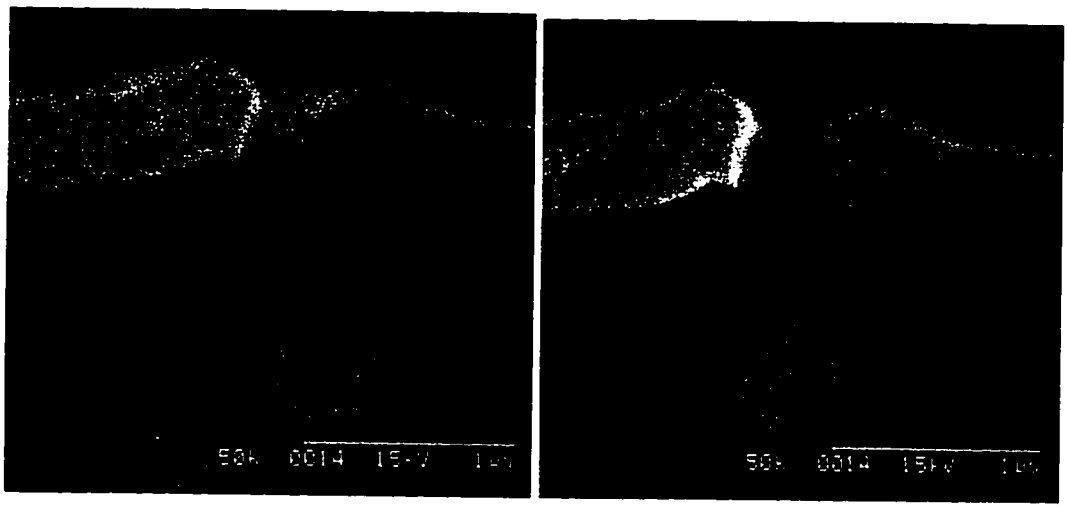
The PMMA/MAA copolymer is more sensitive to electron exposure than the PMMA itself [3]. When developed, this stack of resist layers naturally gives way to a bulb shape opening, which can be used as a successful liftoff profile for a mushroom shaped gate. However as spun, the top layer thickness is fairly close to the bottom layer's and therefore if the resist is developed immediately after exposure, the top opening comes out to be the same as the gate footprint. The initial oxygen plasma ash before developing removes part of the top sacrificial layer to control the extent of the top opening. Figure A.2.3 illustrates the evolution of the resist opening with respect to the O_2 plasma time. Figure A.2.4 shows the effect of the top opening on the evaporated metalization profile.



(a) (b) (c)

Figure A.2.3. Effect of the predevelopment oxygen plasma ash time on the outcome. Note the progressive opening of the top lip on the gatefeeds. (a) no plasma, (b) 10 s, (c) 20 s. The magnification is the same on all three photos.

[2] If a new process needs to be developed using these resists, it is advisable that polymer and copolymer solutions prepared in Anisole (safer solvent) be used instead of the former ethyl lactate solution. Experiments that were carried out with the MMA(17.5)MAA EL 10% copolymer and a PMMA 50K solution in Anisole showed intermixing of these layers. We have observed no intermixing of the PMMA 496K polymer and the EL 10% copolymer however, possibly due to the larger molecular weight (longer chain structure) of the polymer used [2].



(a) (b)

Figure A.2.4. SEM cross sections (with the resist still in place) after metalization, with (a) 20 s and (b) 30 s of O_2 plasma ashing before developing. Note the extra ear on the metal on the right due to wider top opening.

A.2.4. Comments About SiO_2 Evaporation and Liftoff

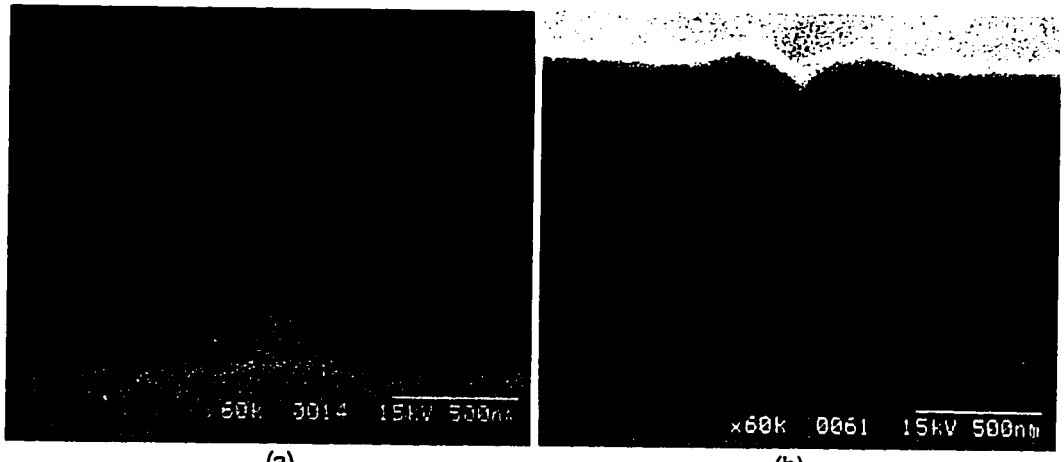
As mentioned earlier in Chapter 4, E-Beam lithography was used to place dummy SiO_2 gates before MOCVD or MBE regrowth of epitaxial passivation. The first lithography results were surprising, however, in that the lifted-off oxide had a triangular shape rather than the expected T shape (see Figure 4.10). There are two apparent reasons for this occurrence:

(i) To observe the cross-sectional resist profiles after development, a small piece of the sample was always cleaved. Because the Hitachi SEM in the clean-room does not have high enough resolution at low voltages, a hummer was used to deposit a 100-200 Å thick layer of gold so that the sample could be observed at intermediate voltages without charging. During the deposition of gold, however, the hummer apparently sputtered some of the resist, yielding deceptive profiles for the subsequent evaporation step. Figure A.2.5 shows this drastic effect.

(ii) Evaporated SiO_2 gathers and closes up on the top resist opening a lot faster than evaporated metal. Figure A.2.6 shows this behavior. For a better oxide profile such as shown in Figure A.2.7 (a), and a successful liftoff, one therefore needs to pay closer attention to the development procedure and the lithographic profiles.

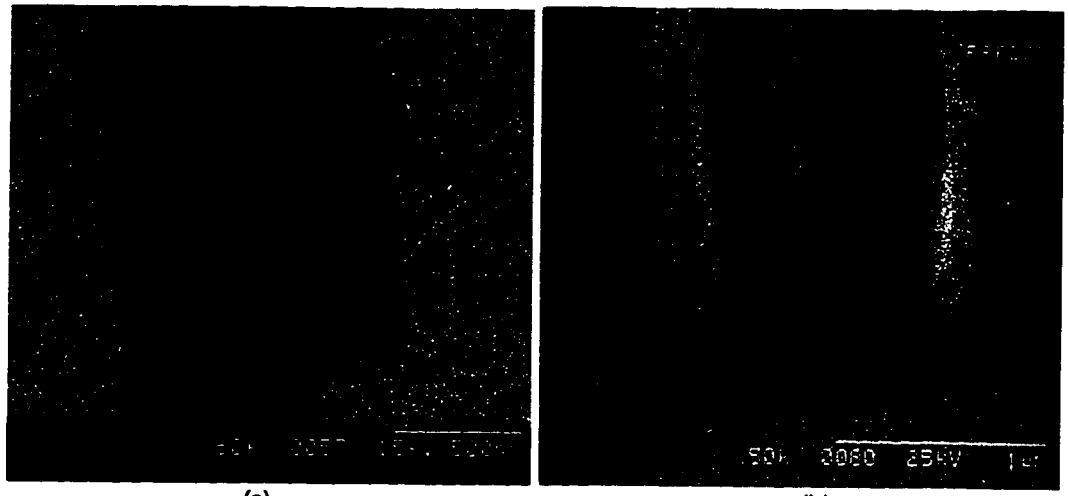
(a) (b)

Figure A.2.5. (a) SEM cross-section of a gate lithography after 2 min. of Au deposition by hummer. The development sequence was: (i) 11 s 300 mT, 100 W, O_2 plasma. (ii) 150 s 1:2 EGMEA:Ethanol at 21°C. (iii) 45 s IPA rinse. (b) Cross-section of the same lithography after evaporation of 5200 Å of Ti after development. The E-Beam resist is still in place. Note the wider top opening in (a) compared to (b) due to hummer sputtering of resist.



(a) (b)

Figure A.2.6. (a) Cross-section from the same lithography sample as in Figure A.2.4, with a longer predevelopment oxygen plasma ash time of 40 s. 5000 Å of evaporated SiO_2 sits on the resist. Compare the shape of the oxide pattern with the metalization in Figure A.2.4. (b) Cross-section of a different sample, with the resist and evaporated oxide surfaces distinctly observable. Notice the deposited oxide shape due to rapid closing of the top gap. This particular resist lithography would give way to a nominally mushroom shaped metal gate, as shown in Figure A.2.7 (b).



(a) (b)

Figure A.2.7. (a) Cross-section of a T-gate SiO_2 profile. (b) A mushroom shaped gate metalization.

A.2.5. Effects of Atmospheric Pressure Regrowth on E-Beam Registration

An immediate side effect of going to atmospheric pressure regrowth to increase the doping concentration was the reduced selectivity of the unmasked areas over the masked areas as mentioned earlier in Chapter 3 (see also Figure 3.9). This became a critical issue in fabricating the devices as most of the SiO_2 mask area was covered with polycrystalline GaInAs deposition. Figure A.2.8 depicts sections of a sample surface after regrowth. As observed, all the mask area except for the active device area is covered with regrowth[3]. The poly regrowth on the mask areas also affected the subsequent process of E-beam registration in that due to lack of contrast between the actual alignment cross (desired regrowth) and the poly around it (unwanted regrowth), registration was not possible.

We thus fabricated a separate mask to cover the crosses but to open up the immediate surrounding area for etching. Figure A.2.9 (a) shows the cross after lithography. Then the poly-GaInAs was etched with a 3:1:50 H_3PO_4:H_2O_2:H_2O solution. This step was followed by a 1:10 BOE:H_2O etch to remove the SiO_2 mask. Finally the epi material was etched down to the InP substrate to provide

[3] In some instances, there was island regrowth on the mask between the source and drain regions of the devices as well, essentially creating a short circuit between the regrown contact regions and rendering the sample useless for further processing.

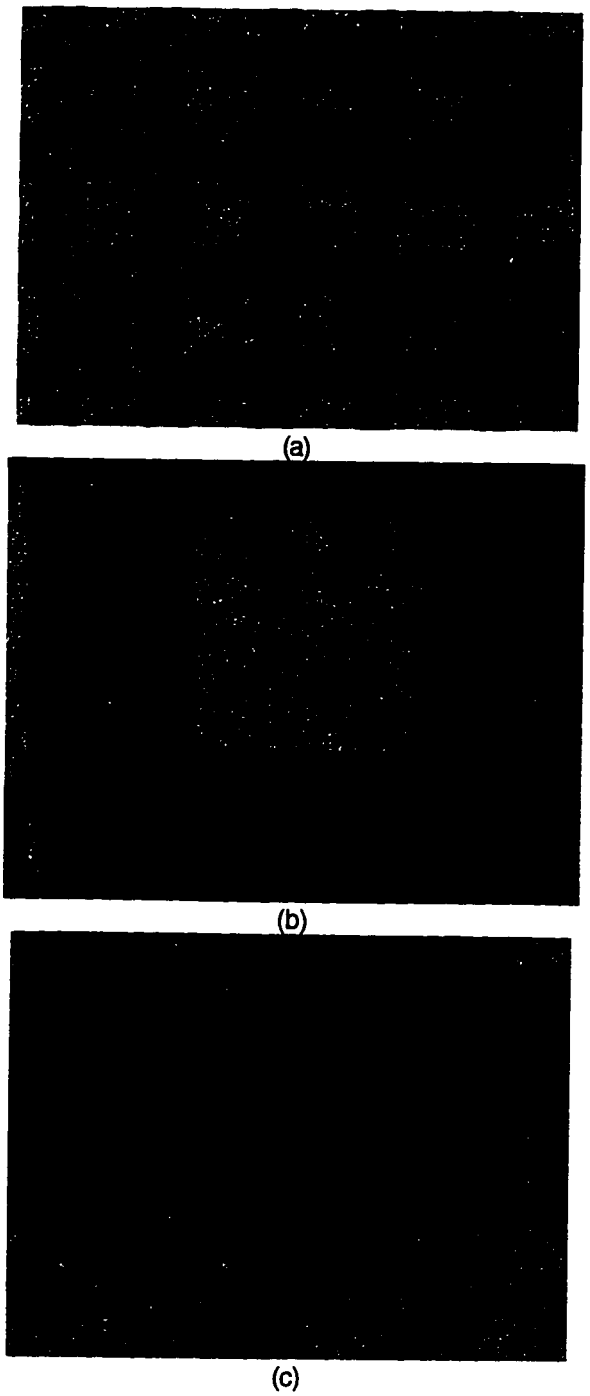


Figure A.2.8. Optical snapshots of the sample surface after atmospheric pressure regrowth. The clear areas are the desired crystalline regrowth on the etched wells. The polycrystalline regrowth covers all mask area except for the active device area. Magnifications: (a) x 20, (b) x 80, (c) x 800.

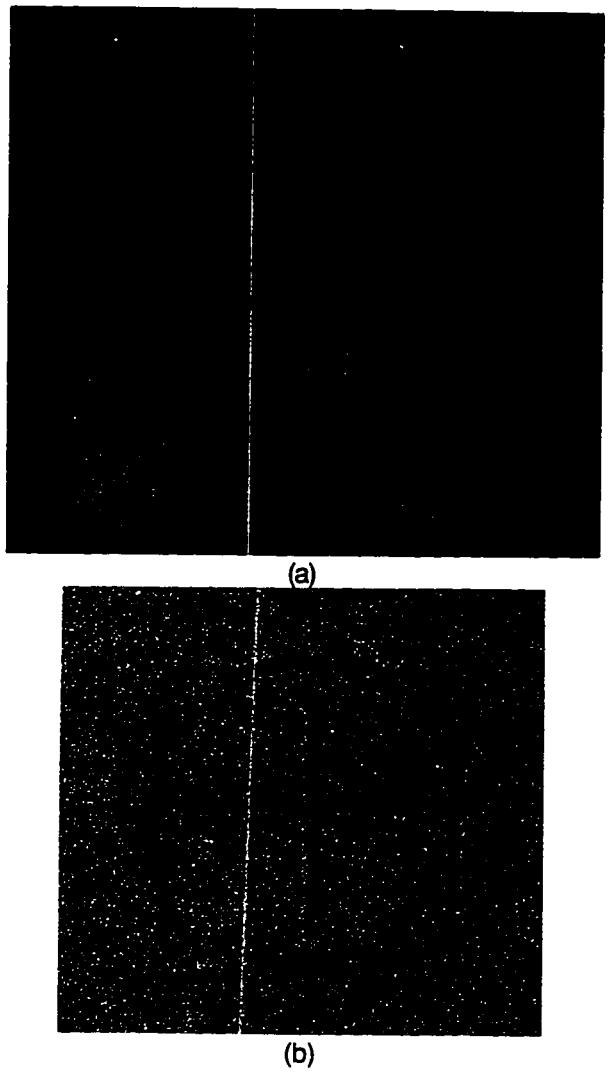


Figure A.2.9. Optical photographs of a cross region (a) after resist lithography has been done to clear the surrounding area, (b) after the surrounding area has been cleared and etched down to the InP substrate. The photos have different magnifications.

for a good contrast for E-beam registration. Figure A.2.9 (b) shows the cross with the surrounding area etched and cleaned. This additional "patch" process was sufficient to enable the subsequent E-beam registration for dummy gate oxide lithography.

References

[1] S.J. Wind, M.G. Rosenfield, G. Pepper, W.W. Molzen, and P.D. Gerber, "Proximity correction for electron beam lithography using a three-Gaussian model of the electron energy distribution," *Journal of Vacuum Science & Technology B (Microelectronics Processing and Phenomena)*, vol. 7, pp. 1507-12, 1989.

[2] J. Ross, Microlithography Chemical Corporation, personal communication, 1996.

[3] P.A. Lamarre, "Developer selection for T-shaped gate FET's using PMMA/P(MMA-co-MAA)/PMMA," *IEEE Transactions on Electron Devices*, vol. 39, pp. 1844-8, 1992.

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Appendix 3 Material Safety Data Sheets

A.3.1. MSDS for PMMA

Microlithography Chemical Corp.
294 Pleasant Street
Watertown, MA 02172-2401
Tel: (617) 926-3322
Fax: (617) 926-2919

MATERIAL SAFETY DATA SHEET PAGE 1
5 January 1994

SECTION I. IDENTIFICATION

CHEMICAL NAME: Organic Polymer Solution
TRADE NAME: NANO™ 495PMMA A 5.5
Positive Radiation Sensitive Resist
PRODUCT #: M130505

SECTION II. TRANSPORTATION INFORMATION

HAZARD CLASSIFICATION: Flammable Liquid
SHIPPING NAME Resin Solution, Flammable
UN NUMBER: UN 1866

SECTION III. TOXICITY HAZARDS

As Anisole

ORAL:	LD50 (rat):	3700 mg/Kg	
	LD50 (rabbit):	2800 mg/Kg	
INHALATION:	LC50:	not listed	
TLV:	ACGIH(TWA)		none established
PEL:	OSHA (8hr TWA)		none established

SECTION IV. HEALTH HAZARD DATA

SKIN IRRITATION: May cause skin irritation.
EYE IRRITATION: Vapor or mist is irritationg to the eyes.
MUTAGENICITY: Not known to be mutagenic.
CARCINOGENICITY: Anisole - negative in rats (NCI)
HAZARDOUS
INGREDIENTS: Anisole (CAS: 100-66-3) 95%.
OTHER
INGREDIENTS: Poly(methylmethacrylate) (CAS: 9011-14-7)

MATERIAL SAFETY DATA SHEET

CHEMICAL NAME: Organic Polymer Solution
TRADE NAME: NANO™ 495PMMA A 5.5
Positive Radiation Sensitive Resist
PRODUCT #: M130505

ACUTE EFFECTS:
May be harmful if swallowed, inhaled, or absorbed through the skin.
Vapor or mist is irritating to the eyes, mucous membranes and upper respiratory tract.
Inhalation of vapors has coused nausea, discomfort and loss of coordination in humans.
Causes skin irritation. Causes moderate skin irritation in rabbits. Low acute dermal toxicity. No sensitization observed in humans.
The chemical, physical, and toxicological properties have not been thoroughly investigated.

FIRST AID:

INHALATION:	If inhaled, remove to fresh air. If patient has stopped breathing, give artificial respiration. If breathing is difficult give oxygen. Contact physician immediately.
INGESTION:	Wash out mouth with water if conscious. Give two glasses of water and INDUCE VOMITING. Get medical attention immediately.
SKIN CONTACT:	Rinse with water for 15 minutes while removing contaminated clothing and shoes. Wash affected area with soap and water. Wash contaminated clothing.
EYE CONTACT:	Rinse immediately with water, flush for 15 min. Get emergency medical assistance.

SECTION V. PHYSICAL DATA

APPEARANCE:	Clear to straw colored liquid
ODOR:	Aromatic
BOILING POINT:	154 °C (307 °F)
SPECIFIC GRAVITY:	1.004
VAPOR PRESSURE:	10 mm @ 42 °C (108 °F)
VAPOR DENSITY:	3.7 (air=1)
H_2O SOLUBILITY:	0.2% @ 20 °C, by wt.
% VOLATILES:	95% by wt
EVAPORATION RATE:	0.1 (BuAc=1)

SECTION VI. FIRE AND EXPLOSION HAZARD DATA

FLASH POINT:	52 °C (125 °F) TCC
AUTOIGNITION TEMP:	475 °C (887 °F)
EXPLOSION LIMITS:	unk. lower unk. upper
EXTINGUISHING MEDIA:	Dry chemical, carbon dioxide, foam.

MATERIAL SAFETY DATA SHEET

CHEMICAL NAME: Organic Polymer Solution
TRADE NAME: NANO™ 495PMMA A 5.5
Positive Radiation Sensitive Resist
PRODUCT #: M130505

SPECIAL FIRE FIGHTING PRECAUTIONS: Wear self-contained breathing apparatus (SCBA) and personal protective equipment to prevent contact with skin and eyes.

UNUSUAL FIRE OR EXPLOSION HAZARDS: Heat will build pressure and may rupture closed containers. Keep containers cool with water spray

SECTION VII. REACTIVITY DATA

STABILITY: Stable
INCOMPATIBILITY: Oxidizing Agents, Strong Acids
HAZARDOUS COMBUSTION OR DECOMPOSITION PRODUCTS: Carbon Monoxide, Carbon Dioxide

SECTION VIII. SPILL OR LEAK PROCEDURES

STEPS TO BE TAKEN IF MATERIAL IS RELEASED OR SPILLED
Evacuate Area.
Eliminate all ignition sources.
Wear self-contained breathing apparatus (SCBA), rubber boots, and heavy rubber gloves. Avoid eye or skin contact. Cover with dry absorbent material and collect in closed container for disposal using non-sparking tools. Ventilate area and wash spill site with ketonic or acetate type solvent after material pickup is complete, rinse with water. All clean-up should be carried out in accordance with federal, state, and local regulations.

WASTE DISPOSAL METHOD
Burn in an EPA-licensed chemical incinerator equipped with an afterburner and scrubber at an approved waste disposal facility. Observe all federal, state, and local environmental regulations.

MATERIAL SAFETY DATA SHEET

CHEMICAL NAME: Organic Polymer Solution
TRADE NAME: NANO™ 495PMMA A 5.5
Positive Radiation Sensitive Resist
PRODUCT #: M130505

SECTION IX. HANDLING AND STORAGE PRECAUTIONS

STORAGE:	Store in tightly closed container in a cool environment away from direct sunlight.
HANDLING:	Keep away from heat, sparks, and flames. Hydroscopic. Do not breathe vapors. Use only with mechanical exhaust. Avoid contact with skin, eyes, and clothing. Avoid prolonged or repeated exposure Wear heavy rubber gloves. Wash with soap and water after handling. Have safety shower and eye wash available.
RESPIRATORY PROTECTION:	In case of spills, use of self-contained breathing apparatus (SCBA) is recommended.
VENTILATION:	Local or general mechanical ventillation is required.
SKIN PROTECTION:	Heavy rubber gloves are highly recommended.
EYE PROTECTION:	Safety goggles are highly recommended.

SECTION X. REGULATORY INFORMATION:

HAZARDOUS LISTINGS:	All ingredients appear on the TSCA Inventory of Chemical Substances, EINECS, and the Japan Hazardous Chemical Listing.
SARA Title III: Section 313	This product IS NOT subject to SARA Title III. Reporting Requirements.

Calif. SCAQMD Rule 443.1 VOC's: 950 g/l; vapor pressure 1 mm Hg @ 20°C

SECTION XI. ADDITIONAL PRECAUTIONS AND COMMENTS

To the best of our knowledge, the above information is believed to be accurate but does not claim to be all inclusive and is intended to be used only as a guide. The supplier makes no warranty of any kind, expressed or implied, concerning the use of this product and shall not be held liable for any damage resulting from handling or from contact with the above product. User assumes all risks incident to its use.

A.3.2. MSDS for the Copolymer (PMMA/MAA)

Microlithography Chemical Corp.
294 Pleasant Street
Watertown, MA 02172-2401
Tel: (617) 926-3322
Fax: (617) 926-2919

MATERIAL SAFETY DATA SHEET PAGE 1
15 July 1993

SECTION I. IDENTIFICATION

CHEMICAL NAME:	Organic Polymer Solution
TRADE NAME:	NANO MMA(17.5)MAA EL 10 Positive Radiation Sensitive Resist
PRODUCT #:	M410010

SECTION II. TRANSPORTATION INFORMATION

HAZARD CLASSIFICATION:	Flammable Liquid
SHIPPING NAME:	Resin Solution, Flammable
UN NUMBER:	UN 1866

SECTION III. TOXICITY HAZARDS

ORAL:	LD50 (mouse): 2500 mg/kg, subcutaneous. 600 mg/kg, intravenous. LD50: >2000 mg/kg. FDA and FAO/WHO approved as food additive.
INHALATION:	LC50: >5000 mg/m^3.

SECTION IV. HEALTH HAZARD DATA

SKIN IRRITATION:	2068 mg/kg/day percutaneous: slight erythema. 3012 mg/kg/day embryo percutaneous: no adverse effects.
EYE IRRITATION:	Moderate temporary irritation.
MUTAGENICITY:	No positive response for several tested salmonella strains.
CARCINOGENICITY:	Not listed in NTP, IARC, or OSHA as a carcinogen.
HAZARDOUS INGREDIENTS:	Ethyl Lactate (CAS: 97-64-3) 90%
OTHER INGREDIENTS:	Poly(methylmethacrylate-co-methacrylic acid) (CAS: 25086-15-1)

MATERIAL SAFETY DATA SHEET

CHEMICAL NAME: Organic Polymer Solution
TRADE NAME: NANO MMA(17.5)MAA EL 10
Positive Radiation Sensitive Resist
PRODUCT #: M410010

FIRST AID:

INHALATION: Remove to fresh air. If patient has stopped breathing, give artificial respiration. Contact physician immediately.

INGESTION: If substantial amounts are swallowed, have patient drink large amounts of water to dilute the product in the system. Contact physician immediately.

SKIN CONTACT: Rinse with water. Wash with soap and water.

EYE CONTACT: Rinse immediately with water, flush for 15 min. Contact a physician if irritation develops.

SECTION V. PHYSICAL DATA

APPEARANCE:	Yellow-brown to brown liquid
ODOR:	Mild, pleasant
BOILING POINT:	150 °C (302 °F)
SPECIFIC GRAVITY:	1.048
VAPOR PRESSURE:	1.2 mm @ 20 °C (68 °F)
H_2O SOLUBILITY:	90% @ 20 °C, by wt; remainder is solid ppt.
%VOLATILES:	90% by wt
EVAPORATION RATE:	<1 (BuAc = 1)

SECTION VI. FIRE AND EXPLOSION HAZARD DATA

FLASH POINT:	53 °C (128 °F) TCC
AUTOIGNITION TEMP:	400 °C (752 °F)
EXPLOSION LIMITS:	1.6% lower 10.6% upper
EXTINGUISHING MEDIA:	Water, dry chemical, carbon dioxide, foam.
SPECIAL FIRE FIGHTING PRECAUTIONS:	Wear self-contained breathing apparatus (SCBA) and personal protective equipment when exposed to products of combustion.
UNUSUAL FIRE OR EXPLOSION HAZARDS:	None

MATERIAL SAFETY DATA SHEET

CHEMICAL NAME: Organic Polymer Solution
TRADE NAME: NANO MMA(17.5)MAA EL 10
Positive Radiation Sensitive Resist
PRODUCT #: M410010

SECTION VII. REACTIVITY DATA

STABILITY:	Stable
INCOMPATIBILITY:	Oxidizing Agents
HAZARDOUS POLYMERIZATION:	Will not Occur
HAZARDOUS COMBUSTION OR DECOMPOSITION PRODUCTS:	Carbon Monoxide, Carbon Dioxide

SECTION VIII. SPILL OR LEAK PROCEDURES

STEPS TO BE TAKEN IF MATERIAL IS RELEASED OR SPILLED
Avoid eye or skin contact. Eliminate ignition sources. Cover large quantities with absorbent material and collect in closed container for disposal. All clean-up should be carried out in accordance with federal, state, and local regulations. If required proper authorities should be notified.

WASTE DISPOSAL METHOD
Burn in a chemical incinerator in an approved waste disposal facility.

SECTION IX. HANDLING AND STORAGE PRECAUTIONS

STORAGE:	Store in original, well closed container.
HANDLING:	Keep away from heat, sparks, and flames. Avoid breathing vapors. Use with adequate ventilation. Avoid contact with skin, eyes, and clothing. Wear impervious gloves. Wash with soap and water after handling.
RESPIRATORY PROTECTION:	In case of large spills, use of self-contained breathing apparatus (SCBA) is recommended as narcosis may occur.
VENTILATION:	General mechanical ventilation is sufficient under normal conditions.
SKIN PROTECTION:	Impervious gloves are recommended.
EYE PROTECTION:	Safety goggles are recommended.

MATERIAL SAFETY DATA SHEET

CHEMICAL NAME: Organic Polymer Solution
TRADE NAME: NANO MMA(17.5)MAA EL 10
Positive Radiation Sensitive Resist
PRODUCT #: M410010

SECTION X REGULATORY INFORMATION

HAZARDOUS LISTINGS:	All ingredients appear on the TSCA Inventory of Chemical Substances, EINECS, and the Japan Hazardous Chemical Listing.
SARA Title III.	This product IS NOT subject to SARA Title III, Section 313 Reporting Requirements.
Calif. SCAQMD Rule 443.1 VOC's:	945 g/l; vapor pressure 1.2 mm Hg @ 20° C.

SECTION XI ADDITIONAL PRECAUTIONS AND COMMENTS

To the best of our knowledge, the above information is believed to be accurate but does not claim to be all inclusive and is intended to be used only as a guide. The supplier makes no warranty of any kind, expressed or implied, concerning the use of this product and shall not be held liable for any damage resulting from handling or from contact with the above product. User assumes all risks incident to its use.