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Device Application of Low-Temperature-Grown $Al_{0.3}Ga_{0.7}As$: GaAs Microwave Power Field Effect Transistor

A Dissertation submitted in partial satisfaction

of the requirements of the degree of

Doctor of Philosophy

in

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by

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June 1997

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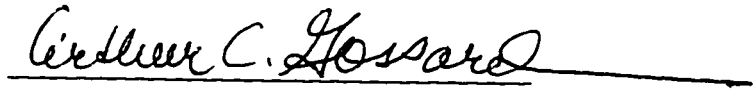

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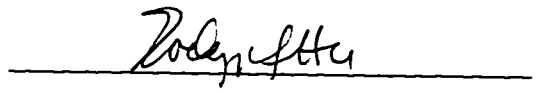

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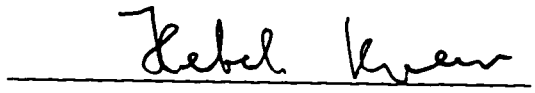

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Dedicated

to

my parents

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ABSTRACT

Device Application of Low-Temperature-Grown $Al_{0.3}Ga_{0.7}As$:
GaAs Microwave Power Field Effect Transistor

by
Nguyen Xuan Nguyen

The performance, uniformity and therefore the cost of reliable GaAs power FETs have been limited by the non-reproducibility of the gate diode characteristics. The main reason for this is the lack of an effective electrical passivation of the GaAs surface adjacent to the gate. In this research project, we have investigated the application of low-temperature-grown (LTG) $Al_{0.3}Ga_{0.7}As$ as an electrical passivation layer for GaAs FETs. In particular, the surface layer engineering to improve breakdown voltage of GaAs FETs with LTG- $Al_{0.3}Ga_{0.7}As$ is systematically studied.

Drawing from the established material properties of LTG-GaAs, a simple model is proposed to explain the physical mechanism through which the LTG materials passivation alleviate peak field in a MESFET structure. The unique existence of the natural compensated deep donors in LTG materials is believed to be responsible for the improved breakdown voltage of LTG passivated devices. Two dimensional device simulation to confirm this model has been performed.

A systematic study of the effect of growth and annealing temperatures on LTG-$Al_{0.3}Ga_{0.7}As$ passivated MESFETs has been performed. Breakdown voltage and low frequency noise characteristics of the devices are foound to be critically dpended on both the growth and annealing temperatures.

A high performance GaAs-based power MESFET which incorporates an LTG-$Al_{0.3}Ga_{0.7}As$ passivation is demonstrated. Record power performance of 1.0 W/mm at 30% power-added-efficiency (PAE), and 0.5 W/mm at 46% PAE has been achieved. These results provide clear testimony for the potential of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation technology for microwave power FETs.

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CHAPTER 1

Introduction

1.1 Overview :

The advent of the commercial wireless communication market has brought forth new demands for compact, low cost, and high performance microwave components and systems. This in turn leads to a demand for low cost and high performance microwave semiconductor circuits and devices. In particular, there are pressing needs for semiconductor devices that have high raw microwave power, high linearity, and high efficiency. Recent developments in compound semiconductor materials and technology have led to the popular belief that compound semiconductor devices would provide the answers to these stringent demands of the industry. In particular, Gallium Arsenide ***ME***tal ***S***emiconductor ***F***ield ***E***ffect ***T***ransistor (GaAs MESFET) has been demonstrated to have the potentials of meeting the demand of both low cost *and* high performance [1-3].

The maturity and simplicity of the GaAs MESFET fabrication technology have led to the establishment of this device and its variation as the work horse of the compound semiconductor industry [3]. However, as of present, GaAs MESFET has been plaqued by a simple, yet detrimental problem that has inhibited its widespread usages - *low yield* [4]. Over the years, studies have led to the conclusion that the main culprit of the low yield problem in GaAs devices is the non-uniform native oxide formed on top of the GaAs surface when it is expose to atmospheric ambient [5-7]. This native oxide depended sensitively on the processing treatments that the samples underwent in the device fabrication procedure, which led to the high device-to-device

non-uniformity and low run-to-run reproducibility. This problem has been continually studied and addressed by material scientists and device engineers through various approaches. To date, the most promising solutions have came from chemical treatments of the GaAs surface. Photochemical oxidation and sulfide chemical passivation such as Na_2S and $(NH_4)_2S$ [8, 9] have demonstrated to be the most promising solutions. However, the drawback of these chemical treatments technology is that they leave the GaAs surface susceptible to thermal and environmental instabilities; therefore device reliability remained an issue.

From a device engineeriing point of view, the problem of low yield in GaAs devices could alternatively be addressed through the development of a *stable and effective electrical passivation technology* for GaAs materials and devices. As shown in Figure 1a and 1b, an ideal electrical passivant layer should have the following properties:

(i) It should maintain (or increase) the breakdown voltage of the FET.

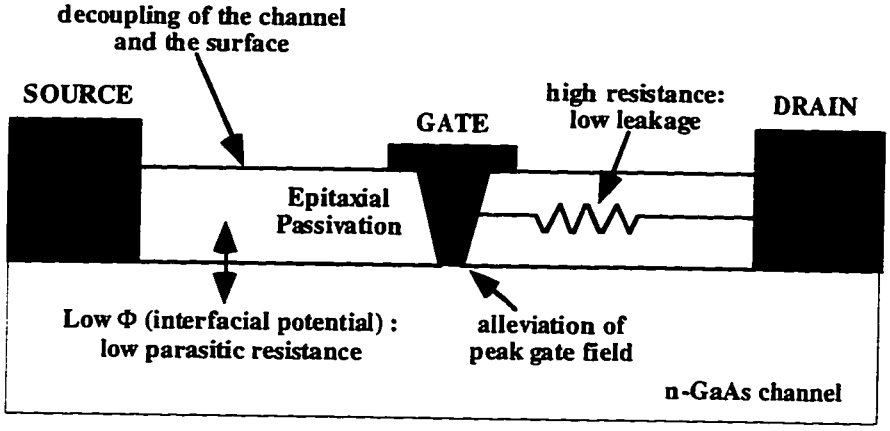
(ii) It should effectively screen the channel from the surface of the device to lower 1/f noise, critical in linear communication systems.

(iii) It should not deplete the underlying channel thereby increasing channel resistance and losses (decreasing efficiency). This property can be alternatively stated as 'the interface potential difference between the passivant and the channel should be low.'

(iv) It should not increase the gate leakage.

Recent advances in a new kind of molecular beam epitaxial (MBE) materials, known as Low-Temperature-Grown (LTG) GaAs and related materials, have been shown to have the potentials of satisfying all of the stated above properties of an ideal passivation layer. The goal of the present research project is to gain definitive

understandings into the device application of LTG materials as an electrical passivation technology; and to further the use of LTG materials as a tool for device engineering to improve breakdown voltage and power performance.



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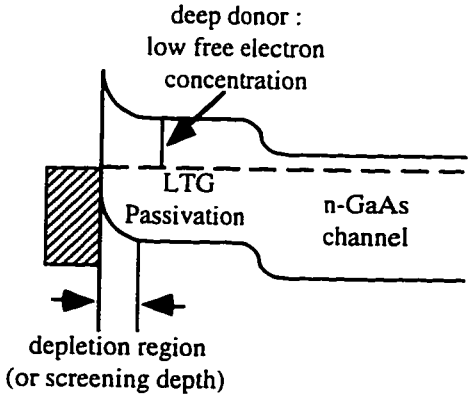


(b)

Figure 1.1: (a) Schematic FET showing important parameters to consider when choosing a surface passivant. (b) Schematic band diagram through gate, passivant and channel of device.

Chapter 1 sets the tone and provides the general background for the remainder of the dissertation. In the next two sections of this chapter, issues and problems in GaAs power MESFET are reviewed; in particular, the important relationship between

surface conditions and breakdown in field effect transistors will be discussed. The chapter then concluded with the last section summarizing the scope of the present dissertation.

1.2 High Power GaAs FET :

Maximum output power in microwave device shares a similar motive as speed in digital integrated circuits - the more, the better. As such, it is highly desirable to maximize the power performance of microwave device in general, and of GaAs FET in particular. The first realization of high power GaAs FET were reported simultaneously by Fukuta *et al* [1] and Napoli *et al* [10] in 1973. Since then, intense efforts had been devoted into maximizing the output power obtainable from GaAs field effect transistors. Figure 1.2 summarized some of the annual progress in the output power of GaAs FET reported.

For high power application, a device must be able to sustain both high voltage and current in order to convert the DC power into microwave or millimeter-wave power. Proper device design of a high power GaAs MESFET required close attentions to various cross-linked design parameters such as doping density profile, channel thickness, and geometric layout, etc. The correlations between these design considerations and the related performance indicators are briefly summarized in Table 1.1.

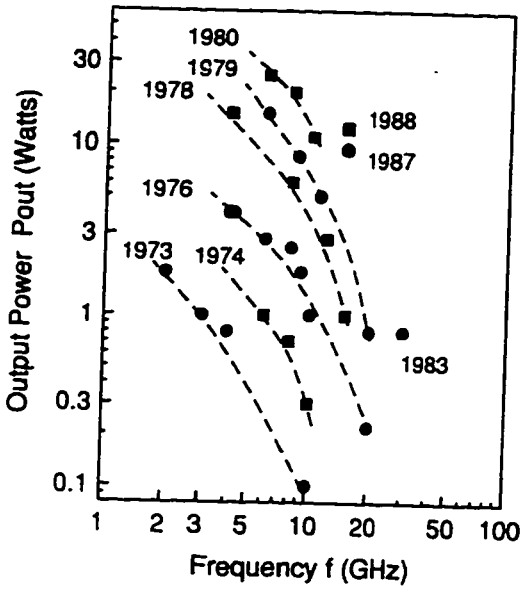


Figure 1.2: Progress in microwave power performance of GaAs FETs - the first practical GaAs power FET was reported in 1973 [3].

Table 1.1 : Microwave power FETs design parameters and figures-of-merit.

Design Parameter	Characteristics	Power Performance
Doping Density	Drain Current	Output Power
Epitaxial Thickness	Transconductance	Gain
Geometric Spacings	Gate Breakdown	Efficiency
Gate Length	Parasitic Resistances	Distortion
Ohmic Contacts	Knee Voltage	Cutoff Frequency
Surface Passivation		Reliability
Metallization		

A nominal class-A bias configuration of a FET for power application is shown in Figure 1.3. As indicated in the figure, the maximum output power of a device is

directly proportional to *both* the maximum drain current and the breakdown voltage. Although, at a first glance, the drain current of the device is a function of just the channel doping and thickness; however, on closer examination of the limitation of its maximum drain current, we immediately see that the maximum drain current is dictated by the criteria that it could be completely pinch-off, *prior* to breakdown. Therefore, the maximum drain current is also indirectly governed by the breakdown of the device. In short, the breakdown voltage is of paramount importance in the power performance of a FET. For GaAs MESFET, work over the years have clearly demonstrated that its breakdown voltage critically depended on the surface condition [6, 11, 12], and in particular the surface condition in the vicinity of the gate.

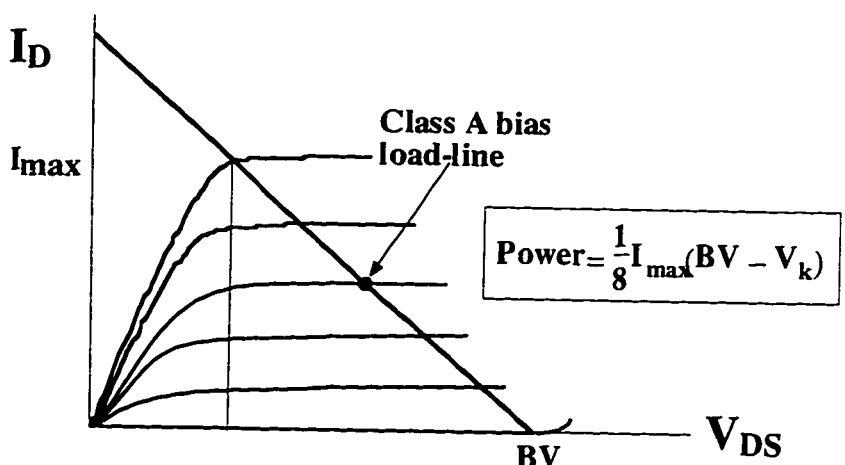


Figure 1.3: Nominal class-A bias configuration of a GaAs power field-effect transistor. The load-line is shown for maximum output power condition, which is directly proportional to the maximum drain current and the breakdown voltage.

1.3 Effect of Surface Condition on Breakdown Voltage:

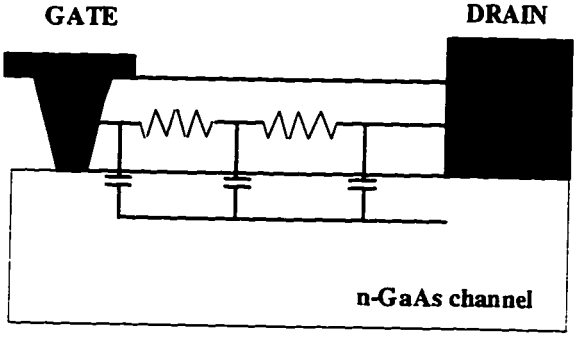
Under nominal bias for microwave power application, the gate-drain region of a MESFET structure sustained the highest potential difference. This potential difference resulted in a local high field region; which in turn led to the eventual breakdown of the device. Direct experimental observations of light emissions from

this high field region have pinpointed its locale at the drain edge of the gate [13, 14]. Therefore, the breakdown voltage of a FET could be increased by one of two means, either by reducing the peak electric field at the gate and/or reducing the injected electron density (gate leakage) which reduces multiplication in the channel. The latter can be achieved independently of the former by inserting a wide band gap material under the gate metal (ie, a Metal Insulator Semiconductor FET, MISFET, structure). The former is the focus of the present research. Any advances made with this approach can also be applied to MISFETs structure for added benefit.

Reducing the electric field at the gate can also be achieved in two ways, schematically shown in figures 1.4a and 1.4b. The first is by distributing the potential between the gate and the drain by adding a shunt resistive path to the channel. Here, in the simplest case, the linear increase in voltage along the resistor is reflected in the channel through the barrier height of the resistor on the semiconductor. The disadvantage of this technique is that the ladder network is a low pass filter. Beyond the cut-off frequency, the effectiveness of the network in redistributing the surface potential rolls off and hence the breakdown voltage of the device decreases with frequency, beyond the pole of the network.

The second means of alleviating the peak electric field, illustrated in figure 1.4b, is by allowing tunnel injection of charge from the drain edge of the gate into states in the passivant close to the gate. Again, this approach may have some frequency dependence related to the capture and emission times from the traps. LTG materials passivation, in particular LTG-GaAs and LTG-AlGaAs, with the appropriate growth and annealing conditions, are capable of providing electrical characteristics that resulted in *either* of the two field alleviation mechanisms stated. Therefore, the

engineering of this materials to tailored their parameters to obtain the desire electrial passivation properties is of great practical interests.



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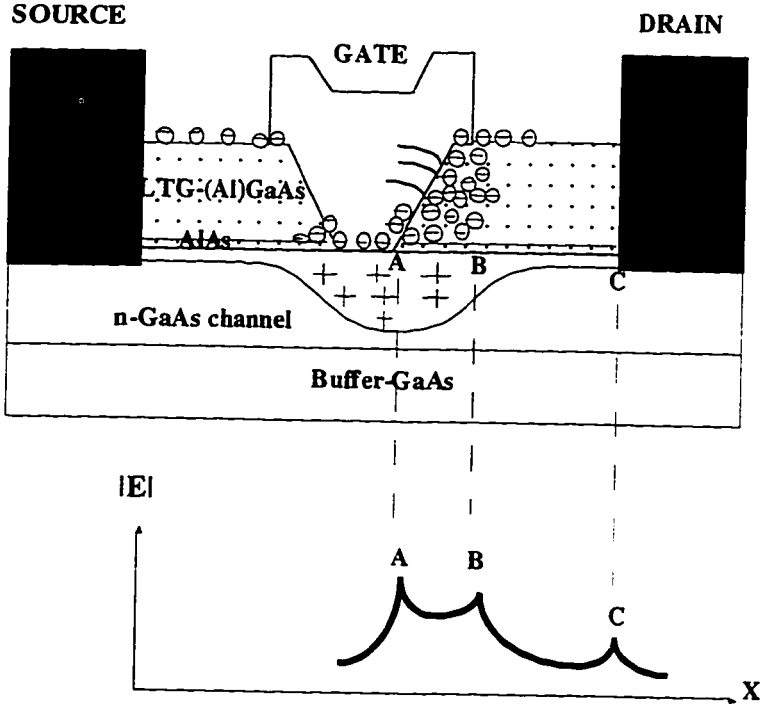

(b)

Figure 1.4: Field alleviation by a) voltage redistribution through an RC ladder network and b) by charge injection into the LTG material in the vicinity of the gate.

1.4 Scope of Dissertation:

As common in the early stage of the research and development for most new materials, there usually existed a vast body of empirical data and reports on the material properties and also different models to explain these properties, some are even in contradiction with others; LTG materials and its applications are no exception to this rule. While this pose no serious problem in the research of the material science of LTG materials, it brought about many unresolved issues and potential contradictions in the paralleled device research based on the new material. Questions such as "What are the relevant material properties to device applications?" required constant attentions. The main focus of Chapter 2 is the *established* material properties of LTG materials that directly related to electronic devices. Other issues, such as the temperature dependence passivation properties of LTG materials such as channel band bending are also investigated and discussed.

Chapter 3 draws on the LTG material properties to explain the effect that LTG passivation has on the breakdown voltage of GaAs FET. In particular, a physical model of the field alleviation by LTG materials passivation, through the compensated deep donors, is proposed. Two dimensional electrostatic simulations of the device are performed to verify the model.

Chapter 4 focuses on the experimental implementation of LTG-$Al_{0.3}Ga_{0.7}As$ passivation in actual devices. The effects of growth temperatures and subsequent annealing treatment of LTG-$Al_{0.3}Ga_{0.7}As$ on the breakdown voltage and other device characteristics are studied.

Chapter 5 presents the characteristics and performance of a high-power GaAs heterostructure field effect transistor that has incorporated an LTG-$Al_{0.3}Ga_{0.7}As$

electrical passivation layer. Record power performance at C-band are presented and discussed.

Chapter 6 concludes the present dissertation with a summary of research conclusions and recommendation for some possible revenues of future research.

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CHAPTER 2

Electrical Properties of Low Temperature Grown Materials

2.1 Introduction:

Device application was the initial driving force in the research and development of low-temperature-grown (LTG) GaAs; and ever since, it has paralleled and complemented the material research of LTG-GaAs and related compounds. The first interest in the device application of LTG material dated back to February 1988 in a paper published by Smith *et al* [1] , where LTG-GaAs was first demonstrated to be an effective buffer for the reduction of backgating in GaAs IC. This first demonstration of the beneficial effect of LTG-GaAs has since generated a flurry of activity in the quest for more understandings of the material properties and other potential device applications of LTG materials. Soon afterward, another device application of LTG-GaAs was reported. The utilization of annealed LTG-GaAs as a surface insulator in a MISFET structure to improve the gate-drain breakdown voltage was demonstrated by Yin *et al* [2] in 1990. This new technology, LTG materials passivation, caught the interests of device engineers because it provides a new tool in dealing with a long standing problem of surface passivation in GaAs devices. The strong dependency of the LTG material properties on its synthesis condition allowed them to be readily engineered to yield desired device characteristics.

These preliminary device results demonstrated the potential of this new LTG-GaAs passivation technology in GaAs FET. However, as with any new technology, new questions arose, and satisfactory answers to them required further investigations and understanding. Questions such as, "What are the unique properties of the LTG materials? How does LTG passivation effect other device characteristics? And what

parameters can we engineer to optimize the device performance?" points to a need for better understanding of the material properties and their correlations to the synthesis process involved.

To date, over two hundred papers have been published on the various properties and models of LTG-GaAs and related materials; some even with conflicting reports, on the properties of LTG materials. As such, it would be beyond the scope of a single chapter in a thesis to provide a comprehensive review of the various reported properties of LTG materials in literature. The objective of the present chapter is to provide a focused summary and review of the LTG material properties that are *pertinent to electronic devices*; and also to present some experimental data that had been obtained recently on the interfacial properties of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer to the underlying normal materials.

The next section focuses on the current established material properties and understanding of LTG-GaAs. This is followed by a section on the reported properties of LTG-$Al_{0.3}Ga_{0.7}As$. The last section of the chapter presents the results of our recent experimental study on the interfacial property of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer and the GaAs channel. In particular, the parameter space of the channel band-bending as a function of growth and annealing temperatures of the LTG-$Al_{0.3}Ga_{0.7}As$ layer have been systematically investigated. This parameter is of great interest in the design of devices with LTG-$Al_{0.3}Ga_{0.7}As$ passivation.

2.2 LTG-GaAs Material Properties:

The unique synthesis characteristics of LTG-GaAs is explicitly stated in its acronym, *low temperature grown*. Unlike conventional molecular beam epitaxy of GaAs, which is nominally grown at substrate temperatures of 580-600°C, LTG-GaAs is grown at a substrate temperature of ~200°C. With all other growth parameters

(beam equivalent pressure and growth rate) similar to that of normal GaAs, this difference in growth temperature alone has resulted in spectacularly different electrical and optical properties of the materials. The exact growth temperature (in the 200°C range) has been observed to intimately influence both structural and electrical properties of the LTG-GaAs film.

Analysis of as-grown LTG-GaAs has revealed that the material contains a large concentration of excess As, between 1-2% (10^{20}-10^{21} excess As atoms per cm^3). which renders the material non-stoichiometric. The amount of excess As depends strongly on the growth temperatures of the GaAs film [3]. Initially, this excess As is incorporated into the GaAs lattice primarily as point defects such as As antisites (As_{Ga}) [4] and possibly As interstitials (As_i) [5]. These defects are believed to be responsible for the observed expansion of the GaAs lattice.

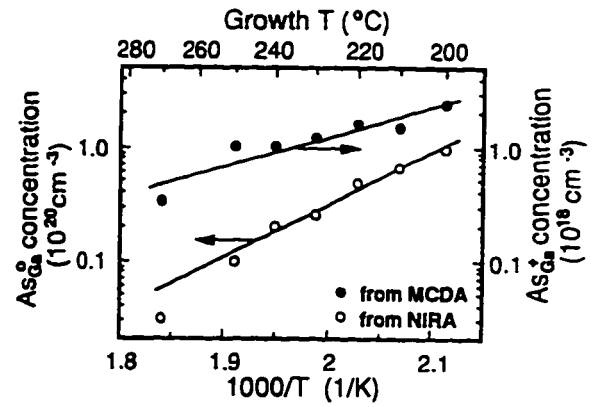
Electron paramagnetic resonance (EPR) [6], near infrared absorption (NIRA) [7], and magnetic circular dichroism absorption (MCDA) [3] experiments have positively identified that AsGa is the main contributor to the observed donor-like point defects in LTG-GaAs. The average concentration of this donor-like defect is about 10^{20} cm^{-3} for samples grown at ~200°C and decreases monotonically to about 10^{18} cm^{-3} for those grown at higher temperatures (>300°C). Extraction of the activation energy of this As_{Ga}-related donor from an Arrhenius plot yields an energy of 0.65 ± 0.01 eV [8]. In addition to the As antisite defect, there is also evidence of another donor-like defect, the As interstitial defect; however this defect is believed to be electrically inactive [8], thus it has not received much attention.

In addition to these two donor-like defects, from stoichiometry consideration, another defect is assumed to exist in large quantity in LTG-GaAs, the gallium vacancy defect (V_{Ga}). Unlike the first two defects, the V_{Ga} defect is acceptor-like. It is

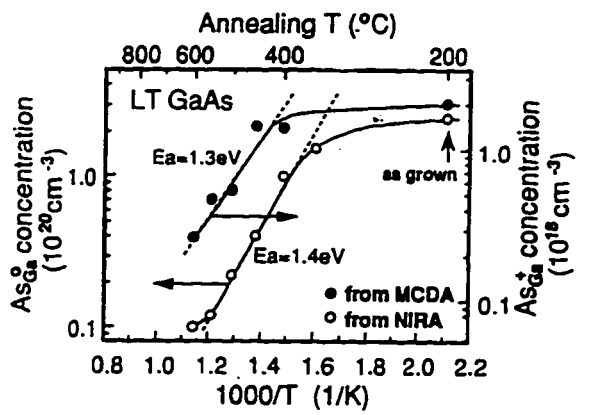
believed to be the source of the large concentration of acceptors observed in the material. Preliminary data from absorption studies and thermally stimulated current experiments have yielded a concentration of 10^{19} cm^{-3}, with an energy level of 0.27 ± 0.3 eV above the valence band for the V_{Ga} point defect [9].

The high concentration of both deep donors and deep acceptors in the as-grown LTG-GaAs results in a compensated deep donor level in the material. Electrically, this compensated deep donor provided a path for hopping conduction of carriers under applied bias. Therefore, as-grown, LTG-GaAs is generally conductive, with resistivity of the order of 10 Ω-cm [10].

Upon annealing at high temperature (>400°C), a dramatic change in the material properties of the LTG-GaAs is observed. The film usually relaxes and the lattice constant returns to that found in normal GaAs. The initial excess arsenic in the film (As_i and As_{Ga}) diffuses and clusters together to form As precipitates. Scanning tunneling microscopy (STM) studies of these precipitates have revealed several structures, from an amorphous structure for smaller size (diameter of 20-30Å) to hexagonal for larger size (>40Å) [11]. Annealing at higher temperatures results in larger precipitates but lowers total precipitate density in the material. In addition, annealing also has dramatically reduced the concentration of both As_{Ga} and V_{Ga} point defects in the LTG-GaAs layer. A recent systematic measurement of these defects as a function of growth and annealing temperatures is shown in figures 2.1



(a)



(b)

Figure 2.1: Defects concentrations in LTG-GaAs as a function of (a) growth and (b) annealing termperatures. The charged As_{Ga} were measured by MCDA and the neutral As_{Ga} by NIRA. The charged As_{Ga} concentration can be view as an indirect measurement of the deep acceptors concentration in the materials, while the sum of both charged and neutral As_{Ga} is equivalent to the total deep donors concentration [3].

Electrically, annealing at high temperatures drastically changes the resistivity of the LTG-GaAs layer. The resistivity increased from 10 Ω-cm in the as-grown LTG-GaAs to 10^6 Ω-cm in the LTG-GaAs annealed at 600°C for 10 minutes. This strong dependence of resistivity on the annealing temperatures of LTG-GaAs and the mechanisms responsible for it have attracted a lot of attentions from material

scientists and engineers in recent years. A summary of the dependence of resistivity of LTG-GaAs on the growth and annealing temperatures is shown in figure 2.2 [12].

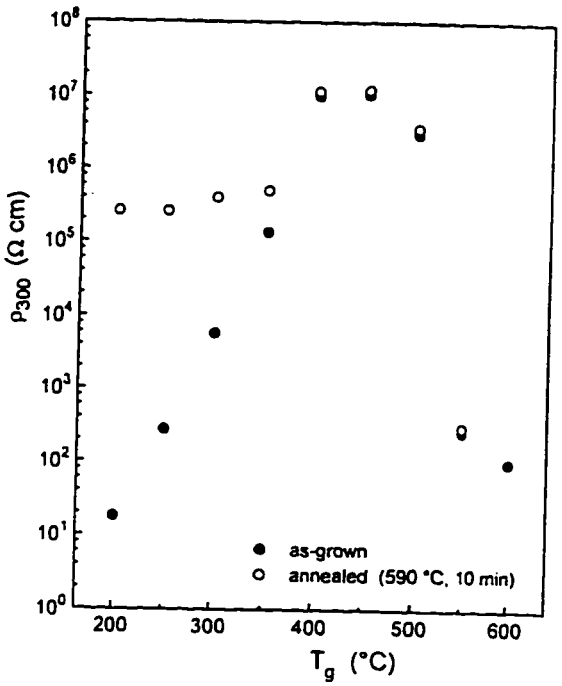


Figure 2.2: Room temperature resistivities as a function of growth temperatures for as-grown and annealed GaAs MBE layers [From [12]].

The microscopic picture of the origin of this unique LTG materials characteristics has been and still is a lively topic of debate among workers in the field. As of present, the two contending models for this unique property of LTG-GaAs are: the As precipitate dominated model and the point defects dominated model. To date, there is insufficient evidence to assert the correctness of one model over the other, and it is generally agreed that further investigations are needed before definitive conclusions could be drawn.

2.3 LTG-$Al_{0.3}Ga_{0.7}As$ Material Properties:

With LTG-GaAs demonstrating many unique and interesting material properties, especially the high resistivity and high breakdown field strength of annealed LTG-GaAs, it was natural for researchers to investigate other low

temperature grown III-V compounds and their potentials. Low temperature grown materials such as $In_xGa_{1-x}As$ [13, 14], InP [15, 16], $Al_xGa_{1-x}As$ [17], and InGaP [18] have been studied and reported. In particular, LTG-$Al_{0.3}Ga_{0.7}As$ has attracted much attention from device engineers because of its close resemblance to LTG-GaAs, but with an added advantage of a larger bandgap. This mean that LTG-$Al_{0.3}Ga_{0.7}As$ can also be engineered to be utilized in applications similar to LTG-GaAs, but with additional benefits. The larger bandgap of the $Al_{0.3}Ga_{0.7}As$ material should further improve the material breakdown field strength and also yield higher resistivity. Preliminary reports of the properties of LTG-$Al_{0.3}Ga_{0.7}As$ show that this is indeed the case.

LTG-$Al_{0.3}Ga_{0.7}As$ is grown at a substrate temperature of about 250°C, about 50°C higher than LTG-GaAs. The slightly higher substrate temperature is required to retain good crystallinity of the Aluminum containing compound. Structurally, LTG-$Al_{0.3}Ga_{0.7}As$ is reported to be similar to LTG-GaAs: the as-grown samples contain an excess concentration of As, and upon annealing at high temperatures, As precipitate formation is observed. However, for the same annealing temperature, the precipitate size and density are lower for LTG-$Al_{0.3}Ga_{0.7}As$ than that found in LTG-GaAs.

Electrical characterization of LTG-$Al_{0.3}Ga_{0.7}As$ film utilizing a metal-insulator-semiconductor (MIS) structure yielded a resistivity of 1.8×10^4 Ω-cm and 6×10^{11} Ω-cm for unannealed and 600°C annealed films, respectively. This resistivity is about three orders of magnitude higher than that found in LTG-GaAs. A study of the transport through annealed LTG-$Al_{0.3}Ga_{0.7}As$ film, using an n-LTG-n structure, revealed that similar to LTG-GaAs, low fields the conduction is dominated by hopping conduction through a defect band; and at high field, is space charge limited.

Temperature-dependent conductivity measurements have identified a donor-like defect with an activation energy of 0.96 ± 0.03 eV [19]. Drawing from the similarity between the structural and transport property of LTG-$Al_{0.3}Ga_{0.7}As$ to that of LTG-GaAs, it is expected that point defects, such as As_{Ga}, As_i and V_{Ga} exist in LTG-$Al_{0.3}Ga_{0.7}As$ with comparable quantity. However, systematic measurements of exact concentrations and associated energy levels of these defects still await further studies.

In the next section of the chapter, a material property that has direct bearings on the application of the material to devices, its *interfacial property*, has been investigated. The dependence of the interfacial property, such as the band-bending, as a function of growth and annealing temperature is reported. Drawing from the reported bulk material properties of the previous two section, a simple hypothesis for the behavior of the band-bending is proposed. The work in this next section was undertaken at UCSB by the author, with the assistance of James Ibbetson in the sample growth and transmission electron microscopic work.

2.4 Interfacial Property of LTG-$Al_{0.3}Ga_{0.7}As$ Passivation:

The strong dependence of material properties on the processing parameters, growth and annealing temperatures, of LTG materials lends itself naturally to the engineering of the materials in device application. In particular, the high resistivity and high breakdown field strength of LTG-$Al_{0.3}Ga_{0.7}As$ make it a potential ideal electrical passivation layer for GaAs device and materials. However, initial efforts to incorporate such passivation layer into a field effect transistor device structure were hampered by a detrimental diffusion of defects and precipitates into the channel during the annealing process of the LTG layers. This diffusion, in turn led to a strong depletion of the carriers in the channel and rendered the channel useless. However, a solution to this problem was soon found - an insertion of a thin undoped AlAs layer

between the LTG passivation layer and the active channel of the device would protect the active channel effectively [20]. The AlAs diffusion barrier, of thickness between 100Å to 200Å, has shown to be effective up to annealing temperature of ~650°C. Recently, other effective diffusion barriers of different materials such as InGaP and AlGaAs/GaAs superlattices have also been reported [21].

While the diffusion barrier has been sufficient in preserving the integrity of the active layer in a device, and therefore allowing the successful incorporation of LTG materials into device structures, it has also brought about other technological issues that raised other concerns. In particular, for LTG-$Al_{0.3}Ga_{0.7}As$, the thin AlAs diffusion barrier layer had led to an intriguing observation at the interface of the LTG-$Al_{0.3}Ga_{0.7}As$ and itself. This phenomenon is best illustrated in a cross-sectional transmission electron micrograph of a nominal device structure, as shown in figure 2.3. Clearly observable in the figure, the interface of LTG-$Al_{0.3}Ga_{0.7}As$ and AlAs is decorated with a much higher concentration of As precipitates in comparison to that found in the bulk of the LTG-$Al_{0.3}Ga_{0.7}As$ layer on top, and the underlying active channel is precipitate free.

From a device standpoint, the observed accumulation of excess As precipitates at the interface raises question about its effect on the device characteristics and performance. In addition, since the properties of LTG-$Al_{0.3}Ga_{0.7}As$ are strongly dependent on the growth and annealing temperatures; the effect of these process parameters on the interface, and in turn on device characteristics, is of great importance. A clear understanding and handle on these effects would yield valuable insights into the suitability of LTG-$Al_{0.3}Ga_{0.7}As$ as a passivation layer for GaAs field effect transistors. In this work, a focused empirical study of the interfacial

barrier, or more accurately the channel band-bending, as a function of the growth and annealing temperature space has been carried out.

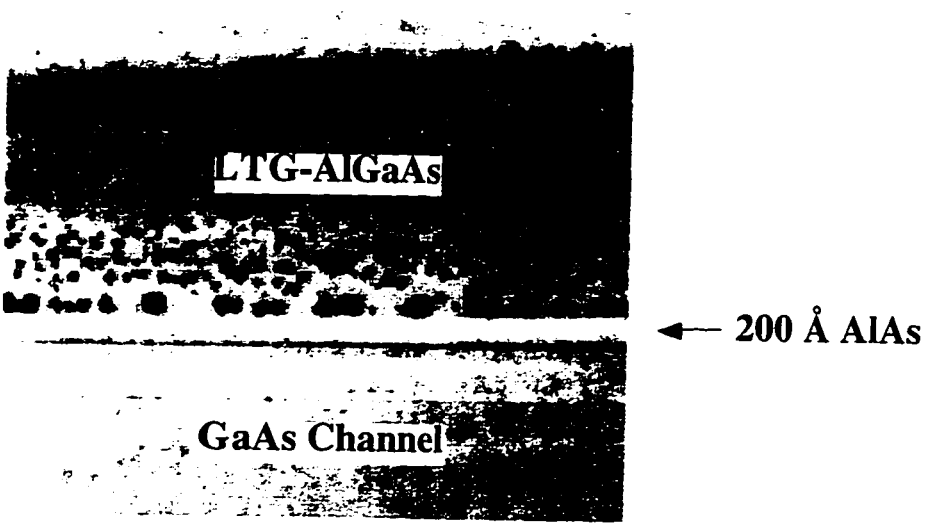


Figure 2.3: Cross-sectional transmission electron micrograph of a device structure with an annealed LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer on top. Arsenic precipitates are seen as black dots in the micrograph. The AlAs diffusion barrier is shown to be effective in preventing the precipitates from diffusing into the device channel. An excess amount of As precipitates decorating the LTG-$Al_{0.3}Ga_{0.7}As$/AlAs interface is also clearly shown [Courtesy of J. P. Ibbetson].

2.4.1 Basic Concept of Experiment:

Normally, in order to determine the channel bend-bending of a heterostructure device, knowledge of the *bulk* Fermi level of each epitaxial layer (usually determined independently) along with the hetero-interface band offsets at all the relevance interfaces of the whole structure would be sufficient. However, in a heterogeneous material system such as that of LTG-$Al_{0.3}Ga_{0.7}As$, the bulk Fermi level is difficult to determine accurately, and the interface between the LTG layer to that of the normal epitaxial layer is still an unresolved question of the material properties. In this work, we have performed a direct electrical measurement of the channel band-bending.

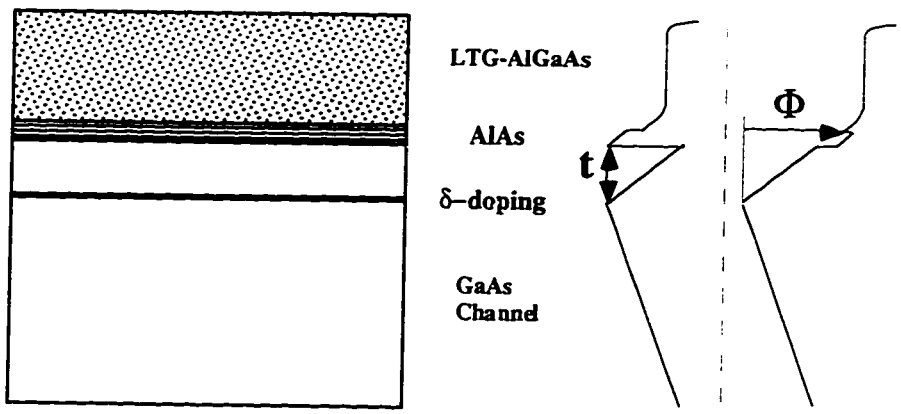


Figure 2.4: Schematic cross section of a δ-doping channel structure, with LTG-AlGaAs passivation on top, used in the study of the interfacial properties of LTG-AlGaAs to the normal channel. A *possible* corresponding band-diagram is shown on the right.

The experiment makes use of a nominal δ-doped channel structure shown in Figure 2.4. Typical epitaxial passivation layers of LTG-$Al_{0.3}Ga_{0.7}As$ were grown on top of the active channel of the device. An independent calibration of the δ–doping density was performed in a different experiment to ensure the accuracy of the correlation between the measured sheet charges and the channel band-bendings. Drawing from figure 2.4, the band-bending,Φ, is directly proportional to the depleted charges in the channel, through the Poisson equation,

$$\Phi = qN_{depleted}\left(\frac{t_{GaAs}}{\varepsilon_{GaAs}} + \frac{t_{AlAs}}{\varepsilon_{AlAs}}\right)$$

where $N_{depleted}$ is the total depleted sheet charge of the channel and t are the respective thicknesses of the undoped layers. Using the above test structure, the effective channel band-bendings, with different LTG-$Al_{0.3}Ga_{0.7}As$ passivation layers, were deduced from the measured sheet charges via the Van der Pauw method.

2.4.2 Effect of Growth and Annealing Temperatures:

Three samples with similar epistructures, except for the growth temperatures of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation layers, have been studied. They were grown in an Intevac Gen II solid source MBE system. The structure consisted of a 5000Å undoped GaAs buffer layer, then a Si δ-doped channel of $1.4x10^{12}$ cm^{-2}; followed by a 500Å layer of undoped GaAs, then 200Å of AlAs and 25Å of GaAs. All these layers were grown at 590°C. The 25Å of GaAs was grown to prevent contamination during the cool-down and to present a clean surface for subsequent growth. Then, the substrate temperature was lowered to a predetermined temperature for the growth of the LTG layers. First, 25Å layer of LTG-GaAs was grown, and then followed by a 2000Å layer of LTG-$Al_{0.3}Ga_{0.7}As$. The 25Å layer of LTG-GaAs was grown first to provide a smooth transition surface for the growth of the LTG-$Al_{0.3}Ga_{0.7}As$ layer. The growth was finished with a 50Å layer capping of LTG-GaAs on top of the whole structure. The growth procedure and parameters of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation layers used in this experiment are designed to be identical to those used in the actual GaAs FET with LTG materials passivation, so that the data obtained from this experiment are of direct relevance to the channel band-bending in the FET structures.

Following growth, the wafers were cleaved into 6x6 mm^2 samples. Annealings (ex-situ) of these samples were performed in an AG & Associates Rapid Thermal Annealing (RTA) unit with flowing forming gas (90% N_2 and 10% H_2) for 1 minute. A typical annealing ramp cycle is shown in figure 2.6. Table 2.1 tabulates the growth and annealing temperature conditions that have been investigated. After annealing, the samples were then processed for mesa isolation of the Van der Pauw pattern; and lastly ohmic contacts were deposited using e-beam evaporation.

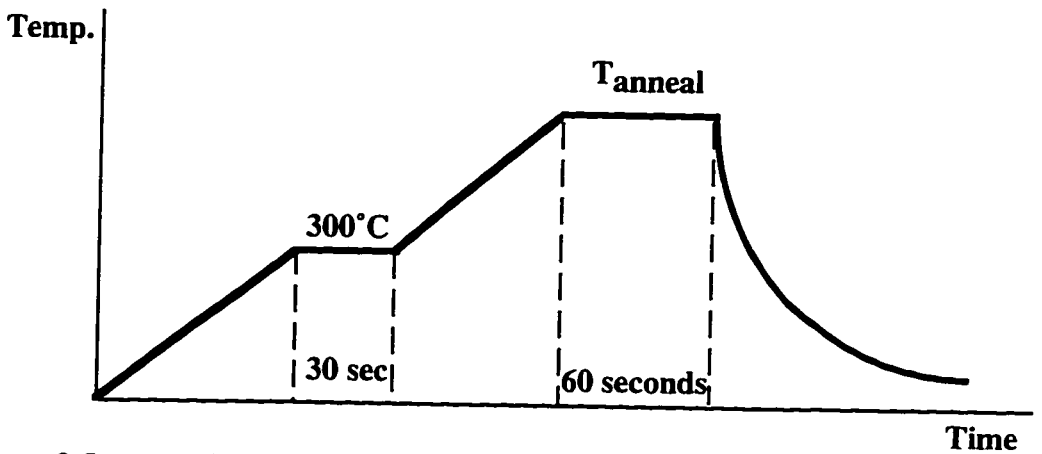


Figure 2.5: Annealing ramp-schedule of the LTG-$Al_{0.3}Ga_{0.7}As$ layers with flowing forming gas (90% N_2 and 10% H_2) ambient.

Table 2.1: Summary of the growth and annealing temperatures of the LTG-$Al_{0.3}Ga_{0.7}As$ layers studied. T_{anneal} is the highest temperature of the annealing cycle shown in Figure 2.5

T_{growth} \ T_{anneal}	425°C	450°C	475°C	500°C	525°C	550°C	575°C	600°C	625°C	650°C
245°C	X	X		X		X		X		X
270°C	X	X	X	X	X	X	X	X	X	X
305°C	X	X		X		X		X		X

The deduced effective channel band-bending (Φ) as a function of growth and annealing temperatures from the measured Van der Pauw data are shown in figure 2.6. The annealing temperature range from 425°C to 650°C. The 425°C lower limit is a consequent of the ohmic alloying temperature for the samples (which is typical in ohmic contacts for conventional GaAs devices); and the upper limit of 650°C has been independently verified as the material limit where the AlAs layer still behaved reliably as an As diffusion barrier. A strong dependence of the channel band-bendings on both the growth and annealing temperatures is observed. Furthermore, this dependence is

also erratic, making it difficult to directly correate the interfacial property to that of the reported bulk material properties. Further studies are needed before conclusions about the nature of the interface can be drawn. In addition, a set of control data obtained from a sample with the passivation layer selectively etched off are also shown in the figure. The channel band-bending of the control data is shown to be relatively independent of the annealing temperatures, this is could be view as an indication of the margin of error in our measurement..

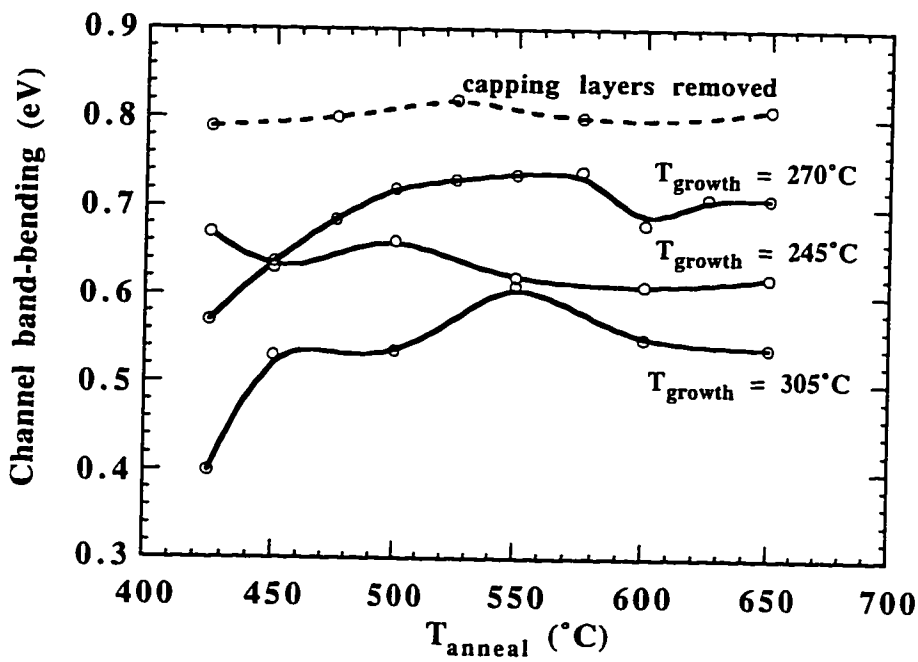


Figure 2.6: Deduced GaAs channel band-bendings due to growth and annealing temperatures of the LTG-$Al_{0.3}Ga_{0.7}As$ layer. The dashed curve is from a sample with the LTG-$Al_{0.3}Ga_{0.7}As$ and AlAs layer selectively etched off by wet chemicals (sample T_{growth} =270°C).

In comparison to LTG-GaAs, of which a plot of the nominal Fermi level as a function of annealing temperatures is shown in figure 2.7, the behavior of the channel band-bending with LTG-$Al_{0.3}Ga_{0.7}As$ passivation as is markedly different. LTG-

$Al_{0.3}Ga_{0.7}As$ passivation resulted in channel band-bendings that are sensitively depended on the detailed growth and annealing temperatures. From a device engineering point of view, these results indicated that different LTG-$Al_{0.3}Ga_{0.7}As$ materials passivation should have different impacts on device characteristics; in particular, parasitic resistances and low-frequency noise would be intimately influenced.

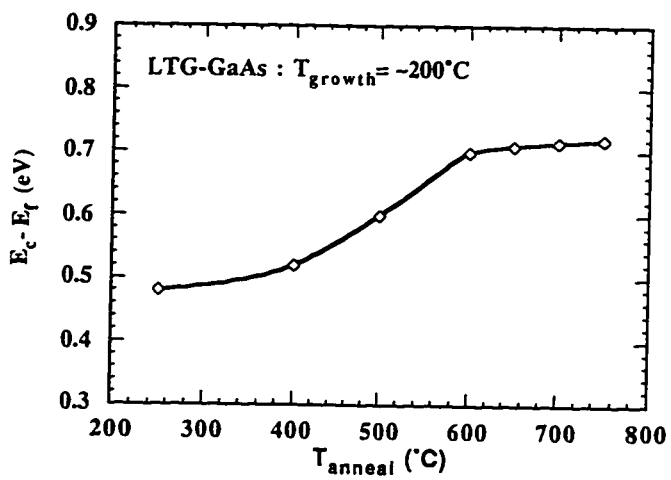


Figure 2.7: Typical Fermi level of bulk LTG-GaAs as a function of annealing temperatures [21].

At equilibrium, the channel band-bending is governed by the Fermi level of the system at the interface between the LTG passivation layer and the rest of the channel. As illustrated in figure 2.3, and again on another sample grown at 270°C shown in figure 2.8, this annealed interface is decorated with a high density of As precipitates.

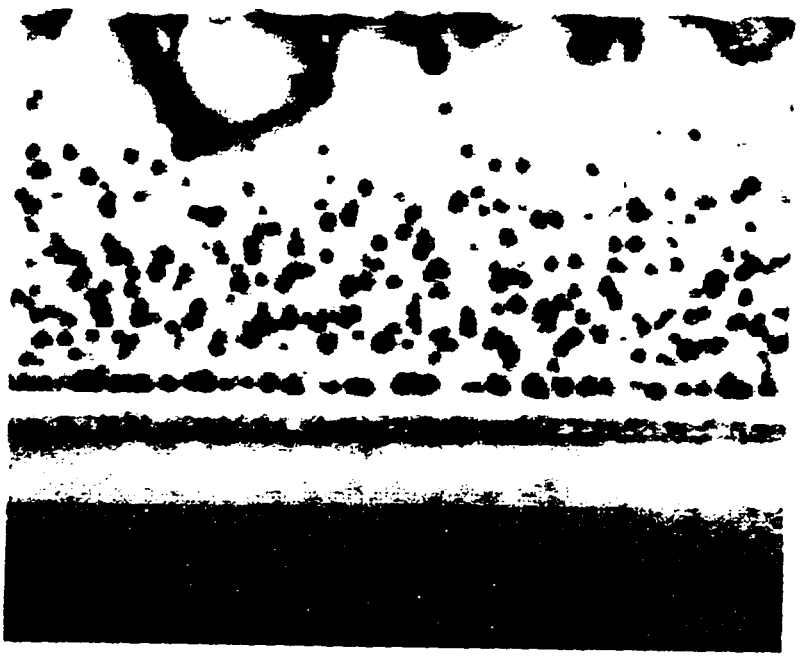


Figure 2.8: Cross-sectional TEM of an LTG-$Al_{0.3}Ga_{0.7}As$ passivated sample grown at 270°C and annealed ex-situ using a RTA unit for 1 minute at 600°C. The interface of the LTG-$Al_{0.3}Ga_{0.7}As$-AlAs layer are shown to be decorated with excess As precipitates (similar to figure 2.3) [Courtesy of J. P. Ibbeson].

However, the data shown in figure 2.6 for samples of different growth temperatures clearly do not converge to a single value for the channel band-bending (i.e., a single Fermi level). Taking into consideration the above channel band-bending data along with the cross-sectional transmission electron micrographs (figure 2.3 and figure 2.8), a picture that emerge from these data is that the precipitates alone are not sufficient to determine the Fermi level of the system, the point defects also played a very significant role. Using the condition of charge neutrality, and nominal reported concentration of deep donors and deep acceptors concentration (annealed LTG-GaAs), it is seen that *some* of the variation of the Fermi level can be accounted for by the change of concentration of defects as a function of annealing temperatures (figure 2.9). However, although the calculation showed a plausible range of change in Fermi level, the magnitude is slightly off. This offset could be due to the uncertainty in the

energy levels of these point defects. Further analysis to isolate the contribution from these precipitates and point defects required more detailed investigations (i.e., corresponding measurements of the defect concentrations *at the interface*). This might not be possible, or very difficult to achieve; since this is an inherrent properties of the LTG materials: the co-existence of both As precipitates and point defects in annealed LTG materials.

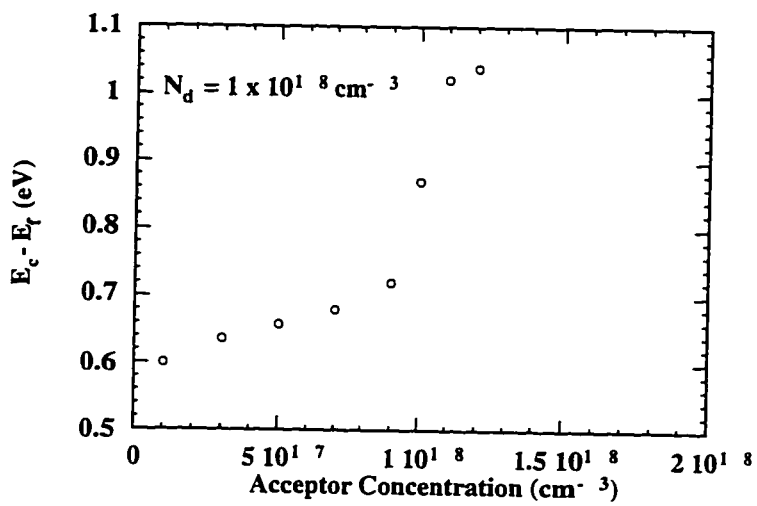


Figure 2.9: Calculated values of the Fermi level as a function of deep acceptors concentration (E_a= 0.3 eV from the valence band) using the condition of charge neutrality with the deep donors assumed to be $1x10^{18}$ cm^{-3} (E_d = 0.65 eV from the conduction band).

2.5 Summary :

Established materials properties that are relevant to electronics devices were reviewed in this chapter. Materials science investigation in recent years have demonstrated that LTG-GaAs consist of a high concentration of point defects. The dominating active defects have been identified as As_{Ga} and V_{Ga}, deep donors and deep acceptors, respectively. Furthermore, the concentrations of these defects have been demonstrated to be a strong function of both growth and annealing temperatures.

Further research are needed before a clear picture of a correlation between the materials properties and processing parameters could be drawn. Meanwhile, the strong dependence of the electrical properties on growth and annealing temperatures of LTG-GaAs could readily be exploited to tailor the materials to yield desired property in their applications to device. Furthermore, emerging derivatives of LTG-GaAs, such as LTG-$Al_{0.3}Ga_{0.7}As$ promised yet even better potentials for device engineering.

Interfacial characteristics between the LTG-$Al_{0.3}Ga_{0.7}As$ passivation and the underlying normal GaAs channel has been systematically investigated. For device application, the data from Figure 2.6 provided a useful map of the parameter spaces for device designing with LTG-$Al_{0.3}Ga_{0.7}As$ materials. Effective channel band bending of device can be readily inferred from the growth and annealing temperatures of the LTG-$Al_{0.3}Ga_{0.7}As$ from this figure.

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CHAPTER 3

Surface Layer Engineering to Improve Breakdown Voltage

3.1 Introduction:

The surface plays a crucial role in the characteristics of compound semiconductors devices, in particular high frequency devices. As of present, the performance, uniformity, and therefore the cost of reliable microwave power FETs has been limited by the non-reproducibility of the gate diode characteristics. The main reason for this is the lack of effective electrical passivation of the GaAs surface adjacent to the gate. In particular, the breakdown voltage of GaAs MESFET critically depends on the surface condition. Over the years, many efforts have been devoted into finding a viable solution to this fundamental problem. From a technological standpoint, the simplest solution for this problem would be to develop a controllable and reliable passivation technology for GaAs devices and materials. This is the approach that we have pursued over the course of this project.

An optimal passivation technology would be one that provides both environmental and electrical isolation of devices to external stimuli. As of present, SiN_x has been clearly demonstrated to be the most suitable environmental passivation layer in terms of preventing the change of the surface properties due to oxidation and humidity. It has been widely accepted by industry as the general environmental passivation layer for all electronic devices. However, an effective electrical passivation technology, on the other hand, has been much more elusive.

To date, the most successful electrical passivation for the surfaces of devices are those by chemical treatment. Photochemical oxidation and sulfide chemical passivation such as Na_2S and $(NH_4)_2S$ [1], have been demonstrated to have the most

potential. However, these chemical treatments still leave devices susceptible to non-uniformity and thermal instabilities. Furthermore, these technologies are inflexible to surface engineerings for device optimization. Therefore, an alternative, stable electrical passivation technology that is susceptible to surface engineering, is still very much sought after.

As discussed in Chapter 2, the electrical properties of LTG materials and their strong dependence on processing parameters, presented the materials as ideal candidates for the aforementioned sought after passivation technology. In this chapter, device surface engineering utilizing LTG passivation to improve breakdown voltage in GaAs MESFET is studied in detail. The first section of the chapter provides a synopsis of the problem of breakdown in GaAs power MESFET. Then the application of LTG materials passivation to improve the breakdown voltage is presented and discussed. A physical model of the LTG material passivation, compensated deep donors (CDD) model, is proposed to explain the field redistribution obtained with passivated devices. This field redistribution would explain the experimentally observed improvement in the gate-drain breakdown voltage of LTG materials passivated FETs. A more quantitative study of the model has also been pursued. A full two dimensional electrostatic simulation and analysis of the device structures with LTG-GaAs passivation was performed. The results are presented and discussed.

3.2 Breakdown Voltage in GaAs Power MESFET:

In general, breakdown in MESFETs occurs when the voltage supported by the depletion layer under the gate metal, and its associated electric field reach a critical limit of the material. When this happen, the resultant avalanche generation of

carriers by impact ionization leads to device failure. Analytically, avalanche breakdown is defined as the point when multiplication of carriers in the depletion region by impact ionization rate reach infinity. Details of avalanche breakdown physics can be readily found in many texts on semiconductor device physics .

For a thick channel device, the depletion region extended downward into the channel, and the breakdown is essentially one dimensional, as shown schematically in figure 3.1a. The breakdown voltage could be analytically computed using Poisson's equation and data from empirically measured critical field of the semiconductor channel involved. One dimensional breakdown voltage as a function of the doping concentration is shown in figure 3.1b.

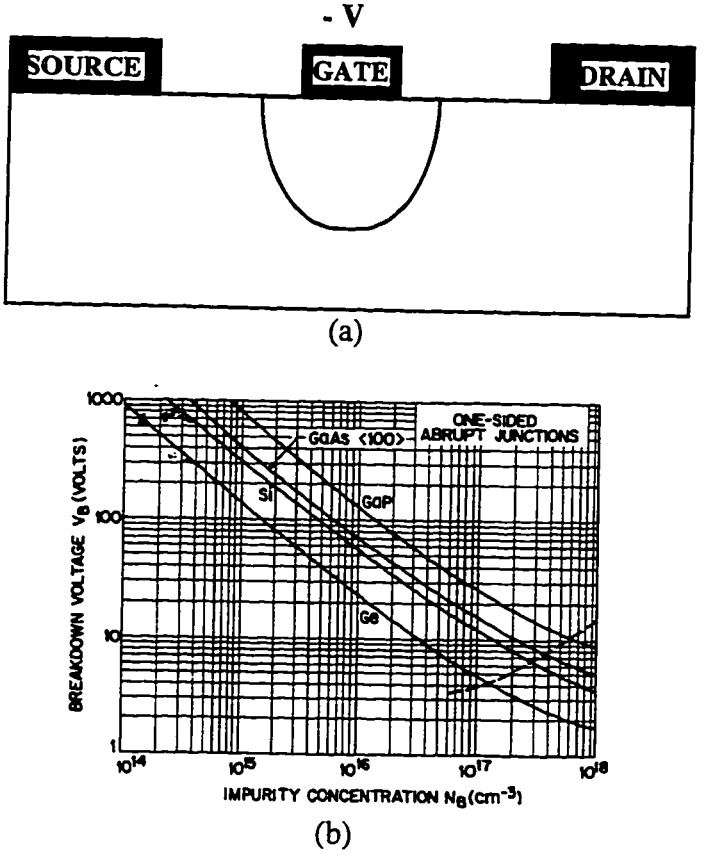


Figure 3.1: a) Schottky gate depletion of a thick channel FET structure - the depletion extended downward into the channel until breakdown occurs (i. e., when

the field at the metal-semiconductor reached the critical field strength). b) One dimensional avalanche breakdown voltage as a function of doping for an abrupt junction.

However, for a thin channel structure, after reaching through the channel and into the buffer, the depletion region extends *laterally* toward the drain contact (shown schematically in figure 3.2). Therefore, the breakdown problem is two dimensional. The voltage that can be supported by such two dimensional depletion region is much higher than that of the one dimensional case, with values depending upon the thickness of the channel. However this simplistic approach to improving the breakdown voltage of FETs is accompanied by a substantial reduction in the channel current density (thinner channel); thereby rendering the approach ineffective for high power devices.

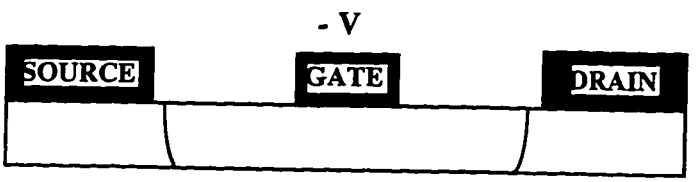


Figure 3.2: Gate depletion in a thin channel structure; the depletion region extends laterally toward the drain after pinching-off the channel - the field distribution is inherrently two dimensional.

The compromising boundary, where the designed device would yield an optimized product of the breakdown voltage and the channel current would resulted in a device structure with a maximum channel current density of 400-450 mA/mm. With this design, the channel delivered the maximum possible current while retaining a *two dimensional* gate depletion characteristics. The breakdown voltage in such structure is very sensitive to the top surface boundary condition of the device. It is

the breakdown characteristics of this high-power device structure on which we have focused our research and development (figure 3.3).

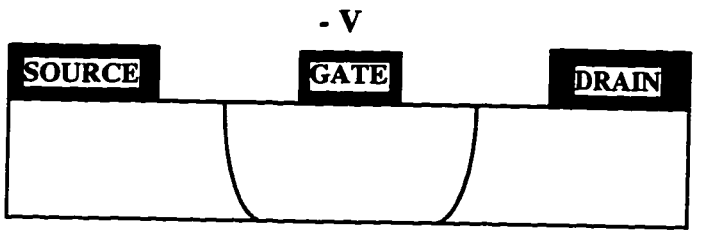


Figure 3.3: High power FET channel design where a compromise between the maximum drain current density and the breakdown voltage is achieved - the depletion region extends slightly toward the drain, and its exact characteristics depends sensitively on the top surface condition.

3.3 Breakdown Voltage Improvement by LTG Materials Passivation:

The advent of LTG materials and their unique properties presented an ideal solution to the aforementioned search for an ideal electrical passivation layer for GaAs devices and materials (discussed in Chapter 1). In effect, the LTG passivation layer presented a top surface boundary condition that can be engineered to deliver desired device characteristics. Indeed, experimental realization of MESFET with LTG-GaAs passivation were soon demonstrated. Subsequently, record breakdown voltage and power performance GaAs-based FETs were reported. But consistent reproducibility of these results has been difficult due to the large parameter space of the LTG materials involved, and also a lack of clear understanding of the exact mechanism that led to high breakdown voltage observed in passivated devices. It is generally hypothesized that the LTG-GaAs passivation acts as a *charges absorber* needed to alleviate the peak gate field [2]. However, a physical model to explain this charge absorption mechanism of the LTG materials awaits further understanding and data from the materials science research.

Recent developments in material science of LTG-GaAs have led us to believe that the compensated deep donor (CDD) of the LTG material is the main cause of the observed improvement in the gate-drain breakdown voltage of the LTG-GaAs passivated FETs. Referring back to the discussion in Chapter 2 on electrical material properties of LTG materials, there are two dominant and unique material properties of LTG-GaAs that are critical to the effectiveness of this passivation technology. First, the materials contained a high concentration of both type of point defects, deep donors and deep acceptors, As_{Ga} and V_{Ga}, respectively. Second, the deep donor concentration is always higher than that of the deep acceptors. At equilibrium, the Fermi level of this material system is determined by the condition of charge neutrality:

$$n_e + N_a^- = n_h + N_d^+$$

where

$$n_e = N_c \exp[-(E_c - E_f)/kT]$$
$$n_h = N_v \exp[-(E_f - E_v)/kT]$$

and

$$N_a^- = \frac{N_a}{1 + \frac{1}{g}\exp[(E_a - E_f)/kT]}$$

$$N_d^+ = \frac{N_d}{1 + g\exp[(E_f - E_d)/kT]}$$

A schematic band diagram of such a system is shown in figure 3.4. As illustrated in the figure, the deep acceptors are completely filled, but the deep donors are only partially filled. The density of empty donors, the compensated deep donors, is equal to the density of the deep acceptors in the system. In a device structure, these compensated deep donors provides the needed empty states for the absorption of negative charges being injected from the gate metal. In effect, they

plays a similar role to that of the empty localized surface states reported by Barton *et al* [3].

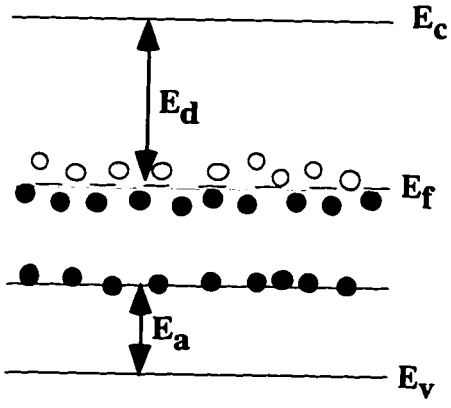


Figure 3.4: Schematic band diagram of LTG-GaAs with both deep acceptors and deep donors, the compensated deep donors are shown as empty states above the Fermi level.

Qualitatively, the compensated deep donors in the LTG passivation layer enables the layer to be effectively charged in the vicinity of the gate. This in turn leads to an alleviation of the peak field at the drain-end of the gate metal, thereby increasing the voltage that the device can accommodate before reaching the critical breakdown field. Mathematically, this is equivalent to a change of the boundary conditions of the electrostatic problem of the device; which can therefore dramatically alter the associated electric field distribution. Furthermore, a recent study by Ibbetson *et al* [4] has also demonstrated that the compensated deep donors led to a charge redistribution in the LTG-GaAs layer under high field. The study demonstrated that, at sufficient field strength, where the space-charged-limited transport is dominated, the CDD resulted in a development of extended space charges throughout the LTG materials. This phenomenon is schematically illustrated in figure 3.5.

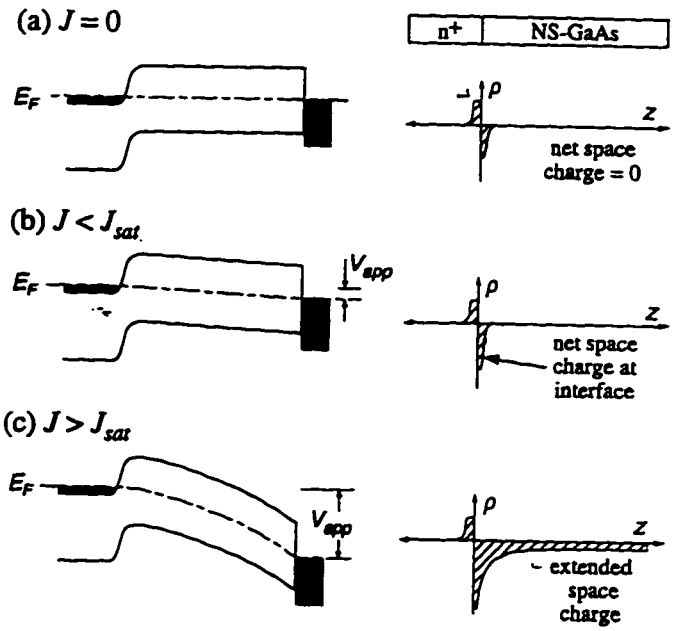


Figure 3.5: Space charge distribution in LTG-GaAs under applied field : a) in equilibrium, b) under low bias and c) under high bias. An extended space charge is developed throughout the LTG-GaAs layer under high field [From [4]]

It should be note here that the discrete trap levels nature of this compensated deep donors model is a simplification of the actual LTG materials properties; for there is recent evidence that the defect actually forms a band rather than discrete levels. Nevertheless, the general physics of the field alleviation by empty states, provided by the compensated deep donors of the model, would still remain valid.

3.4 Two Dimensional Electrostatic Simulation of LTG-GaAs Passivation:

In order to confirm and to quantify the proposed model of the breakdown voltage improvement in LTG passivated MESFET by compensated deep donors, a full two dimensional electrostatic analysis of nominal device structures has been performed. A commercially available two-dimensional device simulation program, Silvaco's BLAZE, was used for this purpose. However, due to the uncertainty in many physical parameters, such as mobility, saturation velocity, impact ionization

rate, and density and energy level of the point defects in LTG-GaAs, no attempt was made to match the simulated device results to those obtained experimentally. The simulations are sought to provide further insights into the effect of LTG-GaAs passivation rather than to quantify its effect on the device numerical figures-of-merit.

3.4.1 Basic Semiconductor Equations :

The Silvaco's BLAZE program self-consistently solves a set of two dimensional equations. These equations governs the current-voltage distribution throughout the device structure. They are the *Poisson equation*, carriers *current continuity* equation, and *drift-diffusion* transport equation:

$$\mathrm{div}(\varepsilon \nabla \Psi) = -\rho \qquad \textit{Poisson Equation}$$

where Ψ is the electrostatic potential, ε is the permittivity, and ρ is the charge density.

$$\frac{\partial n}{\partial t} = \frac{1}{q}\mathrm{div}\vec{J}_n + G_n - R_n$$
$$\frac{\partial p}{\partial t} = \frac{1}{q}\mathrm{div}\vec{J}_p + G_p - R_p \qquad \textit{Current Continuity Equation}$$

where n and p are the electron and hole concentration, J_n and J_p are the electron and hole current densities, G_n and G_p are the generation rate for electrons and holes, R_n and R_p are the recombination rates for electrons and holes, and q is the magnitude of the charge on an electron.

$$\vec{J}_n = nq\mu_n\vec{E} + qD_n\nabla n$$
$$\vec{J}_p = pq\mu_p\vec{E} - qD_p\nabla p \qquad \textit{Drift-Diffusion Equation}$$

D_n and D_p are the diffusion coefficients for electron and hole respectively; and the rest of the symbols are as defined above.

Carrier recombination via trap centers with a fixed lifetime is included in the simulation through the Shockley-Read-Hall model. Generation rates due to impact ionization are specified as :

$$G = \alpha_n \frac{|J_n|}{q} + \alpha_p \frac{|J_p|}{q} \qquad \text{where} \quad \alpha_{n,p} = A_{n,p} \bullet \exp\left[-\left(\frac{E^c_{n,p}}{E}\right)^m\right]$$

The constants A and E^c are obtained experimentally for GaAs material : $A=1.9\text{x}10^5$ cm^{-1}, $B=5.75\text{x}10^5$ V/cm, and m=1.82 for electrons; and $A=2.22\text{x}10^5$ cm^{-1}, $B=6.57\text{x}10^5$ V/cm, and m=1.75 for holes.

LTG-GaAs material was defined as normal GaAs with both deep donors and deep acceptors in the material. Various defect densities of (1-1.4) x 10^{18} cm^{-3} and (0.1-1) x 10^{18} cm^{-3} were specified for donors and acceptors, respectively. These densities corresponds to the reported experimental data for annealed LTG-GaAs.

3.4.2 Simulation Results and Analysis:

The cross-sectional structures of the MESFET used in the simulation are shown in figure 3.6. The channel composition and geometric dimensions for all device structures are the same, and they resembled the actual samples as much as possible. The channels are all 1500Å thick, doped 3 x 10^{17} cm^{-3} with silicon. Geometrically, a gate length of the simulated structure is 1μm, and the gate-source and gate-drain spacings of 2 μm were used. For a control device, a structure with an undoped GaAs passivation layer, and a thin layer of top surface traps, density of $1\text{x}10^{12}$ cm^{-2}, for both deep donors and deep acceptors have been simulated.

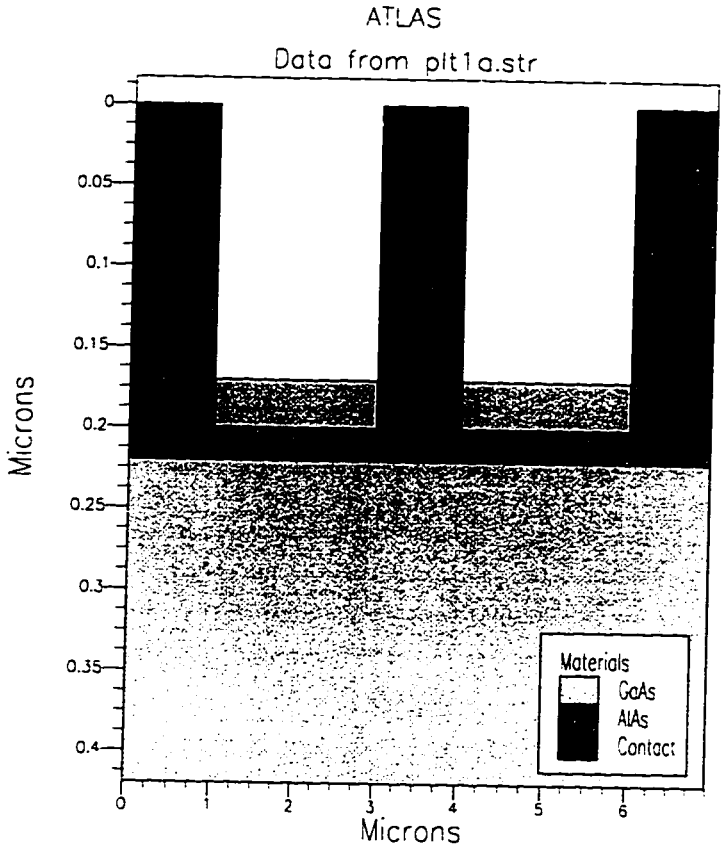


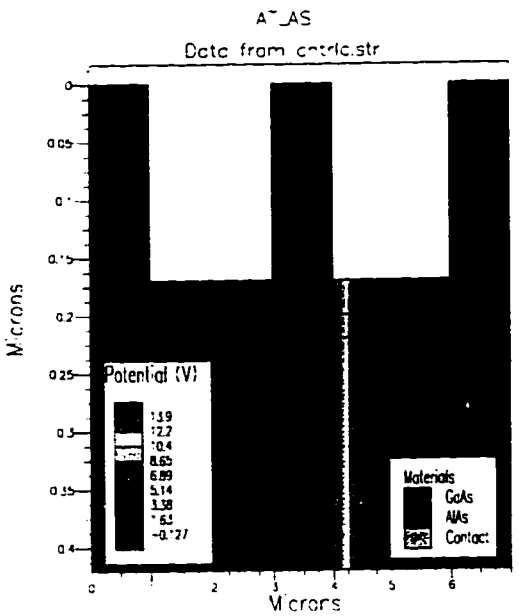
Figure 3.6: Cross section of device structures used in the two dimensional electrostatic simulations. The vertical dimension is the depth profile of the device, and the lateral is the source/drain profile. Geometric dimensions are: 1 μm gate length, and 5 μm source-to-drain spacing. The channel is 1500 Å of n-GaAs doped $3x10^{17}$ cm^{-3}.

The compensated deep donors model of LTG-GaAs proposed in the previous section suggested that the two material parameters that would strongly affect the field alleviation mechanism of LTG-GaAs are the deep acceptors concentration and the energy level of the deep donors. In order to verify this hypothesis, simulations with different deep acceptor density (which is equivalent to the compensated deep donors density) were performed. A table of the simulated parameters are summarized in Table 3.1.

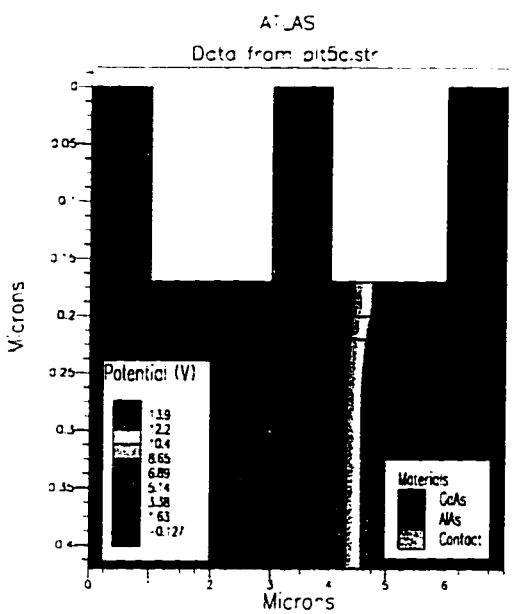
Table 3.1 : Summary of trap parameters used in the device simulation.

N_d (cm^{-3})	N_a (cm^{-3})	$E_c - E_d$ (eV)	$E_a - E_v$ (eV)
1.0×10^{18}	1.0×10^{17}	0.7	0.3
1.0×10^{18}	3.0×10^{17}	0.7	0.3
1.0×10^{18}	5.0×10^{17}	0.7	0.3
1.0×10^{18}	7.0×10^{17}	0.7	0.3
1.0×10^{18}	9.0×10^{17}	0.7	0.3
1.2×10^{18}	7.0×10^{17}	0.7	0.3
1.4×10^{18}	7.0×10^{17}	0.7	0.3
1.0×10^{18}	7.0×10^{17}	0.5	0.3
1.0×10^{18}	7.0×10^{17}	0.3	0.3

Figure 3.7 shown a nominal potential distribution for two device structures, one is the control sample and the other is with simulated LTG-GaAs passivation ($N_d = 1 \times 10^{18}$ cm^{-3} and $N_a = 7 \times 10^{17}$ cm^{-3}). The potential differences between gate to drain contacts for both structures were 15 V. In the control sample, the region of largest potential difference is clearly seen at the drain edge of the gate metal, hence a peak electric field at that point. However, with simulated LTG-GaAs passivation, the electrostatic potential is shown to spread out over a longer distance, thus resulting in a lowered peak electric field at the same locale.



(a)



(b)

Figure 3.7: Simulated two dimensional electrostatic potential distribution with a) undoped GaAs passivation; b) LTG-GaAs passivation (defined with N_d = $1x10^{18}$ cm^{-3} and $N_a = 7x10^{17}$ cm^{-3}).

Systematic simulations of the gate-drain breakdown voltage dependence on the deep acceptors are shown in Figure 3.8. As expected from the compensated deep donor model, the breakdown voltage is a strong function of the deep acceptors density. An improvement of over 75% (12V versus 6.8V) in term of breakdown voltage is observed in figure 3.8. Furthermore, in order to verify that it is the empty states of the compensated deep donors that play the central role in field alleviation and not the total deep donors concentration, a simulation where the deep acceptors concentration were fixed while the deep donors concentration varied were performed. A few selected breakdown voltages as a function of the total deep donors concentration are shown in figure 3.9. The curves showed the breakdown voltages dependence on the total deep donors concentration to be negligible.

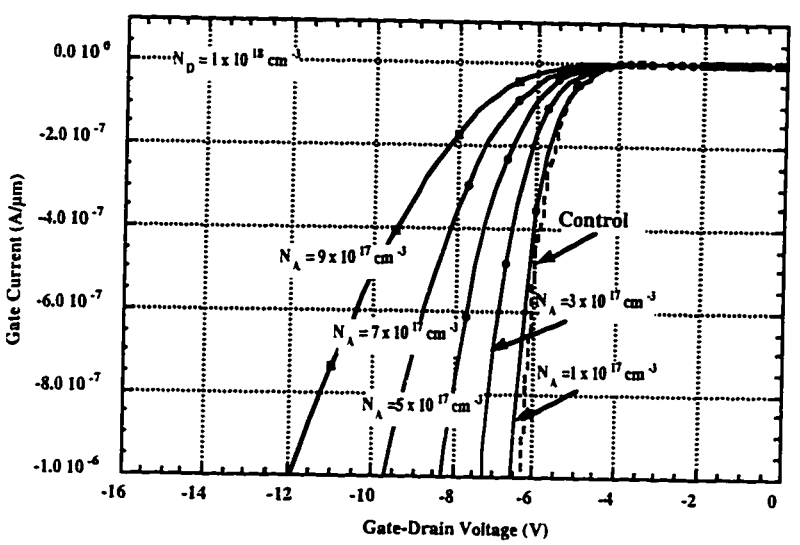


Figure 3.8: Breakdown voltage as a function of deep acceptor concentration of LTG-GaAs. The control sample is defined as having undoped GaAs passivation with just surface traps (N_a=1x10^{12} cm^{-2} and N_d=1x10^{12} cm^{-2})

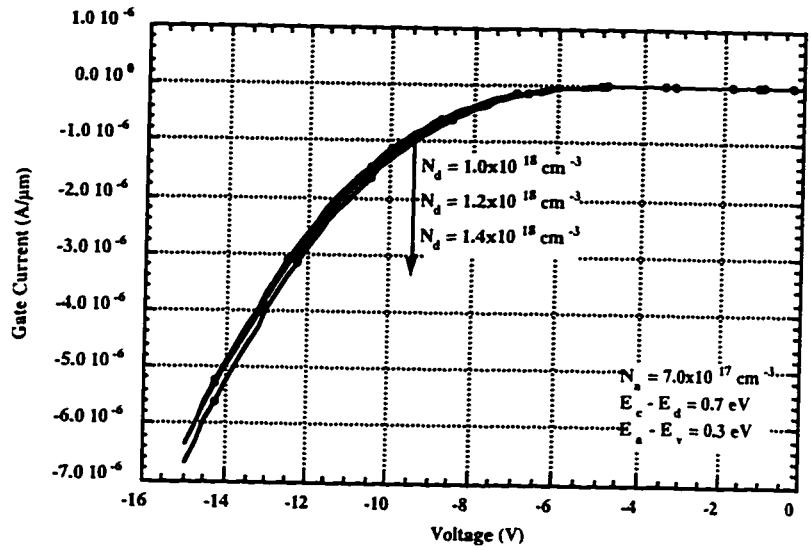


Figure 3.9 : Breakdown voltage dependence on deep donnor concentration of LTG-GaAs. Other parameters of the simulated LTG-GaAs are shown in the inset.

In addition to trap concentrations, the breakdown voltage dependence on the deep donor energy levels were also performed. The effect of the donor levels on breakdown voltages is shown in figure 3.10. For the same concentration of defects in LTG-GaAs, it is seen that the deep donor level at 0.7 eV resulted in an optimal breakdown voltage. Qualitatively, this observation can be explain by the efficiency of the capturing and emission of electrons by the traps; in addition, it is also consistent with our proposed model of CDD. The deep donor level at midgap (0.7 eV) would result in the maximum capture time of the electrons (i.e. maxium retention of electrons) by the CDD traps, hence making the alleviation of the peak field by the LTG passivation most efficience. As this electron trap level gets shallower, re-emission of electrons from the trap increased, thereby drastically reducing the field alleviation efficency of the LTG layer.

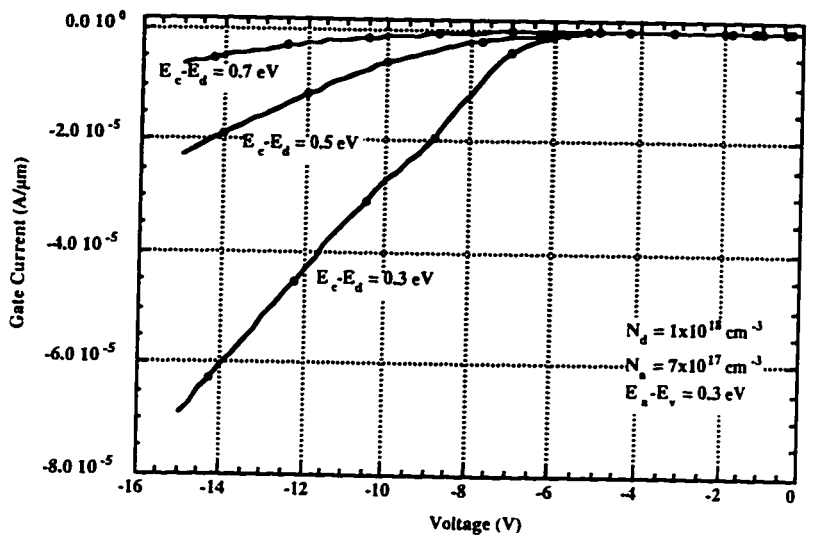


Figure 10: Breakdown characteristics versus deep donor energy levels in simulated LTG-GaAs. The lowest breakdown is achieved with the donor at midgap. The concentrations and deep acceptor energy levels are indicated in the inset.

3.5 Summary :

The present chapter focuses on the physics of the breakdown voltage in GaAs microwave power FETs. In an optimally designed FET structure for high output power, the electrostatic distribution of the device is inherrently two dimensional. Furthermore, this electrostatic distribution depended sensitively on the boundary conditions of the structure. In term of device engineering, these dependences meant that the breakdown voltage of a FET structure is very sensitive to its surface conditions. Consequently, the proper engineering of the surface passivation layer, or equivalently the *boundary condition*, could lead to dramatic improvement in the breakdown voltage of devices.

Experimentally, improved breakdown voltages in GaAs FET have been demonstrated through various geometrical surface engineering techniques [5-7].

Recently, empirical surface engineering with LTG-GaAs and its related materials passivation in GaAs [8-10] had also been demonstrated to dramatically improve the device breakdown voltages in GaAs FETs. However, the exact physical mechanism that lead to this improvement of gate-drain breakdown voltage was unclear. Drawing from recent advances in the understanding of material sciences of LTG-GaAs, we are proposing that the compensated deep donors is the main attribute in the LTG-GaAs passivation that enabled it to improve the breakdown voltage when utilized in a FET structure.

A full two dimensional electrostatic simulation of the effect of LTG-GaAs passivation in FETs using the proposed model of compensated deep donors have been performed. Although the two discrete trap levels used in the model is an oversimplification of the actual traps in LTG materials, the physics of the problem should remain the same. The breakdown voltage in the structure is observed to be strongly dependent upon the compensated deep donors concentration. Futhermore, it is also sensitively depended on the energy level of the donor trap. These strong dependencies would explain the low reproducibility observed in LTG-GaAs passivated devices; this is a consequent of the fact that both the trap densities and energy levels in LTG materials have been reported to be a strong function of both growth and annealing temperatures [11, 12]. However, these dependencies are also indications that the LTG materials passivation would be suitable for material engineerings to obtain high breakdown voltage in devices.

3.6 References:

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CHAPTER 4

Experimental Implementation of LTG-AlGaAs Passivation

4.1 Introduction:

The two dimensional electrostatic simulations from Chapter 3 have clearly confirmed the strong correlation between the gate-drain breakdown voltage of passivated GaAs MESFET, and the defects concentrations in its LTG passivation layer, especially the deep acceptor concentrations. These defects concentrations, in turn, are sensitively dependent upon the synthesis processes, such as, the growth temperature and the subsequent thermal treatment of the LTG materials. Preliminary device results first reported by Chen *et al* [1], and also independently by Yin *et al* [2, 3] in 1992, provided clear experimental demonstration of the feasibility of the LTG material passivation technology. However, in those early works on LTG-GaAs passivated GaAs MESFET, only *one* growth and annealing condition was investigated. Namely, the LTG-GaAs passivation layer was grown at ~200°C and annealed in-situ at 600°C for 10 minutes under arsenic over pressure. Other growth and annealing temperatures, which have been demonstrated to yield unique LTG material properties [4] have not been in investigated in devices. Therefore, from a device engineering point of view, a systematic study of the dependence of the device characteristics on both the growth and annealing temperatures of the LTG passivation layer was called forth. This study would yield imperative informations in determining the suitability of this technology for widespread applications. Such study is the subject of the present chapter. In this study, the LTG-$Al_{0.3}Ga_{0.7}As$ surface passivation for GaAs power MESFET have been investigated in details.

As discussed in section 2.3, LTG-$Al_{0.3}Ga_{0.7}As$ shares many similar properties to those of LTG-GaAs, but with a larger bandgap; thus, the critical breakdown field of LTG-$Al_{0.3}Ga_{0.7}As$ should be higher, and the leakage current in LTG-$Al_{0.3}Ga_{0.7}As$ passivated devices should also be lower. The gate field alleviation mechanism provided by the compensated deep acceptors in LTG materials should also be applicable to LTG-$Al_{0.3}Ga_{0.7}As$ passivation. A combination of these two properties made LTG-$Al_{0.3}Ga_{0.7}As$ passivation a naturally preferred material for high power devices.

The first section of the chapter, following the introduction, describes the device design and fabrication that we have undertaken to experimentally study the effect of growth and annealing temperatures on the gate-drain breakdown voltage. Device results and analysis are presented in the followed section. The impact of the growth and annealing temperatures of the passivation layers on device characteristics such as, current voltage relationships and in particular the gate-drain diode characteristics are presented and discussed. In addition, a preliminary study of the effect of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation parameters on the low-frequency noise characteristics of the devices are also presented. Lastly, a summary of the main findings from the present investigation is given.

4.2 Device Design and Fabrication:

As evidenced in the literature on GaAs power MESFETs [5-7] and also from our independent data [8], the breakdown voltage of a MESFET is found to be very sensitive to its exact surface condition, which in turn depends strongly on the fabrication steps that the device. Systematic measurements of the gate-drain breakdown voltage in conventional GaAs MESFETs across a sample have been shown to varied by over 50% [9]. This large margin of experimental errors, although

typical in standard MESFET fabrication, has made the investigation of the cause of breakdown voltage in GaAs MESFET a daunting one. In particular, it made the systematic study of new techniques for improving breakdown voltage, such as LTG materials passivation, difficult. The task of isolating the effects that arise from the LTG-$Al_{0.3}Ga_{0.7}As$ passivation, and those that are due to processing variations has proved to be non-trivial.

In order to overcome this experimental obstacle, we have designed a device fabrication process that allowed us to minimize the impact of the processing variation on the data, therefore single out the effects of LTG-$Al_{0.3}Ga_{0.7}As$ material parameters on the device characteristics. We started with an epitaxial growth of a typical MESFET structure: 5000Å of undoped GaAs buffer, then 1500Å of n-GaAs channel with Silicon doping of $3.5x10^{17}$ cm^{-3}, and then capped with a 400Å $In_xGa_{1-x}As$ graded contact layer doped to $1x10^{19}$ cm^{-3}. After the growth of the wafer, a refractory metal, Tungsten (W), was used to defined the source and drain contacts. The wafer was then sectored and each piece was separately reload for the regrowth of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer. The samples were loaded into an in-situ etch chamber. Chemical gas etching (CGE) with chlorine was then used to etch away the grading contact layer. A laser monitor was used for process control of the etch depth. Following the etch, each sample was transferred to an Molecular Beam Epitaxial (MBE) chamber for the regrowth of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer. The transferring process between the etching chamber and the MBE chamber was done under ultra-high vacuum to protect the surface of the samples from potential surface contamination and oxidation. The regrowth started with an AlAs barrier layer followed by a non-stoichiometric AlGaAs layer, with growth temperature as the discriminating parameter between the samples.

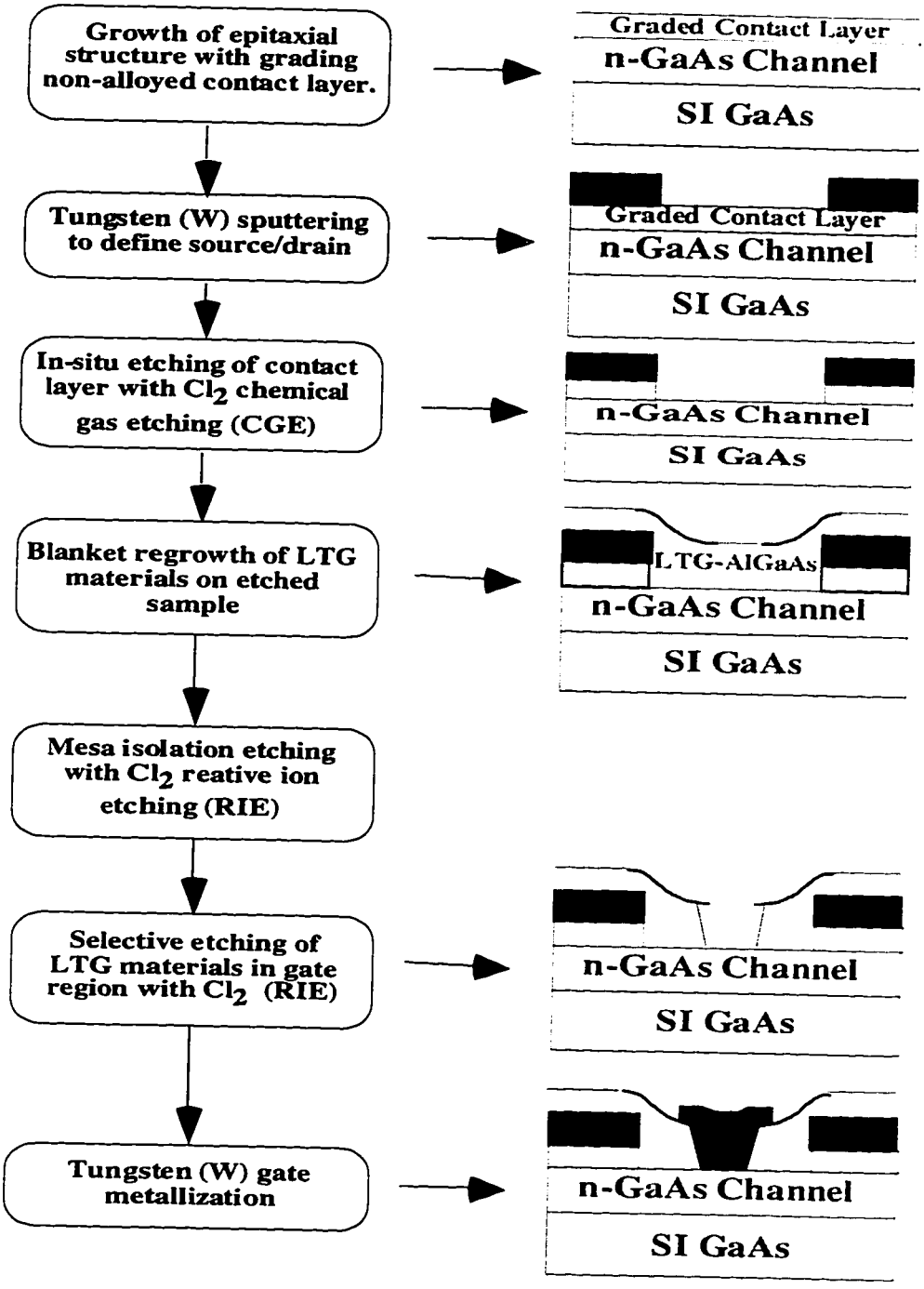


Figure 4.1: Flow chart of an all-refractory metals MESFET fabrication process; the corresponding device cross sections are shown on the right.

Following the regrowth of the passivation layer, the samples were unloaded and processing of the devices continued. Device mesa isolation was defined by

chlorine reactive ion etching (Cl_2 RIE). The polycrystalline overgrowth over the W contacts was selectively etched using Cl_2 RIE. The fabrication process was then finished with the recess etching of the LTG-$Al_{0.3}Ga_{0.7}As$ in the gate region, followed by a gate metallization with W sputtering. A flow chart of the process and the corresponding device cross-section is shown in Figure 4.1. This process provided FETs on identical channel material, with epitaxial passivation grown at various temperatures, ready to be monitored as a functions of annealing temperature. The refractory nature of both the Schottky gate and the non-alloyed ohmic contacts enable them to be relatively independent of the subsequent annealing treatment and allowed us to monitor just the effects of annealing of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer on device characteristics

Utilizing the fabrication process described above, we have prepared samples with different growth temperatures of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer. The growth and annealing parameter space that were investigated are summarized in Table 4.1. The annealing cycle is similar that detailed in Section 2.4.

Table 4.1 : Summary of growth and annealing temperatures investigated.

T_{growth} \ T_{anneal}	none	300°C	400°C	500°C	550°C	575°C	600°C
245°C	X	X	X	X	X	X	X
270°C	X	X	X	X	X	X	X
305°C	X	X	X	X	X	X	X
350°C	X	X	X	X	X	X	X

4.3 Device Results and Analysis:

4.3.1 Characteristics of Devices with Unannealed LTG-$Al_{0.3}Ga_{0.7}As$ Passivation

Figure 4.2 shows the room temperature gate-drain diode characteristics of unannealed devices with different LTG-$Al_{0.3}Ga_{0.7}As$ growth temperatures. The gate-length of the devices is 1.2μm, and the width is 300μm. The source to drain spacing is 5μm. The control device, where normal undoped GaAs passivation material was grown, had a breakdown voltage of 9V (typical for GaAs MESFET channel with similar doping density [10]). The devices with LTG-$Al_{0.3}Ga_{0.7}As$ passivations show dramatic improvement in the breakdown voltage.

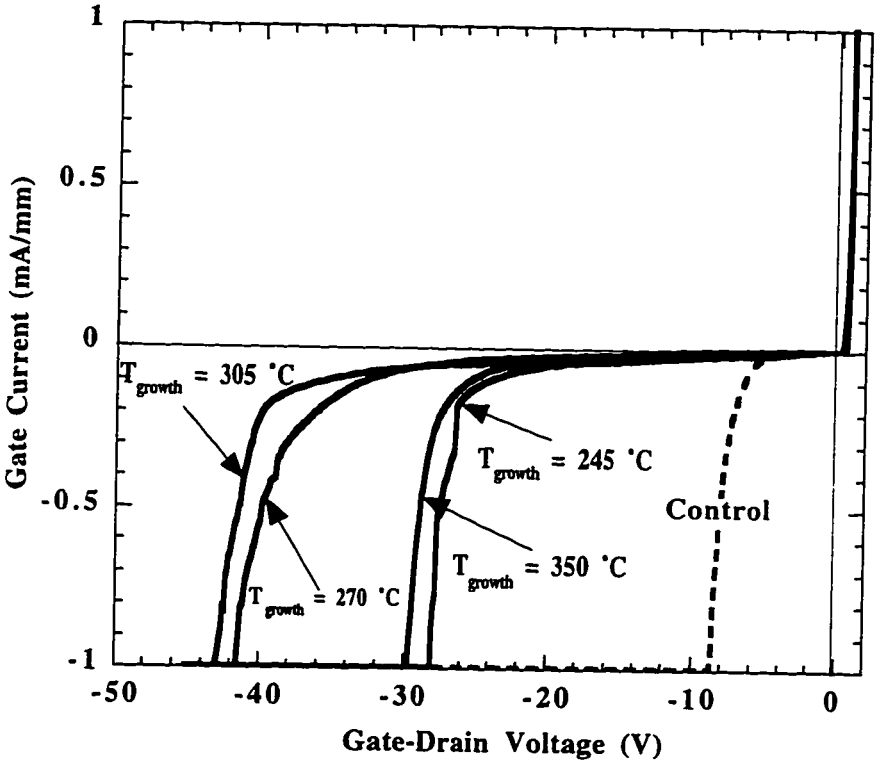


Figure 4.2: Experimental data of MESFET gate-drain breakdown voltage as a

function of growth temperatures of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer. The gate length of the device is 1.2 μm, and the source to drain spacing is 5 μm.

4.3.2 Effect of Annealing on Gate-Drain Breakdown Voltage

A typical current-voltage characteristic is shown in figure 4.3. The full channel currents of the various FETs were similar and therefore the comparison of the breakdown voltages is relevant. Figure 4.4 shows the breakdown voltages of the various FETs as function of anneal temperature. Also shown is the variation of the breakdown voltage of the control sample, as a function of anneal temperature, where the epitaxial passivant was an undoped GaAs layer grown at normal temperature of 600°C. This could, in a sense, be an indication of the margin of error in our measurements. Breakdown voltage was defined as the voltage at which the gate-drain diode leakage was 1 mA/mm.

The main feature of the breakdown voltage dependence on the preparation conditions of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer is the relatively monotonic decrease of the breakdown voltage with anneal temperature, independent of the growth temperature to a temperature of ~550°C. Then, in most samples, there is a precipitous drop in the breakdown voltage over a narrow range of temperature, down to the low breakdown voltage of the control sample. There are two possible reasons for this decrease. Either the concentration of the empty donors (equal in concentration to the filled acceptors assumed to be the Ga vacancy) reduces to below levels which are effective (i.e. ~2-3 x 10^{17} cm^{-3}) or the spreading of the electric field due to the surface resistor formed by hopping conduction is impeded. The dilemma we currently

face is that if electron injection into the hopping band is at all possible (necessary for both mechanisms) then hopping conduction has to occur. The absolute magnitude of

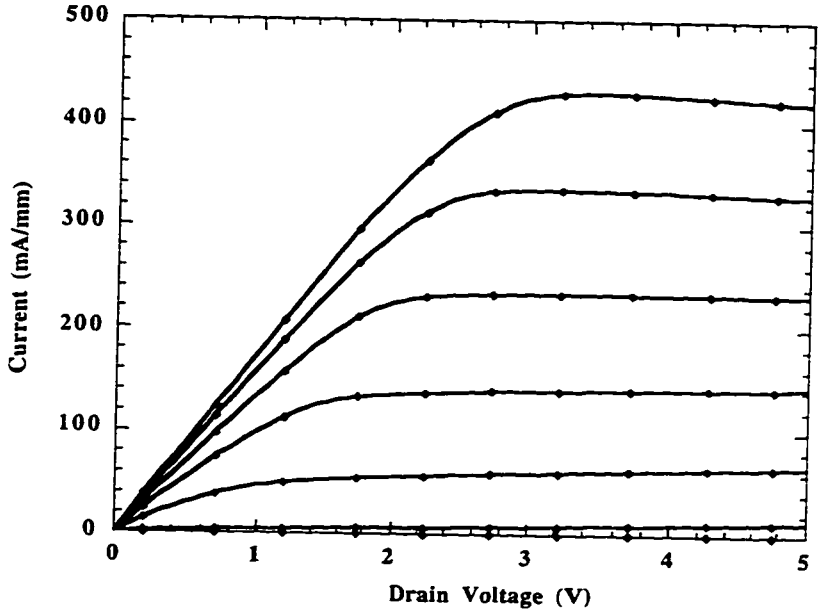
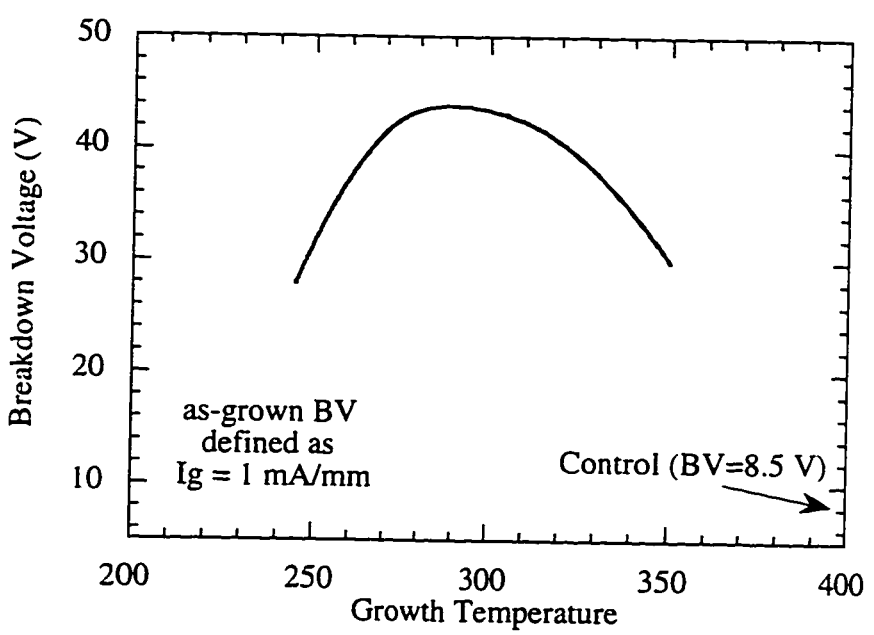


Figure 4.3: Typical current-voltage characteristics of GaAs MESFETs with regrown LTG-$Al_{0.3}Ga_{0.7}As$ passivation. Gate voltage started from 1V, with a step of -1 V.

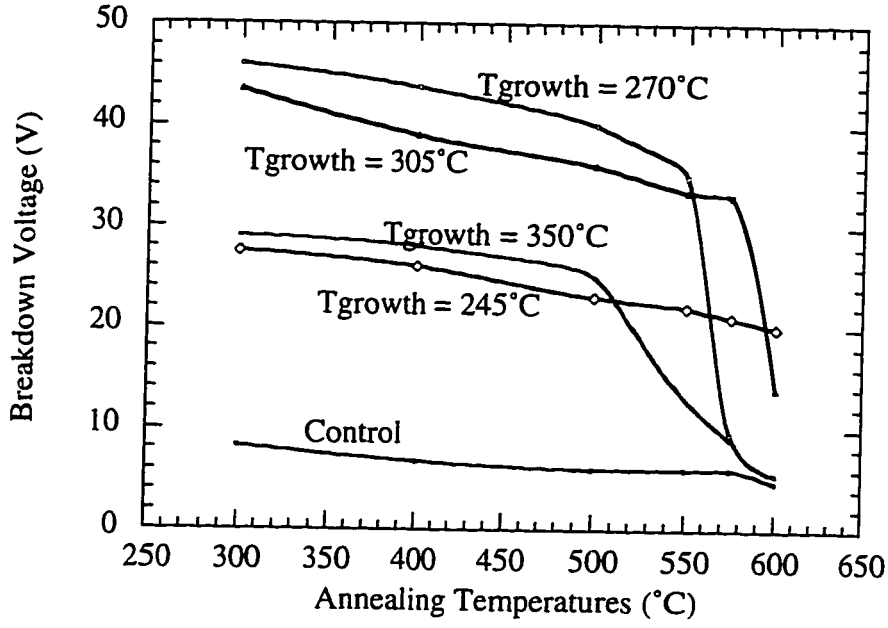
the hopping conductivity is not important since, at DC, the voltage drop is always linear, independent of the resistivity. Hence redistribution of the field should be effective even after a 600°C anneal. This experimentally does not happen as evidenced by the collapse of the breakdown voltage in figure 4.4. The major exception is the sample grown at 245°C, the sample with the highest degree of non-stoichiometry.

The data seem to suggest the following scenario. Annealing the device above 500°C to 550°C leads to the elimination of hopping conduction in the thin (2000Å thick) LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer between the gate and the drain. This can

only happen if the donor density in this surface oriented film decreases substantially faster than in the bulk films on which transport measurements were normally carried out [11] or by a disconnection between the metal and the hopping band. The first can occur by a diffusion of defects laterally to the gate metal, depleting the donor density proximal to the metal thereby increasing the tunneling distance into and effectively disconnecting the hopping band. The sample grown at 245°C does not show the variation with anneal temperature could be simply related to a large enough donor density in the film to survive the issues mentioned above.



(a)



(b)

Figure 4.4: Breakdown voltage as a function of growth temperature and anneal temperature of LTG-AlGaAs cap (a) as-grown and (b) annealed ex-situ using an RTA system.

4.3.3 Effect of Annealing on Low-Frequency Noise

In addition to influencing the gate-drain breakdown voltage, LTG materials passivation has been shown to dramatically affect the low-frequency noise characteristics of the passivated devices. We systematically investigated the effect of the preparation conditions of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation on the low frequency noise of FETs with a gate length of 1 μm. The control sample was the same as that discussed in the earlier section; had undoped GaAs as a passivant. Figure 4.5 and 4.6 display the low frequency noise characteristics obtained for annealing temperatures,

of 500°C and 550°C, respectively for devices with various growth temperatures. As can be seen readily, LTG-$Al_{0.3}Ga_{0.7}As$ passivated devices consistently displayed better lower low-frequency noise than that of the control device.

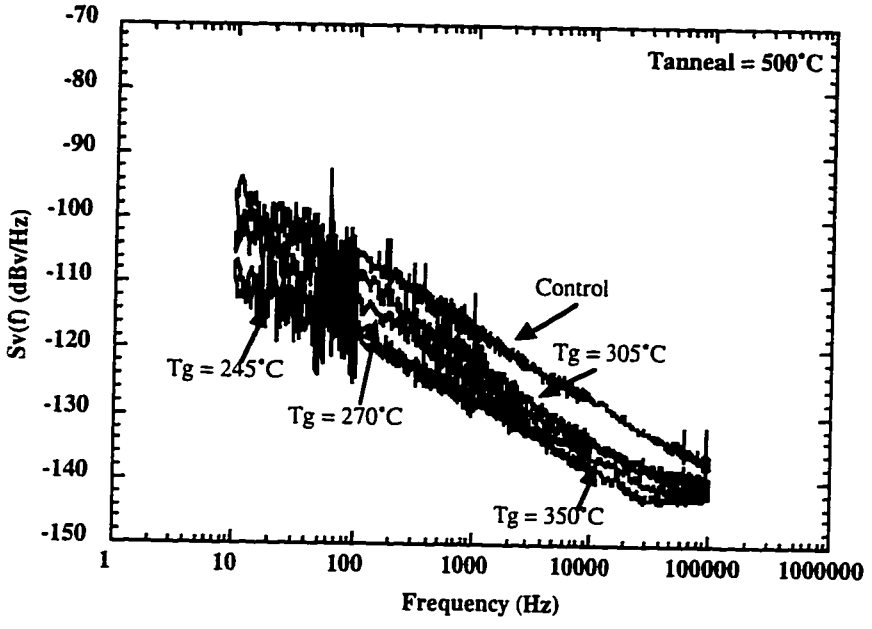


Figure 4.5: Low-frequency noise spectrum of GaAs MESFETs with LTG-$Al_{0.3}Ga_{0.7}As$ passivation grown at temperatures indicated in figure and annealed at 500°C.

As can be seen in figure 4.5, for the annealing temperature of 500°C, the best low frequency noise are obtained for the samples with passivation grown at 245°C and 350°C. The sample with LTG-$Al_{0.3}Ga_{0.7}As$ passivation grown at 245°C showed a corner frequency of 30 kHz, much lowered than the typical 1 MHz corner frequency reported in GaAs MESFET [12]. (Caution is in order here - A true corner frequency can only be defined if the white noise floor of the device is unequivocally established.

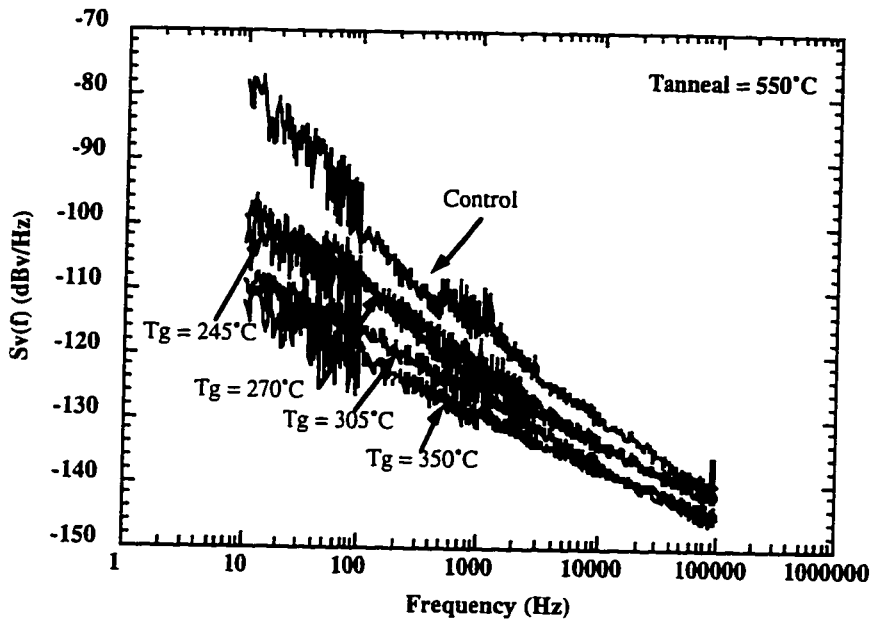


Figure 4.6: Low-frequency noise spectrum of GaAs MESFETs with LTG-$Al_{0.3}Ga_{0.7}As$ passivation grown at various temperatures and annealed at 550°C .

This has not been done in a definitive sense in this case and hence we emphasize the low magnitude of the low frequency noise across the spectrum rather than a corner frequency). However, when annealed at 550°C, the low-frequency noise of the LTG-$Al_{0.3}Ga_{0.7}As$ (245°C) increased while that of the LTG-$Al_{0.3}Ga_{0.7}As$ (305°C) remained essentially the same. Upon annealing at yet higher temperature, 575°C, the low-frequency noise of the LTG-$Al_{0.3}Ga_{0.7}As$ (245°C) recovered the value close to that of the one annealing at 500°C (figure 4.7).

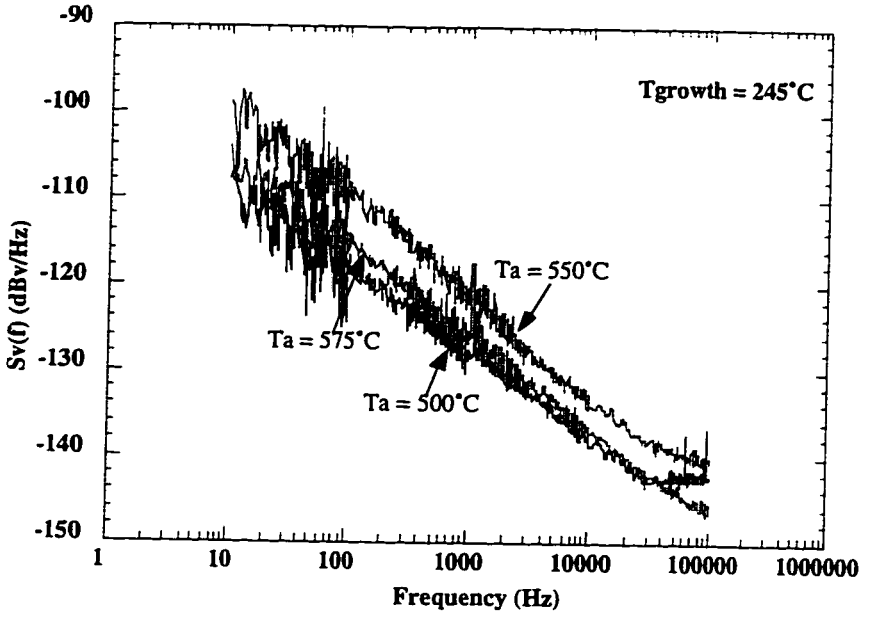


Figure 4.7: Low-frequency noise spectrum of a GaAs MESFET with LTG-$Al_{0.3}Ga_{0.7}As$ passivation, grown at 245°C and annealed at temperatures indicated in the figure.

The understanding of 1/f noise in a surface oriented device such as a FET is extremely difficult. It has been empirically established, [13] and references therein, (with supporting theories presented) that the surface of the FET is a major source of the low-frequency noise. A single trap with a well defined energy provides a generation-recombination (G-R) center and can lead to excess noise at frequencies close to the resonance frequency of the trap and produce a G-R bulge superimposed on the 1/f noise spectrum, but, cannot produce the entire spectrum. Such G-R bulges are common and a classic case is that produced by the DX center in AlGaAs-GaAs HEMTs. A trap-based model for the observed 1/f noise requires a spectrum of energy states. The surface of a FET provides such a continuum of states. The model in its essence is that charge fluctuations at the device surface cause conductivity

fluctuations in the channel which in turn lead to 1/f noise. If that is so then screening the surface effectively should suppress the low-frequency noise. This requires an epitaxial layer with mobile charges which can respond in the time constant typical of the spectrum (1μs) to screen the surface potential fluctuations. This layer should not have detrimental consequences such as high gate leakage and lower breakdown. This requirement seems to be best met by an epitaxial layer with a deep donor hopping band, the very properties of LTG epitaxial layers.

A model that we believed would qualitatively explain the low-frequency noise suppression in LTG passivated devices is detailed below and shown schematically in figure 4.8. A deep donor hopping band at 0.4 eV and an anti-site band at a nominal 0.7 eV is shown. Our model requires charge exchange between the hopping band and the surface so that effective screening can occur. Charge exchange is only possible between bodies with a work function difference. Therefore, the work function of the LTG-epitaxial layer should be smaller than that of the surface i.e. <0.7 eV. Also for screening to effectively occur the hopping band has to be able to communicate with the gate metal and the contact. This requires thermionic field emission to be from the gate metal to the adjacent hopping band. This indicates that the 1/f noise elimination will be determined by the relative magnitude of hopping density of states and the tunneling probability from the gate metal. The required conditions are most effectively achieved with two donor bands (which seem to occur readily in LTG GaAs). Both of these are a function of preparation conditions and is reflected in the data.

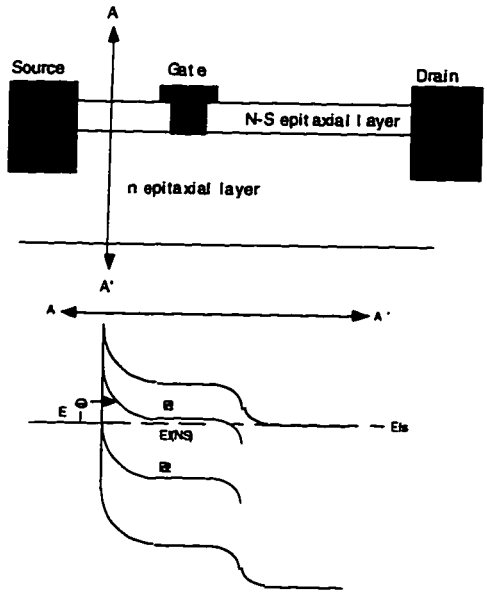


Figure 4.8 : Screening of surface potential fluctuations by hopping band of the LTG materials.

4.4 Summary:

The present chapter presented a thermally stable device fabrication process that is well suited for the study of the LTG materials passivation technology. Devices fabricated using this process allowed us to systematically study the effect of growth and annealing temperatures on the device characteristics. This study in turn clearly demonstrated the potential of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation as a potential electrical passivation technology for GaAs devices and circuits. By engineering the LTG-$Al_{0.3}Ga_{0.7}As$ material properties through its synthetic process, device characteristics could be dramatically impacted. Very high gate-drain breakdown voltage, and also ultra low low-frequency noise have been experimentally demonstrated. Furthermore, the temperature dependence of the breakdown on the growth temperature of the LTG-$Al_{0.3}Ga_{0.7}As$ layer provided strong supporting evidences for the model of field alleviation by the compensated deep donors of LTG materials proposed in Chapter 3.

4.5 References :

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CHAPTER 5

High Performance GaAs Microwave Power FET

5.1 Introduction:

The ultimate manifestation of all device engineering with LTG materials passivation to improve breakdown voltage is in the power performance of the device [1]. The power performance is of paramount importance because no matter how much we have learnt about the effects of LTG-$Al_{0.3}Ga_{0.7}As$ passivation on device, the engineering bottom line remains whether or not the LTG passivated device would be up to expectation when they are used in microwave circuits. For circuit applications, the device power figures-of-merit that mattered are: output power density, power-added-efficiency, linear gain, and intermodulation distortion [2, 3]. These figures-of-merit provides the truest testimonies of the suitability of the LTG passivation technology for microwave power devices.

The next section of this chapter focused on the device design and fabrication of a power field effect transistor which utilized the LTG-$Al_{0.3}Ga_{0.7}As$ passivation technology for improved gate-drain breakdown voltage. Then followed by a section on device results and analysis. DC and RF characteristics of the device is presented and discussed, and then the continuous-wave on-wafer power performance of the device are presented. Finally, a summary of the main points of the chapter is given.

5.2 Device Design and Fabrication:

In order to optimize channel design for high power, a doped channel heterostructure field effect transistor is used [3]. The device epitaxial structure was grown using a Varian Gen II MBE system on semi-insulating LEC GaAs substrate. First, a buffer layer of 5000Å GaAs was grown at a substrate temperature of 600°C.

followed by a 300Å of undoped $Al_{0.3}Ga_{0.7}As$ charge confinement barrier, then a 1000Å layer of n-GaAs channel doped with Silicon at $N_d = 3x10^{17}cm^{-3}$ was grown, followed by another 300Å layer of $Al_{0.3}Ga_{0.7}As$. Next, an arsenic-diffusion-barrier of 200Å of AlAs was grown, which was capped with a 50Å layer of GaAs. The substrate temperature was then lowered to 200°C, where 2000Å of LTG-$Al_{0.3}Ga_{0.7}As$ was grown. The sample was then annealed *in-situ* with As over-pressure at 600°C for 10 minutes. A sample with a similar epitaxial structure but with the replacement of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer by an undoped normal temperature grown $Al_{0.3}Ga_{0.7}As$ was also grown as a control. A schematic cross section of the structure is shown in Figure 5.1.

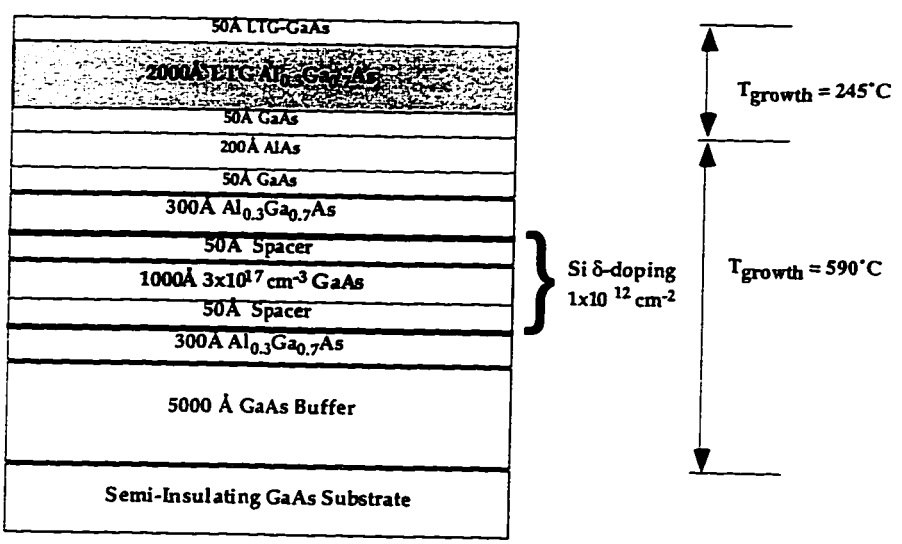

Figure 5.1: Schematic cross section of a high-power GaAs heterostructure field effect transistor (HFET) with LTG-$Al_{0.3}Ga_{0.7}As$ passivation incorporated to improve breakdown voltage. Room temperature Van der Pauw measurement of an actual sample yield a sheet charge of $5x10^{12}$ cm^{-2} and a mobility of 3650 cm^2/V-s.

Processing began with the selective regrowth of the source/drain contacts with n^{++}-GaAs by Metal Organic Chemical Vapor Deposition (MOCVD) [4]. Followed by e-beam evaporation of AuGe/Ni/Au metals. The selective regrowth was

accomplished at 550°C, well below the in-situ annealing temperature of the LTG-$Al_{0.3}Ga_{0.7}As$ layer. Inter-device isolation was achieved by boron ion implantation. Next, a 1.2 μm long gate foot print was defined using photolithography; then Cl_2 reactive-ion-etching was used to etch away the LTG-$Al_{0.3}Ga_{0.7}As$ and expose the channel. Finally, a 2 μm overlapping gate mask was aligned to the defined gate foot print and the gate was formed with life-off of Ti/Au [5]. A scanning electron microscopy (SEM) photograph of a finished device with overlapping gate is shown in Figure 5.2. Details of the fabrication process are described in Appendix A.

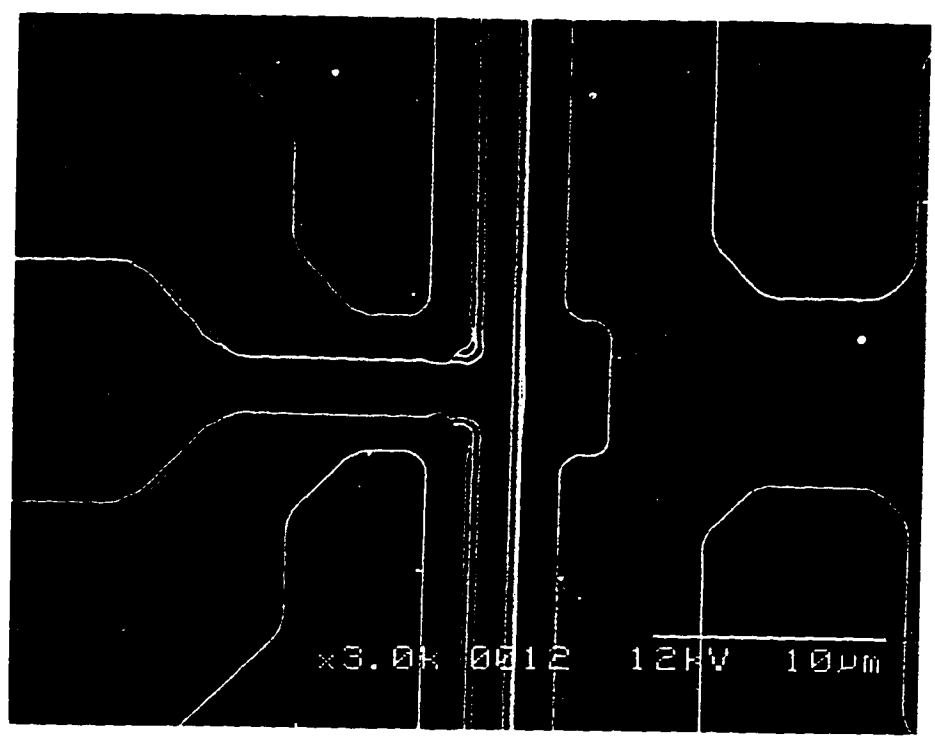

Figure 5.2: Top view of a finished device showing the overlapping gate metals on the LTG-$Al_{0.3}Ga_{0.7}As$ passivation; the gate geometry is 1.2 μm foot-print with a 2 μm overlapping metal.

5.3 Device Result and Analysis:

5.3.1 DC Characteristics

Upon completion of processing, devices were probed and characterized on-wafer. DC measurement were done using an HP-4145B Parameter Analyzer. The gate-drain diode characteristics for both the LTG-$Al_{0.3}Ga_{0.7}As$ passivated FET and that of the control sample is shown in Figure 5.3. As expected, the LTG-$Al_{0.3}Ga_{0.7}As$ device has twice the breakdown voltage as compared to that of the control, with undoped $Al_{0.3}Ga_{0.7}As$ passivation. This reaffirmed that the LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer does indeed act as an effective charge absorber; and alleviated the peak gate electric field for the HFET structure. In addition, the reverse leakage current shown in Figure 5.3 is much lowered than that of LTG-GaAs passivation [6], this is attributed to the large band-gap of the $Al_{0.3}Ga_{0.7}As$ spacer placed underneath the gate metal. The low reverse leakage current is desirable in power MESFET because it would led to an enhancement of the power conversion efficiency in the device (i.e. high power-added-efficiency) [7].

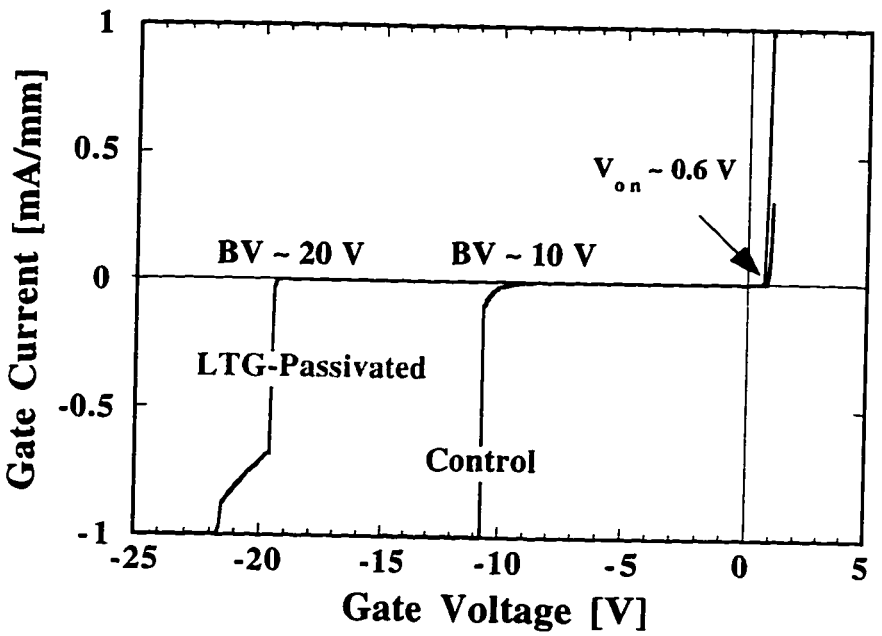

Figure 5.3: Gate-drain diode characterisitics of high-power LTG-$Al_{0.3}Ga_{0.7}As$ passivated GaAs HFET, the device gate foot-print is 1.2 μm, with 5 μm source-drain spacing. The control device had similar epistructure except that the LTG-$Al_{0.3}Ga_{0.7}As$ is replaced with undoped $Al_{0.3}Ga_{0.7}As$.

Figure 5.4 displays a nominal current-voltage characteristics of the device. The maximum drain current at a gate forward bias of 0.5V is about 480 mA/mm. The transconductance of the device is about 140 mS/mm, which is about 40% higher than typical GaAs MESFET [8] (and also those presented in Chapter 4). The enhanced transconductance is due to the improved channel conductance associated with heterostructure. The improved device transconductance is sought after because it usually manifested in higher power gain for the device in power application [9].

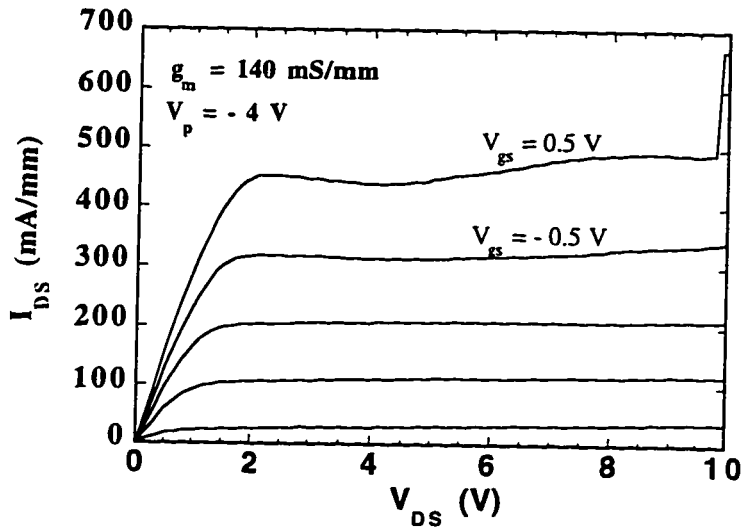

Figure 5.4: Current-voltage characteristics of a 1.2 μm gate-length LTG-$Al_{0.3}Ga_{0.7}As$ passivated HFET.

The device "on-state" breakdown voltage, defined as the drain breakdown voltage with the channel fully opened is ~10V. This high on-state breakdown voltage is attributed to the suppression of hole injection from the contacts through the use of non-alloyed MOCVD regrown contacts. In order to verify this, we have also fabricated a device with normal alloyed contacts. The I-V characteristics is shown in Figure 5.5. The on-state breakdown voltage is clearly lowered while all other device figures-of-merit are similar to that of the non-alloyed contacts device.

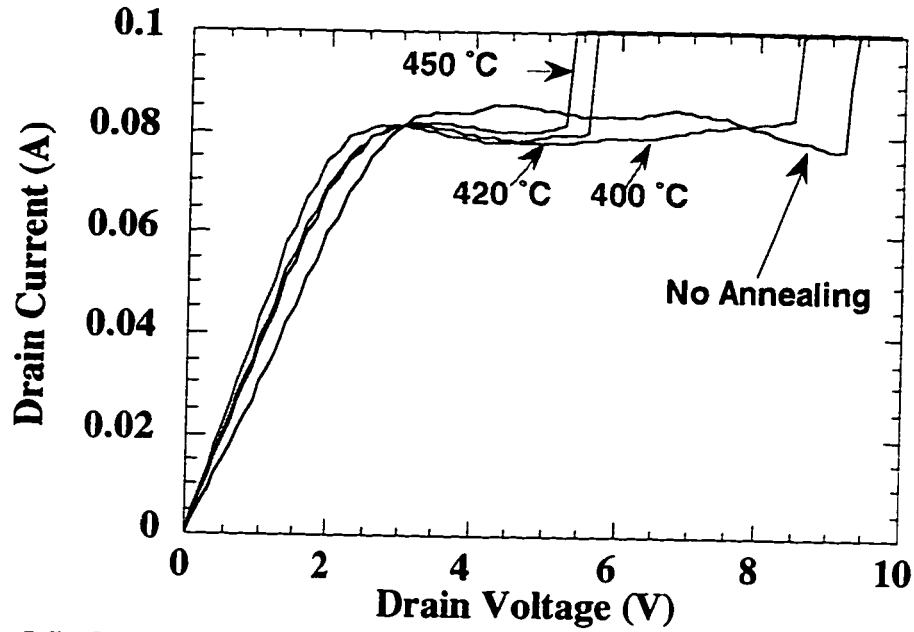

Figure 5.5: On-state breakdown voltage dependence on annealing temperatures of ohmic conctacts.

5.3.2 RF Characteristics

Small signal measurements using an HP-8510B automatic network analyzer were performed on the passivated device. A nominal frequency performance as a function of gate bias, with a drain bias of 5V, is shown in Figure 5.6. The unity current gain cut-off frequency (f_T) of ~7 GHz were obtained throughout the gate bias range. The unity power gain cut-off frequency (f_{max}) showed a stronger gate bias dependence, with f_{max} = 20 GHz at the gate bias of -1V. These high frequency figures-of-merit indicated that the device should be able to perform as a microwave power amplifier.

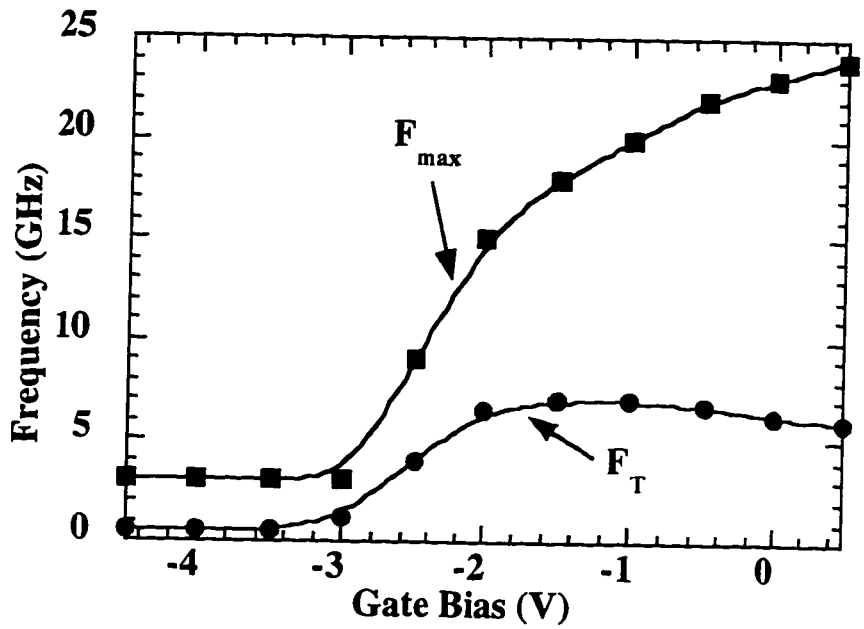

Figure 5.6: Frequency performance as a function of gate bias of an LTG-$Al_{0.3}Ga_{0.7}As$ HFET with 1.2 μm gate foot-print (2 μm overlapping gate).

5.3.3 Microwave Power Performance

The device characteristics discussed above showed promises for potential high power performance. On-wafer continuous-wave power measurements were performed at 4 GHz for a 400 μm wide device. Class-A biasing at a source-drain voltage of 12V and half of the maximum drain current (I_d = 50% I_{max}) was used for the measurement. The device delivered a maximum output power of 1.0 W/mm at 30% PAE (Power-Added-Efficiency) was achieved. The linear gain of the device is 11.5 dB. Figure 5.7 displays the output power and power added efficiency of the device at 4 GHz.

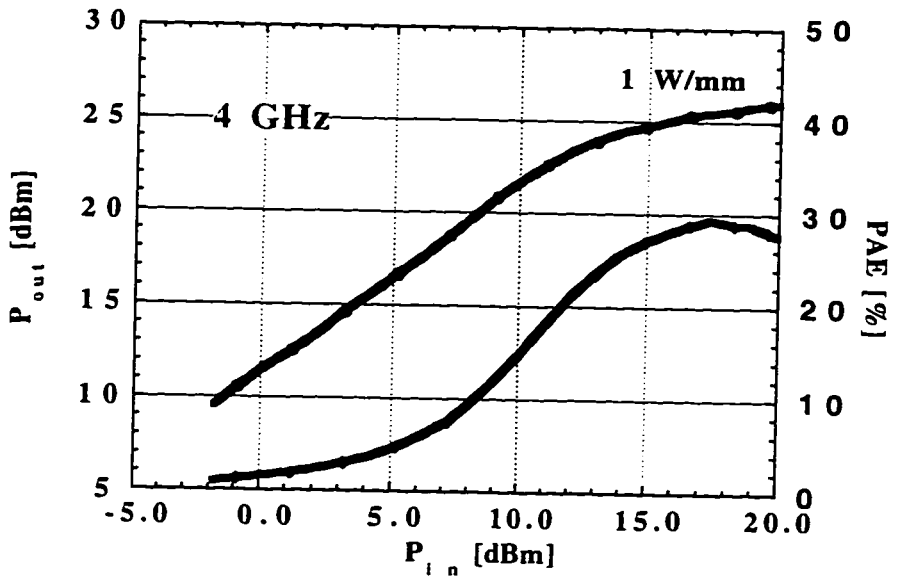

Figure 5.7: Continous-wave power performance of a 1.2 μm gate length LTG-$Al_{0.3}Ga_{0.7}As$ passivated HFET at 4 GHz.

Upon tuning the load for high PAE, a PAE of 46% with an output power of 0.5 W/mm was achieved (Figure 5.8). Higher frequency measurement was also performed and is displayed in Figure 5.9. At 8 GHz, the device in Class-A bias (V_{ds}=9V and V_{gs}=-1.3V) delivered 825 mW/mm at 27% PAE, with a linear gain of 6.5dB.

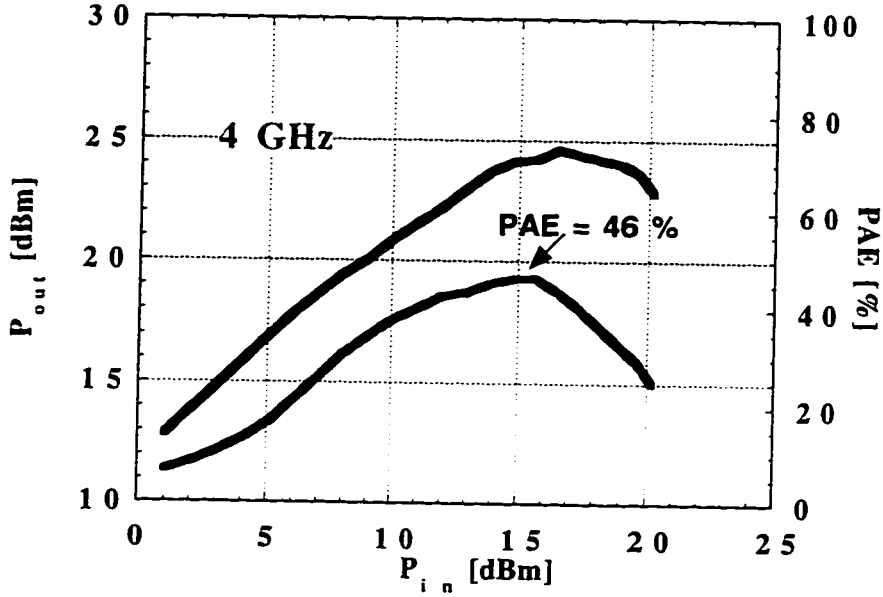

Figure 5.8 : Performance characteristics of an LTG-$Al_{0.3}Ga_{0.7}As$ passivated HFET was tuned for high power-added-efficiency (PAE) at 4 GHz.

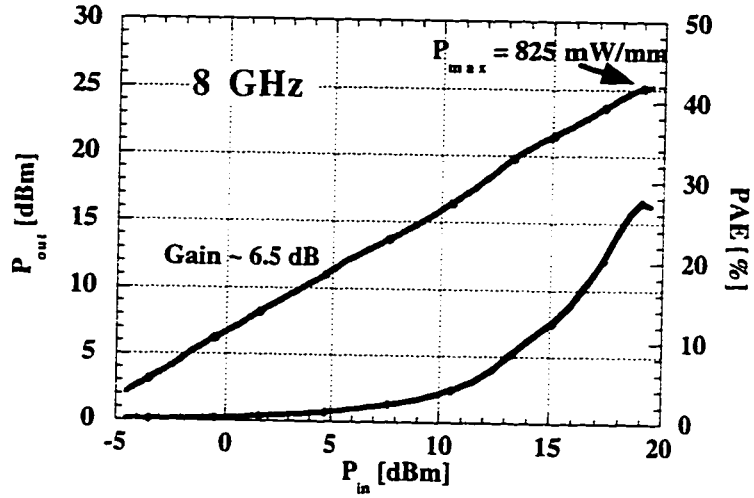

Figure 5.9 : Power performance of an LTG-$Al_{0.3}Ga_{0.7}As$ passivated HFET at 8 GHz.

5.4 Summary :

In this chapter, a high performance GaAs-based microwave power FET has been demonstrated. The device incorporated an LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer in an HFET channel structure. The device characteristics and performance provided convincing testimony to the suitibility of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation technology for GaAs-based power field effect transistor. A high-power FET fabrication process, which utilized non-alloyed selective regrown contacts by MOCVD and an overlapping gate structure, and is compatible with LTG-$Al_{0.3}Ga_{0.7}As$ passivation have been developed.

High performance devices utilizing this process have been realized and demonstrated. A maximum output power density of 1.0 W/mm was obtained with an LTG-$Al_{0.3}Ga_{0.7}As$ passivated HFET, and a high PAE of 46% was achieved when the device was tuned for high efficiency. These results are among the best reported values for GaAs-based FET [3].

5.5 References :

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CHAPTER 6

Summary and Future Work

Summary:

The principal objective of the present research has been to investigate the feasibility and potentials of the application of low temperature grown materials in surface engineering of GaAs devices and materials, as well as to gain a physical understanding into the mechanism that surface passivation with LTG materials has provided in improving the gate-drain breakdown voltage and hence the power performance of passivated devices. From a technological standpoint, LTG materials passivation presents a new technology in the continual search for an effective electrical surface passivation for GaAs devices and materials. Although further progresses and investigations are needed before the growth of LTG materials can become reliable and reproducible; the high controllability associated with MBE growth, promises LTG materials passivation to be a potentially more stable technology for devices. The existence of excess As, hence high deep acceptor and deep donor concentrations, in the LTG layers make the materials unique. Furthermore, the strong dependence of these concentrations on synthesis process, such as growth and annealing temperatures, enabled the materials to be readily engineered for specific device applications.

We have demonstrated the device application of LTG-$Al_{0.3}Ga_{0.7}As$ passivation in GaAs FET to improve the breakdown voltage. A systematic study of

the effects of growth and annealing temperatures of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation layer on the gate-drain breakdown voltage of the FET have been performed. We have also performed preliminary investigation on the effects of LTG-$Al_{0.3}Ga_{0.7}As$ processing parameters on MESFET low-frequency noise characteristics of the passivated devices. Proper LTG-$Al_{0.3}Ga_{0.7}As$ passivation has been observed to dramatically lower the low-frequency noise of the FET.

Drawing from the present knowledge of the material properties of LTG-GaAs, we have proposed a physical model that would explain the observed improvement in the breakdown voltage arose from devices passivated with LTG materials. The model of compensated deep donors hypothesized that, with LTG materials passivation, the empty states of the *compensated deep donors* which enabled the LTG material passivation layer to act as an effective charge absorber and alleviate the peak electric field at the drain-edge of the gate metal in a FET structure. Two dimensional electrostatic simulation using this model of LTG materials clearly confirmed that the deep acceptors concentration (which is equivalent to the compensated deep donors concentration, when $N_d >> N_a$) dramatically effect the breakdown voltage of the device.

We have developed a thermally stable device fabrication process that has enabled us to systematically study the effect of growth and annealing temperatures on the characteristics of LTG-$Al_{0.3}Ga_{0.7}As$ devices. The effect of annealing of LTG materials is equivalently to the changing of defect concentrations in the LTG layer;

and this was *experimentally* demonstrated to have a clear impact on the breakdown voltages and other device characteristics. Device with record breakdown voltage of ~40 V and maximum drain current of 420 mA/mm has been demonstrated as convincing testimony to the potential of the LTG material passivation technology. These results are substantially higher than those obtained with the current technology in the industry for high breakdown, namely gate recess etching [1, 2].

High performance GaAs-based power FET, which incorporated LTG-$Al_{0.3}Ga_{0.7}As$ passivation have also been demonstrated with record performance of 1.0 W/mm at 30% Power-Added-Efficiency(PAE), and 0.5 W/mm at 46% PAE (at 4 GHz). This experimental result provided clear proof of the applicability of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation technology for microwave power devices.

However, there are still other issues that needed consideration and investigation before the LTG materials passivation technology could be truly termed *low cost* and be implemented in existing fabrication process of GaAs power FET.

Suggestions for Future Work

As the device results in Chapter 4 have clearly demonstrated, the exact growth temperature of the LTG materials has critical impacts on the device characteristics, a difference in growth temperatures of ~25°C resulted in drastically difference device characteristics. However, this has been a fundamental in LTG materials research: a lack of a good method to precisely measure growth temperature

near 200°C. Recent developments in MBE technology have shown that the solution for more accurate low temperature measurements is possible in the immediate. Implementation of such technology is a must for LTG materials growth, and it should lead to more reproducible LTG materials and device characteristics.

The stability and reliability of LTG passivated devices also needs more investigation. In particular, thermal stability of the LTG materials requires systematic study and characterization. These studies should be the final tests of the suitability of LTG materials passivation in GaAs power FET. In addition, implementation of LTG materials passivation to other surface sensitive FET structures, such as low In composition (<20%) GaAs Pseudomorphic High Electron Mobility Transistor (PHEMT), would lead to improved power performance at high frequency with low cost, the combination that has been the much sought after by the emerging wireless communications industry.

A high-power PHEMT structure, with large barrier ($Al_{0.43}Ga_{0.57}As$) and high current capability (larger ΔE_C and tellurium doping) have recently been demonstrated [3]. Application of the LTG-$Al_{0.3}Ga_{0.7}As$ passivation technology to this device structure would lead to potentially high performance microwave power devices.

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