UNIVERSITY OF CALIFORNIA
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AlGaN/GaN Microwave Power High-Mobility-Transistors

A dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy
by

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To obtain a Ph.D. degree in Electrical Engineering is still like a dream to me who built radio receivers in middle school with self-made soldering irons and entered a wrong field to get a Bachelor's degree, to work for seven years, and to receive a Master's degree. I am indebted to my advisor Dr. Umesh Mishra who accepted me as his Ph.D. student when I apparently had little formal education in but a passion for Electronics. It is his belief in me, his guidance and encouragement throughout the research period that makes this dissertation possible. I also owe a fundamental thank to Dr. Steve Denbaars for the establishment of a first rate MOCVD growth center and his professional support to electronic devices. I sincerely thank Dr. Steven Long for admitting me into the Solid-state program and his contribution to this work. I appreciate Dr. Robert York for serving in my Ph.D. committee and sharing valuable insight into the implementation of GaN FETs in microwave circuits. I enjoyed taking classes and making acquaintances with many other professors of world fame, including Dr. Herb Kroemer, Dr. Mark Rodwell, and Dr. Evelyn Hu.

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Dedicated to

those in an endless pursuit for a dream

and those who keep it alive

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Journal Publications

1. Y.-F. Wu, B.P. Keller, P. Fini, J. Pusl, M. Le, N.X. Nguyen, C. Nguyen, D. Widman, S. Keller, S.P. Denbaars, and U.K. Mishra, "Short-Channel $Al_{0.5}Ga_{0.5}N/GaN$ MODFETs with power density > 3 W/mm at 18 GHz", *submitted to Electronics Letters.*
2. Y.-F. Wu, B.P. Keller, P. Fini, S. Keller, S.P. Denbaars, and U.K. Mishra, "High Al-content AlGaN/GaN MODFETs for ultra-high performance", *submitted to IEEE Electron Device Letters.*
3. Y.-F. Wu, B.P. Keller, S. Keller, N.X. Nguyen, M. Le, C. Nguyen, T.J. Jenkins, L.T. Kehias, S.P. Denbaars, and U.K. Mishra, "Short channel AlGaN/GaN MODFETs with 50-GHz f_T and 1.7-W/mm output-power at 10 GHz", will be published in *IEEE Electron Device Letters,* Sept. 1997.

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Abstract

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by Yifeng Wu

Microwave power devices with conventional semiconductors have approached their performance limits. To meet the future need in wireless communications, research effort has been directed to wide bandgap semiconductors such as SiC and GaN. AlGaN/GaN High-Mobility-Transistors (HEMTs) are chosen in this dissertation to overcome the drawback of inherently low mobilities in the wide bandgap materials so that both high power and high speed are feasible.

The immature techniques in both growth by metal-organic-chemical-vapor-deposition (MOCVD) and device processing during the earlier research period allow little design freedom. For this reason, the first stage in this work is experimental iterations between device fabrication, characterization and technological improvements. With this approach, basic $Al_{0.15}Ga_{0.85}N$/GaN HEMTs with satisfactory characteristics in all major aspects have been obtained using an insulating GaN buffer with growth initiation at low pressure, an $Al_{0.15}Ga_{0.85}N$ layer with a doped region by Si, Ni/Au as the Schottky-gate metal and, low resistance ohmic schemes either by n^+-GaN regrowth or by the multi-layer metallisation of Ti/Al/Ni/Au in literature.

Design philosophies for device optimization are then generated by first order analyses which point to the advantage of high Al-content. Subsequent experiments confirm the feasibility of this design direction and result in ultra-high performances as represented by a maximum current-voltage product greater than 200 VA/mm and a CW output power density of 2.8 W/mm at 8 GHz with $Al_{0.5}Ga_{0.5}N$/GaN HEMTs by optical lithography. Short channel devices by electron-beam lithography are also fabricated to take advantage of a higher effective saturation velocity. 0.25-µm gate-length $Al_{0.5}Ga_{0.5}N$/GaN HEMTs show a record current gain cutoff frequency of 52 GHz for a wide bandgap field-effect-transistor (FET) and record CW power densities greater than 3 W/mm at 18 GHz for any microwave FET.

Finally, a device operation analysis is carried out. Investigation of delay times against drain bias shows complete depletion of the gate-drain region which explains why breakdown voltages depend on gate-drain spacing. Calculation based on this observation results in an effective saturation velocity of 1.76×10^7 cm/s in the GaN channel, the first experimental value in agreement with the Monte Carlo simulation in literature.

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Table of Contents

Chapter 1

Introduction

1.1 Advantages of GaN for microwave power devices

Microwave power transistors play a key role in today's wireless communications necessary for virtually all major aspects of human activities form entertainment, business to military. As a semiconductor device, the GaAs metal-semiconductor-field-effect-transistor (MESFET) has been a workhorse in the field. Its more than 20 years of development history has exhausted the performance limit. In particular, the highest output power density of 1.4 W/mm at 8 GHz was reported back in the early 80's [i]. Although later effort on using low-temperature-grown (LT) GaAs as a gating or passivation layer increased breakdown voltages, the improvement in power density was very limited (1.57 W/mm) [ii] and under a sacrifice of a reduced operation frequency of 1.1 GHz. In the early 90's, development in InP resulted in a reportedly much higher power density of 1.8 W/mm at 30 GHz with an InP metal-insulator-semiconductor-field-effect-transistor (MISFET) using SiN as the insulator. [iii] However, the overwhelming interface traps led to very unstable IV characteristics so that they were not shown. Subsequent success in InP channel high-mobility-transistors (HEMTs) yielded a power density of 1.45 W/mm at 30 GHz along with excellent IV characteristics [iv]. The higher power performance of the InP devices is mainly attributed to the higher breakdown field and greater high-field velocity of InP than GaAs, but the improvement was far from revolutionary. For a new level of power performance to meet the future need, recent research effort has been directed to the development of wide bandgap semiconductors.

Johnson [v] was the first to point out that the power-frequency limit is a material parameter. For a better understanding of Johnson's figure of merit, a simplified derivation applied to a MESFET is presented below.

The output power density depends on the maximum IV product per unit gate-width:

$$P = I_{max}V_{max}/8 \qquad \text{Eq.1-1}$$

The breakdown voltage V_{max} for a semiconductor junction with uniform doping n is

$$V_{max} = \frac{\varepsilon_s \boldsymbol{E}_{bk}^{2}}{2nq} \qquad \text{Eq.1-2}$$

where $\boldsymbol{E}_{bk}$ is the breakdown field, ε_s is the dielectric constant and q is the unit charge of an electron.

With a channel thickness of d and the electron saturation velocity of v_s, the maximum current density is

$$I_{max} = (nd)qv_s \qquad \text{Eq.1-3}$$

The power density can then be written as

$$P = \varepsilon_s \boldsymbol{E}_{bk}^{2} v_s d/16 \qquad \text{Eq.1-4}$$

Associating the power density with the switching speed of a field-effect-transistor (FET) of gatelength L_g, we finally have the power-frequency product as

$$\begin{aligned} Pf_t &= (\varepsilon_s \boldsymbol{E}_{bk}^{2} v_s d/16)(\frac{v_s}{2\pi L_g}) \\ &= (\frac{\varepsilon_s}{32\pi})(\frac{1}{A})(\boldsymbol{E}_{bk} v_s)^2 \end{aligned} \qquad \text{Eq.1-5}$$

Since $A = L_g / d$ is the aspect ratio of an FET and takes on a value no less than 3 ~ 5, the power-frequency limit is eventually not a geometric parameter but depends on $(E_{bk} v_s)^2$ only.

The ultimate breakdown field E_{bk} is the electric field for band-to-band impact ionization and mainly depends on the band gap E_g; while the saturation velocity is primarily limited by inter-valley scattering and is determined by the energy difference of the satellite and the conduction band edges. Major parameters relating to Johnson's figure of merit for materials used for power devices are listed in Table 1.1-1.

Table 1.1-1 *Major parameters related to power performance at high frequencies for various materials*

	Si	GaAs	GaInP	4H-SiC	GaN
E_g (eV)	1.1	1.4	1.9	3.2	3.4
E_{bk} (V/cm)	$3x10^5$	$4x10^5$	$6x10^5$	$20x10^5$	$20x10^5$
v_s (cm/s)	$6x10^6$	$10x10^6$	$10x10^6$	$20x10^6$	$20x10^6$
μ (cm^2/Vs)	1000	8000	2000	500	1000
κ (W/m°C)	150	43	52	490	130
$*(E_{bk} v_s/\pi)^2$	1	7	16	282	282
$**\mu E_{bk}^2$	1	10	8	22	44
$***\kappa(v_s/\varepsilon_s)^{1/2}$	1	0.46	0.6	5.9	1.76

*Johnson's figure of merit for power-frequency performance of discrete devices;
**Baliga's figure of merit for power loss at high frequencies;
***Keyes' figure of merit for the speed of integrated circuits.
All figures of merit are normalized to silicon. κ is thermal conductivity.

It is seen that with the increased breakdown field and electron saturation velocity, both wide bandgap semiconductors SiC and GaN acquire a Johnson's figure of merit many times higher than conventional semiconductors. Although practically the power performance does not scale proportionally to Johnson's figure of merit due to other effects, a comprehensive simulation taking into major design constraints by Trew et al. predicted a power density of 4 W/mm at 8 GHz for both SiC and GaN MESFETs with a gatelength of 0.5 μm [vi], remarkably higher than the 1 W/mm value generally achieved with GaAs MESFETs. Recent years of intensive research effort on the development of SiC devices has resulted in a high CW power density of 2.8 W/mm at 1.8 GHz [vii]. However, the best reported current-gain cutoff frequency of an SiC MESFET is 14 GHz with a gatelength of 0.4 μm [viii], much lower than that of a GaAs counterpart. This is related to the much lower mobility for SiC and will ultimately limit its operation frequency. Unlike SiC devices which depend on the bulk mobility, GaN-channel HEMTs are able to take advantages of the two-dimensional-electron gas (2DEG) at the AlGaN/GaN interface. GaN's originally higher bulk mobility plus this enhancement by the 2DEG will lead to a channel velocity closer to saturation, therefore a higher current density and higher cut-off frequencies over the competing SiC devices.

1.2 Research background in GaN based FETs

The first GaN based FET was a MESFET fabricated by Khan et al. in early 1993 [ix]. The epi-film was grown on a sapphire substrate by low pressure metal-organic-chemical-deposition (MOCVD). A 6000 Å thick un-intentionally doped (UID) n-GaN layer on a thin AlN nucleation layer was used as the transistor channel, which had a doping density and a mobility of 1×10^{17} cm^{-3} and 350 cm^2/Vs, respectively. A current density of ~ 175 mA/mm along with a peak transconductance of 23 mS/mm was obtained with these 4-μm gatelength devices. Subsequent addition of a 250 Å $Al_{0.13}Ga_{0.87}N$ layer resulted in an AlGaN/GaN HEMT structure with an enhanced mobility of ~ 600 cm^2/Vs. Devices with 0.25-μm gatelength showed a current density of 60 mA/mm and a transconductance of 27 mS/mm [x]. The lower current than the first GaN MESFET might be due to the very poor ohmic contact resistance of 28 Ω-mm resulting from the difficulty in alloying through the AlGaN layer and the immature ohmic scheme of Ti/Au. Nonetheless, an f_t of 11 GHz was measured along with an f_{max} of 35 GHz, close to that of the more mature SiC MESFETs. Similar encouraging performance (f_t and f_{max} of 8 and 17 GHz) was reported with 0.7-μm gatelength GaN MESFETs [xi]. These MESFETs by Binari et al. were essentially inverted hetero-structure FETs (HFETs) with 60 Å of AlN underneath the 2500 Å GaN-channel which resulted in a carrier accumulation at the GaN/AlN interface. The epi-structure was also prepared by MOCVD on a sapphire substrate. Although the transconductance of 20 mS/mm was similar to the devices by Khan due to the large gate-carrier separation of 2500 Å, the inverted HFETs had a much higher current density of 306 mA/mm as a result of a lower source resistance of 6 Ω-mm achieved with the better ohmic contact scheme of Ti/Al [xii].

In the above background (January 1995), we started our research effort on GaN electronics at UCSB. While we were still developing the growth technique of bulk GaN films by MOCVD, Ozgur et al. reported the first GaN-channel HEMT grown by molecular-beam-epitaxy (MBE) [xiii]. Their epi-structure consisted of a resistive GaN buffer and an AlGaN barrier/donor layer. The measured room temperature mobility and carrier density were 500 cm^2/Vs and $1.2x10^{12}$ cm^{-2}, respectively. While the current density of these 3-μm gatelength devices was 300 mA/mm, similar to that by Binari, the transconductance was a markedly higher value of 120 mS/mm. This high transconductance was attributed to the HEMT structure and the low source resistance of 2 Ω-mm resulting from a new ohmic scheme which was not published by then. A few months later, Khan et al. also reported remarkable performance improvements achieved with doped-channel HFETs (DC-HFETs) [xiv]. A 1-μm gatelength device showed a high current density of 600 mA/mm and a large transconductance of 120 mS/mm. The f_t was 18.3 GHz, corresponding to a high f_t-gatelength product of 18.3 GHz-μm. However, subsequent 0.25 μm gatelength devices exhibited lower current density, transconductance and f_t-gatelength product of 300 mA/mm, 90 mS/mm and 9 GHz-μm respectively, indicating poor repeatability. Nevertheless, the f_t of 36.1GHz was much higher than what achieved with SiC MESFETs.

Despite all this exciting progress, no microwave power performance was reported until mid-1996. Also, except for the first long channel MESFET, GaN FETs above had breakdown voltages of only 20 ~ 35 V. As a comparison, GaAs MESFETs with similar current densities of 300 ~ 500 mA/mm generally show breakdown voltages of 7 ~ 15 V (for example [xv]). The 5 times higher breakdown field of GaN should result in 25 times higher breakdown voltages (Eq.1-2), namely 175 ~ 290 V. This indicated a great potential yet to be realized.

1.3 Synopsis

The principal objective of this dissertation is to develop a viable technology for GaN-channel FETs with excellent DC, small-signal RF and especially microwave power performances predicted for such a wide bandgap material. Device analysis is also to be performed to understand the operation mechanism and point way to future optimization.

In order to minimize the disadvantage of a low mobility and to outperform competing wide-band semiconductor devices, the AlGaN/GaN HEMT structure is chosen in this study. Material growth is by MOCVD due to it better maturity. Since detailed material parameters in the AlGaN-GaN system such as conduction band offset and the interface piezo-electric charge density are not well known, the device design and its improvement rely on first order calculations and on experimental analyses of fabricated devices.

Chapter 2 presents basic processing techniques for fabrication of GaN based devices developed in our laboratories and by other research groups. These include etching, Schottky contacts and ohmic contacts.

Chapter 3 describes the development of a basic but high quality AlGaN/GaN HEMT with satisfactory characteristics in all major aspects (including contact resistances, transconductance, pinch-off characteristics, current density, breakdown voltages, small-signal cutoff frequencies and microwave power density). The description starts with our first prototype of AlGaN/GaN HEMT without an insulating buffer and ends with a full-fledged device on a bi-layer insulating GaN buffer.

Chapter 4 discusses the most important issues for a new level of improvement. Based on the discussion, high Al-content devices are developed which show ultra-high power performances. Short channel devices by electron-beam lithography are also fabricated to access its potential to operate in millimeter-wave frequencies.

Chapter 5 depicts an analysis of device operation mode through investigation of the delay time, or the inverse of intrinsic current-gain cutoff frequency, as a function of drain bias. The dependence of breakdown voltage on gate-drain spacing is explained and the electron saturation velocity in the GaN-channel is calculated.

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Chapter 2
Processing Technique

Necessary processing techniques for a complete AlGaN/GaN HEMT include mesa isolation by etching, source/drain ohmic contacts and formation of a Schottky gate. Only techniques related to n-type GaN and AlGaN are discussed in this thesis.

2.1 Etching

Owing to the chemical inertness of GaN and AlGaN, there is not yet a suitable wet etching method for either gate recess or mesa isolation. Fortunately many dry etching schemes are available [i]. Among them, Cl_2 reactive-ion-etching (RIE) is very effective within the facilities of the co-search clean room in UCSB. Fig.2.1-1 and Fig.2.1-2 show the etch rate as a function of Cl_2 pressure and DC bias. It is seen that the etch rate depends much more on the DC-bias than on the Cl_2 pressure, indicating the etching is highly energy driven. For this reason, RIE gate-recess generally introduces damage and reduces breakdown voltages of GaN-based FETs [ii]. However, as a means of mesa isolation, Cl_2 RIE has been proven very satisfactory. Fig. 2.1-3 shows a scanning-electron-microscope (SEM) image of a 4-μm-high GaN mesa etched using a Cl_2 pressure of 10 mTorr and a DC bias of 500 V. The mesa boundary is smooth and well defined by the processing standard of electronic devices. Presumably due to the less damage on the vertical side-wall than the directly bombarded horizontal surface, such an isolation scheme does not seem to reduce breakdown voltages of GaN-channel FETs.

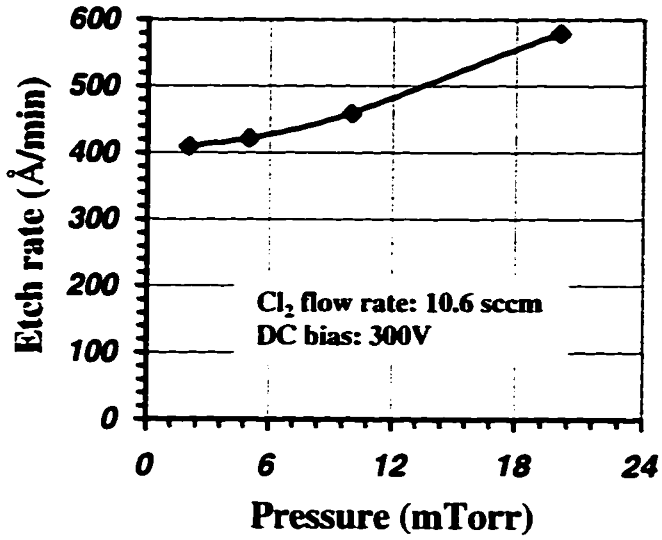

Fig.2.1-1 *Etch rate of GaN by Cl_2 RIE vs. pressure (with RIE machine #1, co-search clean room, UCSB).*

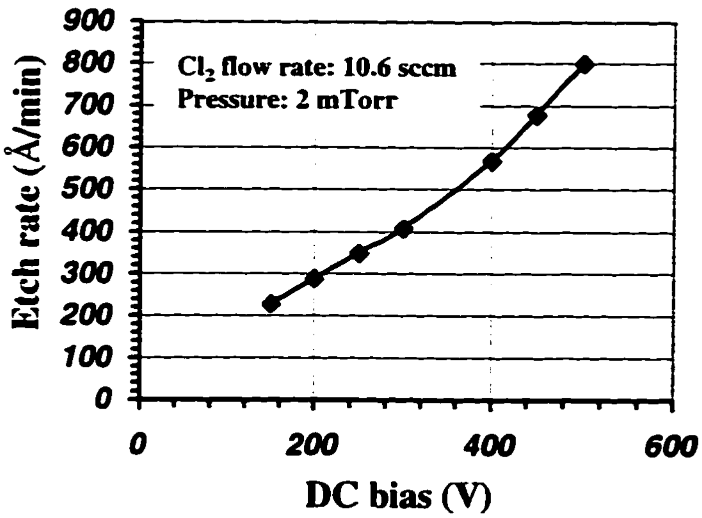

Fig.2.1-2 *Etch rate of GaN by Cl_2 RIE vs. DC bias.*

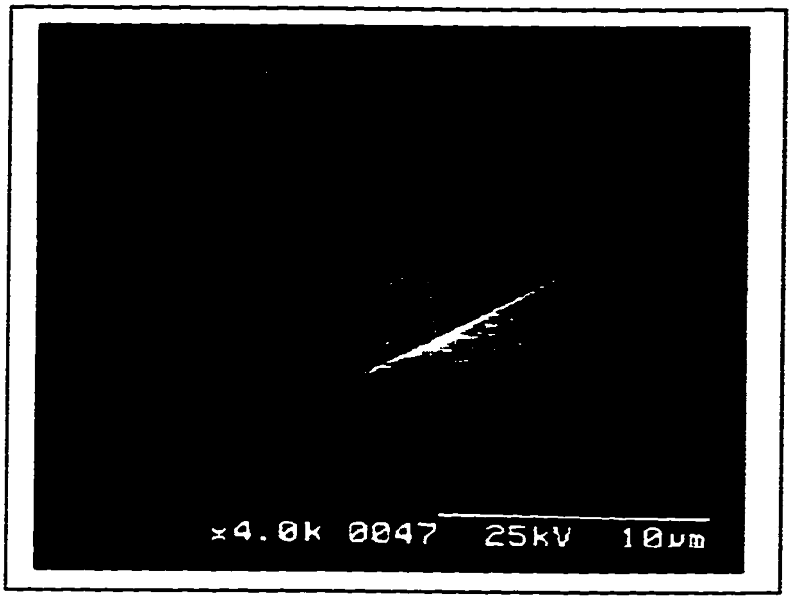

Fig.2.1-3 *SEM image of a 4-µm-high GaN mesa by Cl_2 RIE*

2.2 Shottky contacts

Extensive study has been carried out by many groups to investigate Schottky barriers of different metals on GaN. Unlike GaAs where the Femi-level at the surface is pinned at mid-gap owing to the high density of surface states, GaN exhibited very different Schottky barriers with various metals which generally followed the calculation by work function difference. This indicates a low extend of barrier pining by surface traps. An electron affinity of ~ 4.2 eV can be deduced from published experimental results [iii] [iv] [v]. In particular, Al (with a work function Φ ~ 4.2 eV) always forms a natural ohmic contact on clean n-GaN surfaces; while Au, Pt and Ni (Φ = 5 ~ 5.5 eV) have relatively high Schottky barriers of 0.8 ~ 1.1 eV on n-GaN and are potential candidates for a gate metal of GaN MESFETs. A similar trend were observed on AlGaN [vi].

An important observation is that, except for GaN's extremely high stability, surface cleaning before metal deposition was found necessary for a well behaved

Schottky contact. Fig.2.2-1 shows the IV characteristics of an Au/GaN junction with and without HF cleaning before evaporation of Au. The ideality factor of the former is 1.07, while it is > 4 for the latter, indicating the existence of a thin surface insulator (presumably an oxide layer). Either HF, NH_4OH or HCl could effectively remove such an insulating layer.

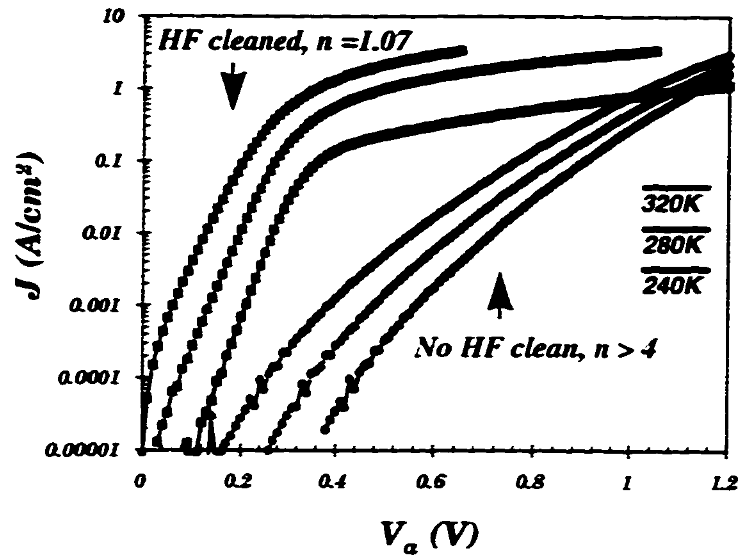

Fig.2.2-1 *IV characteristics of Au/GaN Schottky junctions with and without HF cleaning.*

2.3 Ohmic contacts

As mentioned before, Al forms a natural ohmic contact to n-GaN which was first pointed out by Foresi et al.[vii], but the specific contact resistance is on the order of 10^{-4} Ω/cm^2, not satisfactory for FET fabrication. Ti/Al (220Å/2200Å) annealed at 900 °C for 30 s yielded a much lower contact resistance of 9 x 10^{-6} Ω/cm^2 [viii]. The mechanism was traced to the formation of TiN which is a semi-metal, and in turn a high extend of nitrogen deficiency which is effectively an n-type doping. The resultant n^+-GaN interface and the conductive TiN constitute the necessary components for a tunneling contact. Subsequent investigation by us with a thin Ti (200Å) annealed at 975 °C for 30 s followed by depositing an overlayer of Au resulted in an even lower contact resistance of 3 ~ 5 x10^{-6} Ω/cm^2, supporting the tunneling-contact mechanism [ix]. This separate-layer method resulted in a much better contact morphology but required a re-alignment for depositing the Au layer. More recently, Fan et al.[x] reported a further reduced contact resistance of 9 x10^{-8} Ω/cm^2 by a multi-layer ohmic scheme with Ti/Al/Ni/Au (150Å/2200Å/400Å/500 Å) annealed at 900 °C for 30 s. RIE etching with Cl_2 and then BCl_3, each for 20 s, was used to introduce damage on the ohmic region before metal deposition. The Au layer was for a better conductivity and for preventing oxidation of the Al, while the Ni was for reducing the Au/Al missing. The morphology of the ohmic surface was also improved from that of the Ti/Al scheme.

It is un-clear in reference [viii] whether a surface cleaning was performed before evaporation of the Ti/Al. Repeating the experiment in our labs on n-GaN samples (n = 1 ~ 2 x 10^{17} cm^{-3}) with an HF surface cleaning step resulted in a lower specific ohmic contact resistance of 4 x 10^{-6} Ω/cm^2 and a lower optimal annealing temperature of 650 ~ 700 °C instead of 900 °C.

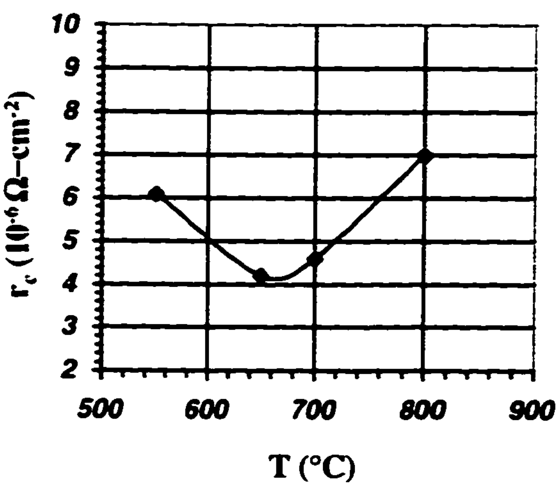

Fig.2.3-1 *Specific contact resistance of Ti/Al on n-GaN vs. annealing temperature.*

This Ti/Al scheme was used in fabricating our earlier AlGaN/GaN HEMTs due to its simplicity. while in the later stage, the Ti/Al/Ni/Au scheme was employed for a higher performance. The specific contact resistance (in Ω/cm^2) for an AlGaN/GaN HEMT is not relevant since the sheet resistance under the ohmic alloy. which was originally the same as that of the channel. is completely different after annealing. In such case. only the transfer contact resistance (in Ω-mm) matters. which directly adds to the on-resistance of the FET. Optimal annealing temperature for an AlGaN/GaN HEMT with the Ti/Al/Ni/Au scheme was found to be ~ 900 °C as shown in Fig.2.3-2. The AlGaN layer was thinned to 100 Å before deposition of the contact metals. This was based on our previous study which showed that the reaction depth of Ti on GaN was about 160 Å [vi]. A similar or less reaction depth is expected on AlGaN. Fig.2.3-3 shows the IV characteristics of two devices with and without such pre-thinning. The difference in the device on-resistances confirms the prediction. Both experiments were performed in the later stage of this research. since the Ti/Al/Ni/Au scheme was not published when our early devices were fabricated.

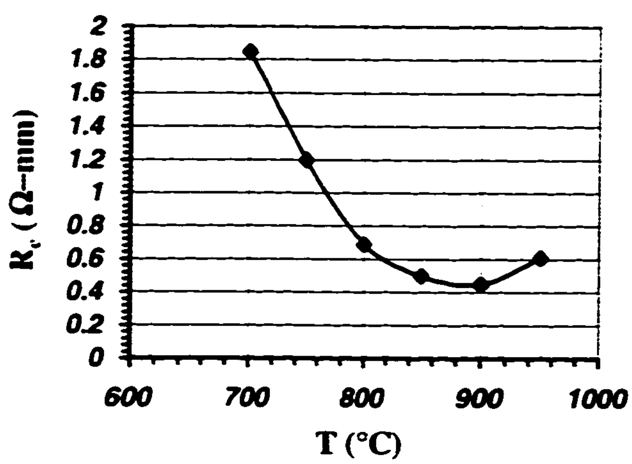

Fig.2.3-2 *Transfer contact resistance vs. annealing temperature. The experiment was performed on an* $Al_{0.25}Ga_{0.75}N$*/GaN HEMT sample in the later stage of this research.*

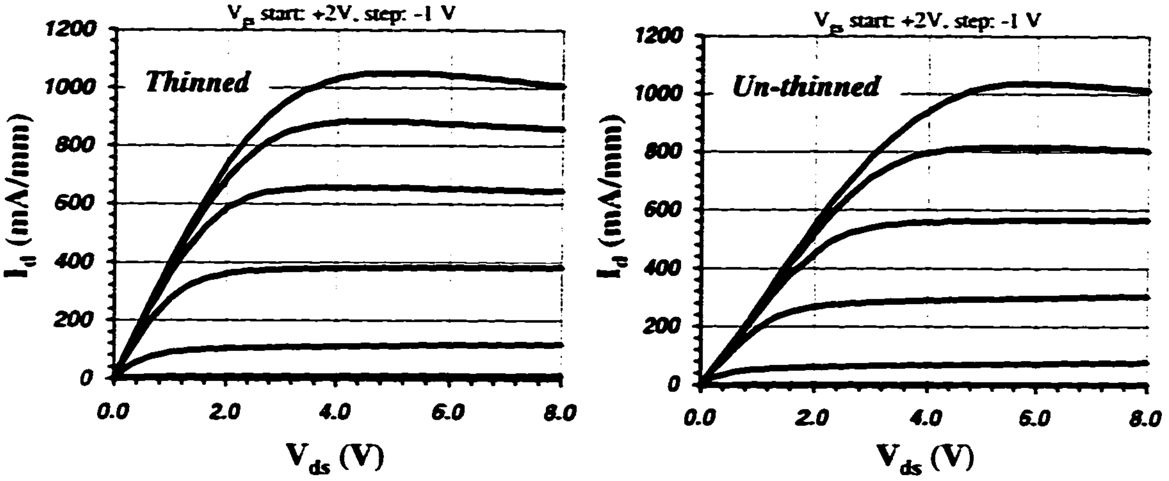

Fig. 2.3-3 *Effect of thinning the AlGaN layer before evaporation of the ohmic metal on IV characteristics of AlGaN/GaN HEMTs. Both devices were on the same epi-structure with an* $Al_{0.35}Ga_{0.65}N$ *layer of 200 Å, which was thinned to 100 Å for the device on the left and not thinned for the device on the right. Ohmic scheme: Ti/Al/Ni/Au (200 Å/2000Å/400Å/500Å) annealed at 870 °C for 20s.*

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Chapter 3
Basic AlGaN/GaN HEMTs

This chapter describes the development of $Al_{0.15}Ga_{0.85}N/GaN$ HEMTs with satisfactory characteristics. The Al content of 15% was chosen since it generally results in the best mobility. The goal characteristics include 1) A high breakdown voltage predicted for GaN; 2) High and uniform transconductance by the standard of a HEMT; 3) A contact resistance lower than or at least close to the channel access resistances; 4) Good pinch-off characteristics—off state current at least 3 orders lower than the on-state current; 5) Cut-off frequencies close to a conventional GaAs MESFET; 6) A reasonably high output power density even on the thermally resistive sapphire substrates.

3.1 Our first prototype of AlGaN/GaN HEMTs—Devices with un-intentionally-doped GaN channels

Growth study of GaN in UCSB started in early 1995 with the MOCVD reactor No. 1, which was originally used for InP-based materials. Sapphire substrates were used due to its high quality and low price. The lattice mismatch (by ~ 15 %) between sapphire and GaN was overcome by optimization of the nucleation layer. The growth was conducted in atmospheric pressure (AP) for a high NH_3 over pressure. In July of the same year, our GaN films were among the state-of-the-art in literature as represented by room-temperature bulk mobilities greater than 600 cm^2/Vs with 1-μm-thick epi-layers [i]. However, the un-intentional (UID) background n-type doping was ~ $2x10^{17}$ cm^{-3}, too high for use as an under-layer (if not a buffer layer) for a HEMT. With the successful installation of MOCVD reactor No.2 in late 1995, which was dedicated to the growth of GaN and its alloys, the background doping density of a GaN film grown at atmospheric pressure was reduced to ~ $4x10^{16}$ cm^{-3}. Subsequent success in growing a strained $Al_{0.15}Ga_{0.85}N$ layer made our first prototype of AlGaN/GaN HEMT possible. The batch number of the sample presented here is 960207GB, grown by Dr. Bernd Keller.

3.1.1 *Device fabrication*

The device layer-structure used for this study is shown in Fig.3.1-1. The growth started with a 200 Å GaN nucleation layer on a C-plane sapphire substrate. This was followed by the 0.3 ~ 0.4 μm GaN channel unintentionally doped (UID) with a background doping density around $4x10^{16}$ cm^{-3}. The $Al_{0.15}Ga_{0.85}N$ gate structure consisted of a 30 Å spacer, a 150 Å Si-doped charge supply layer (n = $3x10^{18}$ cm^{-3}) and a 120 Å unintentionally doped cap. The background doping density of the UID $Al_{0.15}Ga_{0.85}N$ from our reactor was ~ $1x10^{18}$ cm^{-3}. Mesa isolation for the devices was done with Cl_2 RIE. Source/drain ohmic scheme was Ti/Al annealed at 660 °C, while gate metalisation was 5000 Å of Au deposited by electron beam evaporation. The gate length was 1.2 μm.

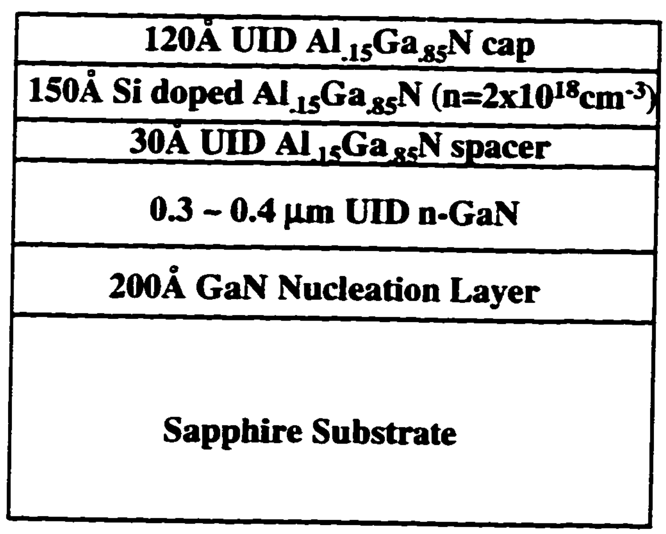


Fig.3.1-1 *Layer structure of the AlGaN/GaN HEMT.*

Capacitance-voltage profiling on the gate diode revealed that most carriers were located at the AlGaN/GaN interface. Hall measurement result on a HEMT sample as seen in Fig.3.1-2 shows a maximum mobility of 5800 cm^2/Vs at < 20 K. The room temperature mobility is 1500 cm^2/Vs, the highest achieved on an AlGaN/GaN structure to date. The Hall carrier concentration of ~ 7.5×10^{12} cm^{-2} remains nearly constant from 320 K to 10 K, suggesting a dominant 2DEG conduction. Transmission-line-model (TLM) measurement yielded a contact resistance of 3 Ω-mm.

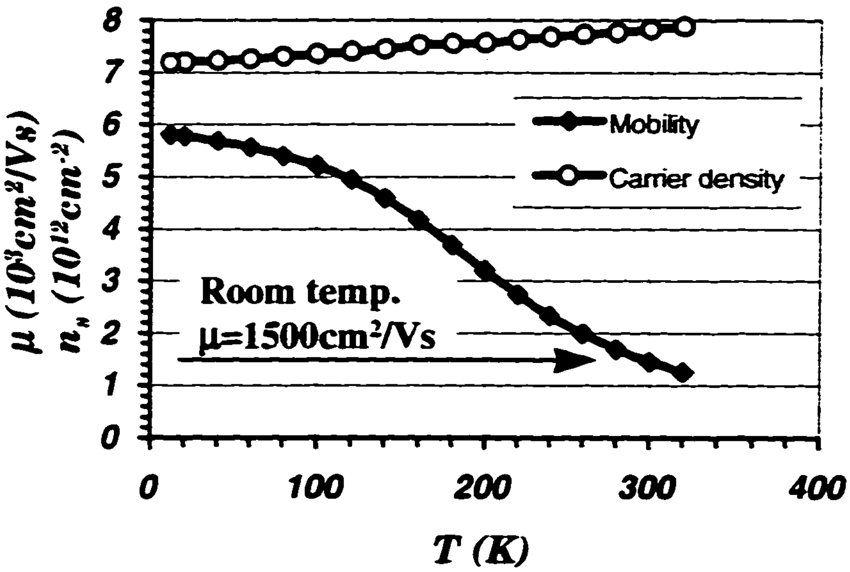
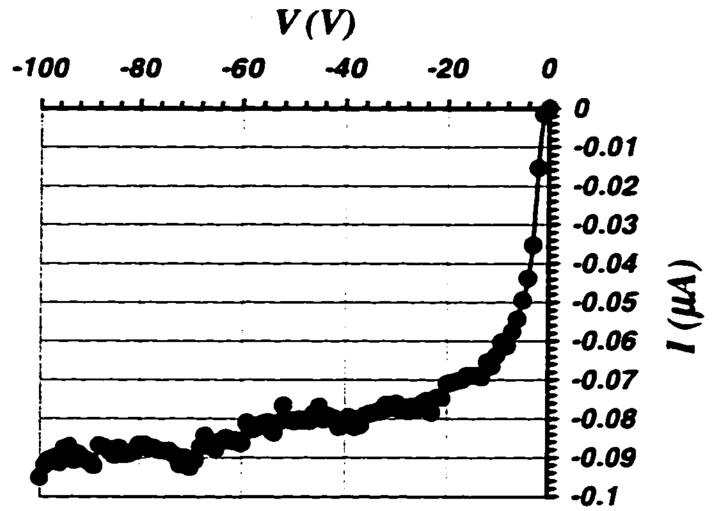


Fig.3.1-2 *Mobility & carrier concentration of an $Al_{0.15}Ga_{0.85}N$/GaN HEMT sample.*

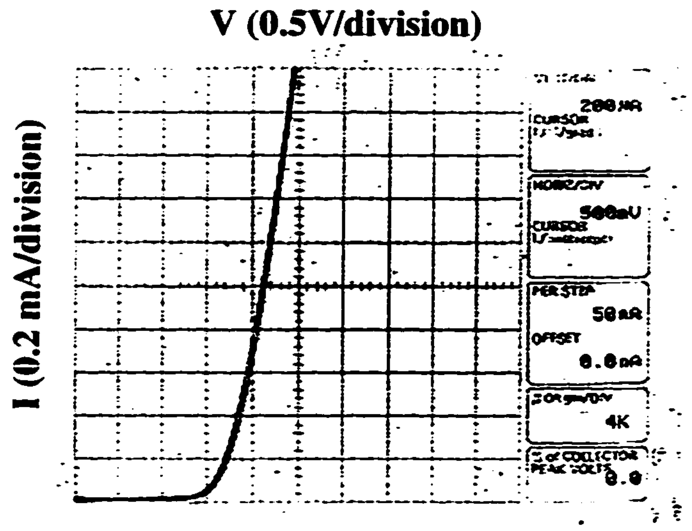
3.1.2 *Device performance*

Fig.3.1-3 is the gate to drain IV characteristics of a device with 3 μm gate-to-drain spacing (L_{dg}) showing a turn-on voltage of 1.7 V and a breakdown voltage of 230 V. The leakage current is 0.1 μA or 0.66 $nA/\mu m^2$ at 100 V (reverse). Devices with L_{dg}'s of 2 μm and 1 μm have lower breakdown values of ~

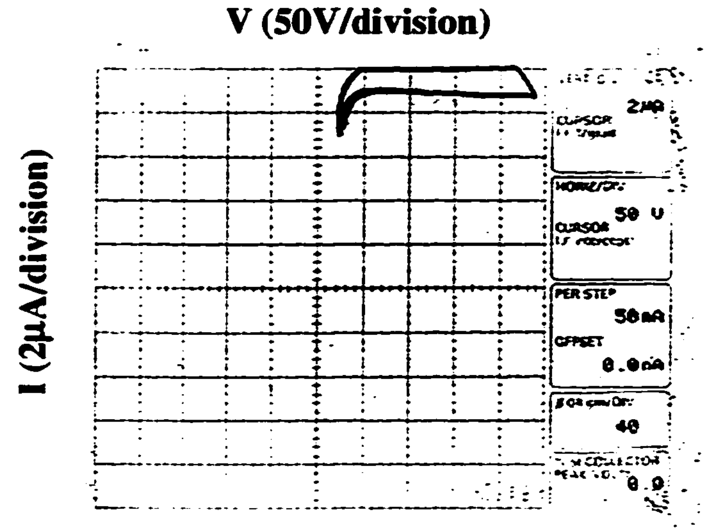
170 V and ~ 100 V respectively. The best measured breakdown voltage was 340 V for L_{dg} = 3μm with a similar HEMT structure without intentional Si doping in the AlGaN layer. At such breakdown voltages, the average electric field on the drain side was up to half of the theoretical value of 2×10^6 V/cm for GaN, approaching the limit of the wide bandgap semiconductor.



(a) Reverse Leakage



(b) Forward



(c) Reverse Breakdown

Fig.3.1-3 *Gate-to-drain diode I-V characteristics of a GaN HEMT with* $L_g = 1.2$ *μm,* $L_{gd} = 3$ *μm,* $w = 150$ *μm.*

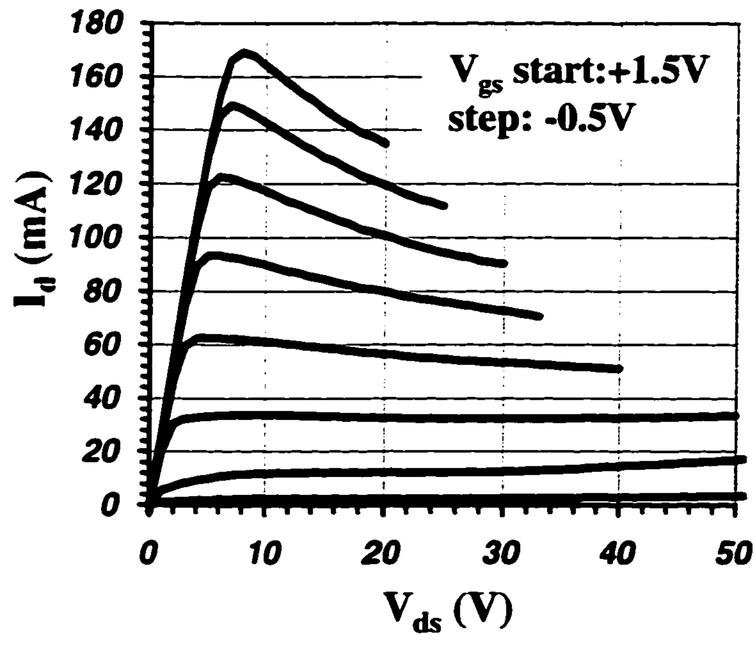


Fig.3.1-4 *Output DC characteristics of a GaN HEMT. (*$L_g = 1.2$ *μm,* $L_{ds} = 4$ *μm,* $w = 500$ *μm)*

The output I-V characteristics of a device with 4 μm source to drain spacing and 0.5 mm width are shown in Fig.3.1-4. Useful current density of 340 mA/mm and quite linear transconductance (g_m) with a maximum value of 120 mS/mm were obtained. A higher g_m of 140 mS/mm was obtained on devices with a source to drain separation of 3 μm. The pinch-off of this particular device is fairly good. However, due to the difficulty in achieving a good wafer uniformity without a thick insulting buffer, most devices showed soft pinch-off characteristics as seen in Fig.3.1-7.

The apparent negative resistance on the I-V curves is attributed to self-heating as a result of the poor thermal conductivity of the sapphire substrate. For a power device, this decreased channel current directly leads to output power reduction. To characterize this effect, we define the current heat dissipation figure of merit (CHDF) = (channel current @ high DC power dissipation) / (peak channel current). In particular, CHDF = (I_{dss}@5W/mm)/$I_{dss,max}$. Devices having low thermal impedance should have a CHDF of 1, while in the case of poor heat removal, CHDF should be < 1. Fig.3.1-5 is a plot of the CHDF of a GaN HEMT as a function of temperature. At 300 K the CHDF of ~ 80 % indicates 20 % of current reduction due to self-heating, while at 80 K the CHDF of 100 % suggests a largely improved thermal conductivity of the substrate, in good agreement with the fact that the thermal conductivity of the ceramic sapphire at 80 K is one order higher than at 300 K.

The DC performance of a GaN HEMT was characterized at various temperatures from 80 K to 573 K as shown in Fig.3.1-6. Both the full channel current and the transconductance increase with decreasing temperature due to the enhanced mobility as a result of reduced phonon scattering. At high temperatures as seen in Fig.3.1-7, the device shows little detrimental parallel conduction but the channel pinch-off becomes softer. This is related to the poor material quality at the GaN-sapphire interface. A simulation by Mansor et al [ii] predicted the electron saturation velocity of n-GaN to be relatively independent of temperature. The highly temperature dependent channel current suggests that a significant part of the HEMT channel is in a gradual channel mode.

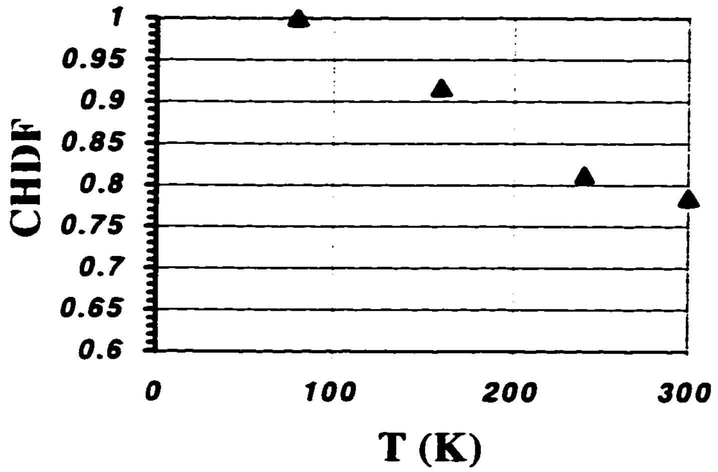


Fig.3.1-5 *CHDF of a AlGaN/GaN HEMT vs. temperature.*

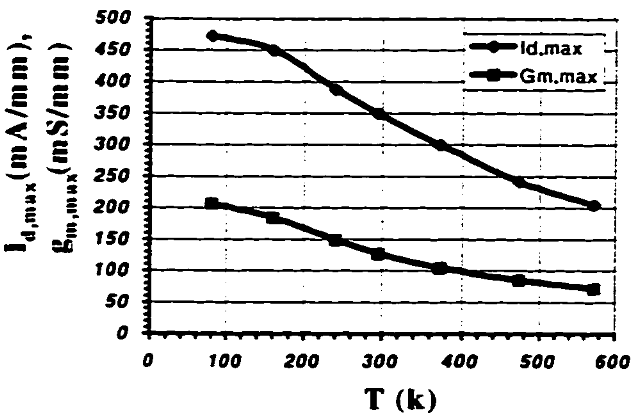


Fig.3.1-6 *Peak channel current and transconductance vs. base temperature.*

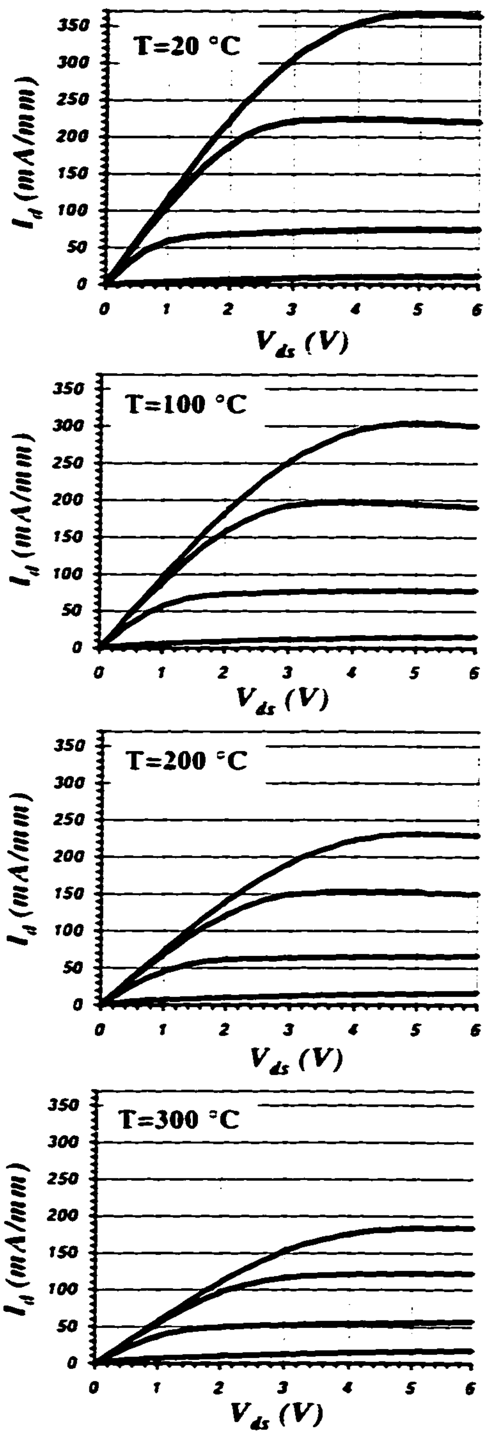


Fig.3.1-7 *Output I-V characteristics of an AlGaN/GaN HEMT at different temperatures.*

Small signal RF performance was characterized with a HP870 Network Analyzer. The highest current cutoff frequency of 6.5 GHz was measured at a source to drain voltage of 15 V while the peak maximum oscillation frequency of 15 GHz was at 20 V. These relatively low cutoff frequencies may be due to a combination of the poor ohmic contact and the drain extension before velocity saturation which will be discussed in chapter 5.

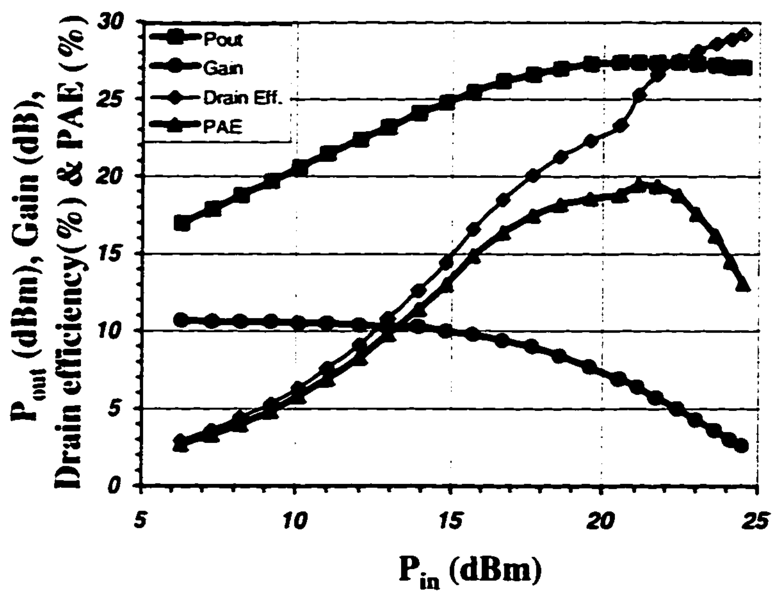


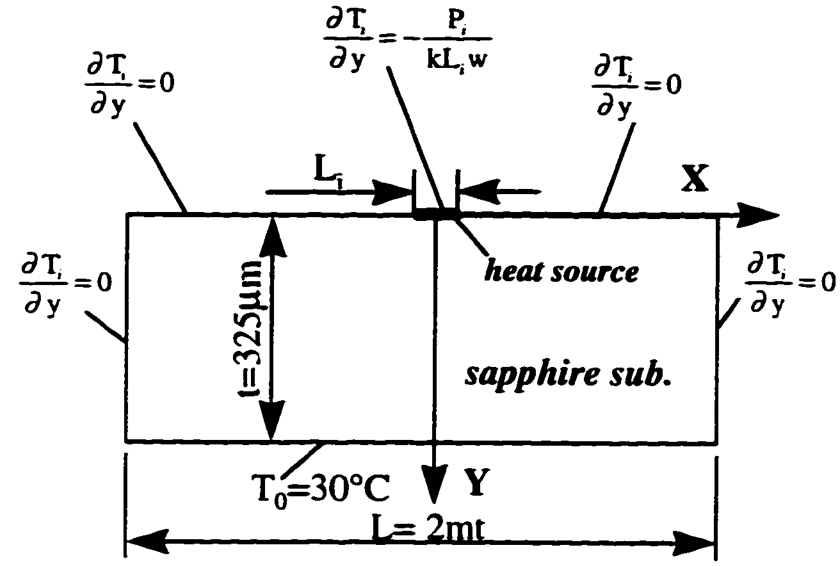
Fig.3.1-8 *RF power performance of a GaN HEMT. Frequency: 2 GHz. Device dimensions:* L_g *= 1.2 μm,* L_{ds} *= 4 μm, w = 500 μm. Quiescent DC bias:* V_{ds}*= 26 V,* I_d *= 66 mA. Small signal gain: 10.6 dB. Maximum power output: 1.1 W/mm with PAE = 18.6 %.*

Microwave power measurements at 2 GHz were performed on wafer without cooling. Manual tuners were used in the experiment. The device under test had a gate width of 0.5 mm. Although its breakdown voltage was larger than 100 V, due to the self-heating problem, a compromised class A quiescent DC bias of V_{ds} = 26 V & I_d = 66 mA/mm was used. The measurement result is shown in

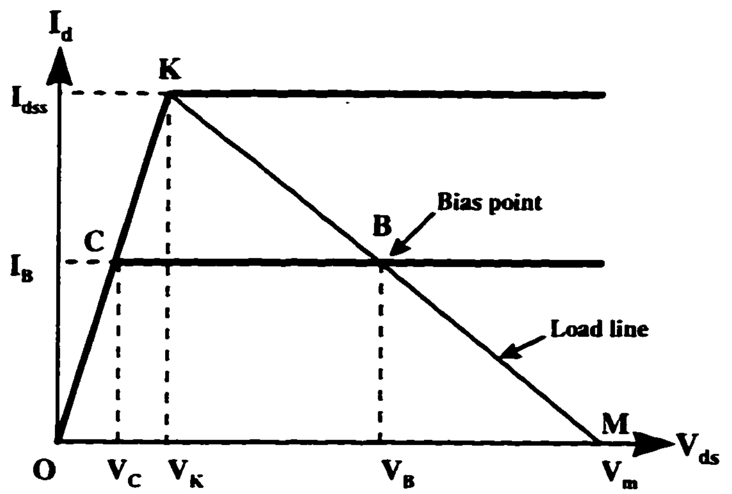
Fig.3.1-8. At the input power of – 21 dBm, a maximum output power of 550 mW was recorded, translating to an output power density of 1.10 W/mm with a power added efficiency (PAE) and a drain efficiency of 18.6 % and 23 %, respectively. The small-signal linear gain was 10.7 dB. At a lower bias voltage of 24 V, the peak output power was 1.02 W/mm with a higher PAE of 20.1 %. Device performance degraded at higher bias than 26 V.

3.1.3 *Thermal simulation*

To understand the limiting factor of the GaN HEMT's power ability, a quantitative temperature calculation is necessary. While a thermal resistance method can be used to estimate the transistor channel temperature, a mathematical thermal simulation produces much more information with a temperature map, revealing the bottleneck in the heat path and pointing the way towards effective device cooling. By neglecting the thin epi-layer and assuming the transistor channel to be the heat generation source, our first simulation estimated a channel temperature of 360 °C for the device in the power experiment [iii], which is very close to the result of 367 °C using the transmission line method proposed by Cooke [iv]. In literature there has been inconsistency in defining the heat-generation source for the thermal calculation of an FET. The gate, the gate-to-drain region and the source-to-drain region were treated as the heat sources by Cooke [ii], Huang et al [v], Culbertson and Lehmann [vi], respectively. Discrepancies as high as 30 % can be introduced with different treatments. In order to increase accuracy, we propose a thermal calculation with a dual-heat-source model. Heat generation is partitioned into the active region—the channel, and the parasitic region—the ohmic contact & the channel access region. The length of the channel is defined as the gate-length plus the gate-to-drain depletion distance, while the length of the parasitic region is considered as the ohmic contact transfer lengths plus the source-to-drain spacing. These are 1.5 μm and 11 μm respectively in our case.



(a)



(b)

Fig.3.1-9 *(a) A two dimensional heat conduction model for the sapphire substrate under the HEMT channel (the device has two gate fingers in a straight line with a gate-feed at the center).*

(b) The piece-wise output IV characteristics for determining the heating power in the parasitic region.

i: index of a heat source
t: sapphire substrate thickness
T_0: heat sink temperature
L: wafer width (2m = L/t)
L_i: length of a heat source
w: device width
k: sapphire thermal conductivity
P_i: power dissipation of a heat source
V_K: knee voltage
V_M: maximum source-to-drain voltage

The two dimensional heat conduction model for a cross-section of the FET [shown in Fig.3.1-9(a)] is established based on the fact that the device width is much larger than the channel length. Temperature rise due to each heat source is found by mathematically solving the steady state Laplace Heat Conduction Equation as:

$$\nabla T_i(x,y) = \sum_{n=1}^{\infty} \frac{2P_i mt}{n^2\pi^2 wL_i k} \frac{\sin[\frac{n\pi L_i}{2mt}]}{\cosh[\frac{n\pi}{m}]} \cdot \cos[\frac{n\pi}{mt}x]\sinh[\frac{n\pi}{mt}y] + \frac{P_i(1-\frac{y}{t})}{2mwk}$$

where for the heat source in the active region i = 1, while in the parasitic region i = 2. Other symbolic parameters are as shown in the figure. The actual temperature can be obtained by super-position: $T(x,y) = \Delta T_1(x,y) + \Delta T_2(x,y) + T_0$. The GaN layer has a much higher thermal conductivity than sapphire and has the effect of relieving heat constriction. An equivalent heat path analysis shows that the effective length of a heat source seen by the sapphire substrate increases by $2t_0\sqrt{\frac{k_0}{k}}$, where k_0 and k are the thermal conductivities of GaN and sapphire respectively; t_0 is the GaN layer thickness. The total power dissipation (P) is determined from the experimental data: P = dc power (P_{dc}) + input ac power (P_{in}) - output ac power (P_{out}), which was 4 W/mm at the maximum power output. A simple analysis with the piece-wise output IV characteristics of an FET [Fig.3.1-9(b)] shows the power dissipation in the parasitic region to be $P_1 = P_{dc}V_k/(V_m+V_k)$, which is ~ 0.65 W/mm in our case. The other 3.35 W/mm is allocated to the channel.

Thermal conductivity of the sapphire substrate is a strong function of temperature [vii]. However, little complication is introduced provided that the temperature (T) dependence of the thermal conductivity (k) satisfies: $k(T+273)^{\alpha}$ = constant, where α is a constant. As a matter of fact, the relation below is a very good approximation with an error less than 9 % through out the temperature range of 20 to 800 °C:

$$k(T) = 0.41\text{x}300/(T+273).$$

With this, a reference temperature distribution $T(x,y)$ can be obtained using the thermal conductivity at 27 °C. Then Kirchhoff's transformation [viii] is applied to find out the true temperature:

$$T_{true}(\text{x,y}) = (T_0+273)\exp\{[T(x,y)-T_0]/300\}-273$$

where all temperatures are in °C.

Fig.3.1-10 is the resultant temperature contour map showing the HEMT channel to be at 318 °C.

Mobility degradation by a factor of 3 is expected at such an elevated temperature [ix]. The substantially increased parasitic resistance due to the mobility degradation, together with the poor ohmic contact, should be responsible for the low PAE of 18.6 %. Increasing bias voltage will accelerate the self-heating problem, leading to further reduction in electron mobility and channel current. This limits the output power of the present device.

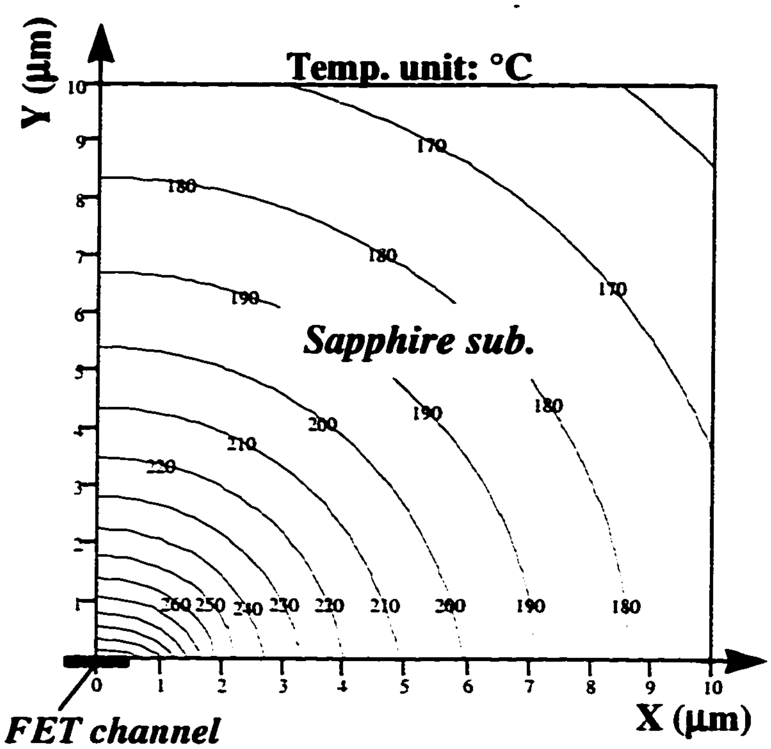


Fig.3.1-10 *Calculated temperature contours of the sapphire substrate under the HEMT channel. [For devices with a thick GaN buffer, the transistor channel temperature can be found as:* $T_c = T_s + \frac{P}{\pi k_0 w} \ln(\frac{L_h + 2t_0}{L_h})$, *where* T_s *is the substrate temperature under the channel,* k_0 *and* t_0 *are the thermal conductivity and thickness of the buffer layer, respectively.]*

The very high temperature gradient around the HEMT channel points out that an effective cooling scheme should involve material of high thermal conductivity placed very close to the device channel. Increasing the epilayer thickness by a buffer can also help heat flux to spread out. Obviously, using a high thermal conductivity substrate like SiC is technically one of the best solutions.

In summary, the first prototype of our AlGaN/GaN HEMTs demonstrated gate to drain breakdown voltages of 230 ~ 340 V (with gate-drain spacing of 3 μm), extrinsic transconductances of 100 ~ 140 mS/mm and full channel currents >

300 mA/mm. A 0.5-mm-wide device produced a CW output power of 1.1 W/mm at 2 GHz without cooling, which was the first experimental microwave power performance in literature. A duel-heat-source mathematical thermal simulation for an FET cross-section was also performed, estimating a channel temperature > 300 °C.

3.2 AlGaN/GaN HEMTs with n^+ re-grown ohmic contacts

The contact resistance of 3 Ω-mm for the above devices was much higher than the access resistance of ~ 0.7 Ω-mm with a source-gate spacing of 1 μm. Such a high resistance not only reduces extrinsic transconductance and cutoff frequencies but also limits the operation efficiency and aggravates self-heating. As a solution to the problem, a new ohmic scheme using n^+ source and drain re-growth was developed.

Two samples with the same nominal epi-layer structure were used for a direct comparison of the n^+ re-growth method with the conventional method. The process flow of the n^+ re-growth method is shown in Fig.3.2-1. First, a 4000 ~ 5000 Å thick SiO_2 pattern was deposited by electron beam (E-beam) evaporation. With this as a mask the $Al_{.15}Ga_{.85}N$ layer and 1000 Å GaN in the source and drain regions were etched by Cl_2 RIE. Then the wafer was transferred into the MOCVD reactor and 3000 Å of n^+ GaN (Si doped to $2x10^{18}$ cm^{-3}) was re-grown. Over-growth was avoided by choosing the proper orientation. Fig.3.2-2 is the SEM image of the re-grown source-drain region, showing clear-cut re-growth boundaries. The SiO_2 was removed with HF after the re-growth and the rest of the process was the same as the conventional device: Ti/Al (200Å/2000Å) was evaporated and annealed at 670 °C. Mesa isolation was done by Cl_2 RIE with photo-resist as the mask. Finally, 4800 Å of Au was deposited as the gate metal.

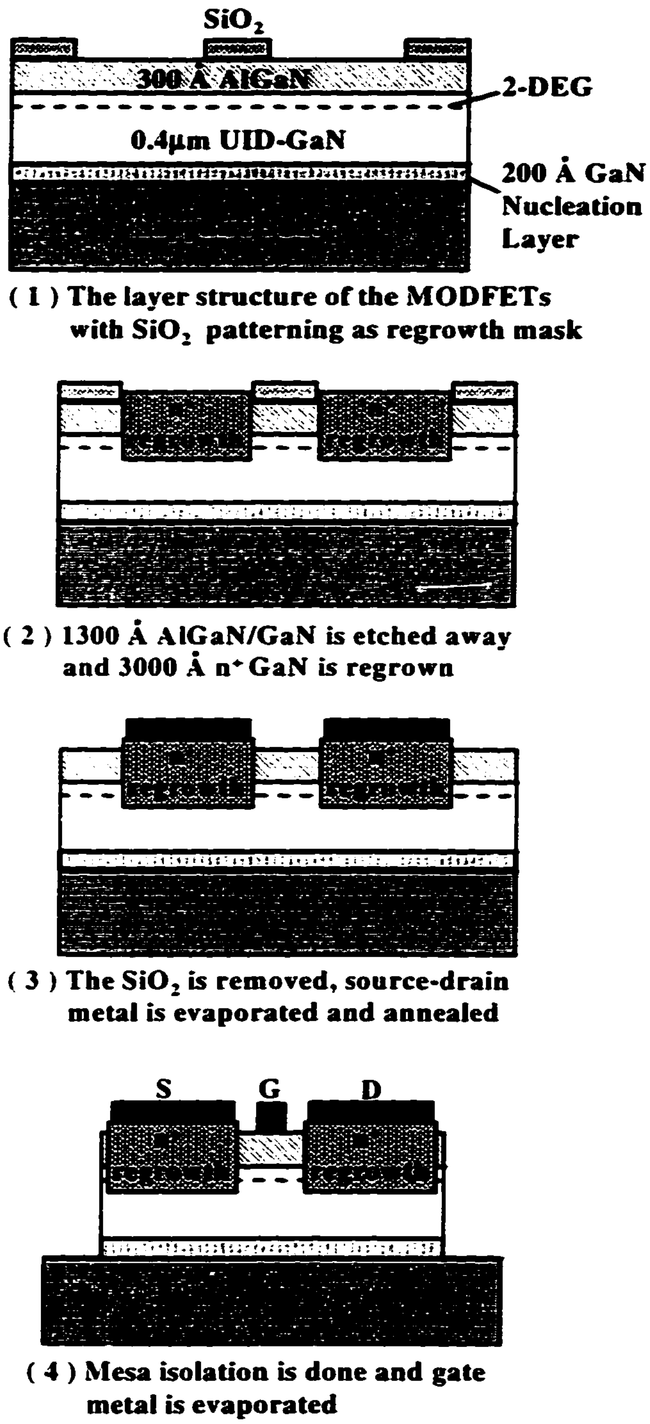


Fig.3.2-1 *Process flow of the GaN HEMT with n^+ re-growth ohmic contacts.*

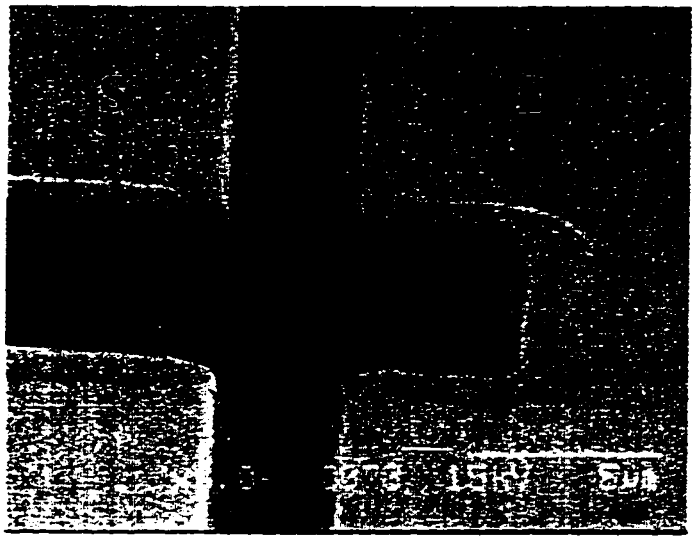


Fig.3.2-2 *An SEM image of the re-grown n^+ GaN source/drain before SiO_2 removal.*

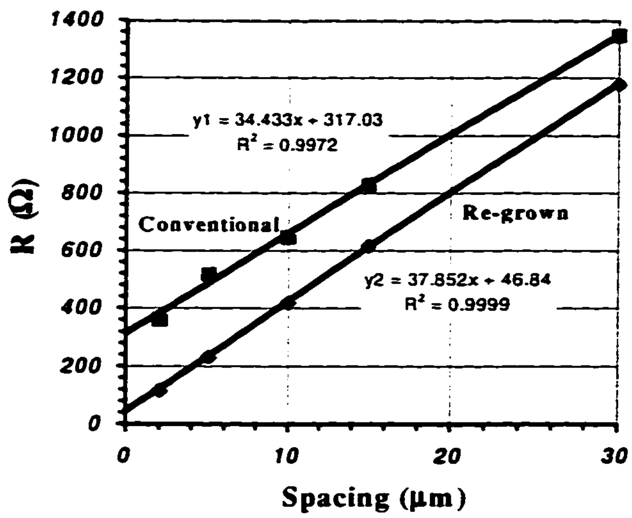


Fig.3.2-3 *The transmission line measurement results for determining contact resistances of the GaN HEMTs. (1. Conventional method: R_c= 3.0 Ω-mm; 2. n^+ re-growth method: R_c= 0.44 Ω-mm.)*

On-wafer TLM patterns, each 19 μm square with spacing from 2 to 30 μm, were used for the contact resistance measurement. Fig.3.2-3 shows the results of both methods. A typical transfer contact resistance of 0.44 Ω-mm was achieved with the re-growth ohmic contact, not far from the 0.2 Ω-mm value generally obtained with a GaAs MESFET. Compared with the 3 Ω-mm value using the conventional scheme, the new method showed an improvement by a factor of 7.

The HEMT output IV characteristics are shown in Fig.3.2-4. The new scheme resulted in a much lower knee voltage of ~ 3 V, a higher transconductance of 170 mS/mm and a better current-gain cut-off frequency of 10 GHz, as compared with the values of 7 V, 130 mS/mm and 7 GHz accordingly for the conventional scheme (gate-lengths were both 1.2 μm). No degradation of breakdown voltages was observed with the new ohmic contact method.

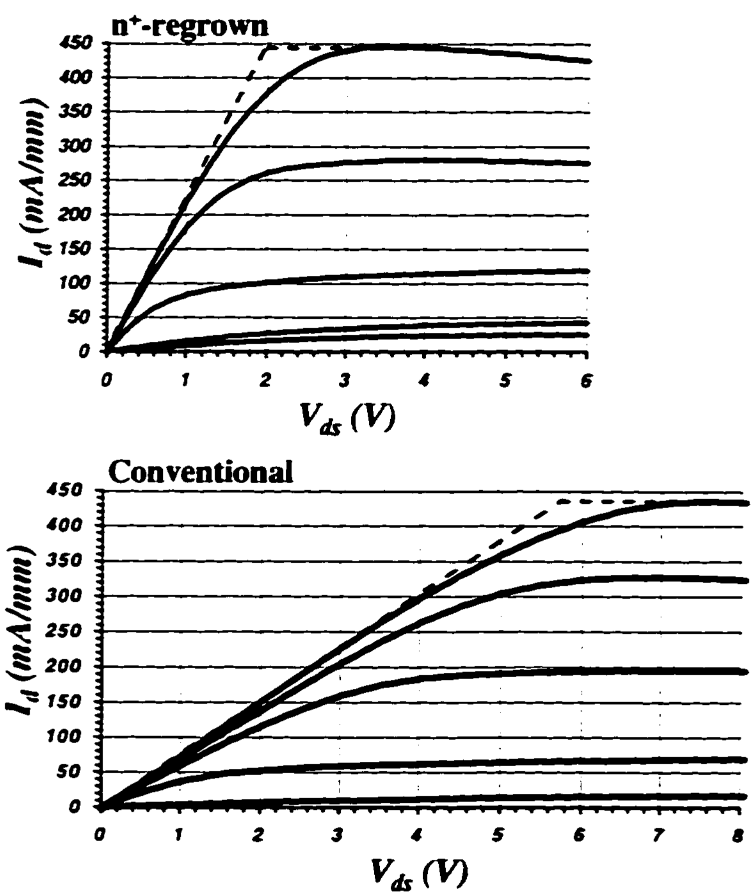


Fig.3.2-4 *Comparison of the output characteristics of the HEMTs with two ohmic contact schemes (V_{gs} start: +1.5V, step: -1V).*

As a short summary, a new ohmic contact scheme for AlGaN/GaN MODFETs with n^+ re-growth was developed, which yielded a low transfer ohmic contact resistance of 0.44 Ω-mm. Since the n^+ ohmic region is defined by E-beam evaporated SiO_2 through lift-off, a clear-cut ohmic edge can be achieved which potentially facilitates fabrication of deep sub-micron devices.

3.3 AlGaN/GaN HEMTs on I-GaN buffer grown at lower pressure

The growth of a number of similar AlGaN/GaN HEMTs without an insulating buffer layer revealed that the wafer uniformity, especially the GaN layer thickness, was very difficult to control. A viable device technology calls for an insulating GaN buffer. Experimental growth investigation by Dr. Stacia Keller showed that when grown under low pressure (LP), an insulating GaN epi-layer could be achieved. The measured resistivity was better than 50 MΩ/sq for a 2 µm thick film. Photo-luminescence showed a dominant yellow band with an activation energy ~ 2 eV, indicating poor optical quality. However, the standard for electrical quality can be very different. As a buffer layer of an FET, the ultimate criteria is generally the subthreshold characteristics of the FET, in particular, the off-state current and the sub-threshold swing (SW).

Due to the Debye tail in charge distribution, it is impossible to turn off an FET abruptly. SW represents how fast the drain current is shut-off by the gate bias below the threshold. The drain current in the subthreshold regime can be expressed as

$$I_d \propto e^{(-\eta \frac{V_{gs}}{kT/q})}$$

where kT/q is the thermal voltage, η the ideality factor.

SW is defined as

$$SW = \frac{dV_{gs}}{d(\lg I_d)} = \eta(\frac{kT}{q}\ln 10)$$

$$= 60(T/300)\eta \ \text{(mV/decade)}$$

The smaller the SW the better. In the ideal case of $\eta = 1$, SW = 60 mV/decade at room temperature. Practically $\eta > 1$. In fact, a typical commercial GaAs MESFET has a room temperature SW of 130 mV/decade, or an ideality factor of 2.1.

To investigate the buffer quality by the above standard, AlGaN/GaN HEMTs were fabricated on a 1.4 µm thick I-GaN layer grown under low pressure. The layer structure was grown by Peter Kozodoy (batch # 960821LP). On top of the I-GaN buffer were a 30 Å UID $Al_{0.15}Ga_{0.85}N$ spacer, a 150 Å $Al_{0.15}Ga_{0.85}N$ donor layer (with Si doping density of $3\text{x}10^{18}$ cm^{-3}) and a 120 Å UID cap. Mobility and carrier density measured on a similar structure were 600 cm^2/Vs and $4.5\text{x}10^{12}$ cm^{-2}, respectively. The device fabrication procedure was the same as before except that the gate metallisation was changed to Ni/Au (200Å/3000Å) for better adhesion. The gate dimension was 1.8 µm x 150 µm. Because the main interest at this stage was the subthreshold behavior, the new ohmic scheme was not used.

The characterization was conducted in atmospheric ambient on a QuieTemp S-1060 high temperature stage by SIGNATONE. The drain output I-V characteristics at various temperatures are shown in Fig.3.3-1. At room temperature the device exhibits a saturation current of 58 mA/mm with a maximum transconductance (g_m) of 33 mS/mm. The relatively low current level is attributed to compensation of donors by deep acceptor traps in the I-GaN buffer. The absence of current reduction at high temperatures can be explained by ionization of deeper donors. The none-linear behavior before current saturation is an indication of poor ohmic contact resistance. With these problems yet to be solved, the device shows good pinch-off at all temperatures investigated. This is a distinctive improvement over the previous devices as shown on Fig.3.1-7 and Fig.3.2-4.

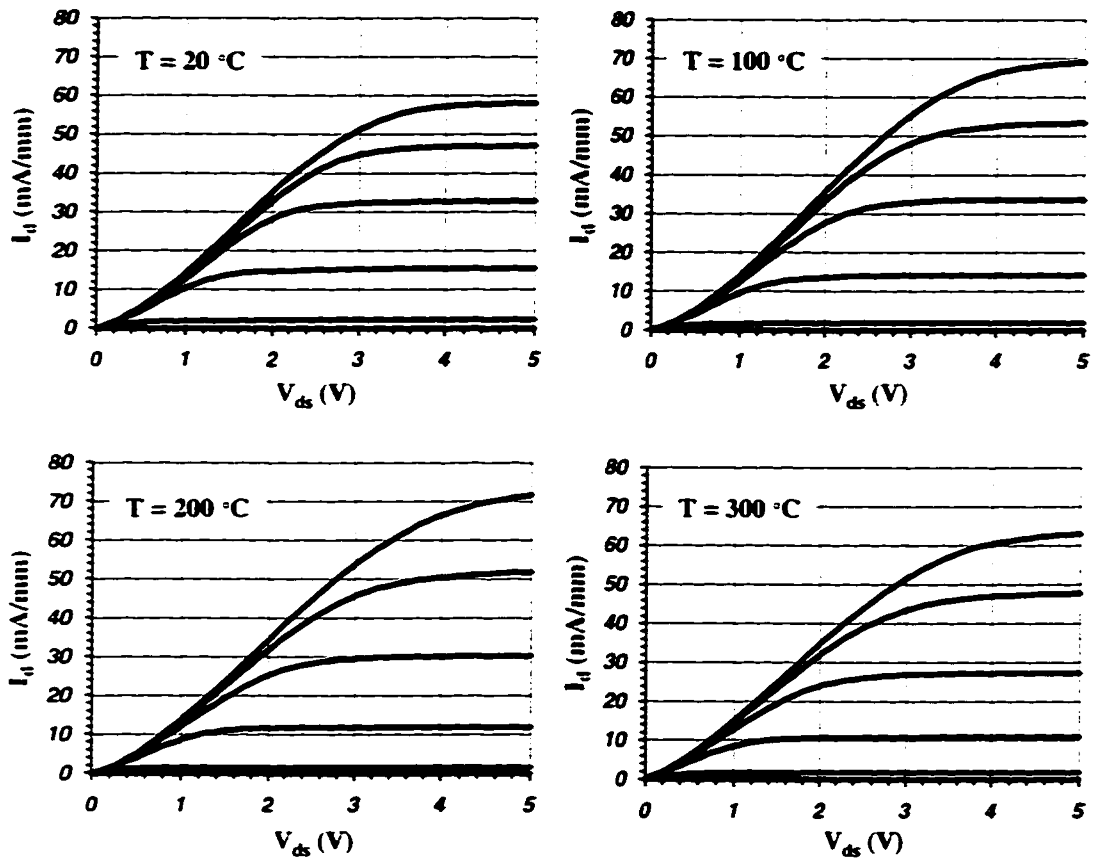


Fig.3.3-1 *Output IV characteristics at various temperatures for an AlGaN/GaN HEMT on I-GaN buffer grown under low pressure (*V_{gs}*, start: +1.0 V, step: -.5 V).*

The gate-control characteristics and the measured subthreshold swing at various temperatures are shown in Fig. 3.3-2 and Fig. 3.3-3. It is seen that the off-state current at room temperature and 300 °C are 6 and 4 orders less than the saturation current. A low SW of 72 mV/decade is achieved at room temperature, which is among the best reported in literature. The corresponding ideality factor η is 1.2. As temperature increases, η also increases. Nonetheless, an η of 2.2 is maintained at 300 °C, the same value as that of a typical GaAs MESFET at room temperature as mentioned earlier.

The above experimental result indicates that, the LP I-GaN is potentially an excellent buffer for AlGaN/GaN HEMTs up to at least 300 °C.

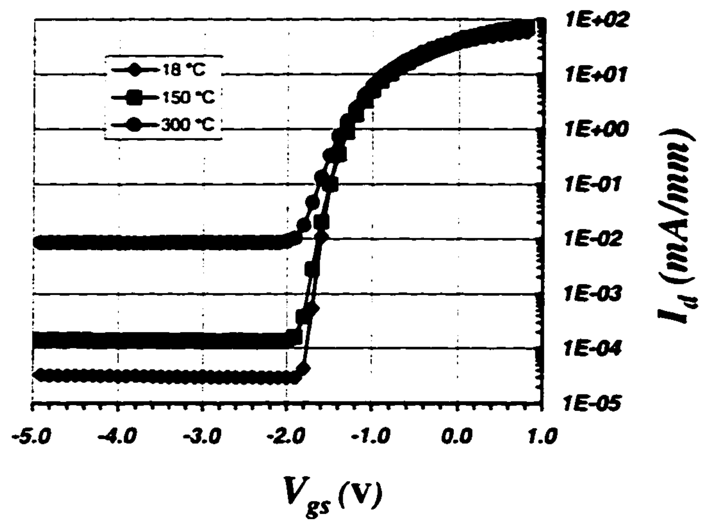


Fig.3.3-2 *Gate-control characteristics at various temperatures (V_{ds} = 5 V).*

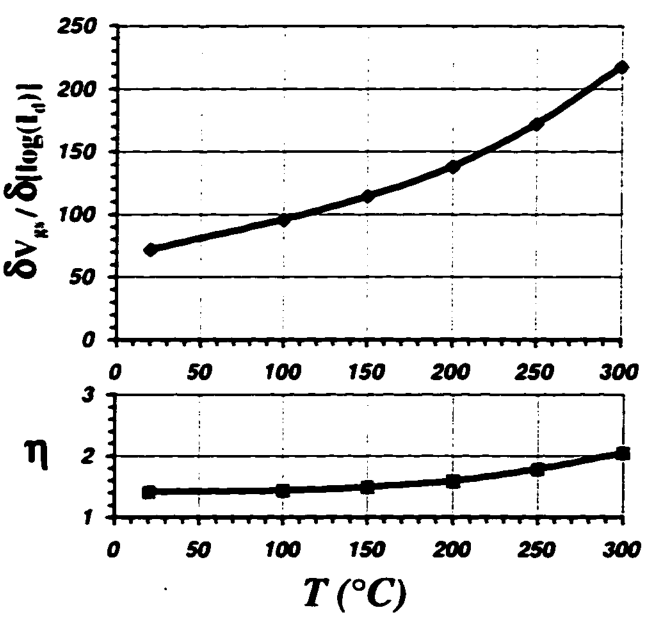


Fig.3.3-3 *Subthreshold swing and its ideality factor vs. temperature.*

3.4 AlGaN/GaN HEMTs on Bi-layer I-GaN buffer

Subsequent investigation showed that growing a GaN layer under atmospheric pressure (AP) on top of the LP I-GaN reduced the yellow band luminescence (indicating a lower deep-level density) yet maintained the insulating nature. Although it is believed to be related to the growth initiation, the exact mechanism for the high resistivity of the top AP GaN is under investigation and not yet known. Nonetheless, this bi-layer I-GaN was eventually accepted as a more desired buffer layer for a high quality AlGaN/GaN HEMT. With it, a high current level, high gate-drain breakdown voltages, excellent pinch-off and a low RF output conductance were simultaneously achieved as presented below.

3.4.1 *Device fabrication*

The growth of the HEMT structure started with a 200 Å GaN nucleation layer, which was followed by 1 μm LP I-GaN and 1 μm AP I-GaN as the device buffer layer. The $Al_{0.15}Ga_{0.85}N$ barrier/donor layer was 400 Å total, where the doped region was 220 Å (Si doped to $3x10^{18}$ cm^{-3}) located above the undoped spacer of 30 Å. The use of the thicker $Al_{0.15}Ga_{0.85}N$ layer was to maximize channel charge without potentially degrading the gate characteristics. Measured Hall mobility and carrier density were 1110 cm^2/Vs and $6.5x10^{12}$ cm^{-2}. The wafer batch number is 960906GB which was grown by Dr. Stacia Keller.

Source-drain ohmic contacts were obtained with Ti/Al/Ni/Au (250 Å / 2000 Å / 400 Å / 450 Å) annealed at 900 °C for 30 s (similar to [x]). Transfer contact resistance was measured to be 0.5 ~ 0.7 Ω-mm, close to what was obtained with the contact scheme by n^+-regrowth. The gate metalisation was Ni/Au (100 Å / 3000 Å). The gate-length was 1 ~ 1.2 μm and the gate-drain separation ranged from 1 to 3 μm.

3.4.2 *DC and small-signal RF performances*

Fig. 3.4-1 shows the output IV characteristics of a typical device with a source-drain spacing, gate-drain spacing and gate width of 3 μm, 1 μm and 75 μm, respectively.

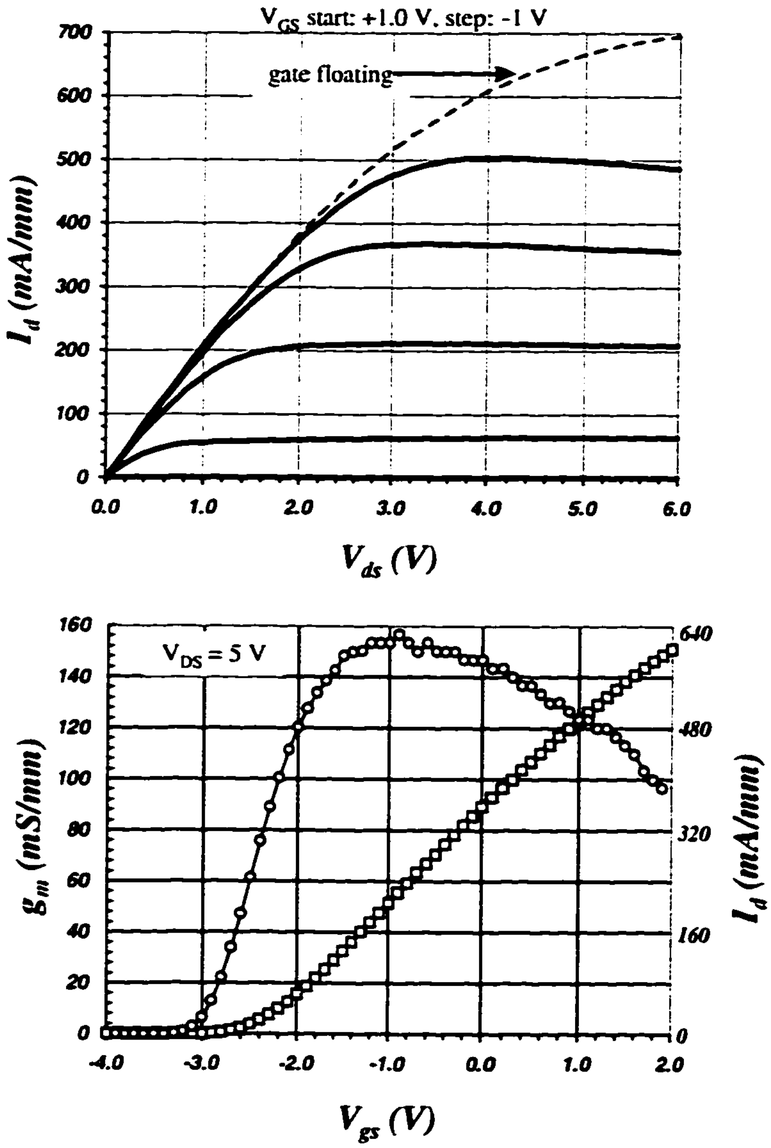


Fig.3.4-1 *Output IV characteristics of an AlGaN/GaN HEMT on a bi-layer I-GaN buffer (L_g = 1.1 μm, L_{ds} = 3 μm, w = 75 μm).*

As seen in the graphs, the drain saturation current is greater than 500 mA/mm while the floating-gate channel current is 700 mA/mm. Transconductance (g_m) is again quite uniform with a peak value of 160 mS/mm at I_d ~ 200 mA/mm and V_{ds} ~ 3 V. With the measured source resistance of 2.1 Ω-mm, the intrinsic transconductance is calculated to be 240 mS/mm. The on-resistances is 4.6 Ω-mm comparable to previous devices with n^+ regrown contacts. The HEMT also exhibits hard pinch-off and a high breakdown voltage of 100 V. Devices with 2 and 3 μm gate-drain spacing demonstrated higher breakdown values of ~ 160 V and ~ 220 V respectively.

Microwave performance as represented by extrinsic f_t and f_{max} was investigated as a function of bias. DC power dissipation was kept below 3 W/mm to minimize self-heating caused by the poor thermal conductivity of the sapphire substrate.

First, the source-drain bias voltage was fixed at 5 V and f_t and f_{max} were measured at various values of drain current. Fig.3.4-2 is the result for a device with source-drain spacing of 3 μm and gate width of 150 μm. The peak f_t of 9.6 GHz is found at a drain current of 200 mA/mm where the maximum g_m is located. It is seen that, for drain current > 130 mA/mm, f_t follows the same trend as the transconductance, similar to a conventional HEMT [xi]. As drain current decreases below 130 mA/mm, f_t also decreases but at a slower rate than the g_m reduction. f_{max}, on the other hand, exhibits a peak at a moderately low drain current of ~ 100 mA/mm. At this point, f_t is still high while the voltage drops across the source and drain series resistances are small, so that most of the source-drain voltage is across the active channel region, resulting in smaller output conductance and gate-drain capacitance.

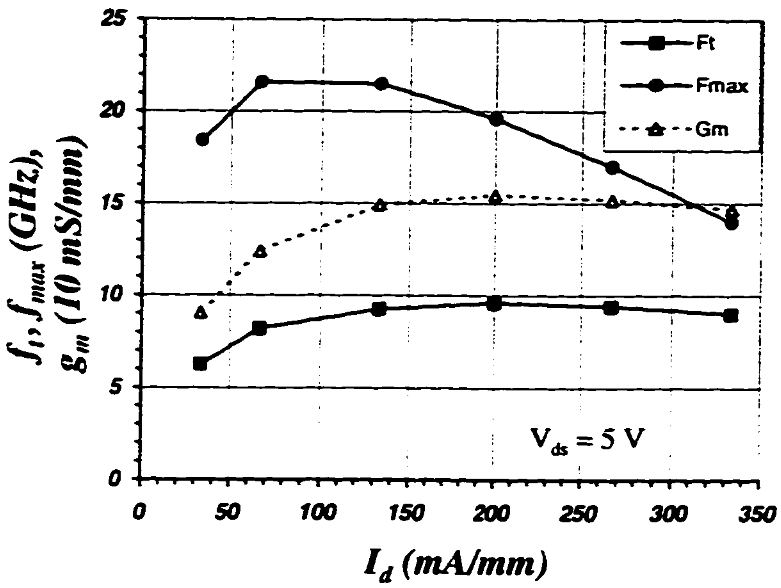


Fig.3.4-2 *Cut-off frequencies vs. drain current at a fixed source-drain voltage of 5 V (L_g = 1.1 μm, L_{ds} = 3 μm, w = 2x75 μm).*

Next, f_t and f_{max} were examined as a function of drain bias voltage while the drain current was fixed at 100 mA/mm and 200 mA/mm respectively as shown in Fig.3.4-3a. It is interesting to notice that the f_t of the AlGaN/GaN HEMT does not degrade with increasing bias voltage for each fixed drain current except a slight reduction at V_{ds} = 30 V, where self-heating may take effect as the DC power consumption reaches 3 W/mm. Although reported GaAs MESFETs [xii] with similar gate-length showed a much higher peak f_t of 18.5 GHz at a low drain bias of 2 V, the f_t dropped to below 8 GHz at 10 V. The f_t of 8 GHz at the drain bias of 30 V for the present AlGaN/GaN device clearly indicates a much higher microwave power ability over its GaAs counterpart. Unlike f_t, f_{max} shows a considerable drain-bias dependence with the maximum value of 27.2 GHz located at I_d = 100 mA/mm and V_{ds} = 20 V, as an optimization of high f_t, small output conductance and negligible self-heating effect. The output conductance extracted from S parameters was 3.3 mS/mm at the peak f_{max}, a factor of 3 ~ 4 improvement over previous

HEMTs without a buffer layer. The high f_{max} is attributed to this reduced output conductance owing to the high quality buffer.

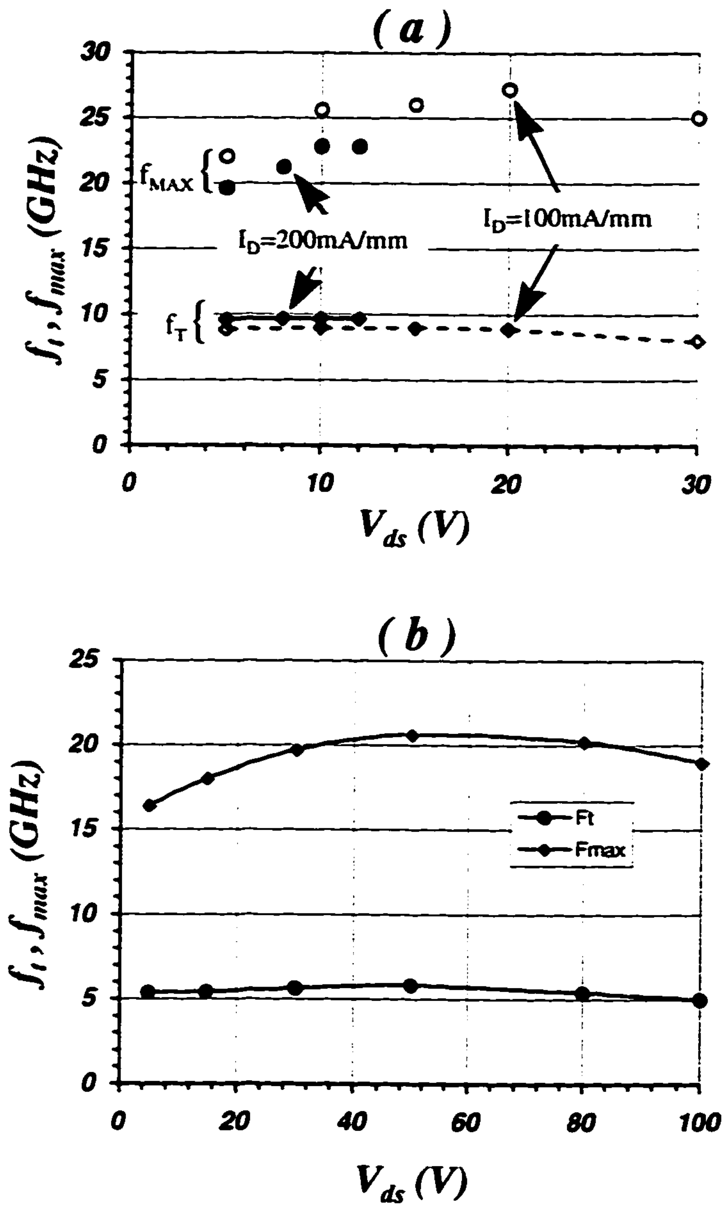


Fig.3.4-3 *Cut-off frequencies vs. drain bias voltage in the case of: (a) fixed drain current of 100 and 200 mA/mm for the same device as in Fig.3.4-2; (b) fixed drain current of 33 mA/mm for a device with gate-drain spacing of 3 μm (L_g = 1.1 μm, L_{ds} = 5 μm, w = 2x75 μm).*

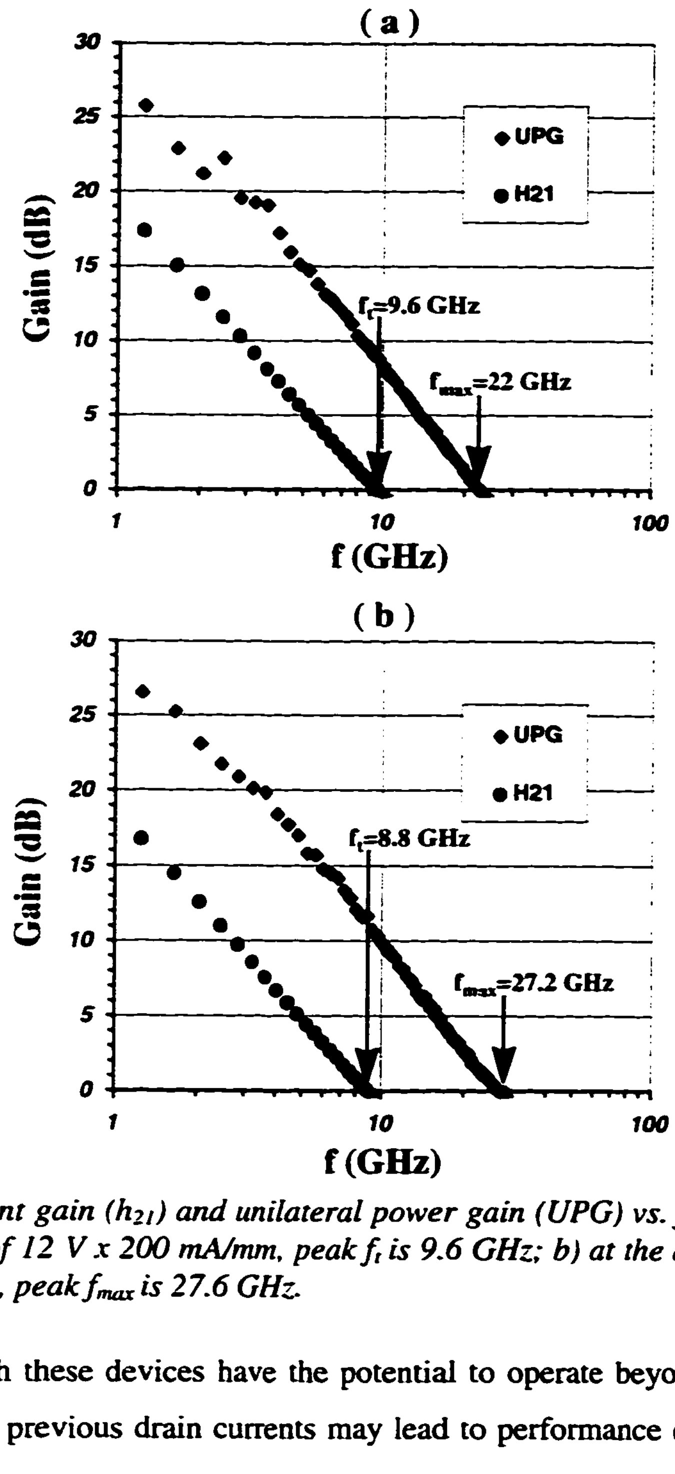


Fig.3.4-4 *Current gain (h_{21}) and unilateral power gain (UPG) vs. frequency. a) at the drain bias of 12 V x 200 mA/mm, peak f_t is 9.6 GHz; b) at the drain bias of 20 V x 100 mA/mm, peak f_{max} is 27.6 GHz.*

Although these devices have the potential to operate beyond 100 V, high bias voltages at previous drain currents may lead to performance degradation due to self-heating. As a compromise, a low drain current of 33 mA/mm was used for investigation of microwave performance with source-drain voltages ranging from 5 V to 100 V. The result for a device with gate-drain spacing of 3 μm is shown in Fig.4.3-3b. Note that such a low current density leads to substantial reduction in extrinsic cut-off frequencies due to an increased channel resistance and a lower active input capacitance. Nonetheless, the device demonstrates f_t and f_{max} of 5.4 and 16.4 GHz respectively at 5 V. As bias voltage increases, f_t exhibits a slight increase, reaching a peak of 5.9 GHz at 50 V. The transistor channel can be divided into a field-dependent-velocity region, or gradual channel region, and a saturated-velocity region. As bias voltage increases, the gradual channel region reduces, leading to an increase in the overall electron velocity and a shorter intrinsic channel transit time. However, the drain delay increases as a result of depletion region extension. The slight improvement of f_t at higher bias voltage up to 50 V may be an overall effect of the two transit times, suggesting that the reduction in the channel transit time over-compensates the increase in drain delay. Cut-off frequencies begin to reduce at 80 V, where the DC power dissipation reaches 2.4 W/mm and self-heating effect may set in. At 100 V, the device is still able to maintain reasonably high f_t and f_{max} of 5 and 19 GHz respectively. If properly cooled, larger drain current will yield much better performances at the same high bias voltage and will enable a more detailed analysis of the devices.

3.4.3 *Power performance*

The microwave power was characterized on-wafer using the Maury Microwave Automated Tuner System. The output power at the fundamental and harmonic frequencies was monitored using the Hewlett-Packard 8566B spectrum analyzer. The input match was selected to maximize the delivered power, and the output match was selected to optimize the output power.

Fig.3.4-5 shows the power performance of a device with two gate fingers of 75 μm each (total gate width = 150 μm). The device was biased at a drain current and voltage of 205 mA/mm and 28 V. The source and load reflection coefficients were $\Gamma_{source} = 0.448e^{j51.04^\circ}$ and $\Gamma_{load} = 0.785e^{j5.20^\circ}$ as optimized by source and load pulling. As seen in the graph, the device demonstrates a small-signal power gain of 12.5 dB. At an input level of 18 dBm, output power saturates at 23.73 dBm, corresponding to an output power density of 1570 mW/mm. The large signal gain, power added efficiency (PAE) and drain efficiency are 5.7 dB, 20.2 % and 27 % respectively. Second and third harmonics at the output were monitored to be 30 ~ 40 dB and 20 ~ 30 dB below the main signal.

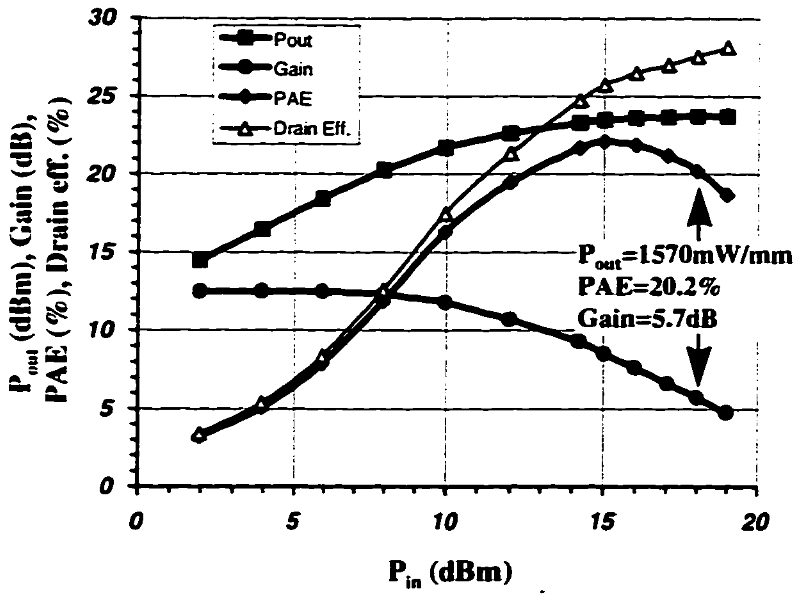


Fig.3.4-5 *Microwave power performance of the AlGaN/GaN HEMTs at 4 GHz. Device dimension: 1.1 μm x 150 μm; DC bias:* I_d *= 205 mA/mm,* V_{ds} *= 28 V; input & output matching:* $\Gamma_{source} = 0.448e^{j51.04^\circ}$, $\Gamma_{load} = 0.785e^{j5.20^\circ}$*; small signal gain: 12.5 dB; saturated output power density: 1570 mW/mm; PAE: 20.2 %; drain efficiency: 27 %; large signal gain: 5.7 dB.*

This power density of 1570 mW/mm, while being equal to what was measured at 1.1 GHz for a GaAs metal-insulator-semiconductor FET (MISFET) with a low-temperature-grown epitaxial layer as the insulator [xiii], has exceeded the highest value ever reported for GaAs based FETs above S band (> 2 GHz) [xiv]. Compared with our first AlGaN/GaN HEMT, the improved device showed significant increase in power density at twice the operating frequency.

3.5 Summary

The device development started with AlGaN/GaN HEMTs with UID n-GaN channels without an insulating buffer. These first prototype devices of us demonstrated a reasonably current density of ~ 330 mA/mm and very high breakdown voltages of 220 ~ 340 V (with 3 μm gate-drain spacing) as expected for a wide-band-gap FET. The poor ohmic contact resistance was then reduced to 0.44 Ω-mm through n^+-regrown source-drain regions; while the soft pinch-off characteristics was improved by inclusion of a LP I-GaN buffer. Finally, the charge loss due to deep traps in the LP I-GaN was overcome by addition of a AP grown I-GaN layer (later investigation showed that the thickness of the LP GaN could be reduced to 1000 Å while keeping the AP GaN on top insulating). With the simplified new ohmic scheme in literature [ix], fabricated 1 μm gatelength AlGaN/GaN HEMTs on the bi-layer I-GaN buffer showed excellent characteristics in all major aspects: high current levels over 500 mA/mm, large transconductances of 160 mS/mm, hard pinch-off and high break down voltages up to 220 V. Devices exhibited fairly uniform f_t in a wide range of drain bias voltage. At biases higher than 10 V, the f_t of the AlGaN/GaN HEMTs exceeded that reported for GaAs MESFETs with the same gate-length, in agreement with the greater high-field electron velocity predicted for GaN [xv]. Even at 100 V, the device maintained f_t & f_{max} of 5 & 19 GHz, which were the first performance demonstration at such a high bias voltage for a microwave FET. These excellent device characteristics translated into an un-cooled power density of 1.57 W/mm at 4 GHz, exceeding the best value reported for GaAs MESFETs. These experimental results indicate the establishment of a comprehensive technology for high quality GaN-channel HEMTs.

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Chapter 4
High Performance AlGaN/GaN HEMTs

In this chapter, effort is focused on device optimization for a new level of performance. In **4.1**, first order analyses are used to illustrate the design directions for high performances. **4.2** presents the DC, small-signal RF and microwave power performances of such devices by optical lithography. In **4.3**, the potential to operate at higher frequencies is investigated with submicron gatelength devices by electron-beam lithography. The device operation mode is also analyzed with the conventional gatelength-variation method. Finally, the feasible finger-width for future multi-finger submicron-gatelength devices is calculated and experimentally examined.

4.1 Design philosophies of high performance AlGaN/GaN HEMTs

***Philosophy #1**: Scale up the figures of merit for power performance*

As mentioned in Chapter 1, the ultimate power-frequency ability of a semiconductor device depends on Johnson's figure of merit: [i]

$$Pf \sim JFOM = \left(\frac{\boldsymbol{E_c} v_s}{2\pi}\right)^2 \qquad \text{Eq.4.1-1}$$

where Pf is the power-frequency product per unit width, $\boldsymbol{E_c}$ is the critical electric field for breakdown and v_s is the electron saturation velocity.

Baliga [ii] also proposed a figure of merit governing the power loss at high frequencies which can be understood as an efficiency figure-of-merit at high frequencies:

$$BHFFOM \sim \mu \boldsymbol{E_c}^2 \qquad \text{Eq.4.1-2}$$

where μ is mobility.

For an AlGaN/GaN HEMT, since the GaN-channel is not doped, the maximum electric field is in the AlGaN layer. A higher Al mole-fraction results in a higher bandgap of the AlGaN, and hence a higher composite breakdown field than that of the already wide band-gap GaN. Also, the resultant larger conduction-band discontinuity (ΔE_c) improves carrier confinement, allowing a high mobility to coexist with a large carrier density. The saturation velocity v_s, relating to the carrier in the GaN channel, remains high with little dependence on the AlGaN layer. These arguments predict higher equivalent figures of merit for AlGaN/GaN HEMTs with higher Al-contents.

***Philosophy #2:** Maximize $n\mu$ product for maximum f_t*

An FET with high mobility, such as a GaAs MESFET, operates nearly in the velocity saturation mode when the gate-length is less than 1 μm. The current-gain cutoff frequency in this mode is

$$f_t = v_s/(2\pi L_g) \quad \text{[iii]} \qquad \text{Eq.4.1-3}$$

where L_g is the gate-length.

A GaN-channel HEMT has a mobility 3 – 5 times smaller and a significant part of the channel may operate in the gradual channel mode. In this mode, the electron velocity is prepositional to the channel electric field, or the voltage across the channel for a specified gatelength. When the source-drain voltage V_{ds} increases from zero, the voltage across the channel increases linearly until the drain side of the channel is pinched off, or, the channel current is saturated. After that, drain extension begins and most of V_{ds} above the knee voltage (i.e. the voltage at current saturation) is dropped in this drain depletion region, leading to little increase in voltage across the intrinsic channel. The onset of the current saturation can be understood as the onset of the voltage saturation across the channel. The maximum value of this saturation voltage V_{dss} is approximately equal to the total active gate swing $V_{GSw} = V_{gm} + V_T$ as seen in Fig.4.1-1, where V_{gm} is the maximum gate-bias before the onset of a parallel conduction in the AlGaN layer (or transconductance compression) and V_T is the threshold voltage (or pinch-off voltage).

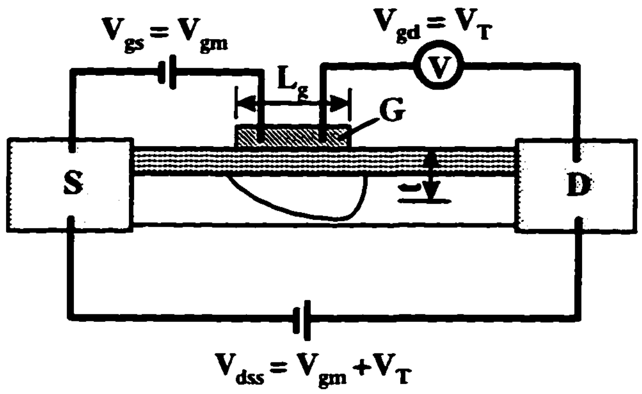


Fig.4.1-1 *Schematics of an FET in gradual channel mode, showing that with the optimum gate bias* $V_{gs} = V_{gm}$, *the saturated voltage across the intrinsic channel is* $V_{dss} = V_{gm} + V_T = V_{GSw}$. *When* $V_{ds} > V_{dss}$, *most extra-voltage will drop in the drain extension region.*

Approximately, the gate-swing:

$$V_{GSw} \sim \text{charge/capacitance} = \boldsymbol{n_s}q/(\varepsilon/t) = \boldsymbol{n_s}tq/\varepsilon \qquad \text{Eq. 4.1-4}$$

where $\boldsymbol{n_s}$ is the sheet charge density in the channel, t is the gate-channel separation, ε is the dielectric constant, q is the unit charge of an electron.

With this, the effective electron velocity can be written as

$$v = \mu\boldsymbol{E} = \mu(V_{GS}/L_g) \sim \mu\boldsymbol{n_s}tq/(\varepsilon L_g) \qquad \text{Eq.4.1-5}$$

where μ is the electron mobility, $\boldsymbol{E}$ is the electric field in the channel and L_g is the gate-length.

Finally the current gain cutoff frequency is found as

$$f_t = v/2\pi L_g \sim \boldsymbol{n_s}\mu t q/(2\pi\varepsilon L_g^{\,2})$$

$$= \boldsymbol{n_s}\mu q/(2\pi\varepsilon A L_g) \qquad \text{Eq.4.1-6}$$

where A is the aspect ratio ($A = L_g/t$).

Now it is seen that to maximize f_t means to maximize the $n\mu$ product for a specified gate-length. However, it is necessary to note that, this relation is based on a pure gradual channel mode. For a practical FET, depending on how significant the gradual channel part is, the improvement of f_t with increasing $n\mu$ product can be different.

By Eq.4.1-6, increasing gate-channel separation t (or using a smaller aspect ratio A) can also increase f_t, but the effective gate-length increases by approximately $2t$ as well (due to the fringing effect), leading to an actual dependence of $f_t \sim t(L_g+ 2t)^{-2}$. The improvement in f_t is discounted. Moreover, reducing A also reduces the output conductance and results in a relatively lower f_{max} [iii]. Increasing $n\mu$ product, however, not only stays away from such disadvantages, but also introduces another benefit: reduced parasitic access resistances, therefore further enhancing extrinsic cut-off frequencies.

Philosophy #3: *Follow the lever rule for maximum charge density*

Since the room temperature mobility is generally insensitive to the 2DEG density, the optimization of f_t directly calls for a maximum 2DEG charge density. Regardless of the doping density in the donor layer, there is a maximum available 2DEG density for a specific HEMT structure before the onset of a significant parallel conduction in the AlGaN layer. To simplify the analysis, a donor sheet is used to represent the finite doped region. The location of this donor sheet can be understood as a weighted center of the doped region.

I) Without piezo-electric charge

In this case, the band diagram before a significant parallel conduction in the AlGaN layer is shown in Fig.4.1-2 with symbols specified.

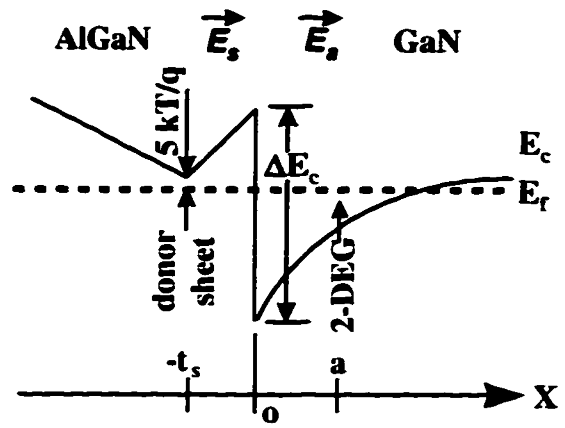


Fig.4.1-2 *Band-diagram of an AlGaN/GaN HEMT structure assuming no piezo-electric charge.* (E_c: *conduction band edge,* E_f: *Fermi-level,* t_s: *spacer thickness,* ***a****: distance between the 2DEG centroid and the AlGaN/GaN interface,* $\boldsymbol{E_s}$: *electric field in the spacer,* $\boldsymbol{E_a}$: *electric field in delta quantum well, :* ΔE_c *conduction band discontinuity,* k: *Boltzmann constant,* T: *temperature in* K, x: *position axis with the origin at the hetero-interface)*

At the onset of the parallel conduction in the AlGaN layer, the conduction band edge of the donor region is about 4 ~ 5 kT/q (in eV) above the Fermi-level (5 kT/q is chosen for the calculation). At equilibrium, the electrostatic potential from $x = -t_s$ to $x = a$ can be written as

$$5kT/q + t_s\boldsymbol{E_s} - \Delta E_c + a\boldsymbol{E_a} = 0 \qquad \text{Eq.4.1-7}$$

The relation between the two electric fields is:

$$\varepsilon_{AlGaN}\boldsymbol{E_s} = \varepsilon_{GaN}\boldsymbol{E_a} \qquad \text{Eq.4.1-8}$$

where ε_{AlGaN} and ε_{AlGaN} are the dielectric constants of the AlGaN and GaN.

With Eq.4.1-7 and Eq.4.1-8, the electric field in the delta well can be solved as

$$\boldsymbol{E_a} = \frac{\Delta E_c - 5kT/q}{\frac{\varepsilon_{AlGaN}}{\varepsilon_{GaN}} t_s + a} \qquad \text{Eq.4.1-9}$$

The 2DEG charge density directly relates to this electric field by

$$\boldsymbol{n_{s,I}} = \frac{\varepsilon_{GaN}}{q}\boldsymbol{E_a} = \frac{\varepsilon_{GaN}(\Delta E_c - 5kT/q)}{q(\frac{\varepsilon_{AlGaN}}{\varepsilon_{GaN}} t_s + a)} \qquad \text{Eq.4.1-10}$$

This is the simple lever rule determining the maximum 2DEG charge density available in an AlGaN/GaN HEMT assuming no piezo-electric charge. If most electrons are in the first sub-band of the delta well, the position of the 2DEG centroid $\boldsymbol{a}$ is in the same order as the classical turning point L which is a function of $\boldsymbol{E_a}$ [iv],

$$\boldsymbol{a} \sim L = (h/2)^{2/3}/(2m^* q\boldsymbol{E_a})^{1/3} \qquad \text{Eq.4.1-11}$$

where h is the Plank's constant, m^* is the effective mass of electrons.

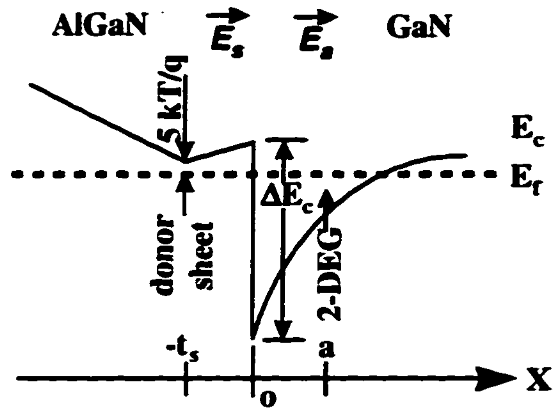
Using Eq.4.1-9, we have

$$\boldsymbol{a} \sim \varepsilon_{GaN}(h/2)^{2/3}/(2m^* q^4 \boldsymbol{n_s})^{1/3} \qquad \text{Eq.4.1-12}$$

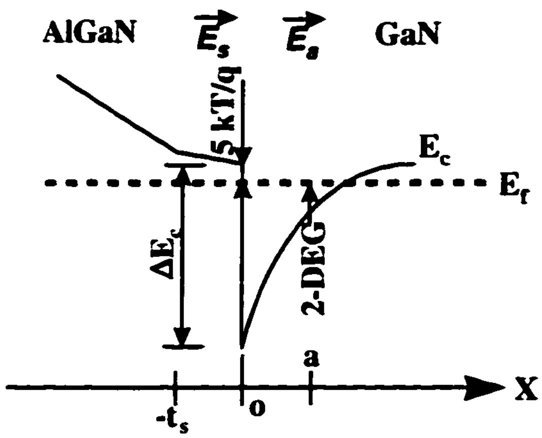
For $\boldsymbol{n_s} = 1\text{x}10^{13}\ \text{cm}^{-2}$, $\boldsymbol{a} \sim 22$ Å.

II) With piezo-electric interface charge

Depending on the strength of the piezo-electric effect, there are two possible band-diagrams as shown in Fig.4.1-3a and b.



a) case ***IIa***



b) case ***IIb***

Fig.4.1-3 *Band-diagrams of an AlGaN/GaN HEMT structure assuming a) moderate piezo-electric charge, b) strong piezo-electric charge.*

In case IIa, Eq.4.1-7 is still valid while Eq.4.1-8 needs to be modified to

$$\varepsilon_{AlGaN}\boldsymbol{E_s} + n_{pz}\mathbf{q} = \varepsilon_{GaN}\boldsymbol{E_a} \qquad \text{Eq.4.1-13}$$

where n_{pz} is the piezo-electric charge density.

Solving for n_s yields the lever rule for case ***IIa***,

$$n_{s,IIa} = \frac{\varepsilon_{GaN}(\Delta E_c + \frac{n_{pz}e}{\varepsilon_{GaN}} t_s - 5kT/q)}{q(\frac{\varepsilon_{AlGaN}}{\varepsilon_{GaN}} t_s + a)} \qquad \text{Eq.4.1-14}$$

Similarly, it can be derived that ***in case IIb***, the maximum 2DEG charge density is

$$n_{s,IIb} = \frac{\varepsilon_{GaN}(\Delta E_c - 5kT/q)}{aq} \qquad \text{Eg.4.1-15}$$

As expected before deriving the lever rules, a most straight-forward way of increasing charge density is to increase ΔE_c. With the lever rules, a more detailed dependence of n_s on ΔE_c can be perceived. By Eq.4.1-12, the interface-to-2DEG distance goes as $a \sim n_s^{1/3}$, therefore the function $n_s(\Delta E_c)$ is close to linear but slightly sub-linear.

In the absence of the piezo-electric charge (Fig.4.1-2 and Eq4.1-10), for a specified ΔE_c, the effective way to increase the 2DEG charge density is to reduce the spacer thickness t_s. This potentially decreases the channel mobility. In the extreme case of $t_s = 0$, the charge density is theoretically maximized, but structure quality of the hetero-interface may suffer from serious degradation. With the natural interface piezo-electric charge as in the case ***IIa*** (Fig.4.1-3a and Eq4.1-14), however, the interface integrity is preserved while the lever is favorably off-balanced to a more effective use of the ΔE_c. In the case of ultra-high piezo-electric charge density as in case ***IIb*** (Fig.4.1-3b and Eq4.1-15), the whole ΔE_c can be used with any reasonable t_s. But such a band-diagram has not been observed in Band-prof using the piezo-electric charge densities reported in literature.

4.2 Al-rich AlGaN/GaN HEMTs

Reviewing of the above design philosophies by first-order analyses, we see no contradiction between each design direction. Instead, all of them concertedly point to the same direction: a high Al mole-fraction.

Theoretically the increased interface piezo-electric charge with increasing Al-content does not constitute ionic scattering because of its periodicity with spacing of one lattice constant. However, the relatively high interface roughness in practical epi-films may couple with this high interface charge density and result in an enhanced interface-roughness scattering. The potentially un-even distribution of the Al atoms may also lead to an enhanced remote scattering.

Experimental investigation of mobility versus Al mole-fraction was once performed by Khan et al., who found that 13 % Al-content yielded the highest peak mobility [v]. For mole-fractions of 20 ~ 25 %, the peak mobility subjected to a degradation by a factor of 3.

To realize the full potential of Al-rich AlGaN/GaN HEMTs, a close attention needs to be paid to this mobility degradation.

4.2.1 *Experimental carrier density and mobility of Al-rich AlGaN/GaN HEMT structures*

According to the lever rules (Eq.4.1-10 and Eq.4.1-14), reducing spacer thickness t_s increases the available 2DEG charge density in cases without and with moderate piezo-electric interface charge. However, since the growth technique for the AlGaN/GaN HEMT structure was not mature yet, a coherent epi-film was difficult to achieve with a very small t_s. Also, a different Al-mole-fraction may result in a different optimum t_s, which adds complexity to the experiment. For these reasons, a conservative structure shown in Fig.4.2-1 were used for all Al-rich AlGaN/GaN HEMTs under investigation.

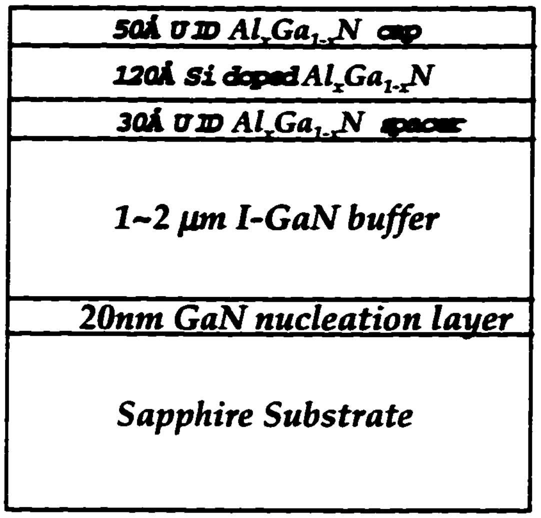


Fig.4.2-1 *The epi-structure used for experimental investigation of Al-rich AlGaN/GaN HEMTs*

Al mole-fractions chosen were 15%, 25%, 35% and 50%. For a given Al mole-fraction, Si input was increased with the intention to observe the saturation in 2DEG density. Fig.4.2-2 shows the highest sheet charge densities experimentally achieved as a function of Al mole-fraction. Each sheet charge was confirmed not to freeze-out at 20 K by the Hall-effect measurement. Also shown are the calculated saturated 2DEG densities assuming both the conduction-band discontinuity and the piezo-electric charge density linearly depend on Al mole-fraction: $\Delta E_c = 0.8X_{Al}(E_{g,AlN}-E_{g,GaN})$ and $Q_{pz} = Q_{AlN/GaN}X_{Al}$. Other parameters used are listed in Table 4.2-1. It is seen that for low Al-contents, the experimental charge densities are higher than calculated, which is attributed to the inaccuracy of the assumed parameters. However, the increase in experimental charge density with increasing Al mole-fraction is less than the calculation. This may be due to the reduced doping efficiency by Si with increasing Al-content which is related to the growth technique. Nonetheless, sheet charge densities of 1.2 ~ $1.3\text{x}10^{13}$ cm^{-2} has been achieved with Al mole-fractions of 35% ~ 50%, nearly a factor of 2 higher than the 7.8×10^{12} cm^{-2} value with 15% Al-content.

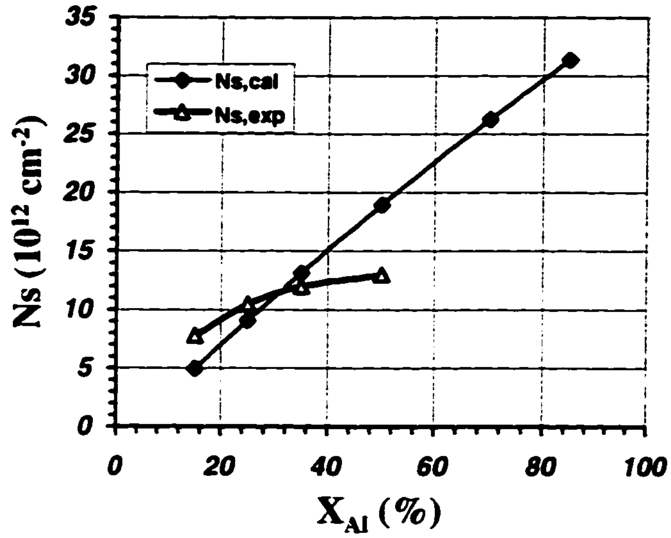


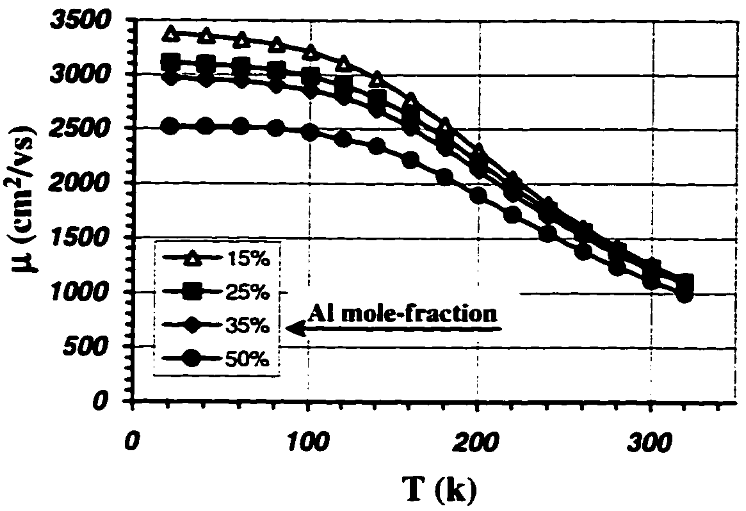
Fig.4.2-2 *Calculated and experimental charge densities in the HEMT channel vs. Al mole-fraction.* $N_{s,cal}$: *calculated 2DEG density;* $N_{s,exp}$: *experimentally achieved sheet density at 20 K.*

Table 4.2-1 Parameters for calculation of charge densities by Bandprof.

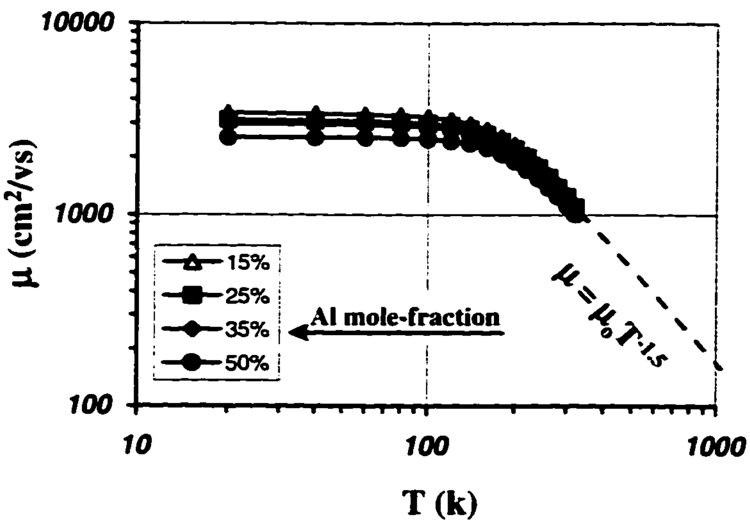
Parameter	Symbol	Value	Reference
Temperature	T	300 K	
Effec. electron mass for GaN	m*	0.2 m_e	iii
Effec. electron mass for AlN	m*	0.48 m_e	—
Dielectric constant for GaN	ε_{GaN}	10.4 ε_0	vi
Dielectric constant for AlN	ε_{AlN}	9.0 ε_0	vi
Band gap for GaN	$E_{g,GaN}$	3.4 eV	vi
Band gap for AlN	$E_{g,AlN}$	6.2 eV	vi
Conduction band offset	η_{Ec}	80 %	vii
Piezo-electric charge density for AlN on GaN	$Q_{pz,AlN}$	2.5×10^{13} cm^{-2}	viii & ix

Donor ionization energy (GaN)	$E_{d,GaN}$	25 meV	x
Donor ionization energy(AlGaN)	$E_{d,AlGaN}$	100 meV	---
Metal-AlGaN barrier height	Φ_b	1.2 eV	---

Unlike what was observed by Khan [v], the mobilities of the Al-rich AlGaN/GaN structures do not subject to serious degradation as seen in Fig.4.2-3. The low temperature (20 K) mobility for the Al mole-fraction X_{Al} of 15% is 3400 cm^{-2}/Vs. It does reduces with increasing X_{Al} but in a mild manner down to 2500 cm^{-2}/Vs for the $Al_{0.5}Ga_{0.5}N/GaN$ structure. The 300 K mobilities, however, are nearly the same indicating that phonon scattering is dominant. When plotted in a log scale, each mobility shows a temperature dependence of ~ $T^{-3/2}$ above 200 K, which is a typical phone-scattering term. For normal FETs operating above 300 K, a high Al-content up to 50% should not affect access resistances if the ohmic contact is not a problem. The much higher mobilities of the Al-rich HEMT structures than what obtained by Khan [v] are attributed the more advanced growth technique today than what was available years ago. For each structure tested here, the charge density remained constant though-out the temperature range with less than 2% variation which is within the accuracy of the Hall-effect measurement system.



(a) In linear scale



(b) In log scale

Fig. 4.2-3 *Measured mobilities vs. temperature for AlGaN/GaN HEMT structures with Al mole-fractions of 15%, 25%, 35% and 50%.*

4.2.2 *Device fabrication*

Devices were fabricated on three epi-films with Al mole-fractions of 25%, 35% and 50%. All wafers were grown by Dr. Bernd Keller. Hall-effect measurements were performed on the leading edge of the wafer. The results are listed below: film-1, batch # 970110FE, $X_{Al} = 25\%$, $n_s = 1.0\times10^{13}$ cm^{-2}, $\mu = 1230$ cm^2/Vs; film-2, batch # 970127FD, $X_{Al} = 35\%$, $n_s = 1.2\times10^{13}$ cm^{-2}, $\mu = 1250$ cm^2/Vs; film-3, batch # 970208FD, $X_{Al} = 50\%$, $n_s = 1.2\times10^{13}$ cm^{-2}, $\mu = 1100$ cm^2/Vs. Note that the these parameters might deviate from the regions on which devices were fabricated. The fabrication process was similar to what was described in chapter 3. The mask-set used, however, was a newer design with much smaller probing pads to reduce parasitic capacitances for submicron devices presented later. The gate-widths were 50, 76, 100, 300 and 500 μm. The gate-source spacing was 1 μm while the gate-drain separations were kept as 1, 2 and 3 μm. The gate-length on the mask was 1 μm for the devices with Al mole-fractions of 25 and 35%, but lithography effort resulted in actual gate-lengths of 0.85 ~ 1 μm. For devices with a 50% Al-content, the gate-length on the mask was reduced to 0.7 μm to push the limit of the conventional optical lithography in the Co-search clean room. The gate-length came out to be 0.7 ~ 0.75 μm with a yield about 85 %.

An important concern for fabricating high quality Al-rich devices is the ohmic contact resistances, since with increasing Al-content, the AlGaN layer is expected more resistive and may also be more difficult to alloy through. Fortunately, no such difficulty was encountered for Al mole-fractions up to 35%. As seen in Fig.4.2-4, the specific contact resistances for the $Al_{0.25}Ga_{0.75}N$/GaN and $Al_{0.35}Ga_{0.65}N$/GaN devices are 0.50 and 0.55 Ω-mm respectively. The $Al_{0.5}Ga_{0.5}N$/GaN device, however, does show a substantially higher contact resistance of 1 Ω-mm.

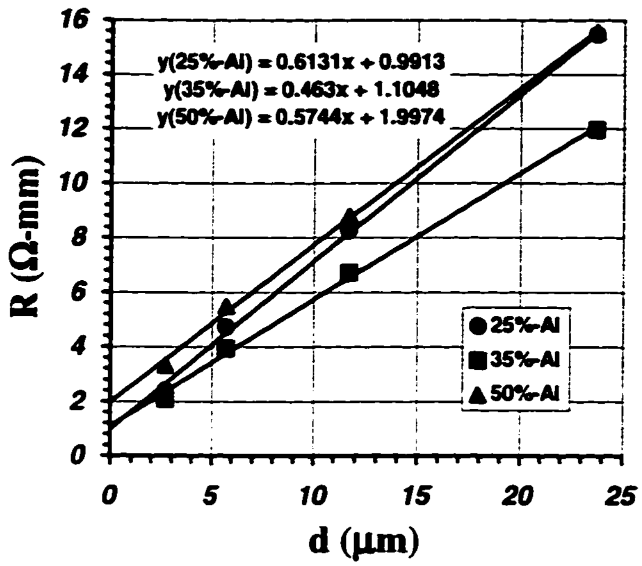


Fig.4.2-4 *TLM measurement results determining ohmic contact resistances for the AlGaN/GaN HEMTs with Al mole-fractions of 25%, 35% and 50%. The transfer contact resistances are 0.5 Ω-mm, 0.55 Ω-mm and 1.0 Ω-mm, respectively.*

4.2.3 *DC performance*

Fig.4.2-5b, c, and d show the I-V characteristics of the Al-rich AlGaN/GaN HEMTs. All characteristics were taken on half of the 50-μm-wide devices to minimize self-heating. For a convenient comparison, those of an $Al_{0.15}Ga_{0.85}N$/GaN device described in chapter 3 are also showed in Fig.4.2-5a.

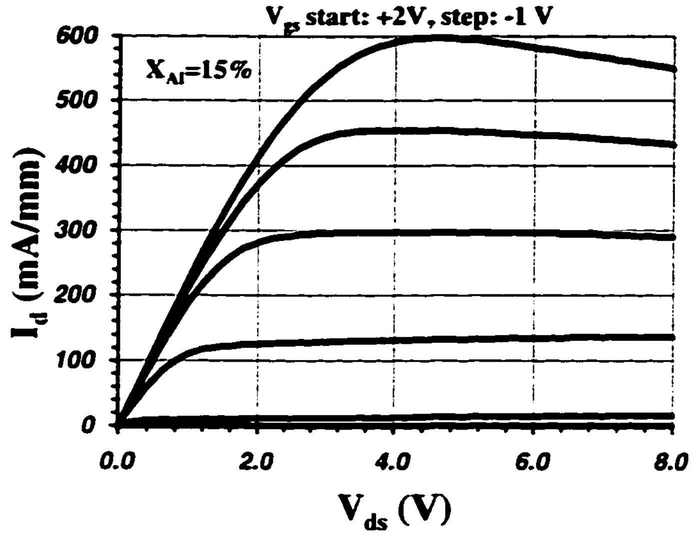


Fig4.2-5(a)

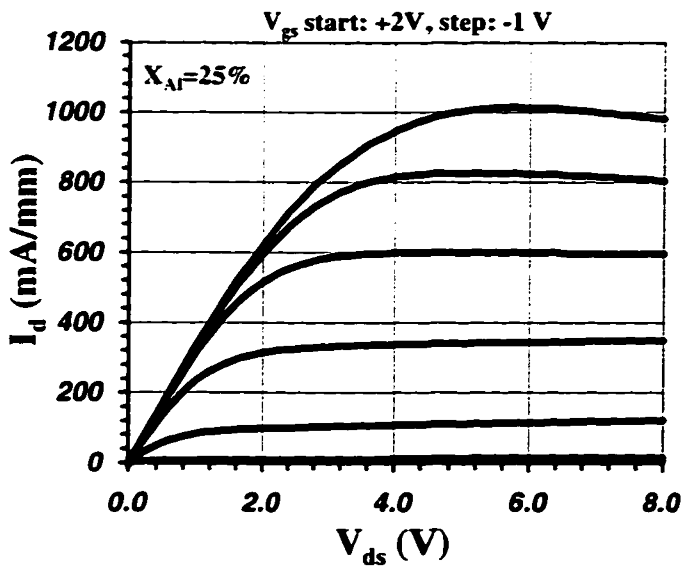


Fig4.2-5(b)

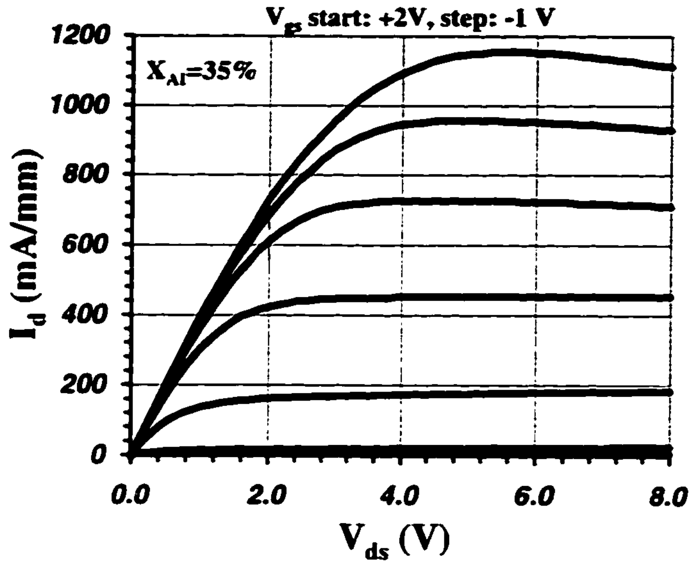


Fig.4.2-5(c)

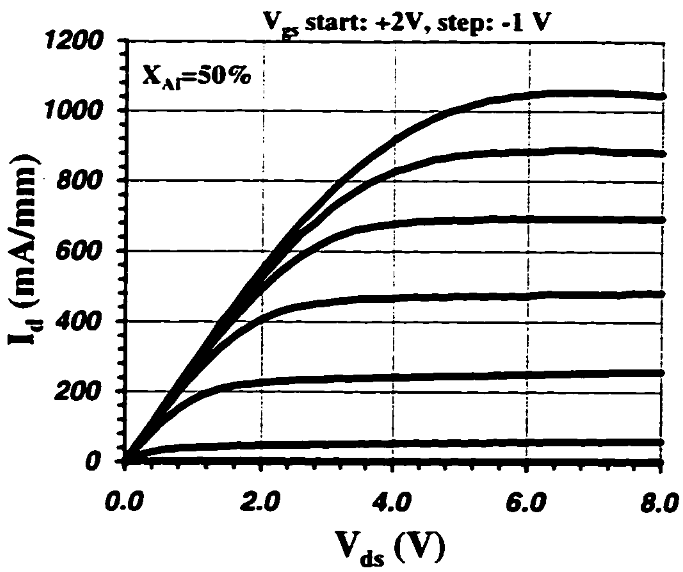


Fig.4.2-5(d)

Fig.4.2-5 *Drain output IV characteristics of AlGaN/GaN HEMTs with Al mole-fractions of a) 15%, b) 25%, c) 35% and d) 50%.*

With a higher charge density of 1×10^{13} cm^{-2} over the 6~7×10^{12} cm^{-2} value for previous $Al_{0.15}Ga_{0.85}N$/GaN devices, the $Al_{0.25}Ga_{0.75}N$/GaN HEMT exhibited a markedly increased current density of 1000 mA/mm. Owing to the high $n\mu$ product, the trade-off of this 67% increase in drain current is only a small increase in knee voltage by 25% (from 4 to 5 V). The peak transconductance is 255 mS/mm located at I_d ~ 500 mA/mm and V_{ds} ~ 4 V. This much higher transconductance over the previous value of 160 mS/mm is attributed to both the thinner AlGaN layer used for the Al-rich devices and the reduced access resistances. The on-resistance is seen as 3 Ω-mm, while the source resistance was measured as 1.45 Ω-mm with which an intrinsic transconductance of 405 mS/mm is estimated. As in the case before, the apparent negative resistance at high current levels is attributed to self-heating where the DC power is as high as 8 W/mm.

As expected by the even higher charge density and the un-degraded contact resistance, the $Al_{0.35}Ga_{0.65}N$/GaN device showed a further enhanced current density of 1150 mA/mm and a higher transconductance of 280 mS/mm, while the knee voltage was maintained a low value of ~ 5 V. The on-resistance, source resistance and intrinsic transconductance are 2.5 Ω-mm, 1.2 Ω-mm and 422 mS/mm, respectively.

The $Al_{0.5}Ga_{0.5}N$/GaN HEMT, however, mildly suffered from the poor ohmic contact resistance. Although having the same charge density as the $Al_{0.35}Ga_{0.65}N$/GaN device, the current density reduced to 1050 mA/mm, the knee voltage increased to 6 V and transconductance dropped to 220 mS/mm. The on-resistance, source resistance and intrinsic transconductance were 4 Ω-mm, 1.9 Ω-mm and 378 mS/mm, respectively

The gate diodes turn-on voltage were1.2 ~ 1.4 V, 1.2 ~ 1.6 V and 1.7 ~ 2.0 V for the Al mole-fractions of 25%, 35%, and 50% respectively. Although the charge densities were largely increased, high-voltage tests revealed that the Al-rich devices did not suffer from degradation in gate-drain breakdown voltages compared with the $Al_{0.15}Ga_{0.85}N$/GaN devices of much lower channel charge. These breakdown voltages were 100 ~ 135 V, 150 ~ 200 V, 220 ~ 280 V for gate-drain separations of 1, 2 and 3 μm, respectively. Devices with a richer Al-content generally have a higher current-voltage product per unit gate-width. The higher Johnson's figure of merit is believed to be a reason for the simultaneous realization of high breakdown voltages and high current densities. Other mechanisms may be present and will be investigated in the following chapter. Fig.4.2-6 is the high-voltage output I-V characteristics of an $Al_{0.5}Ga_{0.5}N$/GaN device with a gate-drain spacing of 3 μm taken by a Sony/Tektronix 370A curve tracer with a single trace of 17 ms for each gate bias. A lower current limit was used to avoid device-failure. The exhibited three-terminal breakdown voltage beyond 200 V and the saturation current density of > 1 A/mm translate to an ultra-high I-V product per unit width of ($I_{max}V_{max}$) > 200 VA/mm. In literature, the only I-V product close to this value was 100 V x 500 mA/mm = 50 VA/mm with a 4H-SiC MESFET [xi]. Ideally, the maximum output power is ($I_{max}V_{max}$)/8. This predicts a possible output power density of 25 W/mm provided that an ultimate thermal management is properly done.

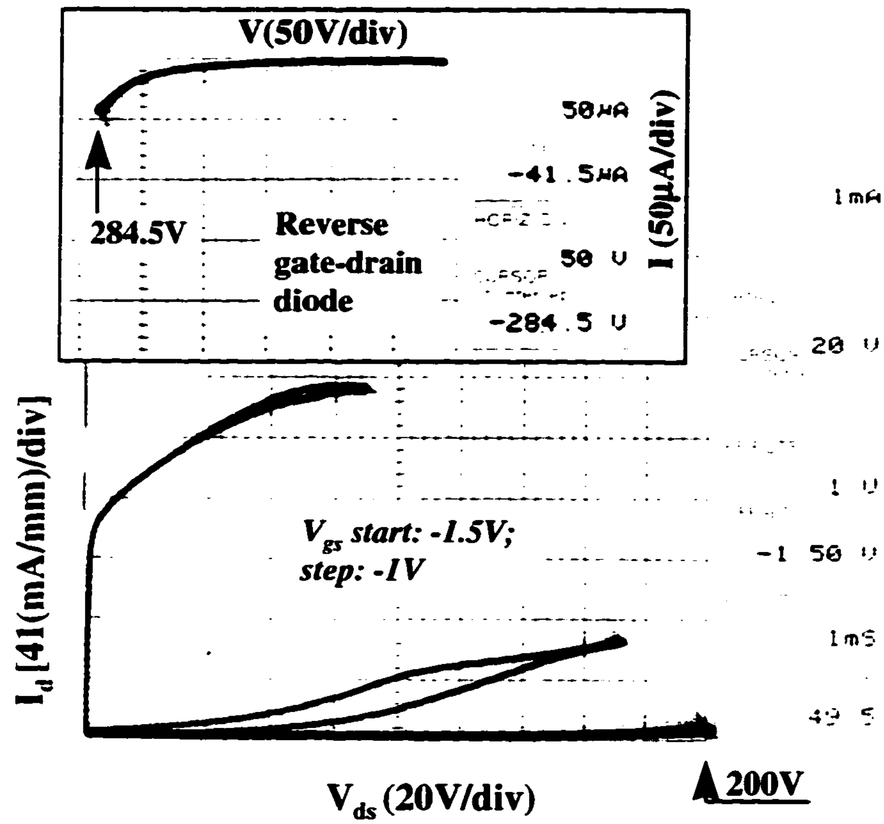


Fig.4.2-6 *The large-voltage output I-V characteristics of an $Al_{0.5}Ga_{0.5}N/GaN$ HEMT showing a three-terminal breakdown voltage > 200 V. (Inset: Reverse I-V characteristics of the gate-drain diode, showing a two-terminal breakdown voltage > 280 V)*

4.2.4 *Small-signal RF performance*

Small-signal microwave measurements confirmed the performance improvement with these Al-rich AlGaN/GaN HEMTs. Fig. 4.2-7a, b and c show the plots of current-gain and unilateral power-gain versus frequency for some of the best devices with Al mole-fractions of 25%, 35% and 50%.

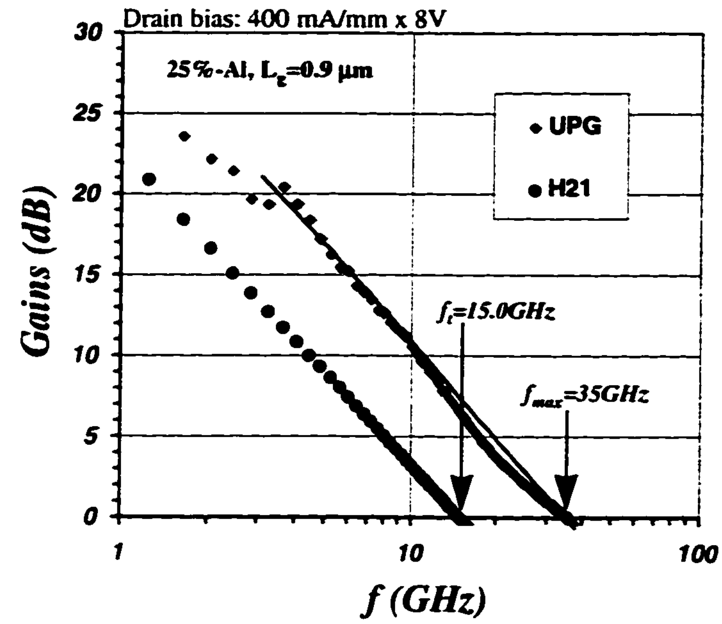


Fig.4.2-7a

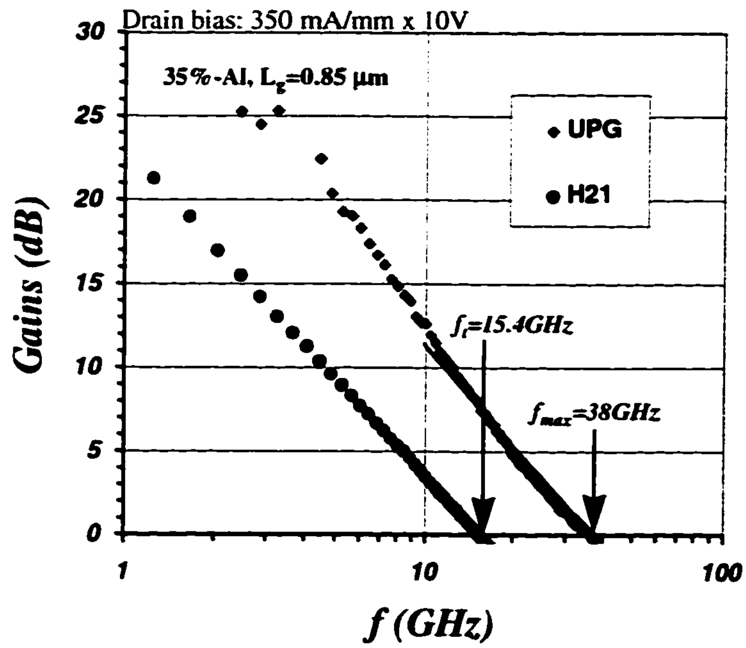


Fig.4.2-7b

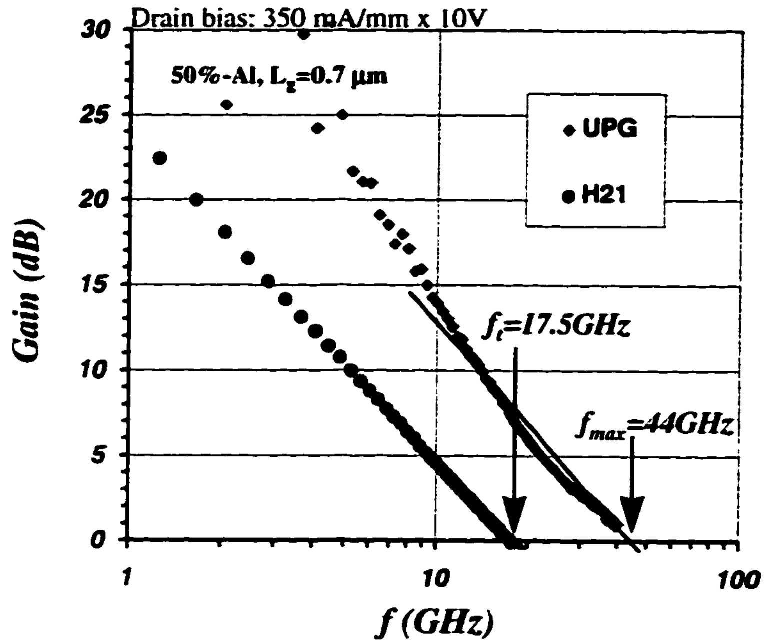


Fig.4.2-7c

Fig.4.2-7 *Current-gain and unilateral power-gain versus frequency for AlGaN/GaN HEMTs with Al mole-fractions of a) 25%, b) 35% and c) 50%.*

The f_t's are 15 GHz, 15.3 GHz and 17.5 GHz for the devices with gate-lengths of 0.9 μm, 0.85 μm, 0.7 μm and Al mole-fractions of 25%, 35%, 50% respectively, corresponding intrinsic values (f_{ti}'s) are 17.2, 17.7 and 21.8 GHz, or intrinsic f_t-gatelength products of 15.5, 15.1 and 15.3 GHz-μm, respectively. All of them are considerably higher than the best value of 11.4 GHz-μm for the $Al_{0.15}Ga_{0.85}N$/GaN devices. For a more detailed comparison of these devices, current-gain cutoff frequencies and other major elements extracted using S-parameters (see chapter 5 for details) are listed in Table 4.2-2.

Table 4.2-2 *Cutoff frequencies and major parameters of AlGaN/GaN HEMTs with various Al mole-fractions.*

X_{Al} (%)	t (Å)	L_g (μm)	Bias: I_d(mA/mm) xV_{ds}(V)	f_t/f_{ti} (GHz/GHz)	$f_tL_g/f_{ti}L_g$ (GHz-μm/ GHz-μm)	f_{max} (GHz)	C_{gs} (pF/ mm)	g_{m0} (mS/ mm)	R_{ds} (Ω-mm)
15%	400	1.1	200x12	9.6/**10.4**	10.6/**11.4**	22	2.85	188	192
25%	200	0.9	400x8	15.0/**17.2**	13.5/**15.5**	35	3.49	385	119
35%	200	0.85	350x10	15.5/**17.7**	13.0/**15.1**	38	3.39	386	136
50%	200	0.7	350x10	17.5/**21.8**	12.3/**15.3**	44	2.50	351	118

Using the $f_{ti}L_g$ value of 15.3 GHz-μm, the effective channel velocity is estimate to be 9.6x10^6 cm/s, about 33% improvement over the previous value of 7.7x10^6 cm/s with the $Al_{0.15}Ga_{0.85}N$/GaN devices. The intrinsic RF transconductance (g_{m0}) at peak f_t is smaller than the peak intrinsic transconductance previously calculated using the IV characteristics, mainly due to self-heating under the DC bias power. Both values were found fairly close at lower bias voltages, indicating a low level of trap density in the transistor channel. It should be noted that self-heating also affects the extracted value of C_{gs} but in a way such that g_{m0}/C_{gs} = constant (see chapter 5 for details), not affecting the calculation for f_{ti}. The output resistance R_{ds} of an FET usually increases with decreasing drain current, increasing bias voltage or increasing gate-length, which explains its variations in Table 4.2-2.

The current gain cutoff frequencies were also investigated as a function of drain current as shown in Fig.4.2-8. The drain bias voltage were fixed at 6 V except for the $Al_{0.5}Ga_{0.5}N$/GaN device which was biased at 7 V because of its higher knee voltage. Due to the increased current densities for the Al-rich HEMTs, the locations for the peak f_t's extend to higher current levels of 350 ~ 500 mA/mm from the previous value of 200 mA/mm with the $Al_{0.15}Ga_{0.85}N$/GaN device. The higher f_t's maintained in a much broader current range will largely enhance the current driving ability.

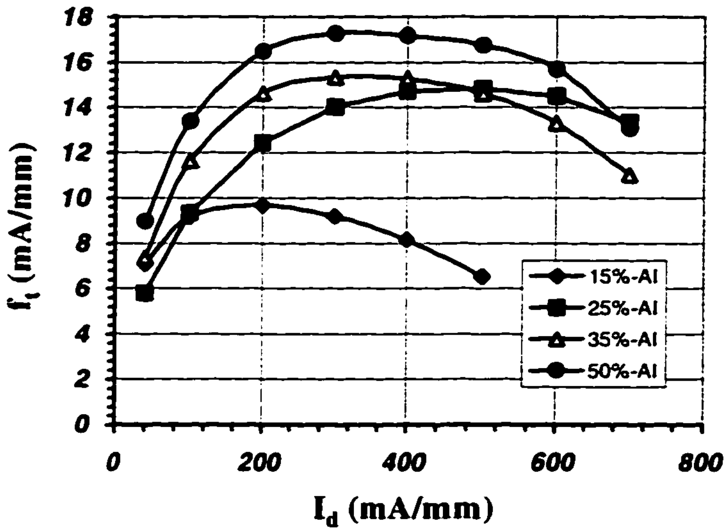
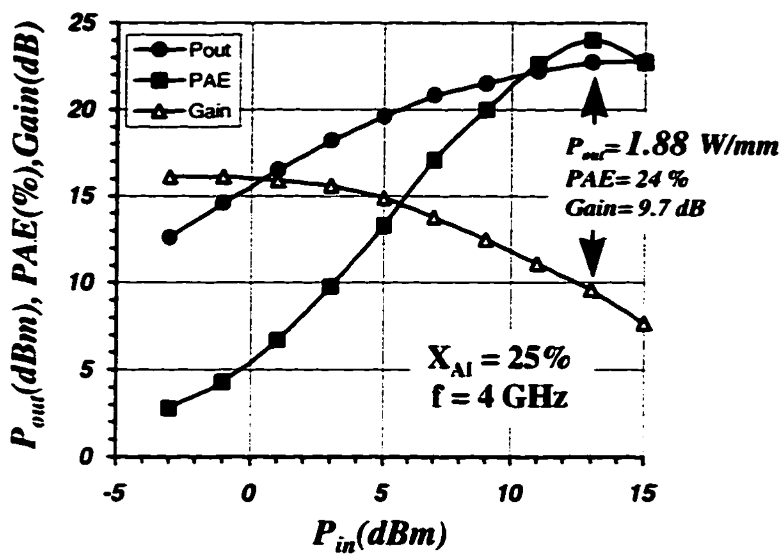


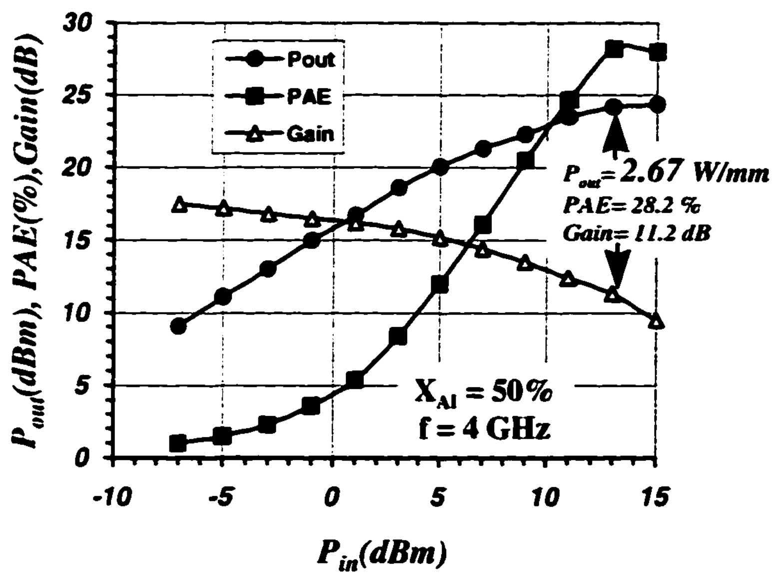
Fig.4.2-8 *f_t vs. drain current for AlGaN/GaN HEMTs with various Al-contents (drain bias: 6V for devices with Al-contents of 15%, 25%, 35%; 7V for the $Al_{0.5}Ga_{0.5}N$/GaN device)*

4.2.5 *RF power performance*

Un-cooled microwave power performance was characterized with the Maury Microwave Automated Load-pull Tuner System in Wright Laboratory, Wright-Patterson Air Force Base. Due to the limited access to this measurement setup and the time-consuming procedures for optimizing bias point and tuning conditions, only devices with Al mole-fractions of 25% and 50% were properly tested. For all measurements presented below, the device width used was 100 μm. The devices were biased in a class-A mode and the input power sweep was from high to low to minimize thermal stress, since the heating power, which approximately equals DC power minus output power, is highest when the input drive is low.



(a)



(b)

Fig. 4.2-9 *Power performance at 4 GHz un-cooled on sapphire substrate (a) for an $Al_{0.25}Ga_{0.75}N/GaN$ HEMT (gate dimension: 0.9μm x 100μm, output power: 22.74dBm, drain bias: 30.2mA x 24V); (b) for an $Al_{0.5}Ga_{0.5}N/GaN$ HEMT (gate dimension: 0.7μm x 100μm, output power: 24.27dBm, drain bias: 34.7mA x 25V).*

The characterization was first started at 4 GHz. Fig.4.1-9a shows the measurement result for an $Al_{0.25}Ga_{0.75}N/GaN$ HEMT. The device was bias at V_{gs} = -0.8 V and V_{ds} = 24 V. Due to self-heating, the drain current was only 29.0 mA, or 290 mA/mm, much lower than the 38 mA found in the low-voltage I-V characteristics (Fig.4.2-5b) for the corresponding gate-bias. The source and load reflection coefficients were $\Gamma_{source} = 0.526e^{i45.76°}$ and $\Gamma_{load} = 0.785e^{i5.23°}$ respectively. As seen in the graph, the device exhibits a small-signal gain of 16 dB, corresponding to a gain-frequency product of 25.2 GHz with the load optimized for output power. At an input level of 13 dBm, the output power saturates at 22.74 dBm, or a power density of 1.88 W/mm. The large-signal gain and PAE are 9.7 dBm and 24% respectively. Although the $Al_{0.25}Ga_{0.75}N/GaN$ HEMT exhibits ~ 4 dB increase in both small-signal and large-signal gains over the previous $Al_{0.15}Ga_{0.85}N/GaN$ device, the increase in power density is only 20%, lower than expected from the 60% higher current density than the $Al_{0.15}Ga_{0.85}N/GaN$ device. Further increasing drain bias was not able to increase power density and led to a largely reduced PAE.

The measurement result for an $Al_{0.5}Ga_{0.5}N/GaN$ HEMT at 4 GHz is shown in Fig.4.1-9b. The bias conditions were V_{gs} = -1.0 V, V_{ds} = 25 V and I_d = 34.7 mA (or 347 mA/mm), while the source and load reflection coefficients were $\Gamma_{source} = 0.658e^{i38.21°}$ and $\Gamma_{load} = 0.785e^{i5.23°}$. The device demonstrates a small-single gain of 17 dB or a frequency-gain product of 28.3 GHz. The output power density, PAE and large-signal gain are 2.67 W/mm, 28.2% and 11.2 dB. This markedly higher power density (by 0.79 W/mm or 42%) over the $Al_{0.25}Ga_{0.75}N/GaN$ device is a direct result form the less gain compression at high input drive. At a lower drain bias of 20 V and 30.5 mA/mm, the PAE was increased to 30% with a lower output power of 2.36 W/mm.

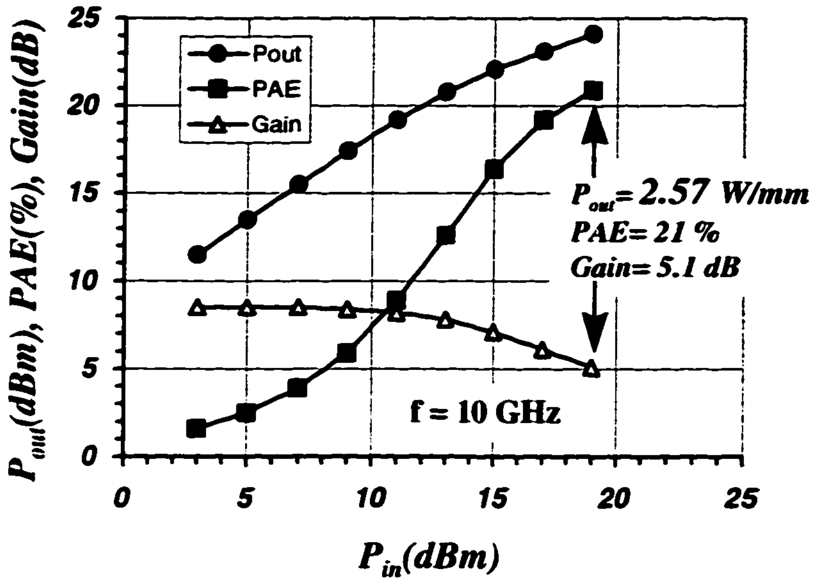


Fig. 4.2-10 *Power performance of an $Al_{0.5}Ga_{0.5}N$/GaN HEMT at 10 GHz uncooled on sapphire substrate (gate dimension: 0.7μm x 100 μm, output power: 24.10 dBm, drain bias: 34.0 mA x 25 V).*

An $Al_{0.5}Ga_{0.5}N$/GaN HEMT was subsequently tested at 10 GHz as shown in Fig.4.2-10. The device was biased with V_{gs} = -1.4 V, V_{ds} = 25 V. The lower gate bias resulted a lower quiescent drain current of 31 mA, but it was self-adjusted to 34.0 mA (or 340 mA/mm) at peak output power. The source and load reflection coefficients were $\Gamma_{source} = 0.362e^{i177.10°}$ and $\Gamma_{load} = 0.773e^{i5.43°}$. The small signal gain is seen as 8.5 dB. Although this corresponds to a lower gain-frequency product of 26.6 GHz than the 27.2 value at 4 GHz due to the lower quiescent current, the gain-compression is smaller, leading to a similar output power density of 2.57 W/mm. The large-signal gain and PAE are 5.1 dB and 21% respectively. The devices were also tested at 8 GHz, yielding a small-signal gain, output power, large-signal gain and PAE of 11.5 dB, 2.84 W/mm (24.54 dBm/0.1mm), 6.6 dB and 23%, respectively.

The CW output density of 2.57 ~ 2.84 W/mm achieved with the $Al_{0.5}Ga_{0.5}N$/GaN HEMTs was the highest for a solid-state FET in X band (8 ~ 12 GHz). This supports the design philosophy that AlGaN/GaN HEMTs with a high Al-content have a higher power-frequency figure of merit. Fig.4.2-11 summarizes the best result in power densities achieved un-cooled on sapphire substrates with various Al mole-fractions. The power density increases monotonicly with Al-content. Higher performance may be available with even higher Al-contents if the AlGaN can be heavily doped.

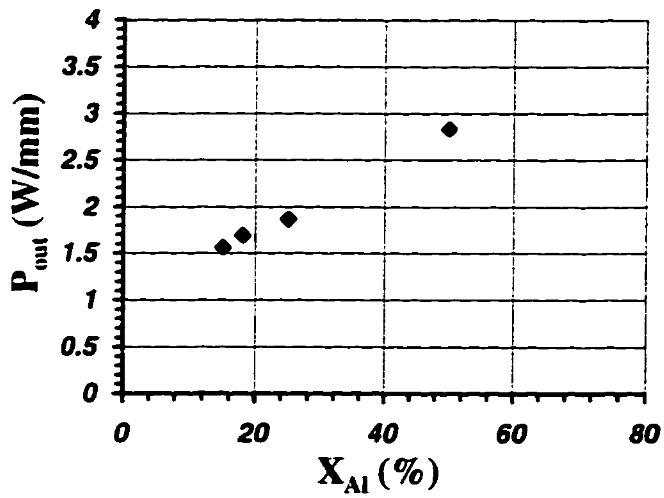
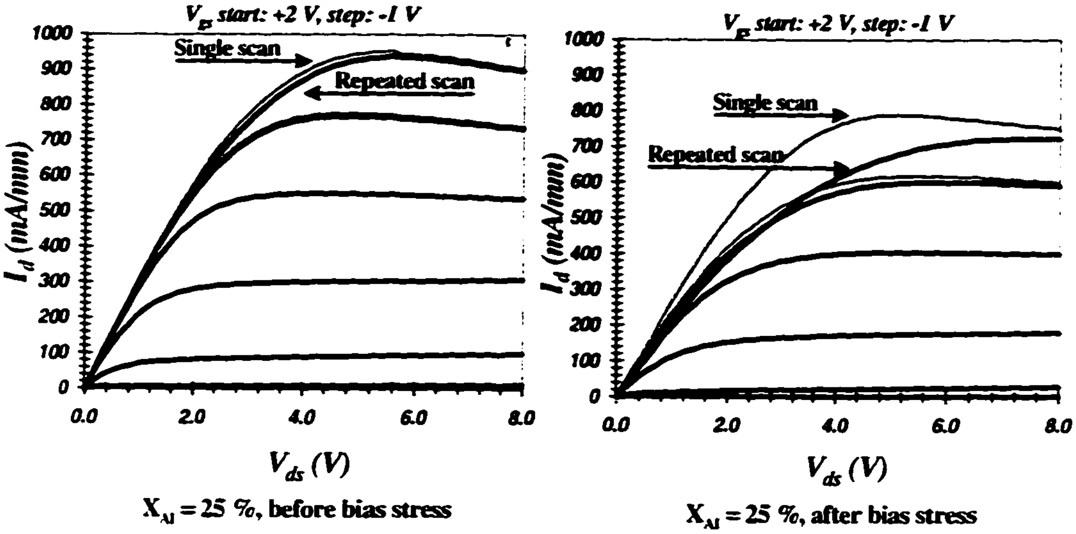
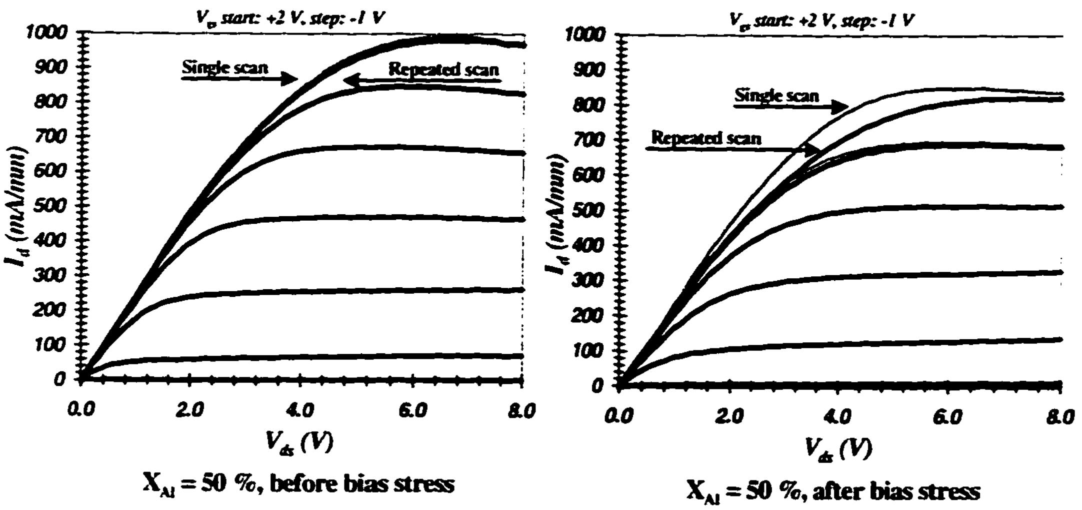


Fig.4.2-11 *Best measured output-power density vs. Al mole-fraction for AlGaN/GaN HEMTs un-cooled on sapphire substrates.*

To find out what happened after the high power stress, the DC and small-signal RF performances of the $Al_{0.25}Ga_{0.75}N$/GaN and the $Al_{0.5}Ga_{0.5}N$/GaN devices were characterized before and after DC bias power of 8.5 W/mm for 10 min. Fig.4.2-12 shows the comparisons of the I-V characteristics.



(a)



(b)

Fig.4.2-12 *Comparisons of I-V characteristics of the AlGaN/GaN HEMTs with Al mole-fractions of (a) 25% and (b) 50%, before and after a high DC-power stress of 8 W/mm for 10 min. (Devices width: 100μm)*

It is seen that before the DC-power stress, both devices exhibited little differences between a single scan and a repeated scan, suggesting a low level of deep traps in the transistor channels. After stress, however, not only the current levels decreased but also obvious hystereses appeared, indicating formation of deep traps. The ratios of current reduction were 23 % and 15 % for the $Al_{0.25}Ga_{0.75}N/GaN$ and the $Al_{0.5}Ga_{0.5}N/GaN$ HEMTs, respectively, by the IV curves of repeated scan. These can be caused by interface reconstruction, reaction between the metal gate and the AlGaN layer or other forms of structure degradation.

The device circuit-elements were also extracted from S-parameters to assess the extent of degradation for each parameters. Results are summarized in Table 4.2-3. When measuring the S-parameters, the $Al_{0.25}Ga_{0.75}N/GaN$ device was biased at V_{gs} = -0.3 V, V_{ds} = 8 V while the $Al_{0.5}Ga_{0.5}N/GaN$ device was at V_{gs} = -0.9 V, V_{gs} = 8 V, which yielded a drain current of 400 mA/mm before stressing.

Table 4.2-3 Comparison of major device parameters before / after DC power stress

Parameter	X_{Al} = 25 % after / before = %	X_{Al} = 50 % before / after
I_{dss} (mA/mm)	725 / 940 = 77 %	830 / 975 = 85 %
f_t (GHz)	11.1 / 13.5 = 82 %	14.6 / 16.3 = 90 %
f_{max} (GHz)	21.9 / 25.1 = 87 %	33.5 / 37.5 = 89 %
R_s (Ω-mm)	1.53 / 1.42 = 108 %	1.65 / 1.63 = 101 %
R_d (Ω-mm)	2.22 / 1.91 = 116 %	2.78 / 2.43 = 114 %
R_{ds} (Ω-mm)	81.0 / 146.1 = 55 %	66.3 / 124.9 = 53 %
g_{m0} (mS/mm)	318 / 286 = 111 %	328 / 343 = 96 %
C_{gs} (pF/mm)	3.81 / 2.76 = 138 %	2.87 / 2.70 = 106 %

A large amount of information can be obtained by such a comparison. First, the increases in drain resistances R_d's are much higher than the increases in source resistances R_s's, showing that the maximum stress was at the drain side where both heat generation and electric field are expected high. Second, both output resistances R_{ds}'s have decreased by nearly a factor of 2, indicating that the electrical quality of the i-GaN as a buffer has degraded. Since this buffer was identical for both devices, the extents of degradation are almost same. Third, the increased gate-source C_{gs} and transconductance g_{m0} for the $Al_{0.25}Ga_{0.75}N/GaN$ HEMT suggests that the metallic gate might have sunk into the $Al_{0.25}Ga_{0.75}N$ layer. The very little change in C_{gs} and g_{m0} for the $Al_{0.5}Ga_{0.5}N$ device can be explained by the higher stability of the $Al_{0.5}Ga_{0.5}N$ / Ni-Au junction under high power stress. Fortunately the Schottky barriers for both devices were well maintained, lending support to device reliability for applications in demanding circumstances.

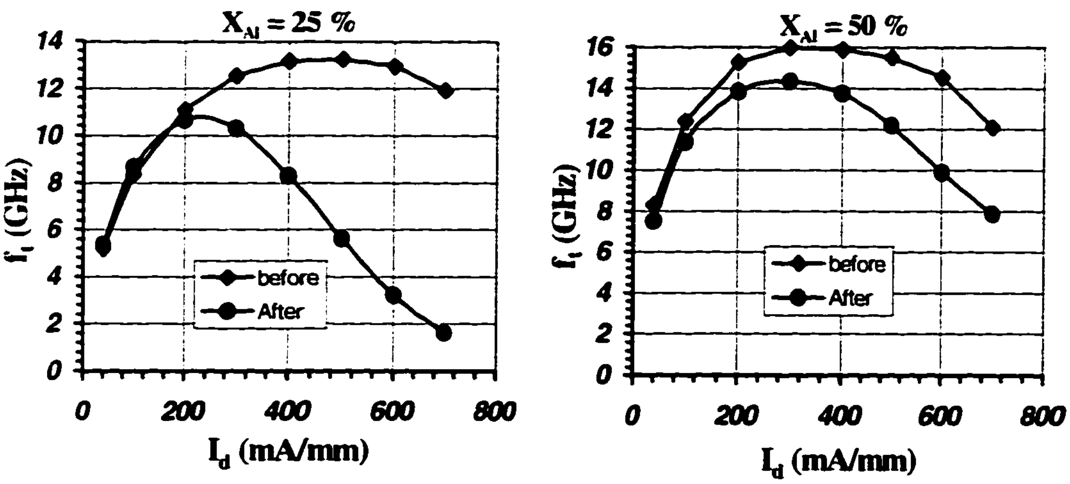


Fig.4.2-13 *Comparisons of f_t vs. I_d for the AlGaN/GaN HEMTs with Al mole-fractions of 25% and 50%, before and after a high DC power stress of 8 W/mm for 10 min. (V_{ds}: 6 V for the $Al_{0.25}Ga_{0.75}N$ device and 7 V for the $Al_{0.5}Ga_{0.5}N$ device).*

The large discrepancy in un-cooled microwave power performance for the two devices can be more appreciated if the f_t as a function of drain current is re-investigated after the power stress as shown in Fig.4.2-13. It is seen that for the $Al_{0.25}Ga_{0.75}N$ HEMT, although the peak f_t has only moderate degradation, its value at high current is drastically reduced. This may be caused by the newly formed traps which absorb part of the voltage and reduce the electric field in the channel for the same external V_{ds}. The loss in current-driving ability at high frequencies leads to a great discount to its apparent high current level. Such a degradation for the $Al_{0.5}Ga_{0.5}N$ device is quite mild, confirming its overall higher tolerance to the power stress.

4.3 Short channel devices

To investigate the potential of AlGaN/GaN HEMTs to operate at even higher frequencies, submicron gatelength devices were fabricated.

4.3.1 *Devices with different Al-contents*

Epi-films with Al mole-fractions of 17.5% and 50% were used in the following study. The corresponding batch numbers are 961120 FE (X_{Al} = 17.5 %, $n_s \sim 8\times10^{12}$ cm^{-2}, $\mu \sim 1150$ cm^2/Vs) and 970224 FA (X_{Al} = 50%, $n_s \sim 1.2\times10^{13}$ cm^{-2}, $\mu \sim 920$ cm^2/Vs), both were grown by Dr. Bernd Keller. The layer structures were the same as shown in Fig.4.2-1. The fabrication process was also the same as presented before, except that the gate definition was accomplished by electron-beam lithography in Hughes Research Labs by Minh Le with a routine 0.25-μm T-gate technology. Scanning-electron-microscope (SEM) inspection after photo-resist development showed a T-shape profile with 0.5 ~ 0.7 μm top opening and 0.20 ~ 0.30 μm footprint (gate-length). The gate metallisation was Ni/Au (100 Å / 3400 Å). TLM measurements yielded transfer ohmic contact resistances of 0.4 ~ 0.6 and 0.9 ~ 1 Ω-mm for the $Al_{0.175}Ga_{0.825}N$ and the $Al_{0.5}Ga_{0.5}N$ devices, respectively, conforming previous results. The sheet resistance of the i-GaN buffer for the former was normal (> 50 MΩ/sq); while it was 2 ~ 10 MΩ/sq for the latter which may affect the device output conductance.

Fig.4.3-1 shows the output I-V characteristics of both submicron gate AlGaN/GaN HEMTs. As expected from the sheet charge densities, the devices exhibit increasing current densities of 900 mA/mm and 1130 mA/mm going from an Al mole-fraction of 17.5% to 50%. The corresponding knee voltages and transconductances are 5 V, 250 mS/mm and 6 V, 240 mS/mm as compromises of current densities, access and contact resistances.

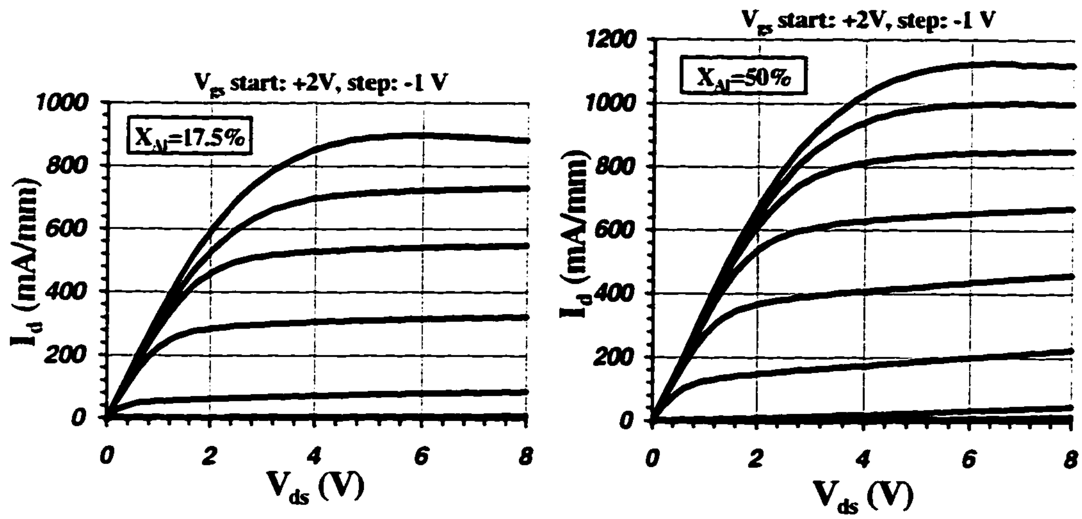


Fig.4.3-1 *Output I-V characteristics of typical 0.25-μm gatelength AlGaN/GaN HEMTs with Al mole-fractions of 17.5% and 50%.*

Typical measured peak f_t's for devices with source-drain spacing of 1.7-μm were 30 ~ 40 GHz and 40 ~ 50 GHz, respectively, for the two types of devices with increasing Al-content. The reason for the generally higher f_t's with the $Al_{0.5}Ga_{0.5}N$ devices will be analyzed in chapter 5. Fig.4.3-2 is the measurement result for an $Al_{0.5}Ga_{0.5}N$ HEMT showing f_t and f_{max} of 52 GHz and 82 GHz respectively. The f_t is the highest reported for a GaN-channel FET to date, while the low f_{max} / f_t ratio is both related to the poor ohmic contact resistance and the relatively low resistance of the I-GaN buffer in this growth batch.

The higher current density of the $Al_{0.5}Ga_{0.5}N$ devices also translated into a higher f_t in a broader current range as seen in Fig.4.3-3, which is of essential importance for large-signal high-speed applications.

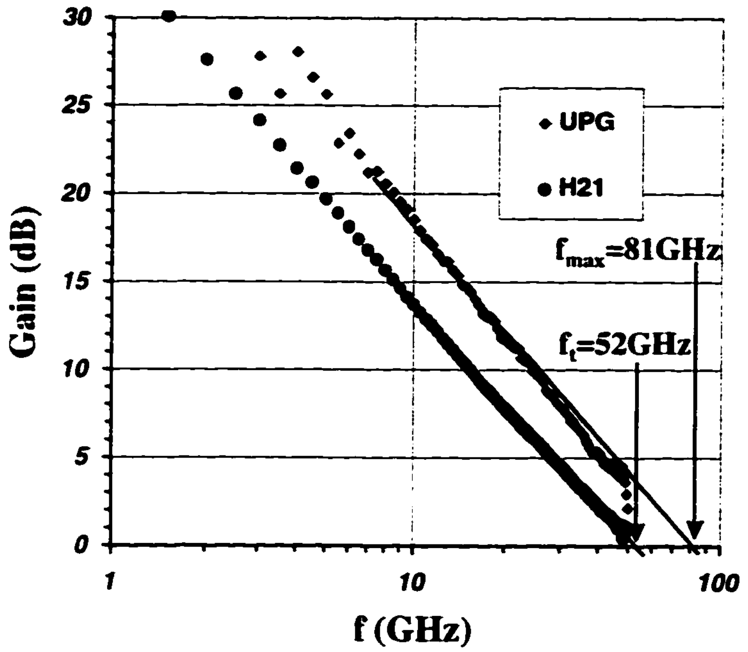


Fig.4.3.2 *Current-gain and unilateral power-gain vs. frequency for a 0.25-μm gate-length $Al_{0.5}Ga_{0.5}N$ HEMT (device width: 100 μm, drain bias: 300 mA/mm x 8 V).*

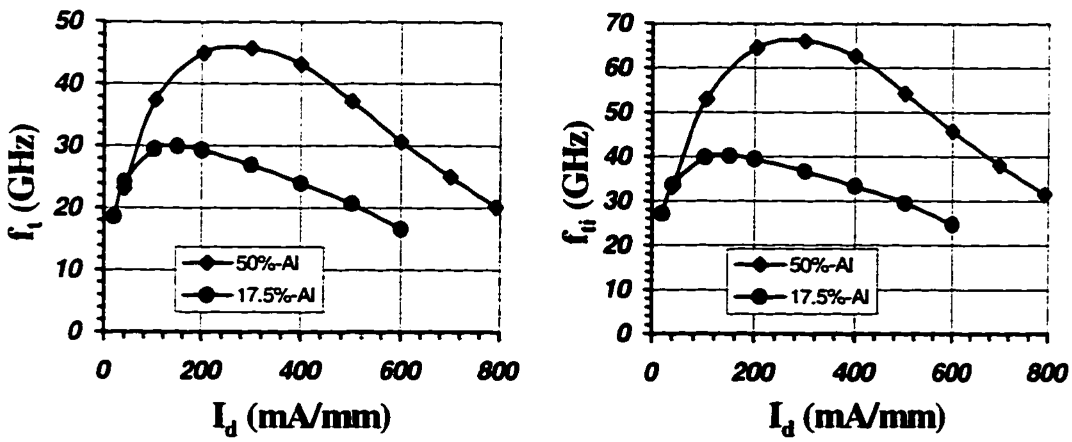


Fig.4.3-3 *Extrinsic current-gain cutoff frequency f_t and intrinsic current-gain cutoff frequency f_{ti} vs. drain current for the AlGaN/GaN HEMTs with Al-contents of 17.5% and 50% (drain bias: 6 V).*

Although the peak f_t value of the $Al_{0.5}Ga_{0.5}N/GaN$ HEMT is still lower than what achieved with conventional HEMTs of similar gate-lengths [xii, xiii], the f_t of the GaN-channel HEMT maintains high in a much broader voltage range as seen in Fig.4.3-4. This ensures a large voltage excursion with high switching speed and shows the potential for the GaN-channel HEMT to outperform previous power HEMTs in millimeter frequencies (> 30 GHz).

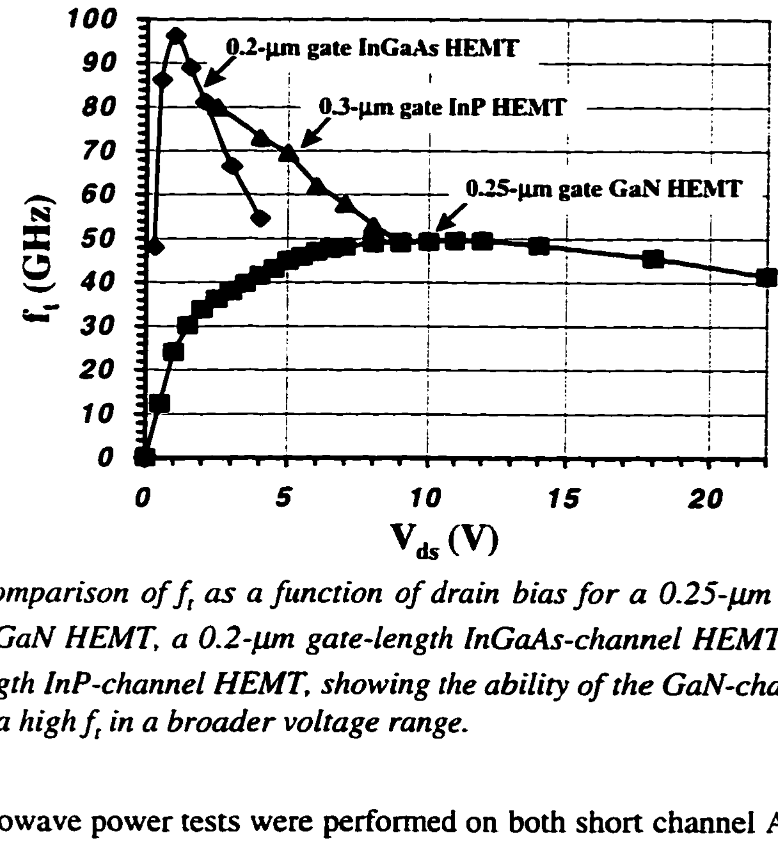
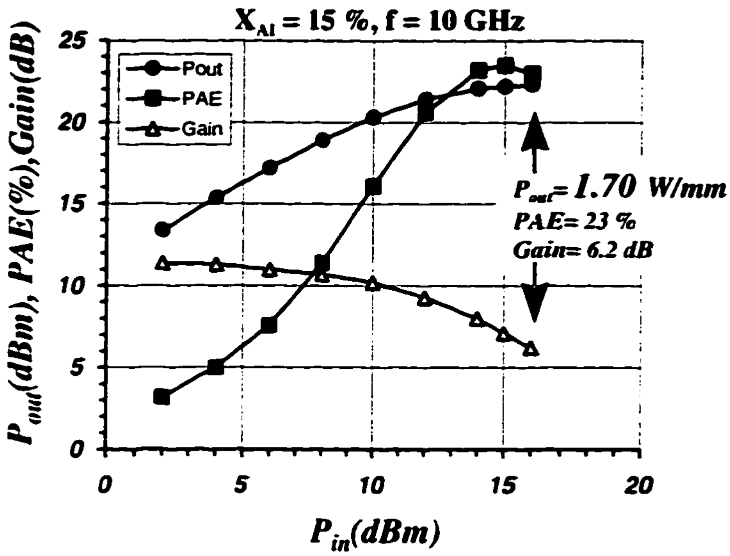
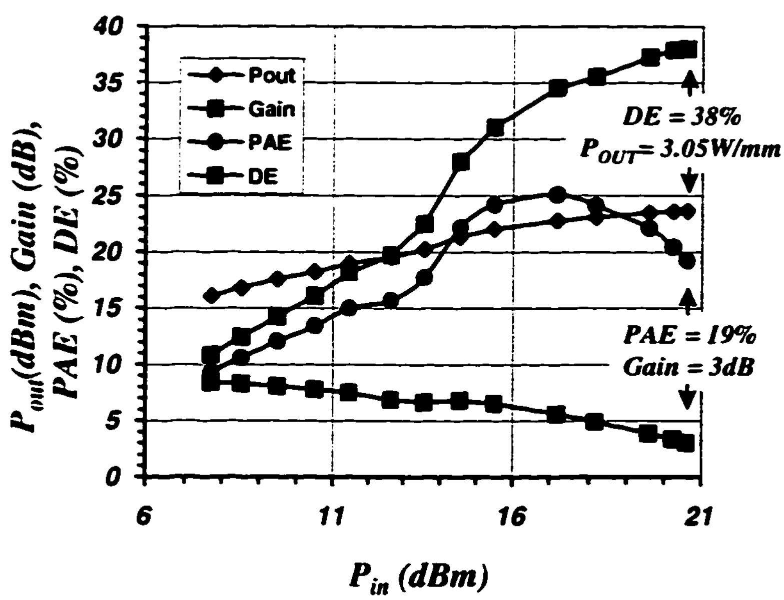


Fig.4.3-4 *Comparison of f_t as a function of drain bias for a 0.25-μm gate-length $Al_{0.5}Ga_{0.5}N/GaN$ HEMT, a 0.2-μm gate-length InGaAs-channel HEMT and a 0.3-μm gate-length InP-channel HEMT, showing the ability of the GaN-channel device to maintain a high f_t in a broader voltage range.*

Microwave power tests were performed on both short channel AlGaN/GaN HEMTs. The $Al_{0.175}Ga_{0.825}N/GaN$ device was characterized at 10 GHz with the passive Maury load-pull system in Wright-Patterson Air Force Base and the $Al_{0.5}Ga_{0.5}N/GaN$ device was at 18 GHz with an active load-pull system in Hughes Space and Communications Company. Fig.4.3-5 (a) and (b) show the measurement results with representative devices. The drain bias and load reflection coefficient at peak output power were 308mA/mm x 18V, $0.773e^{j5.43°}$ and 380mA/mm x 21V, $0.796e^{j18.1°}$, respectively.



(a)



(b)

Fig.4.3-5 *Power performance of (a) a 0.25-μm gate-length $Al_{0.175}$ $Ga_{0.825}N/GaN$ HEMT at 10 GHz (device width: 100 μm) and (b) a 0.25-μm gate-length $Al_{0.5}$ $Ga_{0.5}N/GaN$ HEMT at 18 GHz (device width: 76 μm).*

Although operated at a higher frequency, the $Al_{0.5}Ga_{0.5}N/GaN$ HEMT produced a much higher saturation power density of 3.05 W/mm than the 1.7 W/mm value with the $Al_{0.175}$ $Ga_{0.85}N/GaN$ device of the same gate-length. This again confirms the advantage of using a high Al-content.

4.3.2 *$Al_{0.5}Ga_{0.5}N/GaN$ HEMTs with different gate dimensions*

1) *Performances versus gate-length*

Conventionally, operation mode of an FET, (i.e. gradual channel mode or velocity saturation mode), can be determined by investigation of the current gain cutoff frequency as a function of inverse gatelength. For this reason, $Al_{0.5}Ga_{0.5}N/GaN$ HEMTs with different gate-lengths were fabricated on the same wafer.

Fig.4.3-6 shows the I-V characteristics of three devices located close together but with decreasing gate-length from 0.65, 0.45 to 0.25 μm. Each measurement was taken on half of the 50-μm-wide device. The peak current densities and transconductances are 970 mA/mm, 1040 mA/mm, 1130 mA/mm and 200 mS/mm, 220 mS/mm, 240 mS/mm, respectively. As generally seen in the cases of conventional HEMTs, both the current density and transconductance increase with decreasing gatelength. The trade-off for these improvements is the increasing output conductance, which potentially reduces the f_{max}/f_t ratio and makes the output matching of devices with large gate peripheries difficult.

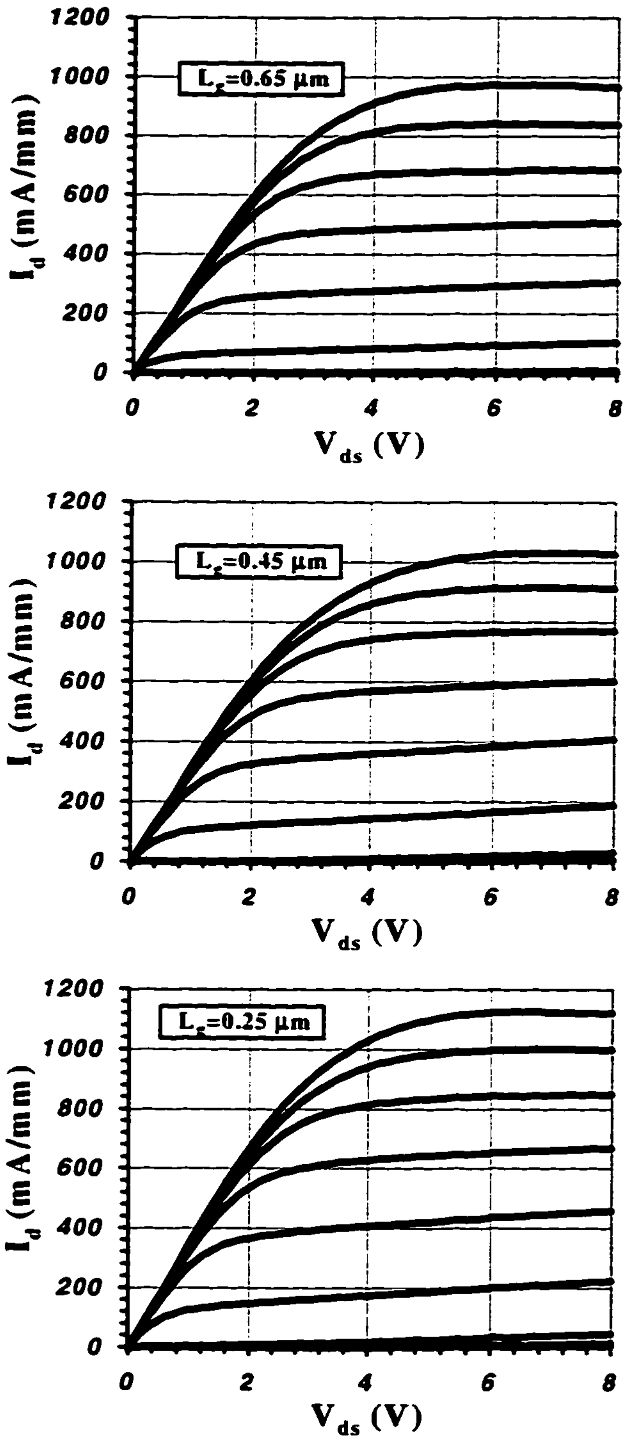


Fig.4.3-6 *I-V characteristics of $Al_{0.5}Ga_{0.5}N/GaN$ HEMTs with decreasing gatelength from 0.65, 0.45 to 0.25 µm (device width: 25µm, V_{gs} start: +2V, step: -1V).*

The measured peak extrinsic current-gain cutoff frequencies f_t's and the extracted *intrinsic* values f_{ti}'s (including results of the previous 0.7-μm gatelength $Al_{0.5}Ga_{0.5}N$/GaN device) are summarized in Fig.4.3-7 with the horizontal axis as the inverse gatelength (L_g^{-1}). For FETs in gradual channel mode, the dependence of f_{ti} on L_g^{-1} is super linear. As seen in the graph, for the $Al_{0.5}Ga_{0.5}N$/GaN HEMTs under study, such dependence is close to linear. Approximately, $f_{ti} \times L_g = 17$ GHz-μm. This suggests that the channel velocity is close to saturation for all gate-lengths under investigation, *provided that the drain extension is much smaller than the gatelength in each case.* The corresponding effective saturation velocity is 1.06×10^{7} cm/s. A more detailed analysis of the drain extension will be carried out in chapter 5.

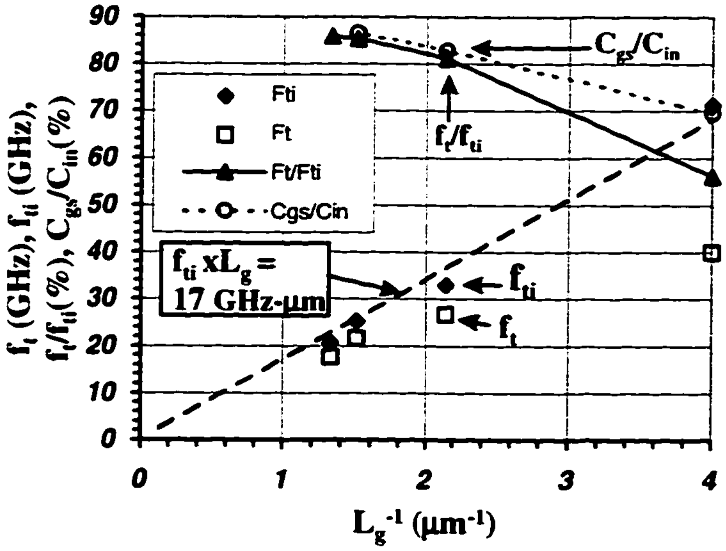


Fig.4.3-7 *Current-gain cutoff frequencies vs. inverse gatelength.*

For a practical FET, when short circuited at the output, the input capacitance can be expressed as:

$$C_{in} = (C_{gs} + C_{gd}) + (C_{gsp} + C_{gdp})$$

where C_{gs} and C_{gd} are the intrinsic gate-source and gate-drain capacitances; while C_{gsp} and C_{gdp} are gate-source and gate-drain parasitic capacitances, including contributions from both the gate-pad and gate-line.

The RF input current is shunt by all the capacitances, but only the part of current entering into C_{gs} constitutes an active drive. This results in an *input-current efficiency* of $\eta_I = C_{gs} / C_{in}$. Since the parasitic capacitances are practically constant for a specific mask design regardless of gatelength, as the gatelength decreases, C_{gs} decreases, C_{gs} / C_{in} decreases. This explains most of the degradation in the f_t / f_{ti} ratio for short gatelength devices as seen in Fig.4.3-7. The rest is attributed to the coupling between the device capacitances and parasitic resistances [xiv]. If an even higher f_t is desired, both the AlGaN layer thickness and the contact resistances need to be reduced.

Not only short gatelength leads to degradation in the f_t / f_{ti} ratio but also in the f_{max} / f_t ratio, as seen in Fig.4.3-8. This is due to the reduced output resistance R_{ds} resulted from the reduced aspect ratio: L_g/t, where t is the gate-to-charge spacing which is approximately the AlGaN thickness plus 22 Å (Eq.4.1-12). To retain a high f_{max} / f_t ratio, the AlGaN layer need to be thinned which is the same solution to maintaining a high f_t/f_{ti} ratio. This will potentially reduce the breakdown voltage and the output power density. Such a trade-off is determined by the Johnson's figure of merit (Eq.4.1-1).

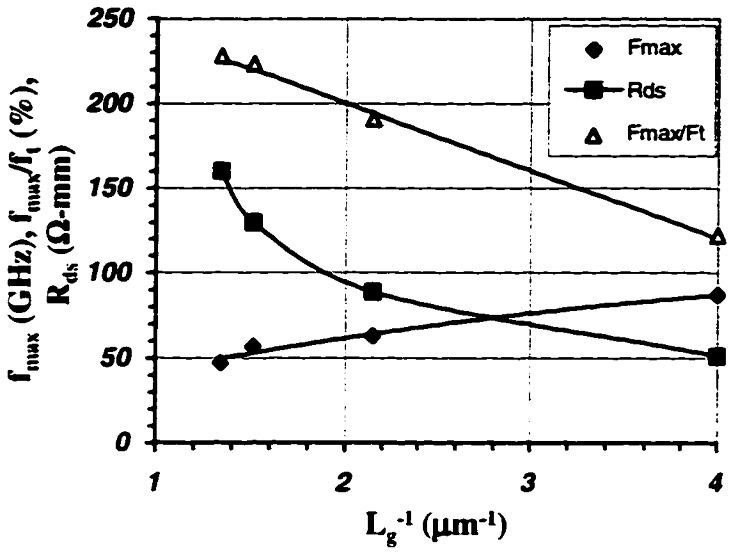


Fig.4.3-8 *Power-gain cutoff frequency, f_{max}/f_t ratio, and output resistance vs. inverse gatelength.*

2) *Performances versus gate-width*

The parasitic gate capacitances of a physical FET include contributions from the gate-pad and the gate-line. The former is practically constant while the latter scales linearly with the gate-width. This can be experimentally shown as seen in Fig.4.3-9, where the capacitances at $L_g = 0$ are pad capacitances. The gate-line capacitances are *fringing capacitances* and have a virtually identical dependence on gate-width: ~ 0.1 pF/mm. Since for a fixed gate-length, C_{gs} also scales linearly with gate-width, the *input-current efficiency* can be expressed as

$$\eta_I = C_{gs}/C_{in} = (C_{gs}/W)/[(C_{g\text{-}line}/W)+C_{g\text{-}pad})$$

where $(C_{g\text{-}line}/W)$ is the gate-line capacitance per unit gate-width and $C_{g\text{-}pad}$ is the pad capacitance.

When the gate-width W = 0, $\eta_I = 0$; while when W >> 1, $\eta_I = C_{gs} / C_{g\text{-}lins}$. This calls for larger gate-width to improve extrinsic f_t, which is experimentally confirmed in Fig.4.3-10. However, for gate-widths greater than 150 μm, such improvement begins to saturate, instead, the power gain cutoff frequency starts to experience substantial reduction as the consequence of increased gate-line resistances.

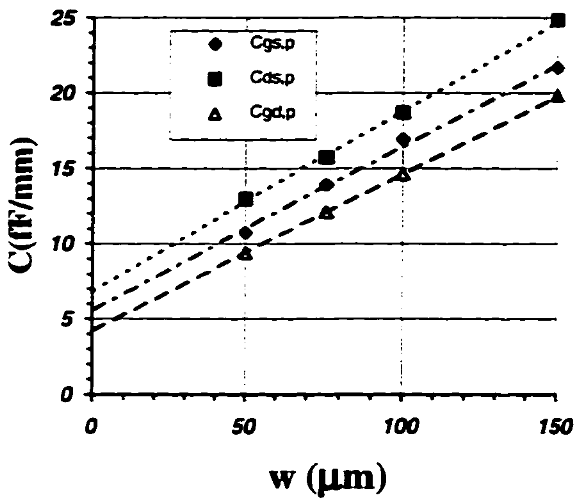


Fig.4.3-9 *A plot of parasitic capacitances vs. gate-width for determining the contributions of the gate-pad and the gate-line.*

A microwave power FET for practical applications should have a raw output power of a few or a few tens of watts. This requires a total gate periphery greater than 1 mm and a multi-finger design has to be employed. For a coherent phase, the width of each finger should be one order less than the wave length. For a low parasitic gate-resistance so that f_{max} maintains high, the gate should also have a limited finger width.

f_{max} has the following dependence on parasitics:

$$f_{max} = \frac{f_t}{2\sqrt{\dfrac{R_g + R_{gs} + R_s}{R_{ds}}}}$$

where R_g is the gate resistance, R_s is the source resistances and R_{gs} is the channel resistance in series with C_{gs}.

For a specific gate-line resistance r_g (Ω/mm) and a finger length of w_g (mm) the lumped-element gate resistance is approximately

$$R_g = (r_g w_g) w_g/3 = (r_g w_g^2)/3 \quad (\Omega\text{-mm})$$

which has been normalized to a unit gate-width (mm).

To ensure the loss in f_{max} to no more than 3 dB, we have $R_g < R_{gs} + R_s$, or

$$w_g < \sqrt{3\frac{R_{gs}+R_s}{r_g}} \quad \text{(mm)}$$

For the current 0.25-µm gatelength AlGaN/GaN HEMTs, r_g is 180 Ω/mm, while each of R_{gs} and R_s is close to 1.2 Ω-mm, yielding

$$w_g < 0.2 \text{ mm (or 200 µm)}$$

Fig.4.3-10 shows the measured f_{max} as a function of gate-width where the devices under test have 2-fingers, or $W = 2w_g$. It is seen that when W = 300 µm, f_{max} reduces to 70.5 %, or by 3 dB, of the original value of 85 GHz. This 3 dB compression point of (300µm)/2 = 150 µm is close to the calculated value of 200 µm. A more serious self heating for wider devices may account for the discrepancy.

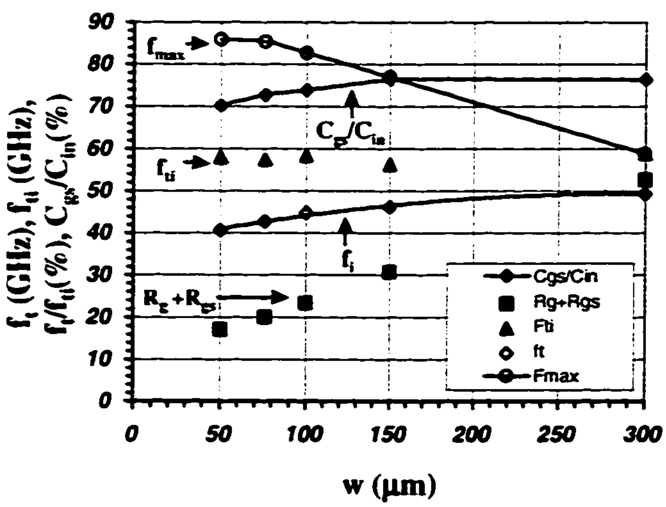


Fig.4.3-10 *Cutoff frequencies and related parameters vs. gate-width.*

4.4 Summary

The use of a high Al-content AlGaN layer was proposed to increase the equivalent figures of merit of the AlGaN/GaN MODFET structure, based on the combined advantages of: 1) the high breakdown field in the AlGaN barrier and the chemical inertness of the Schottky gate, 2) the high charge-mobility product due to a large conduction band discontinuity, 3) the high electron velocity in the GaN channel. It has been shown that the room temperature mobility has little degradation with increasing Al-content up to 50%. 0.7-μm gatelength $Al_{0.5}Ga_{0.5}N$/GaN MODFETs exhibited an ultra-high three-terminal current-voltage product > 200 VA/mm, which is unmatched by FETs in other material systems to date. CW power densities of 2.84 and 2.57 W/mm at 8 and 10 GHz, respectively, were also achieved with these devices by optical lithography. Such power densities in X band measured on sapphire substrates without thermal management were already state-of-the-art for a solid-state FET. Subsequent gate-length shrinkage to 0.25 μm resulted in a current gain cutoff frequency of 52 GHz, the highest for a wide band-gap FET, and a CW output power density greater than 3 W/mm at 18 GHz, the highest for any microwave FET in K band to date.

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Chapter 5
Operation Analysis

In this chapter, extraction of device circuit-model elements is used to analyze the operation mode of AlGaN/GaN HEMTs. Findings with the analysis not only explain the dependence of breakdown voltages on gate-drain spacing but also result in a calculated saturation velocity in closer agreement with prediction by Monte Carlo simulation.

5.1 Circuit-model element extraction

Investigation of current-gain cutoff frequency f_t or delay time τ as a function of drain bias voltage is a powerful tool to understand the operation of an FET. Due to the lower mobility, less mature techniques in ohmic contacts and the un-availability of gate-recess etch, the parasitic resistances of the AlGaN/GaN HEMTs are higher than conventional HEMTs and can mask the nuance of the f_t behavior of the active device which may be of essential importance. For this reason, analysis of the AlGaN/GaN devices should be focused on the intrinsic f_t (f_{ti}) instead of the measured f_t. This necessitates extraction of circuit-model elements.

The HEMT circuit-model and the methods of extracting the model elements were presented in [i]. Fig. 5.1-1 shows this 17-element model which includes the intrinsic FET (in the slashed-line box), resistive access parasitics (R_g, R_s, R_d), series parasitic inductances (L_g, L_s, L_d) and shunt parasitic capacitances (C_{gsp}, C_{gdp}, C_{dsp}). C_{gsp} and C_{gdp} include both the capacitances of the gate pad and the gate line. Although the series inductances (L_g, L_s, L_d) are necessary for the completeness of the model, they are normally too small (15 ~ 30 pH) to have appreciable effect for a 2-finger FET below 100 GHz.

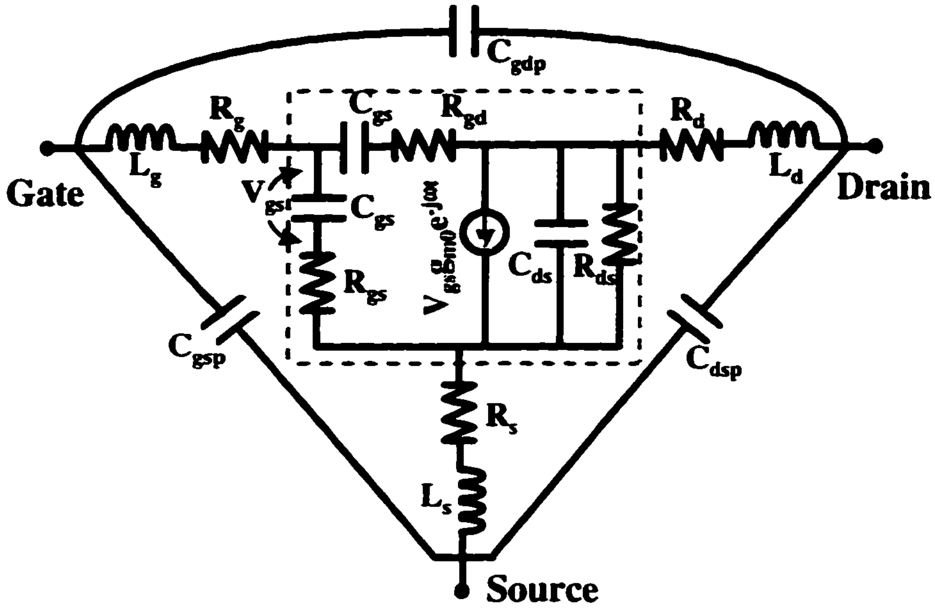


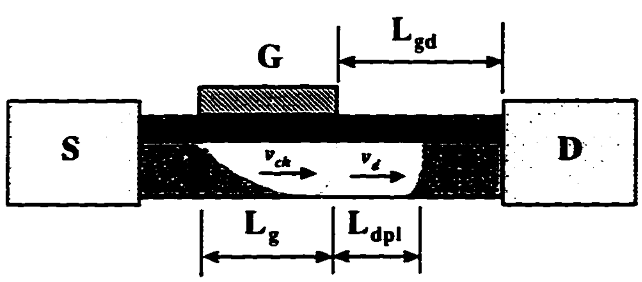
Fig. 5.1-1 *The 17-element circuit model for a HEMT.*

A convenient procedure for the model-element extraction is briefly described below. First, the gate of the FET is deeply reverse biased so that the whole intrinsic device is completely turned off or open. The parasitic capacitances which are the only participating elements in this case are measured. Second, the gate diode of the FET is fully turned on so that the intrinsic device is equivalently shorted. The S-parameters are taken; the parasitic capacitances are stripped off using the result of the fist measurement and the series inductances and resistances are determined. Third, the FET is biased in an active mode. The S-parameters for the whole extrinsic FET are measured and then de-embedded from all parasitics found in the first and the second steps. Each intrinsic element is then finally calculated with the Y-parameters of the intrinsic FET.

It is important to note that the source and drain resistances (R_s & R_d) measured in this manner (also called "the cold FET method") are room temperature resistances. For conventional FETs operating in an active mode with a DC power density below 1 W/mm, their values can be treated as constant. For example, a normal GaAs MESFET has a thermal resistance of 45 °C/(W/mm). With 1 W/mm heating power the channel temperature rises from the room temperature of 300 K to 345 K. The dependence of mobility on temperature can be assumed as $\mu \sim T^{-1.5}$ which yields an increase in access resistance by $[(345/300)^{1.5} - 1] = 10\ \%$. The ohmic contact resistance is usually less sensitive to temperature, rendering a total change in resistance well below 10 %. AlGaN/GaN HEMTs under investigation, however, can have a power consumption of 4 ~ 6 W/mm. A resistance-rise by a factor of 2 ~3 is possible which cannot be determined accurately from S-parameters. This can lead to un-acceptable differences between the actual intrinsic parameters and the derived ones, or *apparent parameters*. However, the major point of interests here is to find out the intrinsic current-gain cutoff frequency, which is determined as $f_{ti} = g_{m0}/[2\pi\ (C_{gs}+C_{gd})]$. When the drain voltage bias is high, which is normally true in the case of high power consumption, C_{gd} is very small and the expression is simplified to $f_{ti} = g_{m0}/(2\pi\ C_{gs})$. If an increase in source resistance by ΔR_s due to the temperature-rise is assumed, it can be derived by nodal analysis that the *apparent transconductance* $g_{m0.ap} = g_{m0}/(1+g_{m0}\Delta R_s)$ [ii]. In the same way the *apparent source-capacitance* $C_{gs.ap} = C_{gs}/(1+g_{m0}\Delta R_s)$. Substitution into the expression for the intrinsic current-gain cut-off frequency yields $f_{ti} = g_{m0.ap}/(2\pi\ C_{gs.ap})$. That is, the derived f_{ti} is independent of the increase in R_s, or temperature.

5.2 Drain extension and saturation velocity

As seen in Fig.5.2-1, the total transit time in an FET can be expressed as $\tau = L_g/v_{ch} + L_{dpl}/2v_d$, where L_g is the gate-length, v_{ch} is the effective electron velocity in the channel, L_{dpl} is the gate-drain depletion length and v_d is the electron velocity in the depletion region. The factor of 2 is due to the imaging effect in the drain neutral region [iii]. Physically, f_t is the inverse of the transit time: $f_t = (2\pi\tau)^{-1}$. Fig.5.2-2 shows the f_t-V_{ds} curve for a typical GaAs MESFET. As drain bias increases from zero, electron velocity in the transistor channel increases so does f_t. On reaching the knee voltage, due to either velocity saturation or pinch-off under the drain side of the channel, f_t approaches its peak. Further increasing drain bias above the knee leads to partial depletion of the access region on the drain side of the gate. This reduces the gate-drain capacitance but increases the transit time by adding drain delay. As a compromise, f_t marginally increases to reach its maximum and then starts to decrease until breaking-down of the device. Similar dependence was found for conventional FETs of different semiconductors. It is important to note that, unless the gate-drain spacing L_{gd} is totally depleted, it is L_{dpl}, instead of L_{gd}, that determines the drain delay.



$$\tau = L_g / v_{ch} + L_{dpl} / 2v_d$$
$$= 1/(2\pi f_t)$$

Fig.5.2-1 *Schematics for calculating delay time in an FET.*

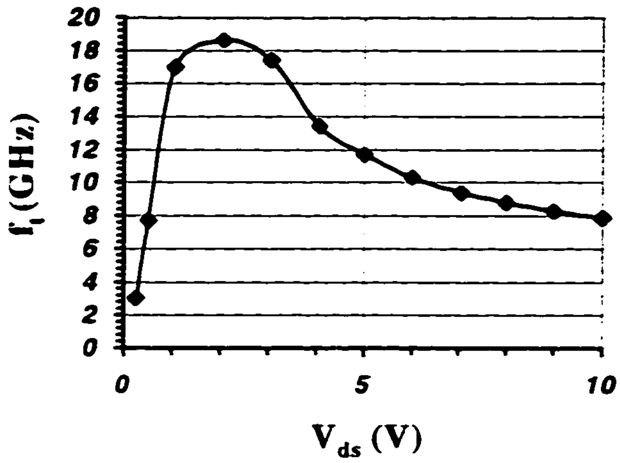


Fig.5.2-2 f_t *vs. drain bias for a 1-μm gate-length GaAs MESFET* [iv].

The relatively low mobility of GaN necessitates a high bias for velocity saturation while the high bias can lead to a long drain-extension. Fig.5.2-3 shows the intrinsic current-gain cutoff frequencies f_{ti}'s and delay times τ's of three $Al_{0.35}Ga_{0.65}N$/GaN devices against drain bias. The gate-lengths were 1 μm, while gate-drain spacings were 1, 2 and 3 μm, respectively. It is seen that addition of each 1 μm gate-drain spacing results in an increase in peak delay (at point ***B***) by approximately an equal amount, which is a clear evidence of complete depletion of the gate-drain region. This agrees well with the previous observation that breakdown voltages highly depended on gate-drain spacing, since with a limited breakdown field, the longer the extension the higher the sustainable voltage. The decrease in delay times after their peaks can be explained by the fact that further drain extension is no longer available after reaching the drain contact. Therefore electric field has to increase to accommodate further increase in bias voltage which leads to an increase in electron velocity in the channel.

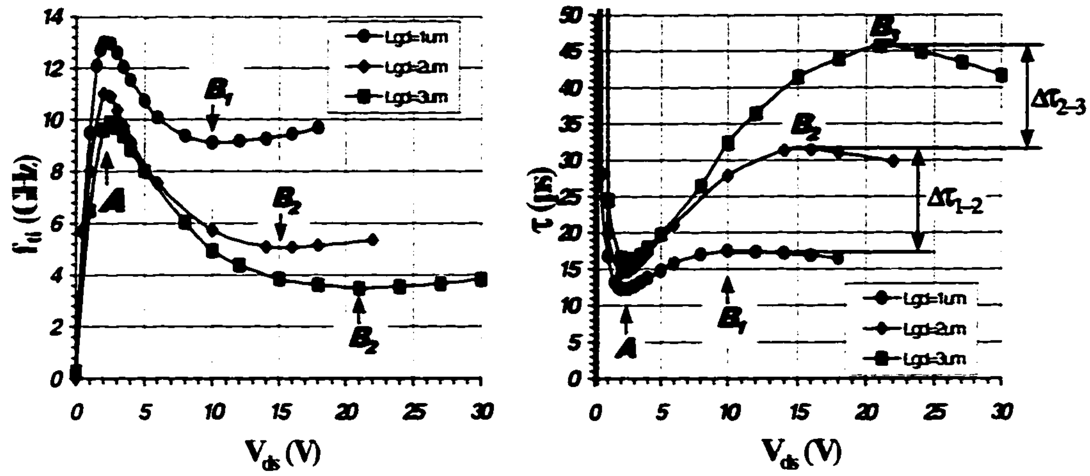


Fig.5.2-3 *Intrinsic current-gain cutoff frequencies (f_{ti}'s) and delay times (τ's) vs. drain bias voltage for three 1-μm gatelength $Al_{0.35}Ga_{0.65}N/GaN$ HEMTs with gate-drain separations of 1, 2 and 3 μm.*

Velocity saturation is more likely with shorter gatelength devices. For this reason, estimation of electron saturation velocity v_s was performed with 0.25 μm gate-length devices as shown in Fig.5.2-4 using experimental data at point ***C***. Assuming $v_{ch} = v_d = v_s$, we have $v_s = (L_g + L_{gd}/2)/\tau$. This yields v_s's of 1.77×10^7 and 1.75×10^7cm/s for the devices with L_{gd} of 0.7 and 1.5 μm respectively. The average effective saturation velocity of 1.76×10^7 cm/s is the first experimental result in good agreement with the peak value of 2.7×10^7cm/s and the high-field saturation value of 1.5×10^7cm/s by Monte Carlo simulation [v] as seen in Fig.5.2-5. The previous calculated saturation velocity of 1.1×10^7cm in Chapter 4 (p87) by the conventional gatelength-variation method is believed an under-estimate since the drain extension was assumed zero.

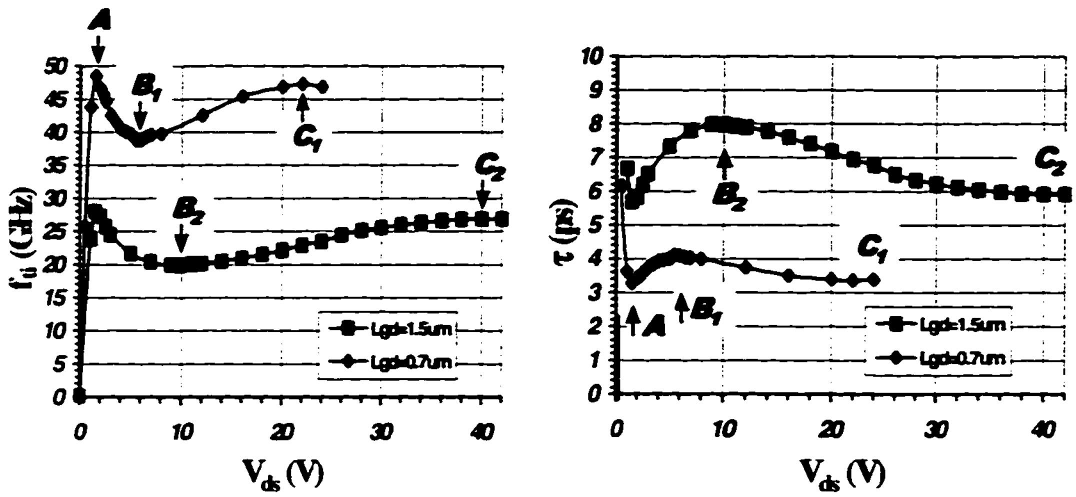


Fig.5.2-4 *Intrinsic current-gain cutoff frequencies and delay times vs. drain bias for two 0.25-μm gatelength* $Al_{0.175}Ga_{0.825}N/GaN$ *HEMTs with gate-drain separations of 0.7 and 1.7 μm.*

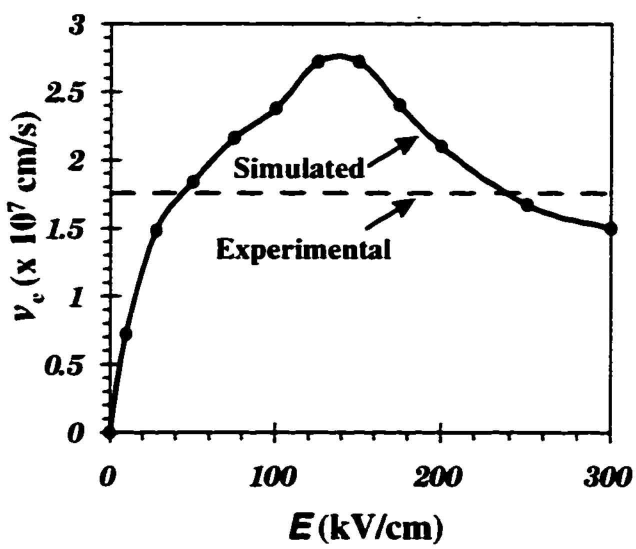


Fig.5.2-5 *Comparison of the experimental effective-saturation velocity in this work and the Monte Carlo simulation result by Gelmont et al* [V].

5.3 A suggested operation mechanism

The AlGaN layers of the GaN-channel HEMTs usually have a doping density greater than 5×10^{18} cm^{-3}. Such a large drain-depletion length of ~ 1 μm with a bias voltage of ~ 10 V is normally impossible. The donor ions in the AlGaN layer should be partially compensated or naturalized by slow electrons of large population. Also, there should be states or a defect band in (or under) the AlGaN for the electrons mentioned above. Electron transport in the defect band can be realized through hoping. Finally, there should be a source and a path for electrons to be injected to this defect band. This can be realized by electron tunneling from the metal gate to (or through) the AlGaN layer. If these hypotheses are true, the operation process of the above AlGaN/GaN HEMTs (i.e. devices with dual f_t peaks) can then be explained as below.

As the drain bias increases from zero, electric field increases, so does the channel velocity. The peak electric field is at the drain side of the gate/AlGaN interface. When it reaches a magnitude ($\boldsymbol{E_c}$) for a sufficient number of electrons to tunnel to the defect band in (or under) the AlGaN layer, the donor ions nearby are effectively compensated (provided that the electron transport in the defect band is very slow). This potentially reduces the electric field, but the reduction in electric field leads to a reduction in electron-injection, resulting in a smaller compensation of the positive ions hence a backup of the electric field. As a balance of this feedback mechanism, the electric field on the drain side of the gate should remain relatively constant. In another ward, the electric field is pinned. The onset of such an electric-field pinning is around point ***A*** in the f_{ti}-V_{ds} curves (Fig.5.2-3 and Fig. 5.2-4), and is before a sufficient velocity saturation in the channel for the FETs under study. Further increasing drain voltage cannot increase the channel velocity. Instead, the drain depletion-length has to extend to accommodate the increased voltage, which leads to a direct increase in delay time, hence a reduction in f_{ti}. This continues until the depletion of the full length of L_{gd} at the turning point ***B***. After that, no more drain-extension is possible to sustain the electric-field pinning, therefore the electric field has to increase for a second time with increasing voltage. As a result, the electron velocity in the channel resumes increasing until it reaches saturation at point ***C***.

At the onset of electron injection from the gate to the defect band, there should be an increase in gate current. Experimentally, such a current increase is confirmed as seen in Fig.5.3-1.

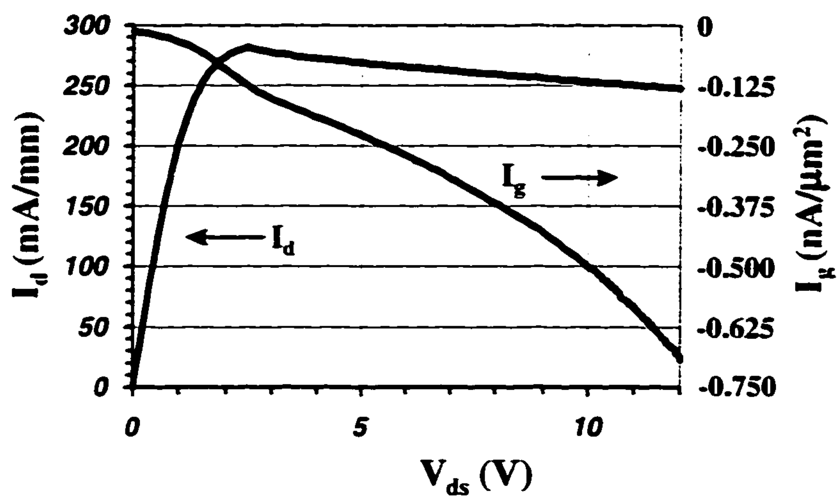


Fig.5.3-1 *Drain and gate current vs. drain voltage for the device in Fig.5.2-3 with* $L_{gd} = 1\ \mu m$.

If the proposed mechanism is true, the f_{ti}-V_{ds} dependence should largely depends on the properties of the AlGaN layer (for example, Al mole-fraction) and the shottky gate barrier height. This is again confirmed experimentally. Fig.5.3-2a shows the drain bias dependence for a 0.25-µm gate-length $Al_{0.175}Ga_{0.825}N$/GaN HEMT, exhibiting two f_t peaks; while Fig.5.3-2b is the same plot for a 0.25-µm gate-length $Al_{0.5}Ga_{0.5}N$/GaN HEMT, showing only one f_t peak. Similar bifurcation was observed for 0.9 ~ 1 µm gate-length AlGaN/GaN HEMTs as seen in Fig.5.3-3a and Fig.5.3-3b, where an $Al_{0.35}Ga_{0.65}N$/GaN device with a gate-barrier of 1.2 V is a dual-f_t-peak FET, while another one with a gate-barrier of 1.7 V is a single-f_t-peak FET.

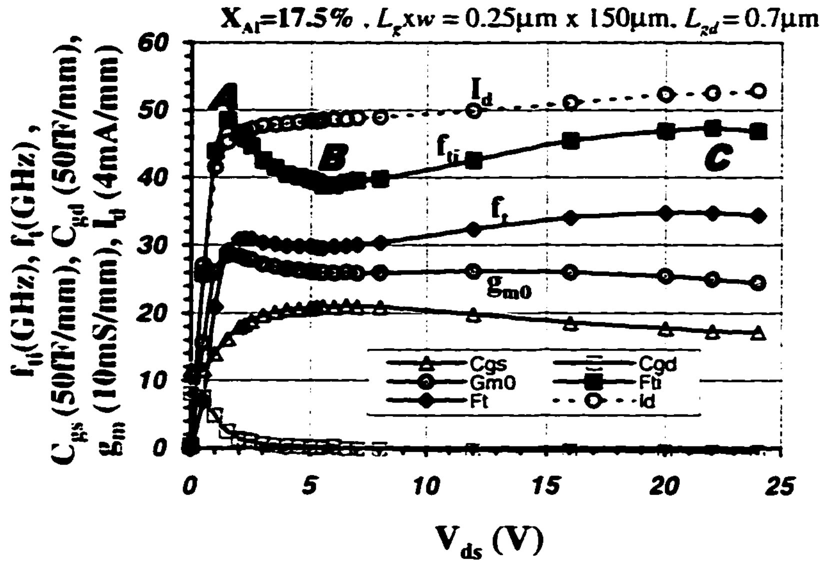


Fig.5.3-2a. *f_{ti} and relevant parameters vs. V_{ds} for a 0.25-µm gate-length $Al_{0.175}Ga_{0.825}N/GaN$ HEMT with a gate Shottky barrier ~1.2 V, a dual-f_t-peak FET.*

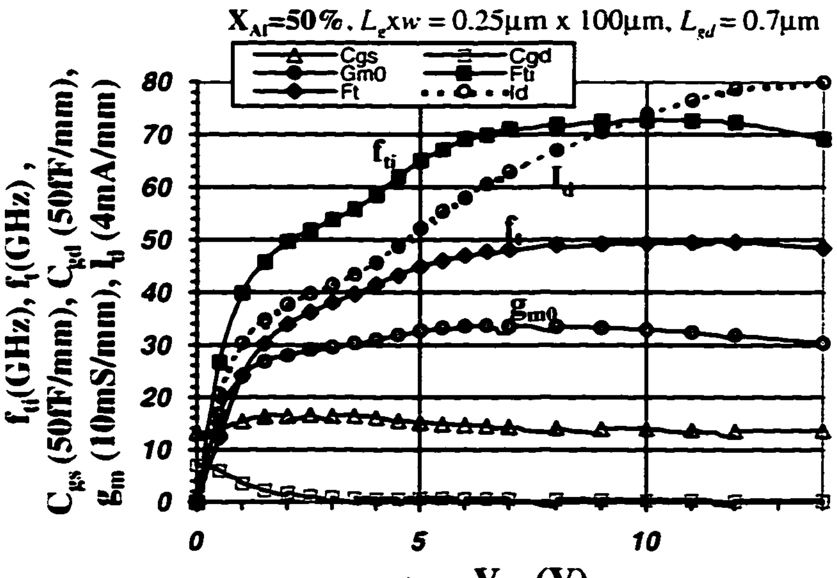


Fig.5.3-2b *f_{ti} and relevant parameters vs. V_{ds} for a 0.25-µm gate-length $Al_{0.5}Ga_{0.5}N/GaN$ HEMT with a gate Shottky barrier ~1.9 V, a single-f_t-peak FET.*

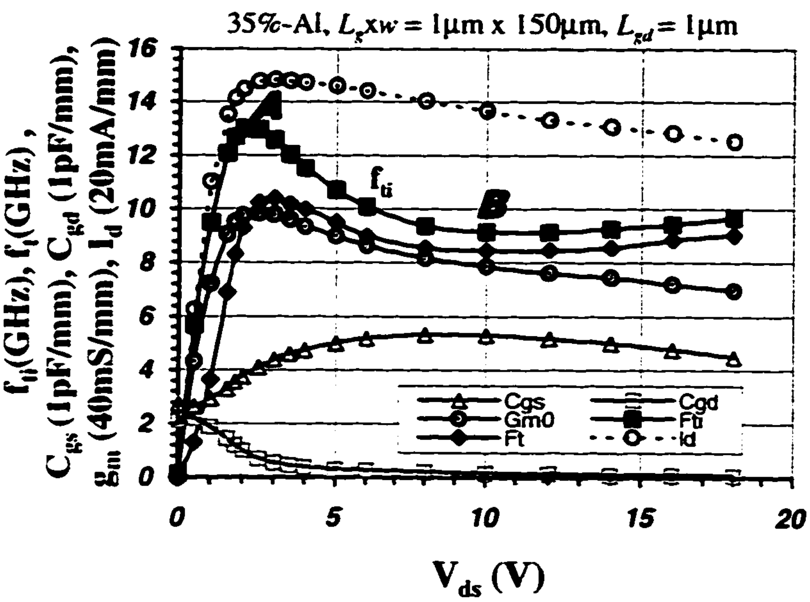


Fig.5.3-3a. *f_{ti} and relevant parameters vs. V_{ds} for a 1-μm-gatelength $Al_{0.35}Ga_{0.65}N$/GaN HEMT with a gate barrier of 1.2 V, a dual-f_t-peak FET.*

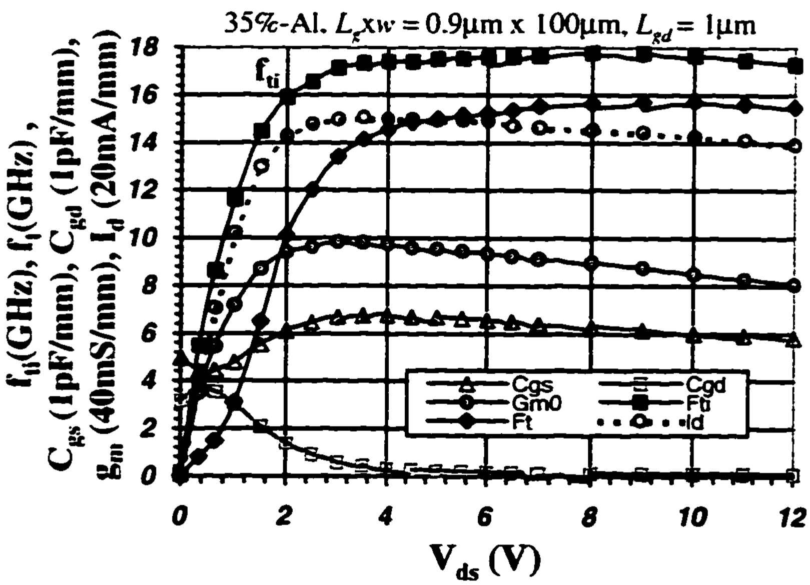


Fig.5.3-3b. *f_{ti} and relevant parameters vs. V_{ds} for a 0.9-μm-gatelength $Al_{0.5}Ga_{0.5}N$/GaN HEMT with a gate barrier of 1.7 V, a single-f_t-peak FET.*

The above proposed operation mechanism for the dual-f_t-peak devices is based on an important condition: the electric-field pinning on the drain side of the gate occurs before a sufficient velocity saturation in the channel. When this condition is not satisfied, the FET is a single-f_t-peak device (Fig.5.3-2b and Fig.5.3-3b). The higher gate barriers of such devices require a higher electric field for tunneling, which in turn leads to a channel velocity closer to saturation before a significant drain extension. Fig.5.3-4 is the f_{ti}-V_{ds} curves for two single-f_t-peak $Al_{0.5}Ga_{0.5}N/GaN$ HEMTs with a gate-length of 0.3 μm and gate-drain separations of 0.7 and 1.5 μm, showing little dependence of f_{ti} on L_{gd} (i.e. the drain extension is not completed at least up to 22 V). Such a device is preferred for its higher peak value of the f_t-gatelength product and, possibly, a higher RF current swing.

Experimentally, the breakdown voltages for the single-f_{ti}-peak devices also highly depend on gate-drain spacing, indicating that the total L_{gd} is also finally depleted, but at a much higher voltage.

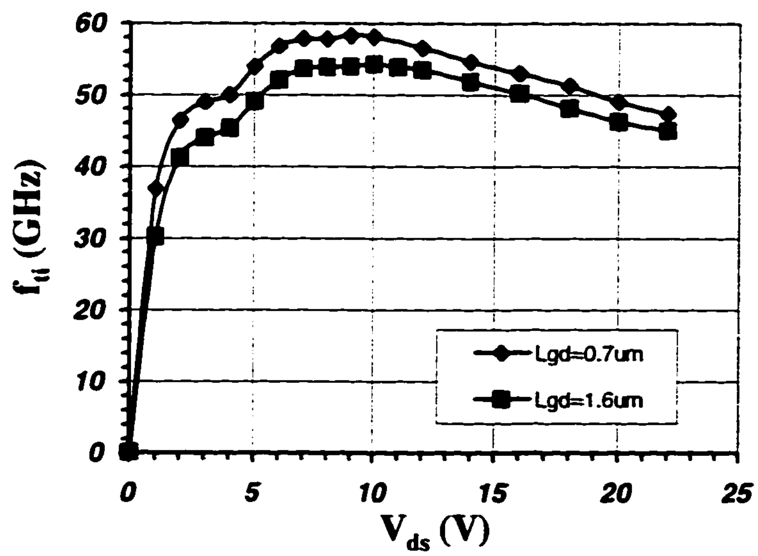


Fig.5.3-4 *Intrinsic current-gain cutoff frequencies vs. drain bias for two 0.3-μm gatelength $Al_{0.5}Ga_{0.5}N/GaN$ HEMTs with gate-drain separations of 0.7 and 1.6μm, showing little dependence on the gate-drain spacing.*

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Chapter 6

Conclusion and Suggested Future Work

6.1 Conclusion

The research for high power microwave AlGaN/GaN HEMTs started with GaN processing techniques, proceeded to the development of a basic $Al_{0.15}Ga_{0.85}N$/GaN HEMTs with satisfactory characteristics, stepped up to high Al-content AlGaN/GaN HEMTs for ultra-high performance, and ended with an analysis of the device operation mechanism. Research findings are summarized below.

Processing technique

A transfer ohmic-contact resistance of 0.4 ~ 0.6 Ω-mm for normal AlGaN/GaN HEMTs were routinely achieved with Ti/Al/Ni/Au (200Å/2000Å/400Å/500Å) annealed at 850 ~ 900 °C. Partial RIE etching of the AlGaN layer was found necessary for realization of such a low contact resistance.

n^+ regrown contacts on AlGaN/GaN HEMTs with UID n-channels yielded a slightly better contact resistance of 0.4 ~ 0.5 Ω-mm with a lower annealing temperature of 670 °C. A 4000 ~ 5000 Å thick SiO_2 layer by e-beam evaporation and lift-off was served as the regrowth mask which was not destroyed in the regrowth condition of 1050 °C for 6 min. The n^+ ohmic edge was as smooth as that of the SiO_2 mask, which potentially facilitates fabrication of deep submicron gate-length devices. The trade-off of the n^+ regrowth method is its processing complexity.

Au (3000 ~ 5000 Å) as a gate metal provided a high Schottky barrier on AlGaN or GaN, but its adhesion was poor. Ni/Au (200 Å / 4000 Å) showed both good adhesion and a high Schottky barrier, therefore is a preferred choice of gate metallisation.

Mesa isolation by Cl_2 RIE was experimentally proved reliable. Gate-drain breakdown voltage up to 340 V with a total leakage current less than 1 nA/mm was achieved with such a simple isolation scheme.

Device and performance

$Al_{0.15}Ga_{0.85}N$/GaN HEMT structures with GaN layers grown at atmospheric pressure (AP) showed superior Hall mobilities up to 1500 cm^2/Vs at room temperature, along with high carrier densities of 7 ~ 8 x 10^{12} cm^{-2}. Fabricated devices showed very high breakdown voltages of 220 ~ 340 V with 3 μm gate-drain spacing. A CW power density of 1.1 W/mm at 2 GHz was also measured which was the first successful demonstration of microwave power performance for a GaN-based FET in literature. However, since the AP GaN was usually n type, the poor quality at the GaN/sapphire interface led to poor pinch-off characteristics.

GaN layers grown at low pressure (LP) showed insulating nature, presumably due to the high carbon incorporation which resulted in a high density of deep acceptors and in turn compensation of the un-intentional n-type dopants. Both a low mobility (500 ~ 600 cm^2/Vs) and a low carrier density (4 ~ 5 x 10^{12} cm^{-2}) were found in AlGaN/GaN structures with LP GaN layers which were attributed to both the poorer structural quality of the LP GaN and the over-compensation of the native n-type doping. The use of a Bi-layer structure with a thin LP GaN layer (1000 Å) and a thick AP GaN layer (> 1 μm) maintained the insulating nature and improved both mobility (~ 1200 cm^2/Vs) and carrier density (~ 7 x 10^{12} cm^{-2}). This led to a basic $Al_{0.15}Ga_{0.85}N$/GaN MEMT with satisfactory specifications in all major aspects including a fairly high current density greater than 500 mA/mm, transconductance of 160 mS/mm, excellent pinch-off characteristics, high breakdown voltage of 220 V with 3-μm gate-drain spacing, reasonably high current-gain and power-gain cutoff frequencies of 9.6 GHz and 27 GHz with 1 μm gate-length. The current density, transconductance and cutoff frequencies were close to those of a high-performance GaAs MESFET while the breakdown voltages were more than 10 time higher. A CW power density of 1.57 W/mm at 4 GHz was measured un-cooled on the thermally resistive sapphire substrate, which was about 50 % higher than generally achieved with GaAs MESFETs.

First-order analyses focusing on further improvement in both power ability and switching speed led to a pursuit in high Al-content AlGaN/GaN devices. Investigation of electrical quality of Al-rich HEMTs pointed out a relatively constant room-temperature mobility with increasing Al mole-fraction up to 50 %. Carrier density increased with increasing Al mole-fraction until 35 % and maintained high (1.2×10^{13} cm^{-2}) up to 50 %. Fabricated Al-rich devices showed a higher intrinsic f_t-gatelength product of 15 GHz-μm compared with the 11 GHz-μm with the $Al_{0.15}Ga_{0.85}N$/GaN HEMT. A general trend of an increased IV product per unit gate-width with increasing Al-content was observed. A three-terminal IV product greater than 200 VA/mm was obtained on devices with Al-contents greater than 35 %, which was not seen with FETs in any other material system. The measured output power density also monotonicly increased with Al-content. In particular, a ***CW*** power density of 2.6 ~ 2.8 W/mm at 8 ~ 10 GHz was achieved with 0.7-μm gatelength $Al_{0.5}Ga_{0.5}N$/GaN HEMTs on sapphire substrates without thermal management. The only comparable performance was a ***pulsed*** power density of 3.3 W/mm at 10 GHz with a 0.5-μm gatelength SiC MESFET [i], which was achieved almost in the same time (early 1997). Subsequent shrinkage of gatelength to 0.25 μm with the $Al_{0.5}Ga_{0.5}N$/GaN HEMTs resulted in a record current-gain cutoff frequency of 52 GHz for a wide band-gap FET. The power density, also ***CW***, was improved to greater than 3 W/mm at 18 GHz, which is the best in K band for any microwave FET to date.

Table 6.1 summarizes the advances of GaN-channel microwave FETs in literature since 1995, while Fig.6.1 highlights the progress in power density and operation frequency in recent years for both GaN-based and SiC-based microwave FETs. It is seen that since its first demonstration of microwave performance in mid-1996 [vii], progression of the GaN-channel HEMTs has been extremely aggressive and has started to overtake that of the SiC MESFETs.

Device operation mechanism

Extraction of device circuit-model elements was used to analyze the operation mode of AlGaN/GaN HEMTs. Investigation of the extracted delay time as a function of drain bias revealed complete depletion of the gate-drain region. This not only explained why the breakdown voltages highly depended on gate-drain spacing but also resulted in an estimated effective saturation velocity of 1.76×10^7 cm/s for electrons in the GaN-channel, which is the first experimental value in good agreement with the peak velocity of 2.7×10^7 cm/s and the high-field saturation of 1.5×10^7 cm/s by Monte Carlo simulation [ii].

Table 6.1 *Progress of GaN-channel microwave FETs in literature since our research was started in 1995*

Reference	Structure	Gate-length (μm)	f_t / f_{max} (GHz/ GHz)	I_{max} x V_{max} (A/mmxV =VA/mm)	P_{out} @ f (W/mm @ GHz)	Subm. Date / Pub. Date
A. Ozgur et al.[iii]	AlGaN/GaN MODFET	3	---	0.3x35 =10.5	---	06/95 08/95
Khan et al.[iv]	$Al_{0.15}Ga_{0.85}N$/ GaN DCHFET	1	18 / ---	---	---	11/95 07/96
Khan et al.[v]	$Al_{0.15}Ga_{0.85}N$/ GaN DCHFET	0.25	36 / 71	---	---	11/95 02/96
Z. Fan et al.[vi]	AlGaN/GaN MODFET	2	---	0.55x20 0 =110	---	05/96 08/96
Wu et al.[vii]	$Al_{0.15}Ga_{0.85}N$/ GaN MODFET	1	6.5/15	0.33x 340 =110	***1.1 @ 2***	05/96 09/96
Khan et al.[viii]	$Al_{0.15}Ga_{0.85}N$/ GaN DCHFET	0.15 ~ 0.25	30/97	0.6 x30 =18	***0.27 @ 10 0.14 @ 15***	07/96 12/96
Wu et al.[ix]	$Al_{0.15}Ga_{0.85}N$/ GaN MODFET	1	9.6/27	0.6 x 220 = 130	***1.57 @ 4***	11/96 06/97
O. Aktas et al.[x]	$Al_{0.15}Ga_{0.85}N$/ GaN IMODFET	2	6/15	0.8 x ---	***1.5 @ 4***	11/96 06/97
Wu et al.[xi]	$Al_{0.15}Ga_{0.85}N$/ GaN MODFET	0.2 ~ 0.3	30~50/ 70~92	0.8 x 60 = 50	***1.70 @ 10***	03/97 09/97
Wu et al.[xii]	$Al_{0.5}Ga_{0.5}N$/ GaN MODFET	0.7	17.5/ 40	1 x 280 = 280	***2.6~2.8 @ 8 ~ 10***	06/97 ---
Wu et al.[xiii]	$Al_{0.5}Ga_{0.5}N$/ GaN MODFET	0.25 ~ 0.3	52/82	1.1 x 70 = 80	***3~3.3 @ 18***	07/97 ---

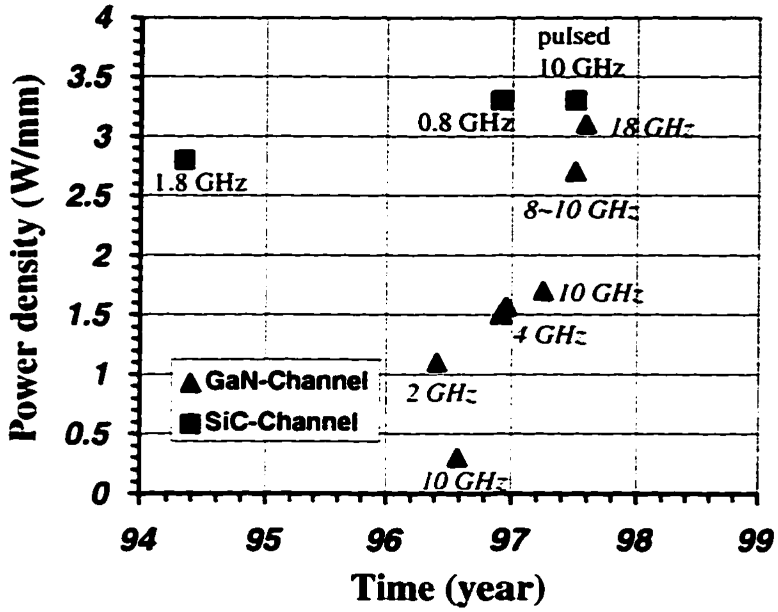

Fig.6.1 *Progress in power density for GaN-based (listed in Table 6.1) and SiC-based (mainly SiC MESFETs* [xiv, xv, i]*) microwave FETs. The time is chosen as the date of submission for publication or the date presented in a conference. All devices operated in CW mode, or else specified.*

6.2 Suggested future work

This thesis represents the first intensive attempt in exploring the microwave power ability of GaN-channel HEMTs. Although excellent performances represented by a power density greater than 3 W/mm at 18 GHz have been achieved, the potential of the AlGaN/GaN HEMTs is believed far from exhausted. Also, many questions are left unanswered. Important aspects of future work are suggested below.

1. Investigation of the conduction-band discontinuity and the piezo-electric dipole strength as a function of the Al mole-fraction. Beware that the latter makes the measurement of the former difficult. The research results will facilitate future device design.

2. AlGaN/GaN HEMTs with Al-content greater than 50 %. It has been shown that better power performance was achieved with higher Al-content. The impact of an Al-content greater than 50 % is worthy of investigation. Initial results showed that $Al_{0.7}Ga_{0.3}N$/GaN HEMTs had very low sheet charge density possibly due to the low doping efficiency of the $Al_{0.7}Ga_{0.3}N$ by Si. Realization of n-type doping in AlN through Ge was reported [xvi] [xvii]. This potentially makes AlN/GaN HEMTs possible.

3. Thermal management and large-area devices. Performance of present AlGaN/GaN HEMTs are believed thermally limited as the thermal conductivity of the sapphire substrate is very poor (0.37 W/cm°C at room temperature). 2D thermal simulation showed that reduction of channel temperature by a factor of 2 ~ 3 can be realized with flip-chip bounding, and by a factor of 8 is possible by using an SiC substrate. Only when the thermal problem is solved are practical large-area devices realizable.

4. Device reliability. Performance degradation as a function of time was observed on present devices at bias conditions yielding the maximum power densities. This has been attributed to self-heating. Long term reliability tests or life-time tests with a successful thermal management are necessary before practical circuit implementation. These should include the stability of the Schottky gate and ohmic contacts.

5. Study of the mechanism for drain extension. The suggested electron injection form the metal gate to the AlGaN layer and its compensation of the positive ions in the AlGaN layer need further verification. Their

effect on large-signal swing should also be investigated with a microwave transition analyzer.

6. Microwave operation at cryogenic temperatures. The largely improved thermal conductivity and reduced base temperature will allow a test of the ultimate performances of the AlGaN/GaN HEMTs.

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Appendix 1

Process Notes

A typical process flow for fabrication of AlGaN/GaN HEMTs is presented below.

1. Source and drain ohmic contacts (Mask level: Source/drain)
   i. Wafer cleaning by ACE and ISO.
   ii. Oven bake at 120 °C for 3 -5 min.
   iii. Spin 5214E at 6 krpm for 30 s.
   iv. Soft bake at 95 °C on hot plate for 1 min.
   v. Remove resist edge bead.
   vi. Expose for 15 s with UV filter at 4.5 mW/cm^2.
   vii. Post-expose bake at 108 °C on hot plate for 1 min.
   viii. Flood expose for 1 min.
   ix. Develop in 1:5.7 AZ-400K:DI-water for 30 - 40 s.
   x. Cl_2 RIE with flow of 5 sccm, pressure of 10 mTorr, RF power of 200 W and DC bias of 400 V for 5 s (etching depth ~ 100 Å).
   xi. E-beam evaporation of Ti/Al/Ni/Au (200Å/2500Å/400Å/5000Å).
   xii. Lift-off by ACE and clean by ISO.
   xiii. RTA anneal at 900 °C for 20 ~ 30 s.
2. SiO_2 isolation of gate-pad (Mask level: Gate-pad isolation)
   i. Wafer cleaning by ACE and ISO if necessary.
   ii. Oven bake at 120 °C for 3 -5 min.
   iii. Spin 5214E at 6 krpm for 30 s.
   iv. Soft bake at 95 °C on hot plate for 1 min.
   v. Remove resist edge bead.
   vi. Expose for 15 s with UV filter at 4.5 mW/cm^2.
   vii. Post-expose bake at 108 °C on hot plate for 1 min.
   viii. Flood expose for 1 min.
   ix. Develop in 1:5.7 AZ-400K:DI-water for 30 - 40 s.

x. Cl_2 RIE with flow of 5 sccm, pressure of 10 mTorr, RF power of 200 W and DC bias of 400 V for 35 s (etching depth ~ 700 Å).
xi. E-beam evaporation of SiO_2 (1500 Å).
xii. Lift-off by ACE and clean by ISO.

3. Gate-metallisation (Mask level: Gate)
    i. Oven bake at 120 °C for 3 -5 min.
    ii. Spin 5214E at 6 krpm for 30 s.
    iii. Soft bake at 95 °C on hot plate for 1 min.
    iv. Remove resist edge bead.
    v. Expose for 20 s with UV filter at 4.5 mW/cm^2.
    vi. Post-expose bake at 108 °C on hot plate for 1 min.
    vii. Flood expose for 1 min.
    viii. Develop in 1:5.7 AZ-400K:DI-water for 30 - 60 s.
    ix. Oxygen plasma ash at 300 mTorr, 100 W, 15 s.
    x. Surface cleaning by 1:8 HCL:Di-water for 20 s.
    xi. E-beam evaporation of Ni/Au/Ni (200Å/4000Å/500Å).
    xii. Lift-off by ACE and clean by ISO.
4. Mesa isolation (Mask level: Mesa)
    i. Oven bake at 120 °C for 3 -5 min.
    ii. Spin 4110E at 6 krpm for 30 s.
    iii. Soft bake at 95 °C on hot plate for 1 min.
    iv. Remove resist edge bead.
    v. Expose for 8 s with at 7.5 mW/cm^2.
    vi. Develop in 1:4 AZ-400K:DI-water for 30 - 60 s.
    vii. Post-expose bake at 105 °C on hot plate for 1 min.
    viii. Cl_2 RIE with flow of 5 sccm, pressure of 10 mTorr, RF power of 250 W and DC bias of 450 V for 2.5 min (etching depth ~ 3700 Å).
    ix. Oxygen plasma ash at 300 mTorr, 100 W, 30s.
    x. Resist removal by ACE and clean by ISO.
    xi. Done and ready for IV test ☺.

Appendix 2

Bias Dependent Cutoff Frequencies and Circuit-model Parameters

Bias dependent cutoff frequencies and relevant parameters of 0.7-µm and 0.25- µm gatelength $Al_{0.5}Ga_{0.5}N/GaN$ HEMTs described in Chapter 4, which produced the best power densities, are presented here. The circuit model used is shown in Fig.5.1-1 in page 95. Symbols used are: f_t, extrinsic current-gain cutoff frequency; f_{max}, power-gain cutoff frequency; f_{ti}, intrinsic current-gain cutoff frequency; g_{m0}, intrinsic transconductance; C_{gs}: gate-source capacitance; C_{gd}: gate-drain capacitance; R_g: gate-line resistance; R_{gs}: channel resistance in series with C_{gs}; R_{ds}: source-drain output resistance. Measured extrinsic source and drain resistance R_s and R_g are also given. Please refer to Fig.4.3-9 in page 90 for extrinsic parasitic capacitances.

Beware that the measurements were performed un-cooled on sapphire substrates. Self-heating effectively reduces extracted values of C_{gs} and g_{m0} as described in page 96.

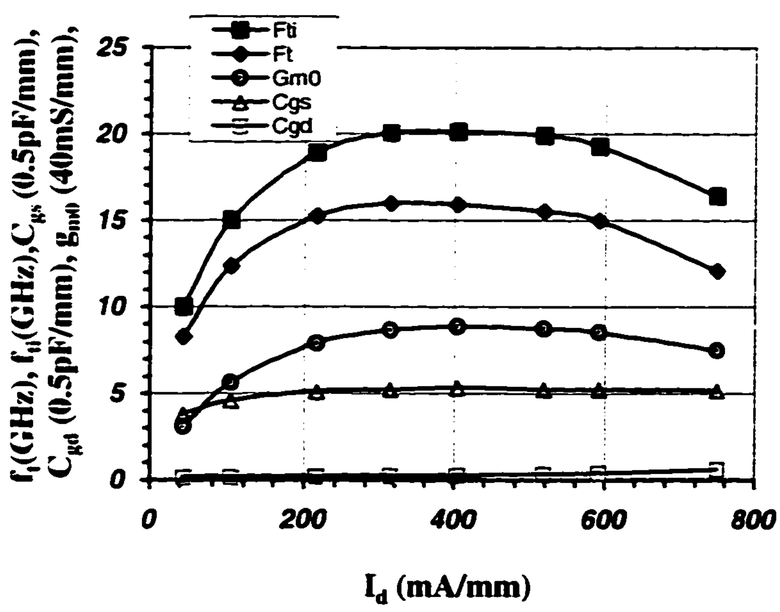

Fig. A2-1 Current-gain cutoff frequencies and relevant parameters vs. drain current for a 0.7 µm gate-length $Al_{0.5}Ga_{0.5}N/GaN$ HEMTs. Extrinsic resistances: R_s = 1.73 Ω-mm, R_d = 2.58 Ω-mm. Drain bias voltage: V_{ds} = 7 V.

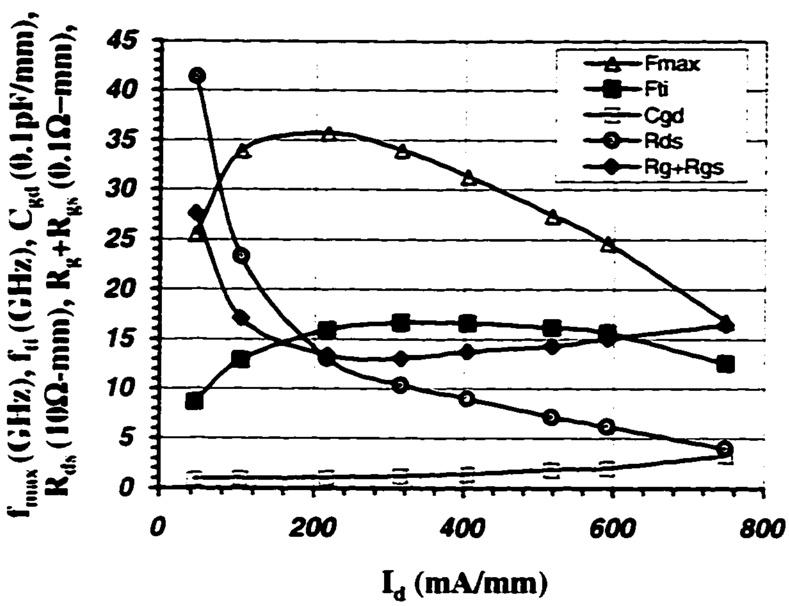

Fig. A2-2 Power-gain cutoff frequency and relevant parameters vs. drain current for the same device in Fig. A2-1 (V_{ds} = 7 V).

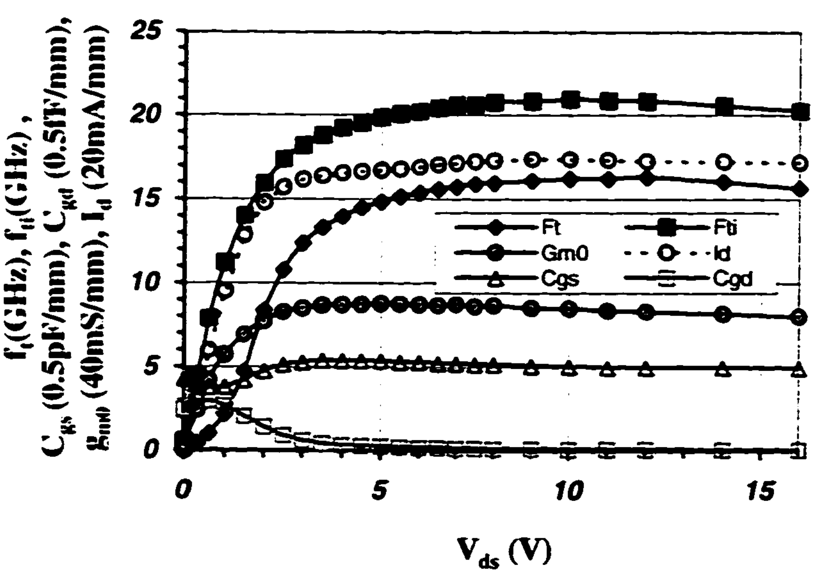

Fig. A2-3 Current-gain cutoff frequencies and relevant parameters vs. source-drain voltage for the same device in Fig. A2-1 (V_{gs} = -2 V).

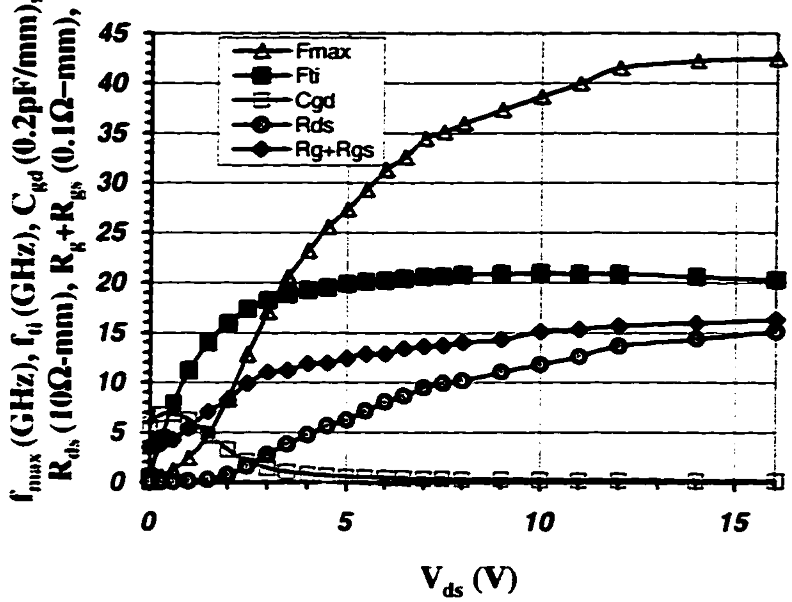

Fig. A2-4 Power-gain cutoff frequency and relevant parameters vs. source-drain voltage for the same device in Fig. A2-1 (V_{gs} = -2 V).

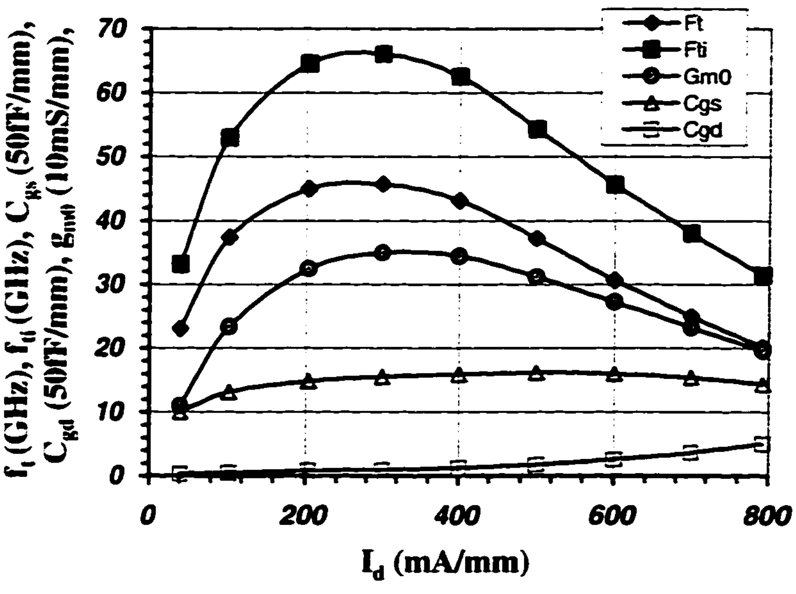

Fig. A2-5 Current-gain cutoff frequencies and relevant parameters vs. drain current for a 0.25-μm gate-length $Al_{0.5}Ga_{0.5}N$/GaN HEMTs. Extrinsic resistances: R_s = 1.32 Ω-mm, R_d = 1.87 Ω-mm. Drain bias voltage: V_{ds} = 6 V.

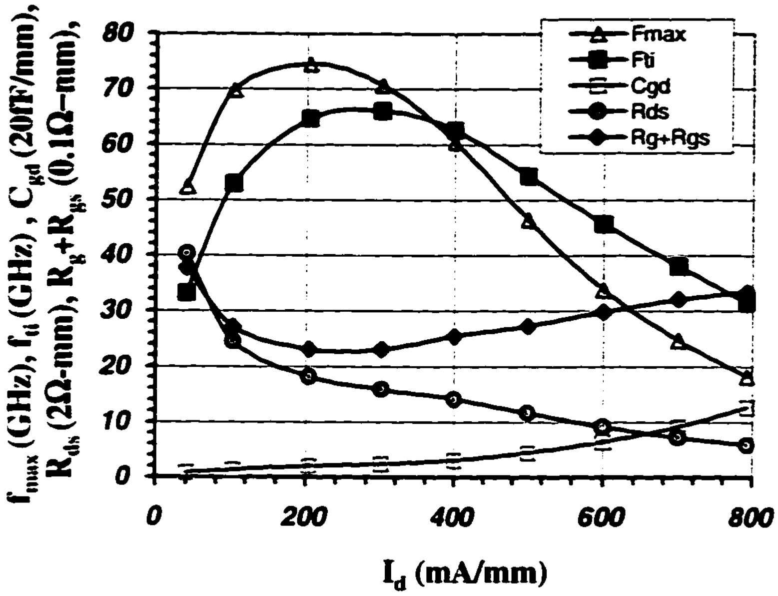

Fig. A2-6 Power-gain cutoff frequency and relevant parameters vs. drain current for the same device in Fig. A2-5 (V_{ds} = 6 V).

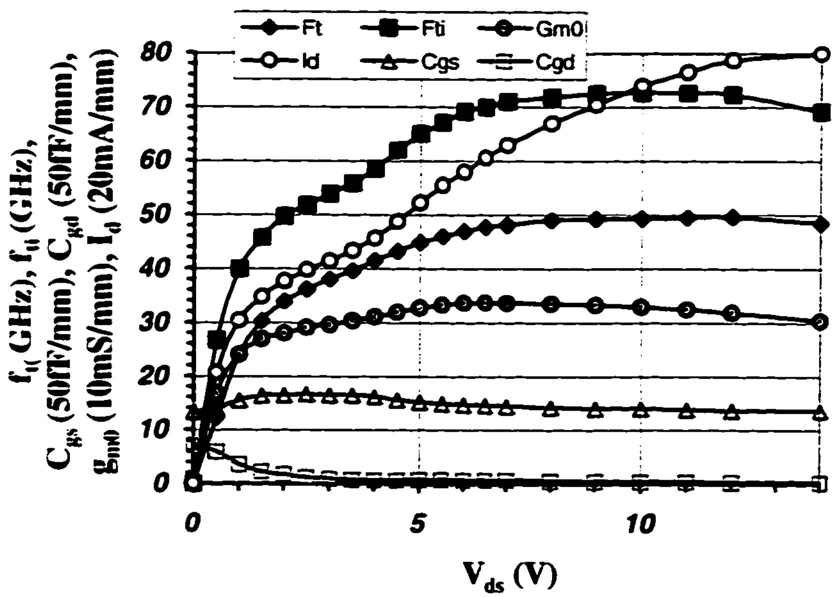

Fig. A2-7 Current-gain cutoff frequencies and relevant parameters vs. source-drain voltage for the same device in Fig. A2-5 (V_{gs} = -3 V).

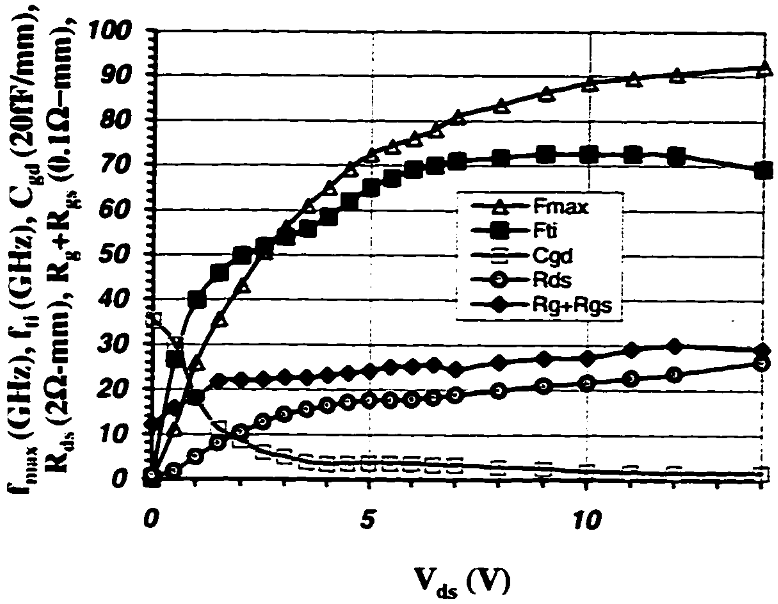

Fig. A2-8 Power-gain cutoff frequency and relevant parameters vs. source-drain voltage for the same device in Fig. A2-5 (V_{gs} = -3 V).