Buck Converter

Non-Idealities and Efficiency Considerations

Key sources of loss in switchmode circuits include:

- transistor loss (on-resistance for FETs)
- diode loss (forward voltage drop)
- winding resistance in inductors

and these of course reduce efficiency to some extent. We will develop some methods for modeling these losses in a general way later, but let's try to estimate them to get a feeling for typical efficiency.

If $\Delta I_i \ll \Delta I_L$ then we can assume that the inductor current is $\Delta I_L = \frac{V_{in}}{R_L}$, so loss associated with winding resistance is

$$P_L = \frac{V_{in}}{R_L} \Delta I_L = \frac{V_{in}^2}{R_L}$$

The rms current in $Q1$ is just $\Delta I_L \sqrt{D}$ so the power loss due to on-resistance $P_m$ is

$$P_m = \frac{V_{in}^2}{R_m} \Delta I_L \sqrt{D}$$

The average current in $D1$ is $\Delta I_L (1-D)$ so the power loss associated with the diode drop is

$$P_d = \frac{V_d}{V_{in}} \Delta I_L (1-D) = \frac{V_d}{V_{in}} (1-D) P_{out}$$

The overall efficiency is then

$$\eta = \frac{P_{out}}{P_{out} + P_L + P_m + P_d} = 1 - \left( \frac{R_m + \Delta I_L \sqrt{D}}{R_L} \right) + \frac{V_d}{V_{in}} (1-D)$$

(10)
in the previous example, let’s assume that
\[ R_s = 0.5 \ \Omega \]
\[ R_m = 1.5 \ \Omega \]
\[ V_d = 0.7 \ \text{V} \]

under maximum load current conditions \((R = R_m = 10 \ \Omega)\)

\[
\frac{R_s + DR_m}{R_m} = \frac{0.5 + 0.5\times 1}{10} = 0.09 \Omega
\]

\[
\frac{V_d}{V_{out}} (1-D) = \frac{0.7}{5} \times (0.58) = 0.081
\]

so \( \eta = \frac{1}{1.173} \approx 85 \% \)

All three loss terms could be reduced to some extent. Winding resistance can be reduced by using a larger diameter wire, but this may require a larger core to accommodate. The on-resistance can be reduced by using a larger FET or parallel FETs, but this not only costs more, it also can impact switching speed due to the increased capacitance. To reduce losses from the diode we could use a Schottky with 0.3-0.4V forward drop, or use a synchronous FET to replace the diode. Clearly, the final design must balance a number of competing factors and always represents a compromise. But efficiencies on the order of 80-90% are pretty typical in a well designed commercial converter.

But...there is more to the story—see next page!
Efficiency Continued

What about the gate driver? There must be a circuit somewhere to generate the gate drive and this will consume some power (?). This is frequently overlooked in most textbook treatments of DC-DC converters; though in fairness this extra loss should be negligibly small in a well-designed control IC.

Another source of loss is associated with the switching transients in the transistor. Our previous analysis assumed that the product of voltage and current was always zero. In reality, the device capacitances limit how quickly the device can be switched on and off. We can get a simple estimate of switching loss with the following very crude model (we'll consider this more carefully later, and is treated in the excellent paper by Balogh).

Approximate switching waveforms for FET w/ inductive load
There is a delay between the start of a
transistor's gate and the corresponding
start of the output voltage change. However,
most of the switching loss happens because of the
rather long tails on the output voltage, and the 
looks like the current in the device is relatively constant during that time.

\[
\int I_d V_{ds} dt = \frac{1}{2} \left( t_r + t_c \right) I_{on} V_{off}
\]

so the average power loss in one switch period is

\[
P_{sw} = \frac{1}{T} \int I_d V_{ds} dt = \frac{T_s}{T} I_{on} V_{off}
\]

Let's take \( T_s = \frac{1}{2} (t_r + t_c) \) as an average
switching time, in which case

\[
P_{sw} = \frac{T_s}{T} I_{on} V_{off} = \frac{C_s}{2} T_s I_{on} V_{off}
\]

which shows that the switching losses increase with switching frequency. Later we will
examine some techniques called zero-volt switching (ZVS) and zero-current switching (ZCS) which seek
to reduce these losses using additional resonant circuit components.