Flyback Converter

Essentially a transformer-isolated version of the Buck-Boost converter (see p. 161 of Greene's).

Gate driven by pulse train:
(duty-cycle modulation)

$$T_{on} = DT$$

Ideal Analysis - Discontinuous Mode

- Assume diode drops negligible
- $$C_L$$ chosen large enough to make $$V_{at}$$ constant
- Transistor is an ideal switch

During the "on" period the primary current ramps up linearly. Because of the polarity on the windings the diode is reverse-biased so no secondary current flows - the primary side just acts like an ordinary inductor with inductance $$L_p$$

$$V_p = V_{in} = L_p \frac{dI_p}{dt} \Rightarrow \frac{dI_p}{dt} = \frac{V_{in}}{L_p}$$

$$I_{on}$$

$$I_{max} = \frac{V_{in} T_{on}}{L_p}$$

Peak stored energy: $$U = \frac{1}{2} L_p I_{max}^2$$
when $Q_1$ turns off the primary voltage changes sign and so does the secondary voltage. The output rectifier diode turns on. Since current can no longer flow in the primary, the energy stored in the core can only flow to the secondary. In the discontinuous mode, the switching period is chosen large enough to allow for a complete transfer of energy to occur, thus resetting the core.

During this discharge period a constant voltage $V_{out}$ appears across the secondary winding, so the current will decay linearly. At the instant of $Q_1$ turn-off, the secondary current will jump to

$$I_{s\max} = \frac{N_p}{N_s} = n \cdot I_{p\max}$$

$\frac{N_p}{N_s} = \text{turns ratio}$

$T_r = \text{"recovery" time}$

$T_d = \text{"dead time"}$

In discontinuous mode, $I_s$ decays to zero as shown before next cycle begins.

As discussed earlier, the amp-turns in an inductor cannot change instantaneously, so the sudden jumps in primary and secondary currents might seem to contradict this, but in fact the same principle is at work here: the "m" period establishes a certain flux in the core, and that flux cannot change instantly when $Q_1$ is shut off. So a current is induced in the secondary to maintain the flux. The amp-turns is continuous considering the primary and secondary together.
For an ideal flyback converter, \( P_{in} = P_{out} \)

\[
P_{in} = V_{in} \langle I_p \rangle = V_{in} \left[ \frac{1}{2} I_{prmax} \frac{T_o}{T} \right]
\]

average primary current

\[
= \frac{1}{2} \left( \frac{V_{in} T_o}{I_p} \right)^2
\]

Note: this is equal to \( \frac{U_{max}}{T} \) as expected

\[
P_{out} = \frac{V_{out}}{R_L} = P_{in}
\]

Note that output voltage does not depend on transformer turns ratio

\[
(3) \quad V_{out} = V_{in} T_o \sqrt{\frac{R_L}{2 L_p T}}
\]

This shows how \( V_{out} \) can be regulated by controlling the duty cycle (\( T_o \))

Max required duty cycle occurs for minimum \( V_{in}, R_L \)

On the secondary side, the average current delivered by the secondary winding must equal the average load current (since \( \xi = 1 \) so):

\[
\Delta Q = \frac{V_{out}}{R_L}, \quad \Delta Q = \frac{1}{2} T_r \frac{I_{prmax}}{T} = \frac{1}{2} T_r n \frac{I_{pmax}}{T}
\]

\[
\frac{1}{2} T_r n \frac{I_{pmax}}{T} = \frac{V_{out}}{R_L}
\]

\[
(4) \quad T_r = \frac{2 V_{out} T}{n R_L I_{pmax}} = \frac{1}{n} \sqrt{\frac{2 L_p T}{R_L}} = \frac{V_{in} T_o}{n V_{out}}
\]

(Note: this can also be derived from volt-second balance;

\[
\frac{1}{N_p} V_{in} T_o = \frac{1}{N_s} V_{out} T_r
\]
To ensure that the circuit remains in the discontinuous mode, the switching period must be chosen such that

\[ T = T_{on} + T_{Tr} \]

The equality defines the boundary using (3) and (4) we can write

\[ T \geq \left( \frac{V_{out}}{V_{in} + \frac{1}{n}} \right)^2 \frac{2Lp}{R_L} \]

\[ T \geq \left( \frac{V_{out}}{V_{in} + \frac{1}{n}} \right)^2 \frac{2Lp}{R_L} \]  (5)

Now we must consider the design of the flyback.

**Specifications:**
- \( V_{out} \): desired constant output voltage
- \( V_{in,\text{min}} \): expected range of input voltages
- \( V_{in,\text{max}} \)
- \( P_{out}, I_{\text{max}} \): max output power or load current

The specifications determine the minimum load resistance,

\[ R_{L,\text{min}} = \frac{V_{out}}{I_{\text{L,\text{max}}}} = \frac{V_{out}}{P_{out}} \]

The designer must then choose a suitable transistor, inductor value \( L_p \), and turns ratio \( n \) to meet the specs, along with a desired switching frequency.
note that the transistor choice will impose further constraints on the circuit

\[ \begin{align*}
  V_d & = V_{\text{in}} + nV_{\text{out}} \leq V_{\text{d(max)}} \\
  I_d & \leq I_{\text{d(max)}}
\end{align*} \]

max allowed current and voltage for transistor

when the transistor turns off, a primary voltage of \( V_p = nV_{\text{out}} \) will be developed, so the maximum voltage is

\[ V_d = V_{\text{in}} + nV_{\text{out}} \leq V_{\text{d(max)}} \]

\[ n \leq \frac{V_{\text{d(max)}} - V_{\text{in(max)}}}{V_{\text{out}}} = n_{\text{max}} \]  \( (6) \)

Thus the transistor choice gives an upper bound on the turns ratio

Similarly the peak current in \( Q_1 \) is given by \( (1) \)

so

\[ I_p = \frac{V_{\text{in}}T_{on}}{I_d} \leq I_{d(max)} \]

\[ n \leq \frac{(V_{\text{in}}T_{on})_{\text{max}}}{I_{d(max)}} = \frac{V_{\text{out}}}{I_{d(max)}} \sqrt{\frac{2I_{p}}{R_{\text{min}}}} \]

Solving for \( I_p \) gives

\[ I_p \geq \left( \frac{V_{\text{out}}}{I_{d(max)}} \right) \sqrt{2I_{p}R_{\text{min}}} = I_{p(max)} \]  \( (7) \)

Thus the transistor peak allowed current sets a lower bound on \( I_p \)
an upper bound on inductance can be found from

\[ L_p \leq \frac{T R_k/2}{\left( \frac{V_{\text{out}}}{V_{\text{in}}} + \frac{1}{n} \right)^2} \]

The design must work for all possible values of \( V_{\text{in}} \) so the worst case is when the R.H.S. is smallest

\[ L_p \leq \frac{R_{L,\min}}{2 \cdot f_s} \left( \frac{V_{\text{out}}}{V_{\text{in},\min}} + \frac{1}{n} \right)^2 = L_{p,\text{max}} \]

Putting (7) and (8) together gives a range of possible values of \( L_p \)

\[ L_{p,\min} \leq L_p \leq L_{p,\max} \]

The only way these can both be satisfied is if

\[ L_{p,\max} \geq L_{p,\min} \]

So

\[ \frac{R_{L,\min}}{2 \cdot f_s} \left( \frac{V_{\text{out}}}{V_{\text{in},\min}} + \frac{1}{n} \right)^2 \geq \left( \frac{V_{\text{out}}}{V_{\text{in},\min}} \right)^2 \]

\[ \frac{R_{L,\min}}{2} \left( \frac{I_{d,\max}}{V_{\text{out}}} \right)^2 \geq \left( \frac{V_{\text{out}}}{V_{\text{in},\min}} + \frac{1}{n} \right) \]

So

\[ \frac{1}{n} \leq \frac{R_{L,\min}}{2} \left( \frac{I_{d,\max}}{V_{\text{out}}} \right) - \frac{V_{\text{out}}}{V_{\text{in},\min}} \]

or

\[ n \geq \frac{R_{L,\min}}{2} \left( \frac{I_{d,\max}}{V_{\text{out}}} \right) - \frac{V_{\text{out}}}{V_{\text{in},\min}} = n_{\min} \]
(6) and (9) define a range for \( n \) \( N_{\text{min}} < n < N_{\text{max}} \) and again a valid design is only possible when

\[ N_{\text{max}} \geq N_{\text{min}} \]

\[ C \quad \frac{R_{2,\text{min}}}{2} \left( \frac{T_{d,\text{max}}}{V_{\text{out}}} \right) - \frac{V_{\text{at}}}{V_{\text{in},\text{min}}} \geq \frac{V_{\text{at}}}{V_{d,\text{max}} - V_{\text{in},\text{max}}} \]

This gives us a bound on the transistor current:

\[ I_{d,\text{max}} \geq \frac{2V_{\text{out}}}{R_{2,\text{min}}} \left[ \frac{V_{\text{out}}}{V_{d,\text{max}} - V_{\text{in},\text{max}}} + \frac{V_{\text{out}}}{V_{\text{in},\text{min}}} \right] \]

Now we have a procedure:

1) specify a max transistor voltage \( V_{d,\text{max}} \)
2) choose a transistor with \( I_{d,\text{max}} \) that satisfies (10)
3) with \( V_{d,\text{max}} \) \( V_{\text{in},\text{min}} \) and \( T_{d,\text{max}} \) specified, choose a desired \( n \) in the range \( N_{\text{min}} \leq n \leq N_{\text{max}} \), large \( n \) leads to high voltage stress, small \( n \) leads to higher currents
4) with \( n \) determined, select \( L_p \) : \( L_{\text{min}} \leq L_p \leq L_{\text{max}} \)

The last step is to design the transformer to give a desired \( L_p \).
Ideal Analysis - Continuous Mode

In the continuous mode the stored energy in the core is never completely discharged. The winding waveforms become

\[
\begin{align*}
I_p & \rightarrow T \rightarrow \frac{T \Delta T_p}{T_0} \rightarrow I_{p,\text{max}} \rightarrow 3 \Delta I_p \\
I_s & \rightarrow I_{s,\text{max}} \rightarrow I_s \rightarrow \frac{T \Delta I_p}{T_0} \rightarrow I_0
\end{align*}
\]

In this case \( \Delta I_p = \frac{V_{in} T_0}{L} \) as before, but the peak current is larger.

In the steady state the flux change in the core should be equal in the on and off periods

\[
\frac{1}{N_p} V_{in} T_0 = \frac{1}{N_s} V_{out} T_r
\]

This is the same as (4), but now \( T_r = T - T_0 \)

\[
\frac{1}{n} V_{in} T_0 = V_{out} \left( T - T_0 \right)
\]

\[
\text{So, } V_{out} = \frac{V_{in}}{n} \left( \frac{T_0}{T - T_0} \right) = \frac{V_{in}}{n} \left( \frac{D}{1 - D} \right)
\]

(11)

In this case, the output voltage does depend on the turns ratio, but again is controlled by the duty-cycle. More importantly, there is no dependence on the load resistance.
The average primary current can be expressed as

\[ \langle I_p \rangle = \frac{1}{T} \left[ I_{p,\text{MAX}} - \frac{1}{2} \Delta I_p T_{\text{ON}} \right] \]

\[ = D \left[ I_{p,\text{MAX}} - \frac{V_{\text{IN}} T_{\text{ON}}}{2 L_p} \right] \]

From \( P_{\text{in}} = P_{\text{out}} \) we get

\[ V_{\text{IN}} \langle I_p \rangle = V_{\text{OUT}}^2/R_L = \frac{1}{R_L} \frac{V_{\text{IN}}^2}{n^2} \left( \frac{D}{1-D} \right)^2 \]

\[ V_{\text{IN}} D \left[ I_{p,\text{MAX}} - \frac{V_{\text{IN}} T_{\text{ON}}}{2 L_p} \right] = \frac{1}{R_L} \frac{V_{\text{IN}}^2}{n^2} \left( \frac{D}{1-D} \right)^2 \]

\[ \left[ I_{p,\text{MAX}} = \frac{V_{\text{IN}} D}{n^2 R_L (1-D)^2} + \frac{V_{\text{IN}} D}{2 f_s L_p} \right] \quad \text{(12)} \]

\[ I_{p,\text{MIN}} = I_{p,\text{MAX}} - \Delta I_p = \frac{V_{\text{IN}} D}{n^2 R_L (1-D)^2} - \frac{V_{\text{IN}} D}{2 f_s L_p} \]

The circuit operates in the continuous mode when

\[ \frac{1}{n^2 R_L (1-D)^2} \geq \frac{1}{2 f_s L_p} \]

\[ \left[ L_p \geq \frac{n^2 R_L (1-D)^2}{2 f_s} \quad \text{or} \quad R_L \leq \frac{2 f_s L_p}{n^2 (1-D)^2} \right] \quad \text{(13)} \]

Condition for continuous mode

Note that the value of \( L_p \) will determine the allowed range of load resistance, so the \( L_p, \text{MAX} \) will set a lower bound on \( L_p \).
As before, the choice of transistor will impose constraints on some of the circuit variables.

The peak voltage is the same as in the discontinuous mode so (6) constrains the turns ratio as before.

Note that (11) is essentially the same as the SEPIC but divided by the turns ratio. This means that the turns ratio can be used effectively to achieve large step-up or step-down ratios without resorting to excessive duty-cycles (which generally lead to reduced efficiencies). However, \( n \) is constrained by the peak voltage issue as noted above. Combining (11) and (6),

\[
V_{\text{in(max)}} + (nV_{\text{out}})_{\text{max}} \leq V_{\text{d(max)}} \quad \text{(Note: \( nV_{\text{out}} \) should be a constant so we can choose any \( V_{\text{in,0}} \) combo)}
\]

\[
V_{\text{in}} \left[ 1 + \frac{\text{D}_{\text{max}}}{1 - \text{D}_{\text{min}}} \right] \leq V_{\text{d(max)}}
\]

\[
V_{\text{d(max)}} \geq \frac{V_{\text{in(max)}}}{1 - \text{D}_{\text{min}}}
\]

(14)

As long as the transistor \( V_{\text{d(max)}} \) is chosen large enough to satisfy (14), then (6) is automatically satisfied and (11) gives the required turns ratio

\[
n = \frac{V_{\text{in(max)}}}{V_{\text{out}}} \left( \frac{\text{D}_{\text{min}}}{\text{D}_{\text{max}}} \right)
\]

The actual turns ratio can be chosen at or below this value in order to get an integer number of turns on the secondary.
Note that the peak current in (12) can be written as

$$I_{p, \text{max}} = \frac{V_{\text{out}}^2}{R_L} + \frac{V_{\text{in}D}}{2f_s L_p}$$

the smallest inductor that can be used and still keep the circuit in the continuous mode is given by (13), alternately expressed as

$$2f_s L_p \geq \frac{R_L (V_{\text{in}D})^2}{V_{\text{out}}^2}$$

Thus the worst case transistor current would be

$$I_{p, \text{max}} = \frac{V_{\text{out}}^2}{R_{\text{min}} (V_{\text{in}D})} + \frac{V_{\text{out}}^2}{R_{\text{max}} (V_{\text{in}D})^2}$$

as long as $R_{\text{max}} > R_{\text{min}}$, the peak current occurs when $(V_{\text{in}D})$ is minimum, which can be shown to be

$$(V_{\text{in}D})_{\text{min}} = V_{\text{in}, \text{min}} D_{\text{max}},$$

$$(V_{\text{in}D})_{\text{max}} = V_{\text{in}, \text{max}} D_{\text{min}}$$

so

$$I_{p, \text{max}} = \frac{V_{\text{out}}^2}{R_{\text{min}} (V_{\text{in}D})_{\text{min}} + \frac{(V_{\text{in}D})_{\text{max}}}{R_{\text{max}} (V_{\text{in}D})^2}$$

The transistor should be selected for this worst-case current. The actual peak current will be smaller if $L_p$ is increased.
Output Spikes due to ESR - two stage filter
Flyback with Multiple Outputs

One advantage of the flyback topology is the relative ease with which additional outputs can be added, which involves an additional secondary winding and rectifier circuit as shown below:

![Flyback Circuit Diagram]

Note that only one of the outputs can be regulated. This is the "master" output.

In the flyback stage, the voltages on the secondary windings are clamped to \( V_{out,1} \) and \( V_{out,2} \), and these are related by the turn ratio, so

\[
V_{out,1} = \frac{N_{s1}}{N_{s2}} V_{out,2}
\]

Since only integer turns are allowed, and \( N_{s2} \) is fixed by earlier design considerations, it is not always possible to set the slave outputs to some precise value. In those cases, the turn ratio is often chosen to give a slightly higher voltage, and use a so-called "saturable reactor" to reduce it to the desired voltage. We'll discuss those later.
Since only one output can be regulated by the feedback loop, the slave output regulation is always worse than the master -- ±8% is not uncommon.

If this is not good enough, one can always insert a linear regulator in the secondary (which would obviously reduce the efficiency). Alternatively, a self-centred/self-regulated buck or boost circuit could be used on the slave secondary (efficient but increases cost/complexity).

We'll return to this discussion later in the context of power-supply design and distributed power architectures.
At this stage we need to discuss transformers.

- Saturation issues
- Real vs. ideal transformer
- Leakage inductance
- Design issues