Switches, Basic Circuits

Up to now we've drawn circuits with ideal switches, like this:

which is the easy way to understand the topology. But once the topology is selected, we need to design a circuit to realize it. In most cases, we will focus on MOSFETs, but the issues will be similar to other devices.

Here is the switch function of an n-channel MOSFET:

\[ q = \begin{cases} 
\text{P-Channel} & \text{if } V_G > V_T \\
\text{N-Channel} & \text{if } V_G < V_T 
\end{cases} \]

The FET is most commonly discrete (on transistor in a package), but whether discrete or combined with other circuitry on-chip, it is designed specifically for power switching.

As a reminder, the MOSFET used in signal processing/logic circuits look something like this:

and have the following characteristics:

1. lateral
2. symmetric (source and drain interchangeable)
3. body (p-well) grounded, or at least tied to a more negative potential than either S or D.

Two broad categories of power MOSFETs are illustrated: lateral and vertical.
For low voltage, high speed switching, lateral devices are often a good choice, because the capacitances are low. Adjustable lateral devices offer better current density and blocking voltage for a given on-resistance. But the distinction is not generally a concern for the circuit designer - the transistor is picked based on performance specifications. For either type, the distinguishing characteristics are:

1. Asymmetric
2. P-well is tied to the source.

This letter means that P-channel FETs are 3-terminal devices. It also means there is P-N junction between the source and drain contacts. This "body diode" is often explicitly indicated in the symbol:

\[ \text{body diode} \]
If the avalanche energy of the p-n junction has been
characterized, the symbol may be

Various capacitances are defined for the FET:

\[ C_{gs} = C_{gs} + C_{gd} \]
\[ C_{oss} = C_{ds} + C_{gd} \]
\[ C_{rss} = C_{gd} \]

More significant when capacitances are general the charges
\[ C_{gs}, C_{gd} \ldots \]

Sum on with an inductive load. For example

\[ V_{in} \]
\[ I \]
\[ V_{gs} \]
\[ V_{D} \]
\[ R_g \]
\[ V_{o} \]

Assume \( I_{c} \) is constant
during the very short
transient.
\( R_g \) represents the total
resistance in series with
the gate, whether integral
to the chime or discrete.

The 4-step analysis is explained in detail in the
paper by Balogh.
State (4): Switch open
- $V_{gs} = 0$
- $V_{ds} = V_0$, $I_d = 0$

State (6): Switch closed
- $V_{gs} = V_{gg}$
- $V_{ds} = I_L$, $V_{ds}$ on
- $I_d = I_L$

Turn on Procedure

Steps:
1. Charging $C_{gs} \rightarrow V_{th}$
2. Charging $C_{gs} \rightarrow V_{miller}$
3. Discharging $C_{gd}$
   - ($V_{gs}$ must be constant since $I_d$ constant)
4. Charging $C_{gd} + C_{gs}$ to $V_{gg}$

The Miller Plateau - step (4) corresponds to the ramp voltage produced at the output of an integrator given a constant input $V_{gs}$, and $R_s$, where the diode plays the role of the switch.