Interleaving Contributes Unique Benefits to Forward and Flyback Converters

Brian Shaffer

ABSTRACT

A 200-W interleaved forward converter design example illustrates how an interleaved topology can reduce the size and cost of power filtering components and also enhance dynamic load response. In this comprehensive design review, the converter operates from a standard 48-V telecom input voltage and outputs 12 V at 200 W in a half-brick footprint. Operating at a switching frequency of 500 kHz per phase, over 90% efficiency is achieved without the use of synchronous rectifiers. The two-inductor interleaved forward converter is compared against a one inductor interleaved forward converter, a push-pull converter, and a half-bridge converter. A 200-W interleaved flyback converter with an isolated regulated output voltage is also presented. This flyback topology has the potential for operation over the universal AC line voltage range, with the added benefit of achieving a high power-factor input characteristic without additional PFC circuitry.

I. INTRODUCTION

In recent years the usefulness of interleaving power stages has become apparent. The best known application is in powering microprocessors, commonly referred to as voltage regulator modules (VRMs). In VRM applications, the converters are non-isolated from input to output. This paper presents the benefits of interleaving power stages for isolated applications. It shows that the two-inductor (2L) interleaved forward converter topology or the interleaved flyback converter topologies are appropriate choices for many high-power applications.

The forward converter shown in Fig. 1 is one of the most studied topologies. Derived from the simple buck converter, the forward converter delivers energy from the input source to the output filter inductor during the on time of the main switch. In contrast, the flyback converter shown in Fig. 3 delivers energy to the output filter capacitor only during the off-time of the main power switch. This different power transfer characteristic has a dramatic impact on the transfer function and the power levels at which a flyback converter is applicable.

The concept of interleaving enables these converter topologies to operate at increased power levels. The benefits of interleaving include:

- Reduced RMS current in the input capacitors enabling the use of less expensive and fewer input capacitors
- Ripple current cancellation in the output capacitor, enabling the use of less expensive and fewer output capacitors
- Reduction of peak currents in primary and secondary transformer windings (2L interleaved forward converter)
- Improved transient response as a result of reduced output filter inductance and higher output ripple frequency
- Separation of heat generating components allowing for reduced heatsink requirements.
- Improved form factor for low profile solutions
- Reduced EMI as a result of reduced peak currents (2L interleaved forward converter)
II. SINGLE FORWARD CONVERTER

For the single forward converter shown in Fig. 1 the following quantities are evaluated and compared to “1L” or “2L” interleaved forward converters, push-pull converters, and half-bridge converters.

Comparison Quantities:
- Transformer peak currents
- Transformer RMS currents
- Minimum transformer turns ratio
- Input capacitor AC RMS current
- Output inductor peak-to-peak ripple current
- Output capacitor AC RMS current
- Power switch peak voltage
- Output rectifier peak voltage
- Output rectifier peak current.

Table 1 summarizes the equations for the above quantities. In Table 6 these equations are evaluated for a 200 W design example and compared to the results from the other topologies listed above. In Table 7, 500 W design examples are compared.

Fig. 1. Single forward converter power stage.

![Fig. 1. Single forward converter power stage.]

Fig. 2. Forward converter waveforms, (A) Primary transformer current, (B) output inductor current (D = 0.4).

![Fig. 2. Forward converter waveforms, (A) Primary transformer current, (B) output inductor current (D = 0.4).]

Fig. 3. Single flyback converter.

![Fig. 3. Single flyback converter.]

Fig. 4. Flyback converter waveforms, (A) Primary transformer current, (B) secondary transformer current (D = 0.6).

![Fig. 4. Flyback converter waveforms, (A) Primary transformer current, (B) secondary transformer current (D = 0.6).]
### Table 1. Single-Forward Converter Equations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Single Forward</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ipks_T1</td>
<td>Iout</td>
</tr>
<tr>
<td>Ipkp_T1</td>
<td>Iout / N1</td>
</tr>
<tr>
<td>Irms_s_T1</td>
<td>Iout * (D_{max}) / N1</td>
</tr>
<tr>
<td>Irms_p_T1</td>
<td>Iout * (D_{max}) / N1</td>
</tr>
<tr>
<td>Nx_min</td>
<td>(Vin_{min} D_{max} / (Vout + Vd))</td>
</tr>
<tr>
<td>Icin_acrms</td>
<td>Iout / N1 * (\sqrt{D} \cdot (1 - D))</td>
</tr>
<tr>
<td>ILout_pp</td>
<td>((Vout + Vd) \cdot (1 - D_{max}) / (Vout - Vd))</td>
</tr>
<tr>
<td>Icout_acrms</td>
<td>(1 - \frac{Vout}{Vin_{max}} \cdot \frac{\sqrt{I}}{\sqrt{3}})</td>
</tr>
<tr>
<td>Vpk_Q1</td>
<td>(\frac{Vin_{min}}{1 - D_{max}} ) or (\frac{Vin_{max}}{1 - D_{min}})</td>
</tr>
<tr>
<td>Vpk_D1</td>
<td>(\frac{Vin_{min} \cdot D_{max}}{1 - D_{max}} \cdot \frac{1}{N1})</td>
</tr>
<tr>
<td>Vpk_D2</td>
<td>(\frac{Vin_{max}}{N1})</td>
</tr>
<tr>
<td>Ipk_D1</td>
<td>Iout</td>
</tr>
</tbody>
</table>

This leads to a fewer number of and less expensive input and output capacitors. In general, semiconductor devices are more reliable and cost effective than capacitors, so the increased voltage stress on the power switches and output rectifiers is considered desirable when compared to having more expense and a larger number of input and output capacitors. Fig. 7 depicts an alternative configuration for interleaved forward converters where only one output inductor (1L) is required. It is shown that the 1L topology has higher peak and RMS transformer currents than the 2L topology.

In Fig. 5 the term “phase” is defined as any one of the individual power stages in the interleaved configuration. Fig. 6 contains the operating waveforms for the 2L interleaved forward converter of Fig. 5 operating at a duty cycle of 0.4. By examining Fig. 6 it becomes clear how to write the expressions for the input and output capacitor ripple currents when the duty cycle of each phase is less than or equal to 0.5 or one divided by x \((1/x)\) where x is the number of phases being interleaved. The effect of interleaving on the duty cycle is to increase the effective duty cycle by the number of phases in the circuit and reduce the peak current by the same factor. In Fig. 5 there are two phases so the effective duty cycle is increased by a factor of two and the peak currents are reduced by the same amount. Another way of describing this phenomenon is to realize that the frequency of the input and output currents are increased by a factor of two over the switching frequency of each individual phase and the power throughput of each phase is inversely proportional to the number of phases.

For the interleaved forward converters shown in Figs. 5 and 7 the same quantities that were evaluated for the single forward converter are again evaluated and used to compare these interleaved converters against each other and to push-pull converters, or half-bridge converters.
Fig. 5. “2L” interleaved forward converter ($D_{max} \geq 0.5$).

Fig. 6. 2L interleaved forward waveforms, $D = 0.4$ (A) Primary transformer current of phase 1, (B) primary transformer current of phase 2, (C) sum of current waveforms (A) and (B) seen at the input capacitor, (D) output inductor current of phase 1, (E) output inductor current of phase 2, (F) sum of output inductor currents.

Fig. 7. “1L” interleaved forward converter ($D_{max} < 0.5$).

Fig. 8. 2L interleaved forward waveforms, $D = 0.8$, (A) Primary transformer current of phase 1, (B) primary transformer current of phase 2, (C) sum of current waveforms (A) and (B) seen at the input capacitor, (D) output inductor current of phase 1, (E) output inductor current of phase 2, (F) sum of output inductor currents.
Interleaved Forward Converter with Two Output Inductors (2L)

Primary and Secondary Transformer Windings Peak Currents ($D \leq 0.5$)

In Fig. 5, the peak secondary current, $I_{pk\_s\_T1}$, is cut in half for two phases.

$$I_{pk\_s\_T1} = \frac{I_{out}}{2}$$

The peak current in the primary winding is then calculated by transforming the secondary current to the primary winding, by dividing it by the turns ratio of the transformer.

$$I_{pk\_p\_T1} = \frac{I_{pk\_s\_T1}}{N\_3} = \frac{I_{out}}{2 \times N\_3}$$

Transformer RMS Currents ($D \leq 0.5$)

The equivalent RMS current of the waveform in Fig. 6A, $I_{rms\_p\_T1}$, equals:

$$I_{rms\_p\_T1} = I_{pk\_p\_T1} \times \sqrt{D} = \frac{I_{out}}{2 \times N\_3} \times \sqrt{D}$$

The secondary winding RMS current is then,

$$I_{rms\_s\_T1} = \frac{I_{out}}{2} \times \sqrt{D}$$

Minimum Transformer Turns Ratio

The equation for calculating the turns ratio for the 2L interleaved forward converter is no different than that for the single forward converter. In the following equation and throughout this paper the quantity $D_{max}$ represents the maximum duty cycle of each phase. In the cases where the effective duty cycle is a multiple of the number of phases, a multiplier is added to the equation.

$$N\_3 \_\text{min} = \frac{Vin \_\text{min} \times D_{max}}{V_{out} + V_d}$$

Input Capacitor AC RMS Current ($D \leq 0.5$)

The AC RMS current in the input capacitors is calculated for two different operating conditions. The initial analysis that follows presents the equations for the case where the maximum duty cycle of each phase is less than 0.5 and then, the case where the duty cycle is greater than 0.5 is presented in a later section. For the following calculations refer to Fig. 6C, which is the summation of the input current waveforms in the primary of transformers T1 and T2. In general, the AC RMS current in the input capacitor as a result of the transformer’s input current waveform is:

$$I_{ac\_rms} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

where $I_{rms}$ = The RMS equivalent of the transformer current – [A]

$I_{dc}$ = The DC equivalent of the transformer current – [A]

hence,

$$I_{cin\_ac\_rms} = I_{pk\_p\_T1} \times \sqrt{2 \times D \times (1 - 2 \times D)}$$

$$I_{cin\_ac\_rms} = \frac{I_{out}}{2 \times N\_3} \times \sqrt{2 \times D \times (1 - 2 \times D)}$$

Output Inductor Peak-to-Peak Ripple Current ($D \leq 0.5$)

The output inductor ripple current for each of the phases is calculated in the same manner as with a single forward converter. By factoring in the off time and the output voltage the peak-to-peak ripple current for each output inductor is given by:

$$I\_\text{Lout\_pp} = \frac{(V_{out} + V_d) \times (1 - D)}{L\_out \times F_s}$$

where, $L_{out} = L_{out\_1} = L_{out\_2}$

$F_s$ = The switching frequency of each phase in Hertz
Output Capacitor AC RMS Current \((D \leq 0.5)\)

The following discussion refers to Fig. 6F, which is the sum of the individual output inductor ripple currents shown in Figs 6D and 6E. Assuming that each of the phases is \(360/x\) degrees offset from one another with equal duty cycles the effective duty cycle of the summed inductor current waveform is \(x\) times the individual duty cycle of each phase. The output capacitors are exposed to this summed current waveform and the resultant AC RMS current is the portion of the waveform that causes heating in the output capacitors. The peak-to-peak ripple current of the summed inductor current waveform is expressed by the following equation.

\[
I_{Out \_total \_ pp} = \frac{(V_{out} + Vd) \times (1 - 2 \times D)}{L_{out} \times F_s}
\]

The AC ripple current in the output capacitors for the 2L interleaved forward topology, \(I_{out \_ acrms}\), is then:

\[
I_{out \_ acrms} = \frac{I_{Out \_ total \_ pp} \times \sqrt{1}}{2 \sqrt{3}}
\]

Output Capacitor RMS Ripple Current Cancellation \((D \leq 0.5)\)

Taking the ratio of the output capacitor AC RMS current in the 2L interleaved case and the AC RMS current of the single forward converter reveals an important reason why interleaving is beneficial. For all values of \(D\) less than 0.5, the following equation is less than one which means that the peak-to-peak ripple current seen by the output capacitors is less than the non-interleaved case. The same is true for the cases where \(D > 0.5\).

\[
\frac{I_{out \_ acrms \_ 2L}}{I_{out \_ acrms \_ FWD}} = \frac{1 - 2 \times D}{1 - D}
\]

Power Switch Peak Voltage

The peak voltage on the power switch is a result from the requirement that the volt second product on the primary transformer winding average to zero. The longer the on-time the more negative the reset voltage must be in order to maintain a volt second balance. Assuming that the reset voltage is a square wave and that the reset voltage is present throughout the entire off time of the main switch, the volt second balance equation is expressed as:

\[
Vin \times D - Vreset \times (1 - D) = 0
\]

\[
Vreset = \frac{Vin \times D}{1 - D}
\]

From Fig. 5, the peak voltage on the power switch, \(V_{pk \_ Q1}\) is equal to the sum of the input voltage and the reset voltage.

\[
V_{pk \_ Q1} = Vin + \frac{Vin \times D}{1 - D} = \frac{Vin}{1 - D}
\]

Fig. 9, \(V_{pk \_ Q1}/Vin\), depicts the penalty that is paid as the duty cycle is increased. When the duty cycle has reached 0.5 the peak voltage on the switch is equal to twice the input voltage.

![Normalized peak voltage on the main switch vs. duty cycle.](image-url)
Fig. 9 which shows the normalized peak voltage on the main switch applies to interleaved converters as well as non-interleaved converters. In Fig. 5 where the duty cycle is allowed to go above 0.5, it is expected that the peak voltage on the main switch is greater than that seen by the main switch for the complementary design using Fig. 7. For example, consider the case where the maximum duty cycle for the 2L design is allowed to go to 0.8 and the corresponding maximum duty cycle for the 1L design is limited to 0.4, then the peak voltage on the switch in the 2L design is 2.86 (5/1.75) times greater than that for the 1L design. The drawback in peak voltage stress for designs using the 2L configuration is immediately obvious, but the reduction in the input and output capacitor AC RMS currents outweighs this disadvantage.

**Output Rectifier Peak Voltage and Current**

The peak voltage on the output rectifiers in the 2L interleaved case is given by,

\[
V_{pk} - D = \frac{V_{in} \cdot D \cdot 1}{1 - D \cdot N^3}
\]

The peak current in the output rectifiers for the 2L interleaved forward configuration is equal to one half of the load current because the output current is made up of the sum of the individual phase currents.

**Transformer RMS Currents (\(D > 0.5\))**

In the 2L interleaved flyback converter, the equations for determining the RMS current in the transformer windings when the duty cycle is greater than 0.5 are the same as the case where the maximum duty cycle is less than 0.5. The RMS current in the transformer windings increases proportionally to the square root of the increase in duty cycle. For example, a doubling in the maximum duty cycle only increases the RMS current in the winding by forty-one percent. This increase is offset by the reduction in AC RMS current in the input and output capacitors. Because the failure rate of capacitors due to overheating is much more of a concern than heat in a magnetic component, the tradeoff of increased RMS current in the transformer for a reduction in AC RMS currents in the input and output capacitors is worthwhile.

**Input Capacitor RMS Current (\(D > 0.5\))**

As was stated earlier, the circuit configuration of Fig. 5 is allowed to go above 50% duty cycle. In such an operating mode, the equations for determining the input and output ripple currents change slightly. Referring to Fig. 8, the total RMS equivalent current of the waveform in Fig. 8(C), \(I_{in\_rms}\), equals:

\[
I_{in\_rms} = I_{pk\_p\_T1} \cdot \sqrt{2 \cdot (D - 0.5)}
+ I_{pk\_p\_T1}
\]

The DC equivalent current of the waveform in Fig. 8(C), \(I_{in\_dc}\), equals:

\[
I_{in\_dc} = I_{pk\_p\_T1} \cdot (2 \cdot (D - 0.5))
+ I_{pk\_p\_T1}
\]
The AC RMS current in the input capacitor as a result of the transformer’s input current waveform is then:

\[ I_{cin\_ac rms} = I_{pk\_p\_T1} \cdot \sqrt{4 \cdot (D - 0.5) \cdot (1 - D)} \]

Substituting \( I_{pk\_p\_T1} \) from above yields:

\[ I_{cin\_ac rms} = \frac{I_{out}}{2 \cdot N^3} \cdot \sqrt{4 \cdot (D - 0.5) \cdot (1 - D)} \]

Fig. 10 depicts the normalized AC RMS input current for the circuit shown in Fig. 5 for duty cycles from zero to one. The normalization factor defines the AC RMS current in the input capacitors as a function of the peak current in the primary windings, \( I_{out}/(2 \cdot N^3) \).

**Output Inductor Ripple Current (D > 0.5)**

The equation for determining the individual phase ripple current is not changed from the case where the maximum duty cycle is limited to 0.5. It is still directly proportional to the output voltage and off time and inversely proportional to the value of the output inductor.

**Output Capacitor RMS Ripple Current (D > 0.5)**

In order to develop the expression for the output capacitor ripple current it must first be understand how the output inductor ripple currents sum for this case where the duty cycle is allowed to be greater than 0.5. The summation of the individual output inductor phase currents, which is the total peak-to-peak ripple current in the output capacitor as a function of duty cycle is given by the following equation [9]:

\[
I_{Lout\_total\_pp} = \left(I_{Lout\_pp}\right) \cdot KI
\]

\[
I_{Lout\_pp} = \frac{(V_{out} + V_d) \cdot (1 - D)}{L_{out} \cdot F_s}
\]

\[
KI = \frac{x \cdot \left( D - \frac{m}{x}\right) \cdot \left( \frac{m + 1}{x} - D\right)}{D \cdot (1 - D)}
\]

where \( x \) = number of phases (2 for our example)

\( m = \text{floor}(x \cdot D) \) is the maximum integer that does not exceed the product of \( x \) and \( D \).

\( I_{Lout\_pp} = \) peak-to-peak inductor ripple current in each phase. [A]

\( KI = \) cancellation effect of interleaving on the individual peak-to-peak inductor ripple current.

![Fig. 10. Normalized AC RMS ripple current seen by the input capacitor vs. duty cycle.](image)
Normalizing the equation for $IL_{out\_total\_pp}$ to the amount of ripple current per phase gives the cancellation effect, $K_I$ that is present as a result of interleaving power stages at various operating duty cycles.

For $x = 2$,

$$K_I = \begin{cases} \frac{(1 - 2D)}{1 - D} & \text{if } D \leq 0.5 \\ \frac{(2D - 1)}{D} & \text{if } D > 0.5 \end{cases}$$

By examining the preceding graphs for the entire range of possible duty cycles, it becomes clear that the optimal operating point for each phase is at a duty cycle equal to one divided by the number of phases with a phase relation of 360 degrees divided by $x$ ($\frac{360}{x}$). The optimal operating point is not always achievable given a wide input range and semiconductor limitations, but the closer the circuit operates near the optimal point the lower the RMS currents in the input and output capacitors will be. At any operating point, Fig. 11 is used to determine the actual amount of peak-to-peak ripple current in the output capacitors given the peak-to-peak ripple current of each individual phase and the operating duty cycle. Because the current waveform after the summation of the individual ripple currents is still a triangle wave, the AC RMS component which flows through the output capacitor is calculated as follows:

$$I_{out\_acrms} = \frac{IL_{out\_total\_pp}}{2} \cdot \frac{1}{\sqrt{3}}$$

**Fig. 11. Cancellation effect on output capacitor ripple current normalized to the ripple current of a single phase vs. duty cycle.**
Power Switch Peak Voltage ($D > 0.5$)

The equation for determining the peak voltage on the power switches is the same as for the single case and the condition where the duty cycle is less than 0.5.

Output Rectifier Peak Voltage ($D > 0.5$)

The equation for determining the peak voltage on the output rectifiers is the same as for the single case.

Output Rectifiers Peak Current ($D > 0.5$)

The peak current in the output rectifiers does not change as a function of duty cycle. It is still equal to half of the load current.

Appendix B contains the empirical circuit waveforms for a 200-W 2L interleaved forward converter design. Figs B7, B8, and B9 demonstrate the ripple current cancellation effect with two interleaved power stages. Figs. B10 and B11 show the improvement in the output transient response which is achievable by interleaving power stages.

A. Interleaved Forward Converter with One Output Inductor (1L)

The circuit configuration in Fig. 7 does not allow for an operating duty cycle greater than 0.5. As a result D4 and Lout2 are removable from Fig. 5 provided that the secondary of T2 is connected to the input side of the remaining output inductor. If the duty cycle were to go above 0.5 in Fig. 7, the forward diodes D1 and D3 would create a short across the secondary of the transformers. With the removal of D4 and Lout2 the resultant peak secondary transformer current is now equal to the full load current. The current waveforms for the 1L configuration are depicted in Fig. 12. Table 3 summarizes the equations that are used in Table 6 to compare the 1L interleaved forward converter to the other topologies listed in this paper.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Interleaved Forward (2L)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ipk_s_T1</td>
<td>$\frac{I_{out}}{2}$</td>
</tr>
<tr>
<td>Ipk_p_T1</td>
<td>$\frac{I_{out}}{2 \times N3}$</td>
</tr>
<tr>
<td>Irms_s_T1</td>
<td>$\frac{I_{out}}{2} \sqrt{D_{max}}$</td>
</tr>
<tr>
<td>Irms_p_T1</td>
<td>$\frac{I_{out}}{2 \times N3} \sqrt{D_{max}}$</td>
</tr>
<tr>
<td>Nx_min</td>
<td>$\frac{Vin_{min} \times D_{max}}{Vout + Vd}$</td>
</tr>
<tr>
<td>Icin_acrms</td>
<td>$\frac{I_{out}}{2 \times N3} \sqrt{2 \times D \times (1 - 2 \times D)}$</td>
</tr>
<tr>
<td></td>
<td>$D \leq 0.5$</td>
</tr>
<tr>
<td></td>
<td>$D &gt; 0.5$</td>
</tr>
<tr>
<td></td>
<td>$\frac{I_{out}}{2 \times N3} \sqrt{4 \times (D - 0.5) \times (1 - D)}$</td>
</tr>
<tr>
<td>I_Lout_pp</td>
<td>$\frac{(Vout + Vd) \times (1 - D_{max})}{Lout \times Fs}$</td>
</tr>
<tr>
<td>ILout_total-pp</td>
<td>$\frac{(Vout + Vd) \times (1 - D)}{Lout \times Fs}$</td>
</tr>
<tr>
<td>I_Lout_total_pp</td>
<td>$\frac{2 \times \left( D - \frac{m}{2} \right) \times \left( \frac{m + 1}{2} - D \right)}{D \times (1 - D)}$</td>
</tr>
<tr>
<td></td>
<td>$m = \text{floor}(2 \times D)$</td>
</tr>
<tr>
<td>Icout_acrms</td>
<td>$\frac{I_{Lout _total _pp} \times \left[ \frac{1}{2} \right]}{3}$</td>
</tr>
<tr>
<td>Vpk_Q1</td>
<td>$\frac{Vin_{min}}{1 - D_{max}}$ or $\frac{Vin_{max}}{1 - D_{min}}$</td>
</tr>
<tr>
<td>Vpk_D1</td>
<td>$\frac{Vin_{min} \times D_{max}}{1 - D_{max}} \times \frac{1}{N3}$</td>
</tr>
<tr>
<td>Vpk_D2</td>
<td>$\frac{Vin_{max}}{N3}$</td>
</tr>
<tr>
<td>Ipk_D1</td>
<td>$\frac{I_{out}}{2}$</td>
</tr>
</tbody>
</table>
Comparison of 2L and 1L Transformer RMS Currents

One major benefit of using two output inductors as opposed to one output inductor is that the resulting RMS currents in the transformers are significantly reduced. Consider the following comparison:

2L primary input RMS current:
\[
I_{rms\_p\_T1\_2L} = \frac{I_{out}}{2} \sqrt{D_{max\_2L}}
\]

1L primary input RMS current:
\[
I_{rms\_p\_T1\_1L} = \frac{I_{out}}{N4} \sqrt{D_{max\_1L}}
\]

Ratio of 2L RMS transformer current to 1L RMS transformer current:
\[
\frac{I_{rms\_p\_T1\_2L}}{I_{rms\_p\_T1\_1L}} = \frac{1}{\sqrt{2}}
\]

As a specific example, consider the case where the load current is equal in both circuits and the duty cycle for the 2L power stages is 0.8 with the duty cycle for the 1L power stages equal to 0.4. In this example the turns ratio, N_{x\_min}, for each of the transformers is equal, then:
\[
\frac{I_{rms\_p\_T1\_2L}}{I_{rms\_p\_T1\_1L}} = \frac{1}{\sqrt{2}}
\]

By configuring the circuit with two output inductors it allows operating duty cycles of greater than 50%, reducing the RMS currents in the transformer by a factor of the square root of two, and reduces the conducted EMI produced because the peak currents are reduced.
### Table 3. “1L” Interleaved Forward Converter Equations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Interleaved Forward (1L)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{pk_s_T1}$</td>
<td>$I_{out}$</td>
</tr>
<tr>
<td>$I_{pk_p_T1}$</td>
<td>$\frac{I_{out}}{N4}$</td>
</tr>
<tr>
<td>$I_{rms_s_T1}$</td>
<td>$I_{out} \cdot \sqrt{D_{max}}$</td>
</tr>
<tr>
<td>$I_{rms_p_T1}$</td>
<td>$\frac{I_{out}}{N4} \cdot \sqrt{D_{max}}$</td>
</tr>
<tr>
<td>$N_x_{_min}$</td>
<td>$\frac{V_{in_min} \cdot 2 \cdot D_{max}}{V_{out} + V_d}$</td>
</tr>
<tr>
<td>$I_{cin_acrms}$</td>
<td>$\frac{I_{out}}{N4} \cdot \sqrt{2 \cdot D \cdot (1 - 2 \cdot D)}$</td>
</tr>
<tr>
<td>$I_{L_{out_pp}}$</td>
<td>$(V_{out} + V_d) \cdot (1 - 2 \cdot D_{max}) / L_{out} \cdot F_s$</td>
</tr>
<tr>
<td>$I_{cout_acrms}$</td>
<td>$\frac{I_{L_{out_pp}}}{2} \cdot \frac{1}{\sqrt{3}}$</td>
</tr>
<tr>
<td>$V_{pk_Q1}$</td>
<td>$\frac{V_{in_min}}{1 - D_{max}}$ or $\frac{V_{in_max}}{1 - D_{_min}}$</td>
</tr>
<tr>
<td>$V_{pk_D1}$</td>
<td>$\frac{V_{in}}{N4} \cdot \frac{1}{1 - D_{_max}}$</td>
</tr>
<tr>
<td>$I_{pk_D1}$</td>
<td>$I_{out}$</td>
</tr>
</tbody>
</table>

#### Summary of 2L vs. 1L Interleaved Forward Converters

Advantages of 2L interleaved forward topology vs. 1L interleaved forward topology:
- Reduced transformer peak currents
- Reduced RMS transformer currents by $\sqrt{2}$
- Reduced transformer heating by a factor of 2
- Reduced input capacitor RMS currents
- Reduced output capacitor RMS currents
- Reduced inductor currents
- Reduction of EMI energy due to lower peak currents
- Distribution of heat generating elements

Disadvantages of 2L interleaved forward topology vs. 1L interleaved forward topology:
- Increased component count
- Possible increase in area of components
- Increased peak voltage stress on primary switch when duty cycle is greater than 0.5
- Control complexity of interleaved drive signals, requires greater than 50% duty cycle per switch

#### B. Push-Pull Circuit Topology

Fig. 13 shows a push-pull converter. In general, a push-pull converter would be considered for the same applications as the interleaved forward converter. The same quantities as defined above are presented here for the push-pull topology and are used to identify the drawbacks of the push-pull converter when being compared to the 2L interleaved forward converter. For the push-pull topology the maximum duty cycle for each switch is limited to 0.5 in order to avoid cross conduction between the switches. Typical waveforms for the push-pull topology are depicted in Fig. 14. Table 4 summarizes the equations for the push-pull topology.
**Fig. 13.** Push-pull converter.

**Fig. 14.** Waveforms for push-pull converter ($D = 0.4$).

---

### Table 4. Push-Pull Converter Equations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Push Pull</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{pk_s _T1}$</td>
<td>$I_{out}$</td>
</tr>
<tr>
<td>$I_{pk_p _T1}$</td>
<td>$\frac{I_{out}}{N5}$</td>
</tr>
<tr>
<td>$I_{rms_s _T1}$</td>
<td>$I_{out} \sqrt{\frac{D _\max + \frac{I_{out}}{2} \sqrt{1 - 2 \cdot D _\max}}{}}$</td>
</tr>
<tr>
<td>$I_{rms_p _T1}$</td>
<td>$\frac{I_{out}}{N5} \sqrt{D _\max}$</td>
</tr>
<tr>
<td>$N_x _\min$</td>
<td>$\frac{Vin _\min \cdot 2 \cdot D _\max}{Vout + Vd}$</td>
</tr>
<tr>
<td>$I_{cin _acrms}$</td>
<td>$\frac{I_{out}}{N5} \sqrt{2 \cdot D _\max \cdot (1 - 2 \cdot D _\max)}$</td>
</tr>
<tr>
<td>$I_{_Lout _pp}$</td>
<td>$\frac{(Vout + Vd) \cdot (1 - 2 \cdot D _\max)}{Lout \cdot Fs}$</td>
</tr>
<tr>
<td>$I_{cout _acrms}$</td>
<td>$\frac{I_{_Lout _pp} \cdot \sqrt{1}}{2 \sqrt{3}}$</td>
</tr>
<tr>
<td>$V_{pk_Q1}$</td>
<td>$2 \cdot Vin _\max$</td>
</tr>
<tr>
<td>$V_{pk_D1}$</td>
<td>$\frac{2 \cdot Vin _\max}{N5}$</td>
</tr>
<tr>
<td>$V_{pk_D2}$</td>
<td>$\frac{2 \cdot Vin _\max}{N5}$</td>
</tr>
<tr>
<td>$I_{pk_D1}$</td>
<td>$I_{out}$</td>
</tr>
</tbody>
</table>
Summary of Push-Pull vs. 2L Interleaved Forward Converter

Advantages of 2L interleaved forward converter vs. push-pull topology:
- Reduced transformer peak currents
- Reduced transformer RMS secondary current
- Reduced peak voltage stress on primary switches
- Reduced peak voltage stress on output rectifiers
- Reduced inductor currents
- Reduction of EMI energy due to lower peak currents
- Distribution of heat generating elements

Disadvantages of 2L interleaved forward converter vs. push-pull topology:
- Increased component count
- Possible increase in area of components
- Control complexity of interleaved drive signals, requires greater than 50% duty cycle per switch

C. Half-Bridge Circuit Topology

The main benefit of the half-bridge topology over the previous topologies is that the peak voltage on the power switches is only equal to the input voltage. Referring to Fig. 15, the same quantities listed above are compared against the 2L interleaved forward converter. In the half-bridge topology the maximum duty cycle for each switch is limited to 0.5 in order to avoid cross conduction between the switches. Typical waveforms for the half-bridge topology are depicted in Fig. 16. Table 5 summarizes the equations for the half-bridge topology.

Fig. 15. Half-bridge converter.

Fig. 16. Waveforms for half-bridge converter power stage \((D = 0.4)\).
### Table 5. Half-Bridge Converter Equations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Half Bridge</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ipk_s_T1</td>
<td>Iout</td>
</tr>
<tr>
<td>Ipk_p_T1</td>
<td>Iout/N6</td>
</tr>
<tr>
<td>Irms_s_T1</td>
<td>Iout * √(Dmax) + Iout * √(1 - 2*D)</td>
</tr>
<tr>
<td>Irms_p_T1</td>
<td>Iout * √(2*Dmax)</td>
</tr>
<tr>
<td>Nx_min</td>
<td>Vin_min * 2*Dmax / 2 * (Vout + Vd)</td>
</tr>
<tr>
<td>Icin_acrms</td>
<td>Iout * √(Dmax * (1 - Dmax)) / N6</td>
</tr>
<tr>
<td>I_Lout_pp</td>
<td>(Vout + Vd) * (1 - 2*Dmax) / Iout * Fs</td>
</tr>
<tr>
<td>Iout_acrms</td>
<td>(I_Lout_pp * I) / 2 / √3</td>
</tr>
<tr>
<td>Vpk_Q1</td>
<td>Vin_max / N6</td>
</tr>
<tr>
<td>Vpk_D1</td>
<td>Vin_max / N6</td>
</tr>
<tr>
<td>Vpk_D2</td>
<td>Vin_max / N6</td>
</tr>
<tr>
<td>Ipk_D1</td>
<td>Iout</td>
</tr>
</tbody>
</table>

**Summary of HB vs. 2L Interleaved Forward Converter**

Advantages of 2L interleaved forward converter vs. half-bridge topology:
- Reduced transformer peak currents
- Reduced transformer RMS currents
- Reduction of EMI energy due to lower peak currents
- Reduced peak voltage stress on output rectifiers
- Reduction of EMI energy at higher frequencies due to longer allowable on times
- Reduced inductor currents
- Distribution of heat generating elements

Disadvantages of 2L interleaved forward converter vs. half-bridge topology:
- Increased component count
- Increased peak voltage stress on primary switches
- Possible increase in area of components
- Control complexity of interleaved drive signals, requires greater than 50% duty cycle per switch

Table 6 contains 200-W design examples for each of the buck derived topologies and Table 7 contains 500-W design examples. The following assumptions were made:
- The output inductance values are equal for all topologies (2L output inductors carry only half the load current).
- The duty cycle for the 1L interleaved forward converter is ½ of that for the 2L interleaved forward converter
- The switching frequency is equal to 500 kHz
- The input range is 36 Vdc – 75 Vdc
- The output voltage is 12 V for all topologies.
### Table 6. Comparison Table for 200-W Design Examples

<table>
<thead>
<tr>
<th>Parameter</th>
<th>200 W Topology</th>
<th>Topology</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Forward</td>
<td>Interleaved Forward (2L)</td>
<td>Interleaved Forward (1L)</td>
<td>Push Pull</td>
<td>Half Bridge</td>
</tr>
<tr>
<td>Dmax</td>
<td>0.52</td>
<td>0.52</td>
<td>0.26</td>
<td>0.45</td>
<td>0.45</td>
</tr>
<tr>
<td>Lout – (µH)</td>
<td>3.20</td>
<td>3.20</td>
<td>3.20</td>
<td>3.20</td>
<td>3.20</td>
</tr>
<tr>
<td>Ipk_s_T1 – (A)</td>
<td>16.7</td>
<td>8.3</td>
<td>16.7</td>
<td>16.7</td>
<td>16.7</td>
</tr>
<tr>
<td>Ipk_p_T1 – (A)</td>
<td>11.6</td>
<td>5.8</td>
<td>11.6</td>
<td>6.7</td>
<td>13.4</td>
</tr>
<tr>
<td>Irms_s_T1 – (A)</td>
<td>12.0</td>
<td>6.0</td>
<td>8.5</td>
<td>13.8</td>
<td>13.8</td>
</tr>
<tr>
<td>Irms_p_T1 – (A)</td>
<td>8.3</td>
<td>4.2</td>
<td>5.9</td>
<td>4.5</td>
<td>12.7</td>
</tr>
<tr>
<td>Nx_min</td>
<td>1.44</td>
<td>1.44</td>
<td>1.44</td>
<td>2.49</td>
<td>1.25</td>
</tr>
<tr>
<td>Icin_ac rms – (A)</td>
<td>5.8</td>
<td>1.1</td>
<td>5.8</td>
<td>2.0</td>
<td>6.7</td>
</tr>
<tr>
<td>I_Lout_pp – (A)</td>
<td>3.9</td>
<td>3.9</td>
<td>3.9</td>
<td>0.8</td>
<td>0.8</td>
</tr>
<tr>
<td>llout_total_pp – (A)</td>
<td>N/A</td>
<td>0.3</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Icout_ac rms – (A)</td>
<td>1.1</td>
<td>1.1</td>
<td>1.1</td>
<td>0.2</td>
<td>0.2</td>
</tr>
<tr>
<td>Vpk_Q1 – (V)</td>
<td>75.0</td>
<td>75.0</td>
<td>48.6</td>
<td>150.0</td>
<td>75.0</td>
</tr>
<tr>
<td>Vpk_D1 – (V)</td>
<td>27.1</td>
<td>27.1</td>
<td>33.8</td>
<td>60.2</td>
<td>60.2</td>
</tr>
<tr>
<td>Vpk_D2 – (V)</td>
<td>52.1</td>
<td>52.1</td>
<td>52.1</td>
<td>60.2</td>
<td>60.2</td>
</tr>
<tr>
<td>Ipk_D1 – (A)</td>
<td>16.7</td>
<td>8.3</td>
<td>16.7</td>
<td>16.7</td>
<td>16.7</td>
</tr>
</tbody>
</table>

For this example the max duty cycle for the 1L interleaved forward converter was increased to 0.45.

### Table 7. Comparison Table for 500-W Design Examples

<table>
<thead>
<tr>
<th>Parameter</th>
<th>500 W Topology</th>
<th>Topology</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Forward</td>
<td>Interleaved Forward (2L)</td>
<td>Interleaved Forward (1L)</td>
<td>Push Pull</td>
<td>Half Bridge</td>
</tr>
<tr>
<td>Dmax</td>
<td>0.52</td>
<td>0.52</td>
<td>0.45</td>
<td>0.45</td>
<td>0.45</td>
</tr>
<tr>
<td>Lout – (µH)</td>
<td>3.20</td>
<td>3.20</td>
<td>3.20</td>
<td>3.20</td>
<td>3.20</td>
</tr>
<tr>
<td>Ipk_s_T1 – (A)</td>
<td>41.7</td>
<td>20.8</td>
<td>41.7</td>
<td>41.7</td>
<td>41.7</td>
</tr>
<tr>
<td>Ipk_p_T1 – (A)</td>
<td>28.9</td>
<td>14.5</td>
<td>16.7</td>
<td>16.7</td>
<td>33.4</td>
</tr>
<tr>
<td>Irms_s_T1 – (A)</td>
<td>30.0</td>
<td>15.0</td>
<td>28.0</td>
<td>34.5</td>
<td>34.5</td>
</tr>
<tr>
<td>Irms_p_T1 – (A)</td>
<td>20.9</td>
<td>10.4</td>
<td>11.2</td>
<td>11.2</td>
<td>31.7</td>
</tr>
<tr>
<td>Nx_min</td>
<td>1.44</td>
<td>1.44</td>
<td>2.49</td>
<td>2.49</td>
<td>1.25</td>
</tr>
<tr>
<td>Icin_ac rms – (A)</td>
<td>14.5</td>
<td>2.8</td>
<td>5.0</td>
<td>5.0</td>
<td>16.6</td>
</tr>
<tr>
<td>I_Lout_pp – (A)</td>
<td>3.9</td>
<td>3.9</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
</tr>
<tr>
<td>llout_total_pp – (A)</td>
<td>N/A</td>
<td>0.3</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Icout_ac rms – (A)</td>
<td>1.1</td>
<td>0.1</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
</tr>
<tr>
<td>Vpk_Q1 – (V)</td>
<td>75.0</td>
<td>75.0</td>
<td>65.5</td>
<td>150.0</td>
<td>75.0</td>
</tr>
<tr>
<td>Vpk_D1 – (V)</td>
<td>27.1</td>
<td>27.1</td>
<td>26.3</td>
<td>60.2</td>
<td>60.2</td>
</tr>
<tr>
<td>Vpk_D2 – (V)</td>
<td>52.1</td>
<td>52.1</td>
<td>30.1</td>
<td>60.2</td>
<td>60.2</td>
</tr>
<tr>
<td>Ipk_D1 – (A)</td>
<td>41.7</td>
<td>20.8</td>
<td>41.7</td>
<td>41.7</td>
<td>41.7</td>
</tr>
</tbody>
</table>
IV. SINGLE FLYBACK CONVERTER IN DISCONTINUOUS CONDUCTION MODE (DCM)

Fig. 3 shows a single flyback converter. Table 8 summarizes the design equations that are used to compare it against its interleaved counterpart shown in Fig. 17. More detail on how to derive these equations is given in the following section dealing with the interleaved flyback topology.

**TABLE 8. SINGLE FLYBACK CONVERTER EQUATIONS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Flyback</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{pk_s T1}$</td>
<td>$N^2 * I_{pk_p T1}$</td>
</tr>
<tr>
<td>$I_{pk_p T1}$</td>
<td>$\frac{V_{in min} * T_{on max}}{L_p}$</td>
</tr>
<tr>
<td>$I_{rms_s T1}$</td>
<td>$N^2 * I_{pk_p T1} * \left( \frac{3 T_r}{T_s} \right)$</td>
</tr>
<tr>
<td>$I_{rms_p T1}$</td>
<td>$I_{pk_p T1} * \sqrt{\frac{D}{3}}$</td>
</tr>
<tr>
<td>$N_{x_{min}}$</td>
<td>$\frac{V_{pk_Q1} - V_{in max}}{V_{out} + V_d}$</td>
</tr>
<tr>
<td>$I_{cin_{ac rms}}$</td>
<td>$I_{pk_p T1} * \sqrt{\frac{D}{3}} * \left( 1 - \frac{3D}{4} \right)$</td>
</tr>
<tr>
<td>$I_{cout_{ac rms}}$</td>
<td>$N^2 * I_{pk_p T1} * \left( \frac{3 T_r}{T_s} \right) * \left( 1 - \frac{3 T_r}{4 T_s} \right)$</td>
</tr>
<tr>
<td>$V_{pk_Q1}$</td>
<td>$V_{in max} + N^2 * (V_{out} + V_d)$</td>
</tr>
<tr>
<td>$V_{pk_D1}$</td>
<td>$\frac{V_{in max}}{N^2} + V_{spike}$</td>
</tr>
<tr>
<td>$I_{pk_D1}$</td>
<td>$N^2 * I_{pk_p T1}$</td>
</tr>
</tbody>
</table>

**D. Interleaved DCM Flyback Converter**

The circuit depicted in Fig. 17 is an interleaved flyback converter. The duty cycle for each phase of an interleaved flyback is not limited to less than 50% because the secondaries inherently have high output impedance and resemble a current source. Fig. 18 shows the input and output ripple currents and their intended overlap at an individual phase duty cycle of 60 percent. This section and the following example show that the interleaved flyback converter is applicable to power levels twice as high as the single flyback converter.

---

**Fig. 17. Interleaved flyback converter.**
### E. Design Equations for an Interleaved DCM Flyback Converter

As with the single interleaved flyback, the first step is to understand the balance equations that allow the DCM flyback converter to regulate its output voltage. Fig. 17 shows an interleaved flyback circuit and Fig. 18 the associated current waveforms for DCM operation. Line regulation is achieved by varying the duty cycle of the power switch such that the product of the switch on time and the input voltage is a constant. This results in constant peak inductor current which translates to a constant output power. During the period when Q1 or Q2 is on, energy is transferred from the input capacitor, Cin, to the primary inductance, Lp, of the transformer. The magnitude of this stored energy per phase is given by:

\[ W_{in} = \frac{1}{2} Lp \cdot (I_{pk\_p})^2 \]

where \( I_{pk\_p} \) is the peak primary current for each phase.

No energy is transferred to the secondary circuit during this period. When Q1 is off, all the energy stored in the flyback transformer is delivered, by way of the secondary winding, to the output filter capacitor and load. Because there are two power stages in parallel, each power stage only needs to deliver one half (½) of the total input power. The average input power is given by:

\[ P_{in} = \frac{W_{in1}}{Ts} + \frac{W_{in2}}{Ts} \]

where,

\[ W_{in1} = \frac{Lp1 \cdot I_{pk\_p} \_ T1^2}{2} \]
\[ W_{in2} = \frac{Lp2 \cdot I_{pk\_p} \_ T2^2}{2} \]
\[ Ts = \frac{1}{Fs} \]
With the assumptions that $L_{p1} = L_{p2}$ and $I_{pk_p\_T1} = I_{pk_p\_T2}$, the above equation simplifies to:

$$Pin = \frac{L_{p1} \cdot I_{pk\_p\_T1}^2}{T_s}$$

The peak primary current ($I_{pk\_p\_T1}$) is dependent on the input voltage ($V_{in}$), the primary inductance, $L_p$, and the on time of Q1 ($T_{on}$):

$$I_{pk\_p\_T1} = \frac{V_{in} \cdot T_{on}}{L_p}$$

The average power output is related to the output voltage and load resistance, by:

$$P_o = \frac{V_o^2}{R_L}$$

Taking into account the efficiency of the power converter gives a more accurate calculation for the peak input current.

$$Pin = \frac{P_o}{\eta}$$

where $\eta$ is the efficiency of the power converter.

Substituting for $pin$ and $I_{pk\_p\_T1}$ in the above equations yields:

$$\frac{V_o^2}{\eta \cdot R_L} = \frac{(V_{in} \cdot T_{on})^2}{L_p \cdot T_s}$$

The DC output voltage is therefore:

$$V_{out} = V_{in} \cdot T_{on} \cdot \frac{\eta \cdot R_L}{\sqrt{L_p \cdot T_s}}$$

or

$$V_{out} = V_{in} \cdot D \cdot \frac{\eta \cdot R_L \cdot T_s}{\sqrt{L_p}}$$

$$D = \frac{T_{on}}{T_s}$$

Note that for a discontinuous flyback converter, the output voltage varies directly with both $V_{in}$ and the square root of $R_L$.

Because of the parallel power stages the transformer peak and RMS currents are reduced by a factor of 2.

**F. Power Switch Peak Voltage**

The turns ratio of the transformer is determined by setting an upper limit on the peak voltage seen by the primary switch, $V_{pk\_Q1} = V_{pk\_Q2}$, with some ample margin to accommodate any leakage inductance spikes that may be present on the drain waveform. In general, the peak voltage on the main switches is selected to fit into the lowest voltage rated switches possible.

$$V_{pk\_Q1} = V_{in} + N7 \cdot (V_{out} + V_d)$$

**G. Primary Inductance Selection to Ensure DCM**

In order to guarantee that the power stage remains in the discontinuous conduction mode throughout the entire input voltage range the maximum on time is selected according to the following equation, at $V_{in\_min}$.

$$T_{on\_max} = \frac{(V_o + V_d) \cdot N7 \cdot 0.8 \cdot T_s}{V_{in\_min} + N7 \cdot (V_o \cdot V_d)}$$

$$D_{max} = \frac{T_{on\_max}}{T_s}$$

The primary inductance is then calculated as:

$$L_p = \frac{(V_{in\_min} \cdot T_{on\_max})^2}{P_{out} \cdot 2 \cdot T_s}$$

Here, the output power is divided by two because the above equation is setting the inductance for each power stage and each power stage only needs to deliver half of the total input power.
H. Transformer Primary Peak Current
The transformer primary peak current is equal to:
\[ I_{pk\_p\_T1} = \frac{\text{Vin}\_\text{min}*T_{on\_max}}{L_p} \]

I. Transformer RMS Currents
Calculate the primary RMS current, \( I_{rms\_p\_T1} \):
\[ I_{rms\_p\_T1} = I_{pk\_p\_T1} \frac{D}{3} \]
The DC component of the primary transformer current, \( I_{dc\_p\_T1} \), is:
\[ I_{dc\_p\_T1} = I_{pk\_p\_T1} \frac{D}{2} \]

The secondary currents have the same shape as the primary current. The only adjustments in the equations are to replace the primary peak current with \( N7*I_{pk\_p\_T1} \) and change D to \( T_r/T_s \) where \( T_r \) is the ramp down time of the secondary current. Because the circuit was designed to operate in DCM, \( T_r \) is required to be less than \( T_{off} \) and hence it is not valid to simply replace D by 1-D as would be the case for the continuous conduction mode (CCM).

\[ T_r = I_{pk\_s\_T1} \frac{L_{sec}}{V_{sec}} \]
where,
\[ I_{pk\_s\_T1} = N7*I_{pk\_p\_T1} \]
\[ L_{sec} = L_p \left( \frac{1}{N7} \right)^2 \]
\[ V_{sec} = V_{out} \]
hence,
\[ T_r = I_{pk\_p\_T1} \frac{L_p}{N7*V_{out}} \]

The secondary RMS current is then:
\[ I_{rms\_s\_T1} = N7*I_{pk\_p\_T1} \frac{T_r*F_s}{3} \]
The DC component of the secondary transformer current, \( I_{dc\_s\_T1} \), is:
\[ I_{dc\_s\_T1} = N7*I_{pk\_p\_T1} \frac{T_r*F_s}{2} \]

J. Input Capacitor RMS Current
The AC component of the primary current waveform, \( I_{cin\_acrms} \) which is the AC RMS current that flows through the input capacitors, is calculated in Appendix A. There is not a closed form expression given so implementing the equations in an automated calculation program like MathCAD™ is suggested.

K. Output Capacitor RMS Current
The AC component of the secondary current waveform, \( I_{acrms\_s\_T1} \), which is the RMS current in the output capacitors, is given by:
\[ I_{out\_acrms} = I_{acrms\_s\_T1} \]
\[ I_{out\_acrms} = N7*I_{pk\_p\_T1} \]
\[ \sqrt{\frac{2*T_r*F_s}{3} * \frac{1-3*2*T_r*F_s}{4}} \]
L. Output Rectifier Peak Current

The peak secondary current is equal to the peak diode current

\[ I_{pk\_D1} = N_T * I_{pk\_p\_T1} \]

Summary of Interleaved-Flyback vs. Single-Flyback Converter

Advantages of interleaved flyback converter vs. single flyback:

- Reduced transformer and semiconductor peak currents
- Reduced transformer and semiconductor RMS currents
- Reduced input and output capacitor RMS currents
- Reduction of EMI energy due to lower peak currents
- Distribution of heat generating elements

Disadvantages of interleaved flyback converter vs. single flyback:

- Increased component count
- Possible increase in component area
- Control complexity of interleaved drive signals for Dmax greater than 50%

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Interleaved Flyback</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ipk_s_T1</td>
<td>( N_T * I_{pk_p_T1} )</td>
</tr>
<tr>
<td>Ipk_p_T1</td>
<td>( \frac{Vin_min * Ton_max}{L_p} )</td>
</tr>
<tr>
<td>Irms_s_T1</td>
<td>( N_T * I_{pk_p_T1} * \frac{Tr}{3^3Ts} )</td>
</tr>
<tr>
<td>Irms_p_T1</td>
<td>( I_{pk_p_T1} * \frac{D}{3} )</td>
</tr>
<tr>
<td>Nx_min</td>
<td>( \frac{V_{pk_Q1} - Vin_max}{Vout + Vd} )</td>
</tr>
<tr>
<td>Icin_acrms</td>
<td>( I_{pk_p_T1} * \frac{D}{3} * \left( 1 - \frac{3 * D}{4} \right) )</td>
</tr>
<tr>
<td>D&lt;=0.5;</td>
<td>D&gt;0.5;</td>
</tr>
<tr>
<td>See Appendix A</td>
<td></td>
</tr>
<tr>
<td>Icout_acrms</td>
<td>( N_T * I_{pk_p_T1} * \frac{2^3Tr}{3^3Ts} * \left( 1 - \frac{3 * 2^3Tr}{4^3Ts} \right) )</td>
</tr>
<tr>
<td>Vpk_Q1</td>
<td>( Vin_max + N_T * (Vout + Vd) )</td>
</tr>
<tr>
<td>Vpk_D1</td>
<td>( \frac{Vin_max}{N_T} + V_{spike} )</td>
</tr>
<tr>
<td>Vpk_D2</td>
<td>( \frac{Vin_max}{N_T} + V_{spike} )</td>
</tr>
<tr>
<td>Ipk_D1</td>
<td>( N_T * I_{pk_p_T1} )</td>
</tr>
</tbody>
</table>
M. Interleaved Flyback Design Example

As an example consider the following design specifications for an interleaved flyback converter designed to operate in DCM:

- \( V_{in_{\text{max}}} = 375 \text{ Vdc} \)
- \( V_{in_{\text{min}}} = 85 \text{ Vdc} \)
- \( V_{out} = 12 \text{ V} \)
- \( P_{out} = 200 \text{ W} \)
- \( F_s = 50 \text{ kHz} \)
- \( \eta = 0.85 \)
- \( R_{L_{\text{min}}} = \left(\frac{V_{out}}{2}\right) / P_{out} = 0.72 \Omega \)

Table 10, DCM single flyback converter vs. interleaved flyback converter, summarizes the values for the equations given in Tables 8 and 9. From these comparisons it is evident that the effect of interleaving power stages is to reduce the peak currents and the RMS currents to manageable levels, even for a 200-W example which would normally be considered outside of the reasonable power levels for a DCM flyback converter.

<table>
<thead>
<tr>
<th>TABLE 10. DESIGN VALUES FOR 200-W FLYBACK EXAMPLES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Parameter</strong></td>
</tr>
<tr>
<td>Dmax</td>
</tr>
<tr>
<td>( L_p ) (( \mu \text{H} ))</td>
</tr>
<tr>
<td>( I_{pk_s \ T1} ) (A)</td>
</tr>
<tr>
<td>( I_{pk_p \ T1} ) (A)</td>
</tr>
<tr>
<td>( I_{rms_s \ T1} ) (A)</td>
</tr>
<tr>
<td>( I_{rms_p \ T1} ) (A)</td>
</tr>
<tr>
<td>( N_x_{\text{min}} )</td>
</tr>
<tr>
<td>( I_{cin \ acrms} ) (A)</td>
</tr>
<tr>
<td>( I_{cout \ acrms} ) (A)</td>
</tr>
<tr>
<td>( V_{pk \ Q1} ) (V)</td>
</tr>
<tr>
<td>( V_{pk \ D1} ) (V)</td>
</tr>
<tr>
<td>( V_{pk \ D2} ) (V)</td>
</tr>
<tr>
<td>( I_{pk \ D1} ) (A)</td>
</tr>
</tbody>
</table>
V. HIGH POWER FACTOR (HIGH-PF) INTERLEAVED FLYBACK TOPOLOGY

A useful modification to the circuit in Fig. 17 is to use the DCM flyback converter as an isolated power factor correction (PFC) stage. The modified circuit is shown in Fig. 19. The main modification between Fig. 17 and 19 is that in Fig. 19 $C_{in}$ is very small and as a result of the rectifier bridge and AC input, the voltage across $C_{in}$ is a rectified sine wave at twice the AC line frequency. Also $C_{out}$ is very large in order to suppress the line frequency ripple voltage on the output and to withstand a holdup time design requirement. In Fig. 19 the converter is operated in discontinuous conduction mode and the bandwidth of the control loop is intentionally much less than the line frequency so as to make the on time constant throughout one half of the line cycle. By operating the converter and control loop in this manner the average input current from the line resembles the wave shape of the line voltage, which by definition results in high power factor correction. With the converter operating in discontinuous conduction mode, this control technique allows unity power factor when used with converter topologies like flyback, Cuk, and SEPIC [3]. The instantaneous and average input current for one line cycle is shown in Fig. 20.

---

**Fig. 19.** High power factor (high-PF) interleaved flyback converter.

**Fig. 20.** (A) Input waveforms for high-PF interleaved flyback converter power, (B) $Q_1$ power switch on and off times, (C) $Q_2$ power switch on and off times, (D) secondary current waveform for high-PF interleaved flyback converter power stages.
VI. CONCLUSION

In recent years the usefulness of interleaving power stages has become apparent. The most well known application is in the powering of state-of-the-art microprocessors, commonly referred to as voltage regulator modules (VRMs). In VRM applications the power stages are non-isolated from their input to their output. This paper presented the benefits that interleaved topologies can have for isolated applications and in doing so has shown that the two inductor interleaved forward converter topology or the interleaved flyback converter topology are appropriate choices for many high power applications.

REFERENCES

[8] UCC28220/1 Data Sheet, Texas Instruments, (SLUS544)
APPENDIX A.
CALCULATION OF THE AC RMS INPUT CURRENT FOR THE INTERLEAVED FLYBACK CONVERTER

This program calculates the ac rms current of two ramp waveforms which have the same duty cycle, but are 180 degrees out of phase from one another.

\[ \text{Vin} := 85 \]
\[ L_p := 156 \times 10^{-6} \]
\[ Ts := \frac{1}{50000} \]
\[ D := 0.51 \]
\[ \text{Ton1} := D \times Ts \]
\[ \text{Ton2} := \text{Ton1} \]
\[ I_{pk} := \frac{\text{Vin} \times \text{Ton1}}{L_p} \]
\[ I_{pk} = 5.558 \text{ Amps} \]

\[ f_1(t) := \begin{cases} \frac{I_{pk}}{\text{Ton1}} & \text{if } t \leq \text{Ton1} \\ 0 & \text{otherwise} \end{cases} \]

\[ f_2(t) := \begin{cases} \frac{I_{pk}}{\text{Ton2}} & (t + 0.5 \times Ts) \text{ if } 0 \leq t \leq (\text{Ton2} - 0.5 \times Ts) \\ \frac{I_{pk}}{\text{Ton2}} & (t - 0.5 \times Ts) \text{ if } t > 0.5 \times Ts \\ 0 & \text{otherwise} \end{cases} \]

\[ I_{rms} := \sqrt{\frac{1}{0.5 \times Ts} \int_0^{0.5 \times Ts} (f_1(t) + f_2(t))^2 \, dt} \]
\[ I_{rms} = 3.266 \text{ Arms} \]

\[ I_{dc} := \frac{1}{0.5 \times Ts} \left[ \int_0^{0.5 \times Ts} (f_1(t) + f_2(t)) \, dt \right] \]
\[ I_{dc} = 2.861 \text{ Adc} \]

\[ I_{ac rms} := \sqrt{I_{rms}^2 - I_{dc}^2} \]
\[ I_{ac rms} = 1.575 \text{ Arms} \]
APPENDIX B.
TWO INDUCTOR INTERLEAVED FORWARD CONVERTER DESIGN EXAMPLE

Specifications:
- \( V_{\text{IN}} = 36\, \text{V to 75\, \text{V}} \)
- \( V_{\text{UVLO-ON}} = 34\, \text{V} \pm 4\% \)
- \( V_{\text{UVLO-OFF}} = 32\, \text{V} \pm 4\% \)
- \( V_{\text{OVLO-OFF}} = 85\, \text{V} \pm 4\% \)
- \( V_{\text{OVLO-ON}} = 83\, \text{V} \pm 4\% \)
- \( V_{\text{OUT}} = 12\, \text{V} \pm 3\% \)
- \( V_{\text{ripple}} < 1\% \)
- \( P_{\text{OUT}} = 200\, \text{W} \)
- \( I_{\text{OUT,MAX}} = 16.7\, \text{A} \)
- \( f_{\text{SW}} = 500\, \text{kHz (per phase)} \)
- Isolation: 500 V
- PWM controller (UCC28221)
- Form factor: ½ brick

N. Topology: Interleaved Forward with Resonant Reset

The example schematic is shown in Fig. B1. The selection of the power stage is covered below. For information regarding the selection of the components around the PWM control chip refer to the application section in Reference 11.

O. Transformer Design

The transformer area product equation given in Reference 10 on page 4 through 8 provides an estimation of the required core size. In this example the transformer core was smaller than the predicted size from the area product estimate, but its operation and suitability for this application was verified at the extreme operating conditions. The transformer is a custom design from Payton America Inc (part number, 50863). The specifications are:
- Number of primary turns = 7 turns
- Primary magnetizing inductance = 35 \( \mu \text{H} \)
- Secondary number of turns = 5 turns
- Primary auxiliary winding = 5 turns

P. Input capacitor Selection

Referring to Table 6, the input capacitor AC RMS ripple current is 1.1 Arms at low line. The maximum AC RMS ripple current in the input capacitors occurs at high line. Evaluating the AC RMS ripple current equation at Vin-max yields a maximum current of 2.98 Arms. The selected film capacitors have an RMS current rating of 12 Amps which easily satisfies this requirement.

Q. Output Inductor Selection

The output inductor is equal to 3.2 \( \mu \text{H} \), which yields a peak-to-peak output ripple current in each phase of 6.39 A at high line and 4.5 A at low line. This amount of ripple current is on the high side, but by factoring in the benefits of ripple current cancellation due to the interleaved power stages, the actual peak-to-peak ripple current seen by the output capacitor is only 4.3 A at high line and 0.343 A at low line.

R. Output Capacitor Selection

Because of the reduced peak-to-peak ripple current seen by the output capacitors, it is possible to use output capacitors with higher ESR than would be allowed for a single forward converter with the same amount of output inductance. In this example, the design specifications dictate that the design have less than 1% total output ripple voltage under worst case conditions, which is at high line. It is customary to allow the resistive portion of the output capacitor to account for half of the output ripple voltage specification. Hence, the maximum allowable equivalent series resistance (ESR) of the output capacitor is 0.014 \( \Omega \). The example design used three capacitors with 0.045 \( \Omega \) of ESR each. Each capacitor has a capacitance of 82 \( \mu \text{F} \).
EXPERIMENTAL RESULTS OF 2L INTERLEAVED FORWARD CONVERTER

S. Circuit Schematic

Fig. B1. 2L interleaved forward converter design example.
T. Layout

Fig. B2: Top view of PCB layout.

Fig. B3. Bottom view of PCB layout.
U. Drain Voltage Waveforms

Vin = 36 V, Iout = 16.7 A

Fig. B4. Q1 and Q2 drain voltages (Vin = 36 V, Iout = 16.7 A).

Vin = 48 V, Iout = 16.7 A

Fig. B5. Q1 and Q2 drain voltages (Vin = 48 V, Iout = 16.7 A).

Vin = 75 V, Iout = 16.7 A

Fig. B6. Q1 and Q2 drain voltages (Vin = 75 V, Iout = 16.7 A).

V. Output Inductor Peak-to-Peak Ripple Current

I_Lout1

I_Lout2

I_Cout

Vin = 36 V, Iout = 8 A

Fig. B7. Output inductor ripple currents and capacitor ripple current (Vin = 36 V, Iout = 8 A).

Vin = 48 V, Iout = 8 A

Fig. B8. Output inductor ripple currents and capacitor ripple current (Vin = 48 V, Iout = 8 A).

Vin = 75 V, Iout = 8 A

Fig. B9. Output inductor ripple currents and capacitor ripple current (Vin = 75 V, Iout = 8 A).
**W. Transient Response 2 Phases and then 1 Phase**

![Graph showing transient response with 2 phases active.](image)

**Fig. B10. Output transient response with 2 phases active (Vin = 48 V, Iout = 5 A to 8 A).**

![Graph showing transient response with 1 phase active.](image)

**Fig. B11. Output transient response with only one phase active (Vin = 48 V, Iout = 5 A to 8 A).**

**X. Efficiency Curves**

![Graph showing efficiency vs. output power.](image)

**Fig. B12. Efficiency vs. output power.**
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
<th>URL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplifiers</td>
<td>Audio</td>
<td><a href="http://www.ti.com/audio">www.ti.com/audio</a></td>
</tr>
<tr>
<td>Data Converters</td>
<td>Automotive</td>
<td><a href="http://www.ti.com/automotive">www.ti.com/automotive</a></td>
</tr>
<tr>
<td>DSP</td>
<td>Broadband</td>
<td><a href="http://www.ti.com/broadband">www.ti.com/broadband</a></td>
</tr>
<tr>
<td>Interface</td>
<td>Digital Control</td>
<td><a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a></td>
</tr>
<tr>
<td>Logic</td>
<td>Military</td>
<td><a href="http://www.ti.com/military">www.ti.com/military</a></td>
</tr>
<tr>
<td>Power Mgmt</td>
<td>Optical Networking</td>
<td><a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a></td>
</tr>
<tr>
<td>Microcontrollers</td>
<td>Security</td>
<td><a href="http://www.ti.com/security">www.ti.com/security</a></td>
</tr>
<tr>
<td></td>
<td>Telephony</td>
<td><a href="http://www.ti.com/telephony">www.ti.com/telephony</a></td>
</tr>
<tr>
<td></td>
<td>Video &amp; Imaging</td>
<td><a href="http://www.ti.com/video">www.ti.com/video</a></td>
</tr>
<tr>
<td></td>
<td>Wireless</td>
<td><a href="http://www.ti.com/wireless">www.ti.com/wireless</a></td>
</tr>
</tbody>
</table>

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated