The switching element, Q, in a SEPIC converter must have a voltage rating high enough to handle the maximum input voltage plus the output voltage not to mention any leakage-inductance-induced spike that is inevitably present. You can approximate the required voltage rating of the MOSFET using Eq. 14.

View all the equations here.
View all the calculated values here.

Where \( V_{DS} \) = the required drain-to-source voltage rating of the MOSFET.

The other parameters governing the selection of the MOSFET include the RMS current given by Eq. 15, as well as the total gate charge and ON resistance \( (R_{DS(ON)}) \) to minimize the switching losses.

The sum of conduction loss and switching loss \( (PQ_{Vinmin}) \) in the MOSFET at \( V_{INMIN} \) is given by Eq. 16:

and the total losses \( (PQ_{VinMAX}) \) in the MOSFET at \( V_{INMAX} \) are calculated using Eq. 17:

**DIODE SELECTION**

The MOSFET package heat dissipation capability should be greater than the maximum of either of the two PQ equations (Eq. 16 or Eq. 17), where \( R_{DSQ} \) = ON resistance, \( Q_{GD} \) = Gate Drain charge, and \( I_{GATE} \) = MOSFET gate driver sourcing/sinking current. A device such as the Si7850DP from Vishay meets the needs to serve as a switch that can withstand up to 60 V.

The waveforms in Fig. 5 show the MOSFET drain voltage and gate voltage at a 40-V input voltage and 1-A output current. This shows that the drain voltage is the sum of the input voltage and the output voltage.

When the primary switch is OFF, the diode conducts the energy stored in the coupled inductors. During this time, the output capacitors also are charged. The main parameters to be considered while selecting the diode include reverse blocking voltage, forward current, reverse recovery time \( (t_{rr}) \) and forward voltage drop. Schottky rectifiers have a lower forward voltage drop than typical PN devices; however, their reverse blocking voltage is less.

The peak reverse voltage \( (V_D) \) that the device will be subjected to is equal to the maximum input voltage plus the output voltage. Thus, the diode reverse voltage rating should be greater than the value calculated using Eq. 18. Because all current to the output capacitor and load must flow through the diode, the average forward diode current \( (I_{DAVG}) \) is equal to the steady-state load current.

**CURRENT LIMITING AND CURRENT SENSING**

The average current rating is given by Eq. 19:

Furthermore, the average current rating of diode D should be greater than value calculated using Eq. 19. The 8TQ080SPBF diode from Vishay is a good match for this design.

The current-sense voltage obtained from the external current-sense resistor is compared with the 300-mV threshold current-limit comparator of the MAX15004. This provides the overcurrent protection to the switch and avoids the saturation problems in the transformer or inductors.

**PROGRAMMABLE SLOPE COMPENSATION**

To select the current-sense resistor value, divide the threshold value by the peak inductor current \( (I_{LPK}) \) at the desired current limit point typically 120% of \( I_{LPK} \) calculated by Eq. 20. In this design, a 190-mV current-limit threshold is used to improve the efficiency and to reduce the power rating of the resistor.
This ground-referenced resistor must be a low inductance type and have a rated power level to meet the requirement. For this application, a parallel combination of two 30-mΩ, 1-W IRC LRC-LR2010LF-01-R030-F power resistors is used. Current spikes caused by the trace leakage inductance and the reverse recovery of the diode (D) could trip the current-sense latch and prematurely turn off the switch. This unwanted spike can be suppressed by adding a small RC filter for effective leading-edge blanking. For this application, a 100-ns external low-pass filter is added. To reduce the current-limit threshold to 190 mV, a 40.1-kΩ resistor is added between the Reg5 and CS pins of the controller.

Slope compensation is required for open-loop stability in a current mode system with 50% or greater duty cycles. Insufficient slope compensation results in subharmonic oscillations at the output at half the switching frequency. Slope compensation can be achieved by adding a compensating ramp to the sensed inductor current ramp at the PWM comparator input. The exact amount of the compensating ramp voltage is determined by the down slope of the inductor current. Experience shows that exact magnitude of the ramp should be half of down slope of inductor current. In the MAX15005A, designers have the flexibility of programming compensating slope with a simple capacitor.

The first step in implementing slope compensation is to calculate the inductor down slope amps per second using Eq. 21:

**LOOP COMPENSATION**

Then, calculate the capacitance value using Eq. 22.

For this application, 180 pF is appropriate. Waveforms in Fig. 6 show the current-sense voltage and slope compensating ramp at 2.5-V input and an output current of 0.875 A.

The MAX15005A has an internal, high-performance (100 dB, 1.6-MHz unity-gain bandwidth) operational amplifier that serves as the error amplifier. This allows users to compensate externally for desired crossover frequency for different inductor and capacitor values. The control transfer function from output to current-sense voltage is defined by Eq. 23, Eq. 24 and Eq. 25. (See Eq. 23, above)

and

(See Eq. 24, above)

\[ D_1 = (1 - D) \]  \hspace{1cm} (25)

Load pole and ESR zero calculations are done using Eq. 26.

As with boost and flyback converters, one RHP zero is present in SEPIC converters due to energy transfer from the output capacitor when SW is ON, and its frequency can be calculated using Eq. 27.

Due to this RHP zero, the system crossover frequency \( (FCV) \) must be reduced well before \( FRHZ \), (i.e., to approximately one-sixth of \( FRHZ \)). This can be done by compensation components \( RF, CF \) and \( CCF \) (R11, C19 and C20, respectively, in Fig. 2 of Part 1). This network has one zero at:

one pole at the origin, and another high frequency pole at:

Once desired crossover frequency \( FCV \) is decided, \( RF \) is selected to program the error amplifier gain to achieve desired \( FCV \). To select the value, calculate the gain of the power stage at the desired crossover frequency using the previous control transfer function and Eq. 28. Calculate the \( CF \) and \( CCF \) values using Eq. 29 and Eq. 30, respectively.

where \( FCV \) is the smaller of \( FRHZ/6 \) or \( FLOAD/6 \).

**CALCULATED VALUES**

The waveforms in Fig. 7 and Fig. 8 show the SEPIC supply’s load transient response and the line transient response, respectively. The output voltage ripples less than 3% of the output voltage with a 50% load step. This converter recovers smoothly after the line transients.

During cold-crank starts in automotive applications, the battery voltage can go as low as 2.5 V. This SEPIC design can supply regulated power to the load even with this low battery voltage. In such a case, the waveforms in Fig. 8 show the cold-crank condition of 12.6 V to 2.5 V, with a low-output voltage ripple and an output current of 0.875 A. The graph in Fig. 9 shows the efficiency for different loading conditions at different input voltage levels.

In the final design, here are the actual calculated values for a converter in the example shown. Referenced equation numbers are included for each equation.

\[ C17 = 100 \, \text{pF} \]

**REFERENCES :**

R10 = 56 kΩ

For more SEPIC converter examples, visit [www.maxim-ic.com](http://www.maxim-ic.com).

Fig. 5. Waveforms of MOSFET drain and gate voltage with a 40-V input and 1-A output.

Fig. 6. Waveforms of the current sense voltage and slope compensating ramp with a 2.5 V input and 0.875-A output.
Fig. 7. Waveforms of the SEPIC supply’s load transient response and the line transient response.

Fig. 8. Waveforms show the cold crank condition of 12.6 V to 2.5 V, with a low output voltage ripple and an output of 0.875 A.
Fig. 9. Efficiency vs. load current for 2.5-V to 40-V input voltages.
\[ V_{DS} = 1.15 \times (V_{INMAX} + V_{OUT}) \]  
\[ IQ_{RMS} = \sqrt{\left( I_{DC}L^2 + II_{PK}^2 + I_{DC}L \times II_{PK} \right) \times \frac{D_{MAX}}{3}} \]  
\[ PQ_{\_V_{INMIN}} = IQ_{RMS}^2 \times R_{DSQ} \times D_{MAX} + (V_{INMIN} + V_{OUT}) \times II_{PK} \times \frac{Q_{GD} \times F_S}{I_{GATE}} \]  
\[ PQ_{\_V_{INMAX}} = \left( \frac{IQ_{RMS} \times D_{MIN}}{D_{MAX}} \right)^2 \times R_{DSQ} \times D_{MIN} + (V_{INMIN} + V_{OUT}) \times II_{PK} \times \frac{Q_{GD} \times F_S}{I_{GATE}} \times \frac{D_{MIN}}{D_{MAX}} \]  
\[ V_D = 1.2 \times (V_{INMAX} + V_{OUT}) \]  
\[ ID_{AVG} = I_{DC}L \times (1 - D_{MAX}) + 0.5 \times \Delta I \times (1 - D_{MAX}) \]  
\[ R_{SENSE} = \frac{190mV}{1.2 \times II_{PK}} \]  
\[ M_C = \frac{V_{OUT} \times R_{SENSE} \times 10^{-3}}{t} \]  
\[ C_{SLOPE} = \frac{2.5 \times 10^{-9} A}{M_C} \]  
\[ V_o(s) = \frac{V_{IN} \times F_M}{3R_{GS} \times D_i^2} \times \frac{\left[ -D \times C_s \times L^2 \times s^3 + 2D_i^2 \times C_s \times L \times D^2 \times s + R_o \times D_i^2 \right]}{R_o \times D_{EN}(s) + F_M \times V_{IN} \times \left[ -D \times C_s \times L \times s \times T_s \times s^3 + A + B + \frac{R_o \times T_s}{L_s} + \frac{1 - D^2}{D_i^2} \right]} \]  
\[ D_{EN}(s) = L^2 \times C_s \times C_{OUT} \times s^4 + L^2 \times C_{OUT} \times s^3 + L \times \left[ D^2 \times C_{OUT} + D_i^2 \times C_{OUT} + 2 \times C_s \times D_i^2 \right] s^2 + \frac{L}{R_o} \left[ D^2 + D_i^2 \right] s + D_i^2 \]  
\[ D_i = (1 - D) \]  
\[ R_F = \frac{V_{OUT}}{V_{CS}} \times (F_{CV}) \times R_1 \]  
\[ F_{LOAD} = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT}} \]  
\[ F_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR} \]  
\[ F_{RH2} = \frac{(1 - D)^2 \times R_{LOAD}}{2\pi \times L \times D \times 0.5} \]  
\[ C_f = \frac{1}{2\pi \times F_{ESR} \times R_F} \]
LOOP COMPENSATION

Where $A =$
\[
2D_1^2 \times C_s \times T_s \times R_o + \frac{1-D^2}{D_1^2} \times C_s \times L_s + \frac{D}{D_1^2} \times C_{\text{OUT}} \times \frac{L}{s^2}
\]

$B =$
\[
-T_s \times D^2 + \frac{R_o \times C_{\text{OUT}}}{D_1} + \frac{D \times L}{D_1^2 \times R_o}
\]

CALCULATED VALUES

\[C_{17} = 100 \, \text{pF}\]
\[R_{10} = 56 \, \text{k}\Omega\]

\[D_{\text{MAX}} = \frac{V_{\text{OUT}} + V_D}{V_{\text{INMIN}} + V_{\text{OUT}} + V_D - IL(R_L + R_{\text{DSQ}} + R_{\text{SENSE}})} = 84.59\]

\[L = L1, L2 = \frac{V_{\text{INMIN}} - IL(R_L + R_{\text{DSQ}} + R_{\text{SENSE}})}{2\Delta IL \times F_s} \times D_{\text{MAX}} = 15 \, \mu\text{H}\]

\[C_{\text{IN}} = \frac{\Delta I L}{4 \times \Delta V_{\text{IN}} \times F_s \times 0.5} = 4.7 \mu\text{F}/50 \, \text{V}\] ceramic + 470 \mu\text{F}/50 \, \text{V}
 electrolytic capacitors (C1, C2)

\[C_{\text{OUT}} = \frac{I_{\text{OUT}} \times D_{\text{MAX}}}{\Delta V_{\text{OUT}} \times 0.7 \times F_s} = 5 \times 10 \mu\text{A}/16 \, \text{V}\] ceramic and 180 \mu\text{F}/16\text{V}
 electrolytic capacitors (C7-C12)

\[C_s = \frac{I_{\text{OUT}} \times D_{\text{MAX}}}{\Delta V_{\text{OUT}} \times 0.9 \times F_s} = 3 \times 10 \mu\text{F}/50 \, \text{V}\] ceramic
 capacitors (C4-C5, C6)

\[I_{\text{Q RMS}} = \sqrt{(I_{\text{DC}} L^2 + I_{\text{LPR}}^2 + I_{\text{DC}} \times L \times I_{\text{LPR}}) \times \frac{D_{\text{MAX}}^3}{3}} = 8.68 \, \text{A (SI7850DP MOSFET)}\]

\[V_D = 1.2(V_{\text{INMIN}} + V_{\text{OUT}}) = 62.4 \, \text{V} \] (8TQ080SPBF Schottky diode)

\[R_{\text{SENSE}} = \frac{190 \, \text{mV}}{1.2 \times I_{\text{LPR}}} = 15 \, \text{m}\Omega/2 \, \text{W} \] (2X 30m\Omega/1)

\[C_{\text{SLOPE}} = \frac{2.5 \times 10^{-9} \, \text{A}}{M_C} = 180 \, \text{pF} \] (C14)

\[R_f = \frac{V_{\text{OUT}}}{V_{\text{CS}}} \times (F_{\text{CV}}) \times R_1 = 1.5 \, \text{K} \] (R11)

\[C_f = \frac{10}{2\pi \times F_{\text{CV}} \times R_f} = 100 \, \text{nF} \] (C19)

\[C_{\text{CF}} = \frac{1}{2\pi \times F_{\text{ESR}} \times R_f} = 270 \, \text{pF} \] (C20)