SEPIC Converters

Solve Automotive Power Needs

Today’s automotive electronic systems provide new comfort and convenience functions. However, the electronic circuits that deliver the various functions have different power management needs that can be supplied by SEPIC converters.

SINGLE-ENDED PRIMARY INDUCTANCE CONVERTER (SEPIC) TOPOLOGY IS A GOOD CHOICE FOR AUTOMOTIVE POWER SYSTEMS THAT REQUIRE AN OUTPUT VOLTAGE BETWEEN THE LOW AND HIGH VALUES OF THE INPUT VOLTAGE. SEPIC TOPOLOGY FITS THIS APPLICATION BECAUSE ITS DUTY RATIO CAN BE VARIED AROUND 50% TO PROVIDE AN OUTPUT VOLTAGE THAT IS EITHER BELOW OR ABOVE THE INPUT VOLTAGE. ADDITIONALLY, COMPARED TO FLYBACK CONVERTERS, SEPIC CONVERTERS AVOID THE PROBLEMS WITH LEAKAGE INDUCTANCE AND SNUBBERS.

Fig. 1 shows the basic SEPIC topology. In the steady-state during the switch (SW) on-time, energy is stored in inductor L1. The inductor currents IL1 and IL2 ramp up at a slope determined by the input voltage and the inductances L1 and L2. The L2 inductor current ramps up at the same rate through coupling capacitor CS and SW. The CS positive terminal is at ground potential, and the voltage across L2 is VIN, which is the same as the voltage across L1. At this point in time, the output capacitors supply the load current while diode D is reverse biased. When the SW turns off, diode D is forward biased, and it conducts the energy stored in both inductors to the load while also charging the output capacitor. The voltages across the inductors are clamped to output voltage with the same inductor down-slope currents.

Current-mode PWM controllers, such as the MAX15004/15005, operate over an automotive input voltage range from 4.5 V to 40 V (load-dump). The input voltage can go down as low as 2.5 V (cold-crank) after startup if VCC is supplied by an external bias voltage. The controllers integrate all the building blocks necessary for implementing fixed-frequency SEPIC converters. By operating the converters at a high switching frequency, designers can use smaller power components. Additionally, the converters include easy slope compensation, synchronization, hiccup-up current limit and overvoltage protection features to reduce the number of external components needed in the system.

To optimize SEPIC converter performance, let’s examine the design procedures to select the component values for the controller and evaluate the performance with some measurements in a practical design. The typical specifications are used to demonstrate the actual design. The system specs are VIN = 6 V to 40 V.
and $V_{\text{OUT}} = 12 \text{ V/1 A}$; the input voltage can go down as low as 2.5 V in cold-crank condition once $V_{\text{CC}}$ is supplied through $V_{\text{OUT}}$. With $V_{\text{IN}}$ as low as 2.85 V, the circuit delivers 85% of its rated output power.

Fig. 2 shows the schematic developed with the above specifications that can power an automotive infotainment display.

**POWER SECTION DESIGN**

Voltage-mode control was passed over in favor of current-mode control, because current-mode control responds immediately to line voltage changes and provides inherent overcurrent protection for the switching device. Due to its simpler dynamics and inherent protection features, a peak current-mode control architecture is used in the MAX15005A. Peak current-mode control compares the amplified output-voltage error with the primary inductor current signal. Using the MAX15005A pulse-width modulator (PWM), the primary inductor current ramp is compared against the amplified output-voltage error.

The inner current control loop contains a small current-sense resistor that senses the primary switch current. The resistor transforms this current waveform into a voltage signal that is fed directly into the inverting input of the PWM comparator. The slope-compensated voltage is summed inside the chip and then fed to the PWM comparator to avoid subharmonic oscillations when duty ratios are greater than 50%. This inner loop determines the response to input voltage changes. The outer voltage control loop involves comparing a portion of the output voltage to a reference voltage at the input of the internal error amplifier. The amplified error voltage is then connected to the noninverting input of the PWM comparator. The PWM comparator output drives a MOSFET driver after overcurrent, overvoltage and thermal-protection logic.

Peak current-mode control requires simpler compensation, has pulse-by-pulse current limiting, and has better dynamic line regulation. In order to limit peak currents through components, continuous conduction mode (CCM) was chosen. In the CCM, RMS currents in the coupled inductor, the switch and the diode can be half as compared to currents in discontinuous conduction-mode operation, requiring the larger components. Because the output ripple current is less than it would be if discontinuous mode were used, the output capacitors also are smaller. Continuous conduction mode, however, requires higher magnetizing inductances to stay in CCM throughout the entire operating range and maintain a right-half-plane zero in its transfer function.

Selecting the switching frequency is the foundation of the optimization and design compromise flow to determine all the component values. A higher switching frequency leads to smaller component sizes with fair efficiency, while lower frequency increases the achievable efficiency but will require slightly bulkier components. The MAX15005A switching frequency (FS) is programmable from 15 kHz to 1 MHz.
using an external resistor (RT) and capacitor (CT) network. Ideally, FS can be set below 150 kHz so that the third harmonics can remain below AM band, thus minimizing RF noise (interference). Some applications, such as VFD converters, require very low EMI and prefer switching frequencies as low as 20 kHz. The converter switching frequency (FS) is externally synchronizable to further assist in keeping the EMI low and away from the tuned AM band.

After selecting the power circuit topology, the next decision is to determine the maximum duty cycle (DMAX) of the switch, Q, in Fig. 2. The duty cycle is the ratio of on-time of Q to total period (D = TON/T). In a CCM SEPIC converter, the maximum duty cycle will determine the component current ratings and impact the maximum voltage stress on the switching elements. The MAX15005A can provide a maximum duty cycle of 85% with a minimum on-time of 100 ns.

The dc transfer function of a CCM SEPIC converter is given by Eq. 1 and Eq. 2:

\[ D_{\text{MAX}} = \frac{V_{\text{OUT}} + V_D}{V_{\text{INMIN}} + V_{\text{OUT}} + V_D - I_L(R_L + R_{\text{DSQ}} + R_{\text{Ssense}})} \]  

\[ D_{\text{MIN}} = \frac{V_{\text{OUT}} + V_D}{V_{\text{INMAX}} + V_{\text{OUT}} + V_D - I_L(R_L + R_{\text{DSQ}} + R_{\text{Ssense}})} \]  

Where:
- \( V_{\text{OUT}} \) = Output voltage
- \( V_D \) = Diode drop
- \( R_L \) = Inductor DCR value.

The maximum duty cycle occurs at \( V_{\text{INMIN}} \) and is determined to be 84.5% when the minimum on-time of the switch is 1.08 μs (both of these values are within the limits of the IC). Fig. 3 shows the RTCT oscillator waveform, gate drive waveform and output voltage at 6-V input, 12-V output and 1-A output.

**INDUCTOR SELECTION**

In SEPIC converters, both the inductors are subject to the same voltages and same ripple currents. Thus, both inductors have the same values. However, peak current rating would be different. These days, coupled inductors are readily available with 1-to-1 turn ratios with a coupling factor nearly equal to 1. This saves board space and eliminates the need for a snubber. With coupled inductors, the value of inductance will be half of the individual inductors. The coupled inductance value is selected using Eq. 3.

\[ L = L_1, L_2 = \frac{V_{\text{INMIN}} - I_L(R_L + R_{\text{DSQ}} + R_{\text{Ssense}})}{2 \times \Delta I_L \times F_S} \times D_{\text{MAX}} \]  

Where:
- \( \Delta I_L \) = Acceptable inductor ripple.

Due to the dc isolation capacitor between input and output, average inductor currents \( I_1, I_2 \) are equal to the input current and the load current, respectively. Use the following equation to calculate and ensure the peak inductor current \( I_{L(pk)} \) is lower than the saturating current specification of the coupled inductor:

\[ I_{L(pk)} = 1.2 \left[ I_{\text{OUT}} \times \frac{D_{\text{MAX}}}{1 - D_{\text{MAX}}} \eta \right] + I_{\text{OUT}} + \Delta I_L \]  

Where:
- \( \eta \) = assumed efficiency.

The required RMS current rating of the inductors that causes the heat losses and temperature rise is given by Eq. 5:

\[ I_{L(rms)} = \sqrt{I_{dc}^2 \frac{\Delta I_L^2}{3}} \]  

Where:
- \( I_{dc} \) = \( IL(pk) - \frac{\Delta I_L}{2} \)

This design uses a 15-μH MSD1278-153ML coupled inductor from CoilCraft.
INPUT AND OUTPUT CAPACITORS SELECTION

The input currents in SEPIC architectures are continuous. The inductor reduces the ripple currents as well as the required input capacitance. However, a higher value for the input capacitor may be necessary to ensure better impedance interaction with the source input. RMS current rating and the capacitor value needed to maintain specified input ripple are given by Eq. 6 and Eq. 7, respectively.

\[
\Delta C_{\text{IN}} = \frac{\Delta I_L}{\sqrt{12}} \tag{6}
\]

\[
C_{\text{IN}} = \frac{\Delta I_L}{4 \times \Delta V_{\text{IN}} \times F_s \times 0.5} \tag{7}
\]

Where:
\(\Delta V_{\text{IN}}\) is the acceptable input ripple.

The SEPIC output capacitor has to supply the full load current when SW is ON (and the inductors are charging). The output capacitor thus sees large ripple currents, and it must be able to handle the RMS current given by Eq. 9:

\[
\Delta I_{\text{out}} = I_{\text{OUT}} \sqrt{\frac{V_{\text{OUT}}}{V_{\text{RMIN}}}} \tag{9}
\]

Additionally, the output capacitor value should be selected to maintain the specified output voltage ripple, which includes both ESR ripple and capacitive ripple given by Eq. 10 and Eq. 11.

\[
C_{\text{OUT}} = \frac{I_{\text{OUT}} \times D_{\text{MAX}}}{\Delta V_{\text{OUT}} \times 0.7 \times F_s} \tag{10}
\]

\[
\text{ESR}_{\text{OUT}} = \frac{0.3 \times \Delta V_{\text{OUT}}}{I_{\text{OUT}}} \tag{11}
\]

The waveforms in Fig. 4 show the output and input voltage ripples at 6-V input and 1-A output current. Output peak-to-peak ripple is 128 mV and input peak-to-peak ripple is 25 mV, which are less than 1% of their final values.

COUPLING CAPACITOR SELECTION

The coupling capacitor, \(C_s\), provides dc isolation between input and output. Because the load is isolated from input, the total supply shutdown current can be reduced below 10 µA by turning off the MAX15004/5 through its ON/OFF pin. The coupling capacitors need to carry large ripple currents. Thus, non-polar ceramic capacitors, which have excellent ESR, ESL and ripple current ratings, are best suited to the task. The value of the coupling capacitor depends on the maximum ripple across it and can be calculated using Eq. 13:

\[
C_s = \frac{I_{\text{OUT}} \times D_{\text{MAX}}}{\Delta V_{\text{OUT}} \times 0.9 \times F_s} \tag{13}
\]

Because it carries large ripples, the capacitor of choice should be a low ESR, low ESL ceramic-type device. The value of the coupling capacitor depends on the maximum ripple across it and can be calculated using Eq. 13.