Microwave Integrated Circuits using Thin-Film BST

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**Advanced Opaque Thin-Film Technology for Radar and Communications**

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**UCSB:**
- Bob York: circuits and devices
- Jim Speck: interfacial studies, microscopy
- David Clarke: micromachining and lift-off
- Amit Nagra (post-doc): circuits and devices
- Padmini Periaswamy (post-doc): growth and material science
- Troy Taylor (GSR): materials, devices, characterization
- Pete Hansen (GSR): materials, devices, characterization
- Erich Erker (GSR): BST multiplier circuits
- Bruce Liu (GSR): Tunable filter circuits and MEMs

**ANL:**
- Orlando Auciello: Material science and growth
- Stephen Streiffer: Material science and growth
- Dave Kaufmann: MOCVD and characterization
- Robert Erck: MOCVD construction
- Allen R. Krauss: surface ion scattering
- Peter Baumann (post-doc): MOCVD growth
- Jaemo Im (post-doc): RF Magnetron Sputtering
- Anil Dhote (post-doc): surface ion scattering
- James Giumarra (GSR): MOCVD growth

**HRL:**
- Jonathan Lynch: circuits and systems applications
Outline

• Thin-Film BST Varactors
  
  Features and applications

• MICs using Thin-Film BST
  
  Distributed Phase Shifter/Delay Lines
  
  Frequency Multiplier

• Increasing Q – The Holy Grail
  
  Improved processing technology
  
  Conductor contributions
  
  Material and growth optimization

• Conclusions
Inexpensive varactor diode replacement technology

Optimal use of thin-film BST for circuit performance

Strong potential for integration into existing IC processes

Cost + Performance + Manufacture

Processing issues for this technology are largely unresolved
# Millimeter-wave Thin-Film Varactor Technologies

<table>
<thead>
<tr>
<th></th>
<th>GaAs</th>
<th>BST</th>
<th>MEMS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Tunability</strong></td>
<td>High (3:1 typ)</td>
<td>Moderate (2-3:1 typ)</td>
<td>Low (&lt;1.5:1)</td>
</tr>
<tr>
<td><strong>(at high Q)</strong></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td><strong>RF Loss</strong></td>
<td>Moderate (Q&lt;60 typ.)</td>
<td>Moderate (Q&lt;30 current)</td>
<td>Very Good (Q&lt;200)</td>
</tr>
<tr>
<td><strong>(Q)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Control Voltage</strong></td>
<td>&lt;10V (unipolar)</td>
<td>10-20 V (bipolar)</td>
<td>50-100 V (bipolar)</td>
</tr>
<tr>
<td><strong>Tuning Speed</strong></td>
<td>Fast</td>
<td>Fast</td>
<td>Slow</td>
</tr>
<tr>
<td><strong>Power Handling</strong></td>
<td>Poor</td>
<td>Excellent</td>
<td>Excellent</td>
</tr>
<tr>
<td><strong>IMD</strong></td>
<td>Poor</td>
<td>Poor</td>
<td>Excellent</td>
</tr>
<tr>
<td><strong>Packaging</strong></td>
<td>Hermetic</td>
<td>??</td>
<td>Vacuum!!</td>
</tr>
<tr>
<td><strong>Cost</strong></td>
<td>Moderate to High</td>
<td>Low?</td>
<td>Low?</td>
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</table>
Which applications **intelligently** exploit BST Varactors?

- Devices requiring rapid, continuous tuning at low-voltages
  - Phase-shifters and Delay lines
    - (Antenna arrays, Delay-locked loops, Phase linearization)
- Frequency conversion devices requiring fast nonlinearity
  - Frequency multipliers, upconverters, dividers
- Inexpensive broadband or frequency-agile components
  - Tunable matching networks, splitter/combiners

**Advantages:** Low cost, cheap packaging, high-power, at good performance

Which applications **do not**?

- Devices requiring high Q-factors (currently)
  - Tunable filters, phase-shifters in certain applications, VCOs
- Low-voltage devices requiring low IMD
Good Applications of BST

360 deg. Delay Lines
• Phased Arrays
• Delay-Locked Loops
• Phase Modulators

Reflection Phase Shifter
• Phased Arrays

Small Delay Elements
• Phase Linearization
  (open- and closed-loop)

Tunable Matching Networks
• Broadband power-splitters/combiners
• Post-production tuning

Frequency Conversion
• Multipliers
• Up-converters

Pro: High-power, Continuous phase, Low voltage
Con: IMD, loss

Pro: Inexpensive, good power handling, exploits nonlinearity

Pro: low voltage, cheap, parts savings/inventory

Pro: inexpensive mm-wave access
Con: loss/Q
Interdigitated capacitors

Salient features
- BST deposited directly on substrate
- BST film thickness 0.1-0.5 µm
- Interdigitated metal electrodes on BST
- Finger spacing ~1 µm
- Finger width ~ 2 µm

Advantages
- Avoids problem of growth on bottom electrode
- Easy to fabricate/integrate
- High power handling capability

Disadvantages
- Large fringing capacitance reduces tunability
- Large finger spacing results in lower applied control/tuning field
- High control voltages (~100 V)
This presentation will describe our research on parallel plate BST capacitors.

**Parallel Plate capacitors**

**Salient features**
- BST deposited directly on electrode
- BST film thickness 0.1-0.2 µm
- Top electrode stripe width 2 µm

**Advantages**
- Very small fringing capacitance
- Maximum utilization of film tunability
- Lower control voltages (15-30 V)
- Power handling adjustable at expense of control voltage

**Disadvantages**
- Bottom electrode hard to process
- Fabrication/integration process is more complicated
Considerations

Desirable Features of a Viable Thin-Film Varactor Technology

- Reproducibility
- Inexpensive substrates
- Standard growth/processing steps
- Low tuning voltages
- Compatible with low-cost packaging

Integrated Monolithic Capacitors using Sputtered/MOCVD material on low-cost substrates
**Choice of substrate**

**Substrate effects on BST growth**
- Growth template for BST film
- Substrate thermal expansion and resultant BST stress
- Withstand high temperatures in oxidizing environment

**Substrate effects on circuit performance**
- Dc leakage through substrate
- Loss tangent at microwave frequencies
- Substrate dielectric constant
- Bias dependence of properties

**Possible choices:** Silicon, sapphire, quartz, MgO, Strontium Titanate

**Reasons for silicon**
- Demonstrated compatibility with BST film deposition procedures and prior demonstrations of good BST properties on silicon
- Existing information on BST growth conditions could be exploited to quickly optimize film properties
- Doped silicon is a bad microwave substrate but high resistivity silicon has reasonably low loss tangents
- Low cost and easy availability of high resistivity silicon (>3000 ohm-cm)
- Possibility to use micromachining to reduce effective dielectric constant
Micromachining of Silicon

Key Results

- Micromachining can be used to reduce the substrate losses and conductor losses
- Micromachined substrates have lower effective dielectric constant
Electrode and Integration Issues

**Electrode Issues**
- Oxidation resistance
- Withstand high temperatures ($T_{\text{deposition}} \approx 550-700^\circ \text{C}$)
- Sufficient conductivity
- Adhesion
- Minimal diffusion
- SiO$_2$ void formation
- Pt hillock formation (compressive stress)
- Dielectric isolation
- Stabilized adhesion layer (complete oxidation of TiO$_2$)

**Processing Issues**
- Pt etching
- Reactive Ion Etching (RIE)
- Plasma etching
- RIE and plasma damage
- HF etching
- Mesa formation by etching
- Si$_3$N$_4$/metal deposition
- Repeated solvent cleaning for lithography
- High device yield for working transmission lines

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**Electrode stack for BST device incorporation**

- Top Electrode
  - BST
  - Pt
  - TiO$_2$
  - SiO$_2$
  - Substrate

Pt: bottom electrode
TiO$_2$: adhesion
SiO$_2$: diffusion
Substrate: low $\varepsilon$, High resistivity

Robust electrode stack required in order for BST thin film varactor technology to hold any future promise
**He**\(^{++}\) **RBS Conditions**

- BST/Sapphire
- 2.5 – 2.65 MeV
- He dose of 20\(\mu\)C/run
- Beam Current ~ 10-25 nA
- 7° sample tilt angle

No peak overlap due to Pt (Channel ~500)

Clear look at RBS Spectra

All RBS data courtesy of Dr. Peter Revesz at the Cornell Center for Materials Science
Stoichiometry vs. Sputtering Pressure

Composition of the film determines its electrical properties

Ba, Sr, and Ti species have pressure dependent fluxes due to their different masses (scattering)

**SPUTTERING CONDITIONS**

$T_{\text{Surface}} = 565 \, ^\circ\text{C}$  \hspace{0.5cm}  Rf power = 150 W (3.3 W/cm$^2$)

90/10 Ar/O$_2$ (sccm)  \hspace{0.5cm} thickness ~ 75-100 nm

![Graph showing Ba/Sr vs. Pressure]
**Dielectric Constant vs. Pressure**

**SPUTTERING CONDITIONS**

\[ T_{\text{Surface}} = 650 \, ^\circ \text{C} \quad \text{Rf power} = 150 \, \text{W} \, (3.3 \, \text{W/cm}^2) \]

90/10 Ar/O\textsubscript{2} (sccm) \quad \text{thickness} \sim 100 \, \text{nm}

Dielectric Constant at 1 Mhz

Sputtering pressure and resulting film composition strongly influences dielectric properties

Further Studies:

*Flux/pressure/temperature dependent film growth parameters*
Scanning Antennas

Mechanical Scanning

- Simple design
- Cost Effective
- Slow
- Single beam
- Susceptible to jamming

Electronic Scanning

- Complex design
- Expensive
- Fast scanning
- Multiple beam capability
- Can reject interference/jamming
Commercial Applications of Phased-Arrays

- Collision Avoidance Radars
- Ground terminal for LEO/MEO Satellite communication
- Mobile satellite communication for automobiles/aircraft
- Wireless point-to-point and point-to-multipoint links
- Surveillance and traffic-control radars
- Spot-beam satellite down-links
Collision-Avoidance Radars

Challenges:
- low-cost (<$500)
- Small aperture (77-150 GHz)
The Phase Shifter cost is a significant array cost driver.
Transmission-line

Equivalent circuit

\[ Z_0 = \sqrt{\frac{L}{C}} \quad \omega < \sqrt{\frac{2}{LC}} \]

\[ \nu = \frac{1}{\sqrt{LC}} \]

Loaded Transmission-line

Varactor provides variable phase delay:

\[ \Delta \phi = \omega \sqrt{L(C + C_d)} \]
A.S. Nagra and R.A. York, “Distributed Analog Phase Shifters with Low Insertion Loss,”
IEEE Transactions on Microwave Theory and Techniques, vol. 47, No. 9, pp.1705-1711, September 1999

- For every substrate there is an optimal loading factor for lowest loss
- Phase shifters on substrates with lower dielectric constant have lower losses
OBJECTIVES

- Fabricate large area, polycrystalline BST films on “inexpensive” substrates, with:
  - High tunability >2:1
  - Low loss tangent \(\tan \delta <0.01\)
  - High device yield 100 %

- Integrated Parallel-plate tunable capacitors
  - Efficient utilization of tuning voltage

- Integration on Si substrates
  - Large area, inexpensive

- RF Sputtering or CVD
  - Proven scaleable and reproducible growth
BST Parallel-Plate Capacitor: Layout Challenges

Problems

• Phase shifters require small capacitors
• Small active areas required
• Top electrode lithography crucial
• Tight alignment tolerances

Solution--- two capacitors in series

Ease of processing
larger contact area
no contact to bottom electrode

Defect density
higher yield
graceful degradation

Power handling
double allowed RF voltage swing
Ka-band Loaded-Line Phase Shifter

- High-yield device layout (modified liftoff)
- BST/Pt/HR-Si Parallel-Plate process

Note: Non-optimized Circuit!!!

Phase shift: 0 to 160° @ 30 GHz  
\[ V_{bias} = 0 \text{..} 20 \text{ V} \]

Insertion loss: -5.5 dB @ 30 GHz

Return loss: <-18 dB, 0-30 GHz

Photo of UCSB Circuit
Influence of Loss and Tunability

Tunability: how much we can vary capacitance of film
\( C_{\text{max}}/C_{\text{min}} \) (or \( e_{\text{max}}/e_{\text{min}} \))

Device loss and tunability are important
**INITIAL PROCESS METHOD**

**Starting Material**
- Pt
- BST
- Substrate

(a)

**BST Etch with HF.**
- Pt
- BST
- Substrate

(b)

**Deposit SiN (PECVD, 250°C)**
- Pt
- BST
- SiN
- Substrate

(c)

Possible Layer Formation Between BST/SiN.

**SiN Etch with RIE (SF6/Ar/O2), Pt Etch using Cl2.**

(d)

**SiN Deposition, Window Etch with RIE (SF6/Ar/O2)**

(e)

**Top Contact Metallization**

(f)

Window Etch
Very critical step that defines capacitor areas. Very likely to damage the BST film. Possibility of leaving a thin SiN layer (lowers overall capacitance & tunability) and/or thinning the film.
Planar BST Capacitor Design

\[ R_s \approx \rho \frac{3w}{t_{Pt}l} \]

\[ C = \frac{1}{2} \frac{\varepsilon_r \varepsilon_0 wl}{t_{BST}} \]

\[ G = \omega C \tan \delta \]

\[ C_{fringe} \approx \frac{\varepsilon_{SiN} \varepsilon_0 w(3w + l)}{t_{SiN}} \]
**Conductor Losses**

\[ Q_c \equiv \frac{1}{\omega R_s C} = \frac{1}{\omega} \left[ \frac{2t_{Pt}t_{BST}}{3 \rho w^2 \varepsilon_r \varepsilon_0} \right] \]

**Dielectric Losses**

\[ Q_d \equiv \frac{\omega C}{G} = \frac{1}{\tan \delta} \]

**Total Q-factor for Device**

\[ Q_{tot} \equiv \frac{\text{Im}(Z)}{\text{Re}(Z)} = \frac{1}{\frac{1}{Q_c Q_d^2} + \frac{1}{Q_c} + \frac{1}{Q_d}} \]

**Effect of capacitor layout on RF losses**

- \( t_{Pt} = 1000\text{Å} \)
- \( t_{BST} = 750\text{Å} \)
- \( \varepsilon_r = 250 \)
- \( \tan \delta = 0.016 \)

- \( w = 2 \text{ microns} \)
- \( w = 5 \text{ microns} \)
Projected Q Limits

Conductor Losses

- $Q_{ser}$ vs Frequency, GHz
- $w = 1\mu m$, $2\mu m$, $3\mu m$
- $t_{Pt} = 2000\AA$
- $t_{BST} = 750\AA$
- $\varepsilon_r = 250$

Total Losses

- $Q_{tot}$ vs Frequency, GHz
- $w = 1\mu m$
- $\tan\delta = 0.002$, $0.005$, $0.01$, $0.02$
**Effects of RF process on C-V data**

- Good uniformity in the original and processed films
- Tunability not significantly affected by device processing
- Loss tangent shows significant degradation after device process
- RIE Steps appear to be responsible
Loss model for BST Test Capacitors

$R_s$: fixed series resistance due to bottom Pt electrode
$G$: leakage due to free/mobile charge
$C$: Intrinsic BST capacitor with associated dielectric loss

Total Q-factor of the BST device in terms of loss components

\[
\frac{1}{Q_{\text{total}}} = \frac{1}{Q_{\text{leakage}}} + \frac{1}{Q_{\text{BST}}} + \frac{1}{Q_{\text{Pt}}}
\]
Leakage loss mechanism

$Q_{\text{leakage}} = \frac{\omega C}{G}$

- $Q_{\text{leakage}}$ increases linearly with frequency which implies that $G$ is not frequency dependant.

- Leakage losses limit the overall Q-factor at low frequencies.
- Leakage losses increase with increasing bias voltage.
- Leakage Q-factor not of concern in the GHz frequency range.
Series resistance losses

**Quality Factor**

\[ Q_{Pt} = \frac{1}{\omega R_s C} \]

\[ R_s = \frac{\rho_{pt} W}{t_{pt} l} \]

- Pt losses become important at higher frequencies
- Series resistance can be lowered by layout- long stripes with narrow widths
- Increasing Pt thickness helps reduce series losses

**Graph**

- BST/ Pt/ Sapphire
- Total Device Quality factor
- Frequency (Hz)
- Quality Factor
- Frequency losses decrease faster for thinner Pt at high frequencies
Extracting Pt effects

- Used at high frequencies where $Q_{\text{leakage}}$ can be neglected
- Simultaneously deposit BST on 2 samples with different Pt thickness (ratio $n$)
- Intrinsic BST losses should be identical due to simultaneous deposition
- Ratio of metal losses known

$n$: ratio of Pt metal thickness

$Q_{\text{tot}1}, Q_{\text{tot}2}$: measured total $Q$

\[
\frac{1}{Q_{\text{tot}1}} = \frac{1}{Q_{\text{BST}}} + \frac{1}{Q_{\text{pt}1}}
\]

\[
\frac{1}{Q_{\text{tot}2}} = \frac{1}{Q_{\text{BST}}} + \frac{1}{n Q_{\text{pt}1}}
\]

2 linear equations in 2 unknowns -> solve for $Q_{\text{BST}}$
Predicted and measured device Q

Assumed values
\[ C = 37 \text{ pF} \]
\[ R_s = 1.1 \text{ ohms} \]
\[ G = 1.94 \text{ nS} \]

Theoretical Q-components
\[ Q_{\text{leakage}} = 60 \text{ at } 500 \text{ Hz} \]
\[ Q_{\text{pt}} = 40 \text{ at } 100 \text{ MHz} \]
\[ Q_{\text{BST}} = 150 \]

- Theoretical \( Q_{\text{leakage}} \) and \( Q_{\text{pt}} \) assumed to have ideal frequency response
- Theoretical \( Q_{\text{BST}} \) assumed to have no frequency dependence
- Reasonably good agreement with measured \( Q_{\text{total}} \)
- Some evidence of dispersion at high frequencies
Same Distributed Circuit Topology as Phase Shifter!

- Tripler Circuit
- Preliminary test (non-optimized)
- Circuit driven at 8GHz
- Conversion to 24GHz
- Extremely good power handling

\[ P_{\text{out, max}} = \sim 15 \text{ dBm} \]

Conversion loss = \sim 20 dB

demonstrates versatility of the distributed circuit approach
• Progress in RF Magnetron sputtering of BST
• RF device processing and electrode stacks
  
  Developed new processed for monolithic BST circuits, avoiding etching damage to films

• Distributed phase-shifter concept
  
  First monolithic BST phase shifters at 20GHz with >30 deg/dB
  First monolithic BST-based multipliers

• Future Work
  
  Improve understanding of material dispersion
  Next generation BST circuits using optimized devices and processes
Thank you!