Microwave Integrated Circuits using Thin-Film BST

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Abstract — We discuss the development and potential applications of a microwave varactor technology using thin-film BST on inexpensive substrates. BST thin-films have been developed and optimized specifically for microwave integrated circuits, using both MOCVD-grown and RF magnetron-sputtered films. The material optimization efforts have concentrated on achieving high tunability and simultaneous low loss, and also developing robust electrode systems for circuit fabrication on silicon substrates. We present advances in monolithic microwave integrated capacitors and application to high performance and low-cost phase-shifter circuits. Efforts in frequency multiplication devices will also be presented.

I. INTRODUCTION
Thin-film BST has several properties that make it attractive for high-frequency applications, including:

- **High dielectric constant:** in the range of 200-300 typically, useful for small-area bypass capacitors and MEMS switches.
- **Field dependent permittivity:** as much as 4:1 variation in permittivity, useful for tunable RF circuits such as phase-shifters, filters, and VCOs.
- **“Fast” polarization response:** allows for rapid tuning and frequency conversion devices.
- **High breakdown field:** typically >2 \times 10^6 V/cm, allows for large bipolar voltage swings and hence good power-handling.

Another important feature of this technology—especially pertinent in comparison to semiconductor-based alternatives—is the wide variety of substrate materials available for thin-film deposition. Using inexpensive substrates and demonstrated high-volume deposition technologies, we believe that very low cost microwave circuits can be realized using thin-film BST. In this paper, we discuss some preliminary considerations for constructing useful microwave integrated circuits using discrete variable capacitors (varactors), based on thin-film BST technology.

II. POTENTIAL APPLICATIONS
Desirable electrical characteristics for a thin-film varactor technology include high tunability, low RF loss tangents (high Q-factors), and good power-handling capability. The tuning voltage range would ideally be scaleable and commensurate with the desired power handling specification. Equally important for commercial viability are issues of reproducibility, use of proven high-volume deposition technologies, and the use of standard integrated-circuit processes for foundry compatibility.

There are currently three competing technologies for discrete integrated microwave varactors that can satisfy some fraction of these requirements. Some important features are contrasted in Table I. Note that the entries reflect data appropriate to general-purpose, continuously variable varactors, suitable for mm-wave operation in a wide assortment of varactor applications. This caveat rules out, for example, hyperabrupt-doping profiles for widely tunable Si or GaAs varactors, since these tend to be too lossy for practical use in, say, a phase-shifter application. Similarly, in some cases it may be possible to enhance the Q-factor well beyond the values listed as “typical”, but this tends to come at the expense of reduced tunability.

<table>
<thead>
<tr>
<th></th>
<th>GaAs</th>
<th>BST (2:1 typ.)</th>
<th>MEMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tunability (at high Q)</td>
<td>High (4:1 typ.)</td>
<td>Moderate (2:1 typ.)</td>
<td>Low (&lt;1.5:1)</td>
</tr>
<tr>
<td>RF Loss (Q)</td>
<td>Moderate (Q&lt;10 typ.)</td>
<td>Moderate (Q&lt;50 current)</td>
<td>Very Good (Q&lt;200)</td>
</tr>
<tr>
<td>Control Voltage</td>
<td>&lt;20V (unipolar)</td>
<td>10-20 V (bipolar)</td>
<td>50-100 V (bipolar)</td>
</tr>
<tr>
<td>Tuning Speed</td>
<td>Fast</td>
<td>Fast</td>
<td>Slow</td>
</tr>
<tr>
<td>Power Handling</td>
<td>Poor</td>
<td>Excellent</td>
<td>Excellent</td>
</tr>
<tr>
<td>IMD</td>
<td>Poor</td>
<td>Poor</td>
<td>Excellent</td>
</tr>
<tr>
<td>Packaging</td>
<td>Hermetic</td>
<td>??</td>
<td>Vacuum</td>
</tr>
<tr>
<td>Cost</td>
<td>Moderate</td>
<td>Low?</td>
<td>Low?</td>
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It is apparent that there are pros and cons for each technology, and therefore the choice depends strongly on the particular application requirements. There are two classes of applications which appear to favor, in broad terms, thin-film BST varactors: 1) those that require rapid, continuous tuning at low voltages, such as phase-shifters or delay lines, and 2) frequency conversion devices, such as frequency multipliers or upconverters, that exploit the “fast” capacitive nonlinearity. Neither of these applications can be addressed by MEMS varactor devices, which are too slow. In both categories, BST-based components can be designed for much higher
power-handling capacity than a comparable GaAs-based varactor. On the other hand, applications demanding very high Q-factors—such as narrowband tunable filters for communications, or even phase shifters if lowest possible insertion loss is an important objective—are not appropriate for implementation with BST varactors, at least at present, due to persistently high material losses in the microwave range. Furthermore, the same nonlinearity that affords frequency conversion devices can be a drawback for linear components such as phase shifters due to intermodulation distortion (IMD)—the generation of unwanted third-order mixing products within or across neighboring frequency bands.

In comparison to semiconductor alternatives thin-film BST devices promise to be extremely competitive in terms of cost, without a significant sacrifice in performance for many applications. In order to fully exploit this advantage, careful attention must be paid to the choice of substrate, deposition methods, circuit design, and packaging.

III. CHOICE OF SUBSTRATE

There are several candidate substrates for microwave integrated circuits using BST films. Our work has thus far concentrated on high-resistivity (HR) Silicon, for the following reasons: 1) strong interest in BST for DRAM applications has demonstrated a compatibility with BST film deposition procedures and prior demonstrations of good BST properties on silicon; 2) this existing information on BST growth conditions could be exploited to quickly optimize film properties; 3) although doped silicon is a poor microwave substrate, HR silicon has reasonably low loss tangents; 4) HR silicon (>3000 ohm-cm) is widely available at low cost; and 5) silicon afford the possibility of using micromachining to reduce effective dielectric constant, which is helpful in lowering transmission-line losses.

Figure 1 – Comparison of transmission-line losses on silicon for various configurations on coplanar waveguide.

Special care is required when implementing low-loss high frequency transmission-lines on Silicon. A parasitic Schottky diode is formed when the transmission-line metalization is in direct contact with the substrate, leading to excessive losses and undesired leakage paths if the fields extend into undepleted semiconductor. In addition, such transmission-lines show a bias-dependence to electrical properties such as characteristic impedance and wave velocity, which greatly complicates measurements and calibration. Attempts to overcome the leakage problem by including an insulating film between the metal and semiconductor result in a parasitic MOS structure that can exacerbate losses due to charge inversion, as shown in fig. 1. The best solution appears to be the use of micromachining techniques to remove the substrate in the regions of significant field penetration. This is a unique advantage of Silicon substrates in comparison to other inexpensive insulating substrates.

IV. DEVICE LAYOUT AND PROCESSING

Discrete BST varactors can be realized in a vertical (parallel-plate) or planar (interdigital electrode) configuration. In general, interdigital devices are simpler to fabricate and integrate into circuits, but suffer from reduced tunability (due to large fringing capacitance) and higher control voltages. Based on the observations of Section II, we believe that integrated parallel-plate devices are especially attractive for most microwave and millimeter-wave applications. Vertical devices have lower control voltages and higher tunabilities and the control voltage or power handling capacity are easily manipulated through control of the material thickness.

Figure 2 – Layout (plan view and cross section) of an integrated parallel-plate varactor structure.

The fabrication of vertical BST varactors is similar to most standard IC capacitor technologies, except that the electrical properties of the dielectric material (BST) are very sensitive to processing, and the high temperature growth step forces the use of refractory base electrodes of limited conductivity, leading to a potentially significant loss contribution. These electrodes have also proved difficult to etch, limiting the permissible thicknesses and hence further exacerbating losses.
Our initial efforts at process development and vertical device integration have focused on the use of two series-connected devices as shown in fig. 2, using platinum base electrodes. In this approach, the devices are first isolated using a wet etch of the BST followed by an ion-milling of the Pt base electrode. The BST/Pt “island” is then encapsulated by SiN, through which holes are dry etched (RIE) to define the top contacts area. A typical C-V curve for a 100nm film of Ba$_{0.8}$Sr$_{0.2}$TiO$_3$ on 100nm of platinum are shown in fig. 3.

![C-V curve](image)

**Figure 3**— Capacitance-voltage characteristics for 100nm film on Pt-coated HR Si (inset: photograph of monolithic device)

V. MATERIAL AND INTEGRATION ISSUES

BST thin-film technology is still relatively immature, with numerous problems to be solved. Fig. 4 shows a canonical device cross section illustrating the complexity of the problem. In addition to growth optimization of the BST material itself, the electrodes and electrode-BST interfaces are sources of difficulty, as well as the electrode-substrate interface.

![Device cross section](image)

**Figure 4**— Device cross section illustrating relevant integration issues.

Platinum base electrodes are most commonly used for oxidation resistance and compatibility with high temperature growth. However, special care must be taken to avoid excessive compressive stress in the Pt which can lead to hillock formation, which in turn can lead to device shorting. Another pernicious difficulty involves adhesion of the Pt electrode to the substrate, sometimes leading to process-induced delamination. Special care must be taken the development of the diffusion barriers and adhesion layers to solve these problems. For the sub-electrode stack shown in fig. 4, we have found that careful control of SiO$_2$ growth parameters, and stabilization (complete oxidation) of the TiO$_2$ layer, is essential for a high yield process.

For material deposition, we believe that sputtering and CVD techniques are especially promising for the development of low-cost microwave circuits. To date, most of our work has used sputtered BST. In either case, careful study of the influence of growth parameters on material properties, and correlation with device (electrical) properties, is required. This involves a complex parameter-space that most researchers have only begun to explore. As a first step, conditions to achieving stoichiometric polycrystalline films have been established, as shown in fig. 5.

![Influence of gas pressure on BST stoichiometry](image)

**Figure 5**— Influence of gas pressure on BST stoichiometry for sputtered films (100nm films grown at 565 °C, 90/10 Ar/02 sccm, 50/50 Ba/Sr target).

VI. THIN-FILM PHASE SHIFTERS

Several groups [1-7] are now investigating the possibility of implementing phase shifter circuits using BST. In these circuits the BST either forms the entire microwave substrate [1,3] on which the conductors are deposited (thick films/bulk crystals), or a fraction of the substrate with thin BST films sandwiched between the substrate and conductors [2,4-7]. In contrast, our approach relies on discrete, vertical BST capacitors periodically loading a transmission line. When designed correctly [8-10] this structure behaves like a synthetic transmission line whose phase velocity can be controlled by changing the value of the external loading capacitors. The parallel plate capacitor topology utilizes the tunability of the BST film effectively and requires much lower control voltages. The periodic loading allows the structure to be optimized for good loss performance. Also, since the transmission lines are fabricated on lower dielectric constant substrates such as high resistivity silicon, the conductor losses are reduced.

The schematic of the proposed phase shifter circuit is shown in figure 6(a). For frequencies much below the
Bragg frequency, this structure behaves like a synthetic transmission line [8-10] with modified propagation velocity and characteristic impedance. The properties of the synthetic transmission line depend on the inductance per unit length (which remains unchanged from that of an unloaded line) and the total capacitance per unit length (modified due to loading by BST capacitors). For the phase shifter application the value of the loading capacitors is chosen such that the impedance variation is small but by utilizing the correct number of sections the phase shift can be made as large as desired.

![Equivalent circuit for varactor-loaded transmission line](image1)

Figure 6 – (a) equivalent circuit for varactor-loaded transmission line. (b) Photograph of monolithic tripler circuit using coplanar waveguide.

The Ka-band phase shifter circuit was fabricated on high resistivity silicon (4 kΩ-cm) using standard monolithic fabrication techniques. The unloaded CPW had a characteristic impedance of 100Ω, which was reduced to 50Ω after loading with BST varactors (zero bias capacitance of 96 ff). The length of the unit cell (spacing between diodes) is chosen to be 340 mm resulting in a Bragg frequency of 55 GHz. In order to obtain a phase shift of 160° at 20 GHz, 9 identical cells are connected in series resulting in a total length of 3.06 mm. CPW center conductor and gap dimensions of 15 mm and 150 mm respectively are used here. In order to preserve the symmetry of the structure, the periodic loading capacitors are implemented using two devices (48 ff each) connected in parallel from the CPW center conductor to either ground plane, as shown in fig. 6(b).

Figure 7 shows the differential phase shift (with respect to the zero bias insertion phase) as a function of frequency for several bias values. As is expected for a variable velocity transmission line, the circuit produces a phase shift that varies linearly with frequency. The circuit is capable of continuous 0-160° phase shift at 30 GHz with any desired resolution. The maximum insertion loss at 30 GHz occurs at zero bias and is only 5.8 dB, as shown in fig. 7. The return loss is less than 12 dB over all phase states.

Using measured data for the BST varactors, the simulated phase shift was 155°, in good agreement with the measured data. The simulated insertion loss was 4.8 dB, which is about 1 dB lower than the measured data.

This disparity between the measured and simulated insertion loss results is due to the inability of the simulations account for parasitic losses in the silicon.

![Relative phase shifter at different bias states](image2)

Figure 7 – Relative phase shifter at different bias states, and worst-case insertion loss and reflection coefficient for the circuit of fig. 6.

An important observation from the simulations is that the bulk of the phase shifter insertion loss is due to the low quality factor of the BST capacitors (Q~15). Further improvements in BST film quality should lead to phase shifters with even better insertion loss performance. Fig. 8 shows predicted loss performance versus the effective device loss tangent, which includes both conductor and material loss contributions (inverse of the total Q-factor). Compelling results will be obtained when the device Q approaches 100.

![Projected total loss for a 360 degree delay line on Silicon](image3)

Figure 8 – Projected total loss for a 360 degree delay line on Silicon, as a function of effective device loss tangent (inverse of total device Q-factor), assuming a 2.5:1 tunability.
VII. DISTRIBUTED FREQUENCY MULTIPLIERS

By operating the BST-loaded transmission-line of fig. 6 under large signal RF drive conditions, harmonic generation can be obtained. We have explored distributed frequency multipliers analytically using generalized telegraph equations, introducing a simple second order polynomial model for the voltage dependence of the capacitance:

\[ C_i(V) = C_0 + C_2V^2 \]  \hspace{1cm} (1)

For simplicity, the capacitors are assumed to be uniformly distributed over the length of the line. Some mathematical manipulation gives a system of two differential equations of first order for the complex amplitudes of first and third harmonic.

\[ \frac{\partial V_1}{\partial x} = A + A_2|V_1|^2 + 2|V_3|^2 V_1 + A_1 V_1^2 V_3 \] \hspace{1cm} (2 a, b)

\[ \frac{\partial V_3}{\partial x} = B + B_2|V_3|^2 + |V_3|^2 V_3 + B_3 V_3^2 \]

Higher order harmonics can be ignored due to Bragg attenuation. In these equations the constants \(A_i\) and \(B_i\) depend on the line parameters and the properties of the nonlinear capacitors as well as on the input frequency. \(V_1\) and \(V_3\) are the complex voltage amplitudes of the first and third harmonic and \(x\) is the position along the line. Solutions of these equations for an assumed generator voltage at the fundamental are shown in fig.9, indicating that there is an optimum length and maximum conversion efficiency of -13dB for this design.

Preliminary experiments were carried out using the periodic delay line of fig. 6. Measured conversion losses are shown in fig. 10, with the best result being 20.3 dB at 24 GHz output frequency (8 GHz input), corresponding to an input power of 35 dBm, and 32.7 dBm at the first harmonic and 14.7 dBm at the third harmonic at the output. The resulting values are in reasonably good agreement (2dB in conversion loss) with the simulations, especially for large input power, which is the operation regime of interest. For the circuit described here we have not implemented the optimum length indicated by the simulations, but in any case further refinements to the material properties are required to achieve optimum efficiency.

![Figure 9 - Simulation of the NLTL, amplitude of 1st and 3rd harmonic along the line](image)

VIII. DEVICE OPTIMIZATION AND FABRICATION

Microwave circuit and device results are thus far encouraging, but the performance is limited by low overall device Q-factor. Much attention has been focused on material contributions to the loss in the literature, but most efforts have concentrated on low-frequency leakage contributions to loss, which are irrelevant at microwave frequencies. Our measurements indicate RF loss tangents on the order of Q-50 in the microwave regime, with significant dispersion apparent above 1 GHz. These losses are thought to be due to disorder in the material due to defects or impurities, and efforts are underway to explore this more closely.

![Figure 10 - Simulation and measurement results of output power \(P_{out}\) and conversion gain \(G_{conv}\) over input power \(P_{in}\)](image)

![Figure 11 - Influence of processing on (a) capacitance and (b) loss in a vertical BST varactor](image)
However, note that our overall Q-factor for the devices at 20GHz is approximately 15, which is not fully explained by the material contributions alone. We have identified two other significant contributors to device loss: processing damage, and series resistance due to the Pt electrodes.

The influence of processing on one of our vertical devices is shown in fig. 11. Although there is little effect on the device capacitance and tunability, the device loss tangent is significantly affected by the reactive-ion etching steps to define the Pt base electrode island and the top-contacts to the films. Additional efforts are required to modify the processing of the vertical devices to avoid exposure of the BST films to such ion damage.

![Equivalent circuit of BST varactor](image)

**Figure 12 – Equivalent circuit of BST varactor.**

Losses due to the conductors are somewhat easier to quantify although more difficult to solve. Fig. 12 illustrates the equivalent circuit of the BST varactor of fig. 2. The base electrode contributes a series resistance $R_s$, while the material losses are modeled by a parallel conductance $G$. The individual Q-factors associated with these loss mechanisms can be combined to give a total device Q as follows:

\[
Q_c \equiv \frac{1}{\omega R_c} \quad Q_d \equiv \frac{\omega C}{G} \\
Q_{\text{tot}} \equiv \frac{\text{Im}(Z)}{\text{Re}(Z)} = \frac{1}{Q_c} + \frac{1}{Q_d}
\]

It is extremely important to recognize that the conductor contribution is highly dependent on the geometry of the capacitor layout. To minimize this resistance, long narrow stripes of conductor are favored, as suggested in fig. 2. For a lithographic “design rule” of dimension “w”, the closest allowable separation of the conductors is $3w$, as shown in fig. 2. Figure 13 is a plot of conductor Q contribution versus frequency and w.

![Conductor losses](image)

**Figure 13 – Influence of design rules on conductor contributions to loss in the microwave range.**

Note that fig. 13 assumes a Pt base electrode of 200nm, which is twice that currently used in our process. With our current Pt layer and design rules (2.5μm), our conductor Q is approximately the same as the BST material contribution, which effectively halves the total Q of the device. By modifying our process to use thicker base electrodes and tighter lithography, we believe total device Q-factors will improve significantly as indicated in fig. 14.

![Projected Q versus frequency and loss tangent for a 1μm design rule process and 200nm Pt](image)

**Figure 14 – Projected total Q versus frequency and loss tangent for a 1μm design rule process and 200nm Pt.**

IX. ACKNOWLEDGEMENTS

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