UNIVERSITY OF CALIFORNIA

Santa Barbara

MMICs using GaN HEMTs and Thin-Film BST Capacitors

A Dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in

Electrical and Computer Engineering

by

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Hongtao Xu

ACKNOWLEDGEMENTS

There are many people whom I would like to acknowledge for their assistance and support in completing this work, both technical and moral.

First, I would like to thank my advisor Prof. Robert York, for his intelligent guidance and his generous support and encouragement during the course of my doctoral studies.

Appreciation is also extended to the members of my advisory committee, Prof. Umesh Mishra, Prof. Steve Long and Dr. Yifeng Wu for serving on my committee as well as their valuable guidance.

During the last five years, I have enjoyed the research life in York and Mishra groups. I benefited greatly from Stacia, Sten, Lee and Arpan in GaN initiative and Nadia, Peter and Troy in BST initiative for their contribution of state of the art material. Likun, Baki, Naiqian, and Yun, I am thankful for teaching me processing techniques. Chris, who is in the same project, shared duties and labs with me. Ale, Huili, Dario, Rob C. and Siddharth gave me uncountable suggestions on GaN HEMT design, analysis and characterization. Nadia, Jaehoon and Justin helped me understand BST material and device design. Visiting Professor Steven Gao gave me much help on the power amplifier design. Valuable discussions and generous help from group members are key resources of my work. I am grateful to all of them: Raj, Val, Vicki, Pengcheng, Bruce, Paolo, Jiwei, Tomas, Yuvaraj, Felix, Man Hoi, Conradin, Michael, Haijiang and Ilan. Thanks to all the friends I have met during my

time at UCSB. I am also grateful for the funding from ONR and ARO that made this work possible.

Thanks to the cleanroom management team, Jack Whaley, Bob Hill, Neil Baker, Brian Thilbeault and Don Freeborn, and all cleanroom users for their help on processing development. Thanks also go to Laura Clausen, Valerie De Veyra and Suzanne Foti for their administrative support.

I would like also to acknowledge my family for their understanding and constant support during my study years. And, I am deeply grateful for the love, encouragement and understanding of my beloved wife, Hui, who shared all my joy and bitterness everyday during my graduate studies. Without her, this work would not be possible.

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1. **H. Xu**, S. Gao, S Heikman, U. K. Mishra and R. A. York, "A High-Efficiency Class-E GaN HEMT Power Amplifier at 1.9 GHz," submitted to *IEEE Microwave and Wireless Components Lett.* 2005
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ABSTRACT

MMICs using GaN HEMTs and Thin-Film BST Capacitors

by

Hongtao Xu

GaN HEMTs have been considered as candidate devices for next generation high-power microwave applications. They feature fast speed, high power density, and also low noise. Many research works are underway from material improvement, fabrication development and device optimization. An increasing number of microwave circuits based on GaN HEMTs have been demonstrated, but there are still many challenges to make high-performance integrated microwave circuits. One of these problems is the limited availability of high quality integrated passive components for Monolithic Microwave Integrated Circuits (MMIC). Therefore, the exploration and integration of novel integrated passive components is a key solution to broaden the functionality of GaN MMICs.

Barium Strontium Titanate (BST) tunable capacitors have been studied for years as microwave components because of their high tunability, compact structure, decent quality factor and high capacitance density. In order to optimize the loss in the BST capacitors, a geometry dependent RF model is established to analyze high frequency performance at the device level. Several tunable microwave circuits, such as tunable

filters and phase shifters, are demonstrated using these design techniques. Also successful integration of the BST process with GaN HEMT circuits in the form of a 5 GHz GaN HEMT oscillator is presented. BST thin film technology is shown to be useful for the design of frequency agile circuits and reduction of layout area in various microwave application.

In this research, a full MMIC fabrication process has been developed based on GaN HEMTs. BST tunable capacitors, spiral inductors, metal-insulator-metal (MIM) capacitors and thin film resistors have been successfully integrated in GaN HEMT microwave integrated circuits. Field-plated GaN HEMT structures were also employed and analyzed to improve the power and efficiency performance of transistors. Various microwave circuits, including LNAs, oscillators and power amplifiers, were designed and fabricated to study high frequency noise, phase-noise and power behaviors. Results from these circuits show superior properties of of GaN MMICs, especially from perspectives of power density and efficiency.

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Chapter 1. Introduction

1.1. Introduction

Microwave integrated circuits have experienced tremendous growth over the past 50 years. The emergence of novel integrated components is the engine pulling the progress of microwave circuit into new eras. As with digital integrated circuits, the history of microwave integrated circuits is a history of advances in material growth and device fabrication techniques. These new technologies enabled the progress in microwave integrated circuits (MICs), monolithic microwave integrated circuits (MMICs) and millimeter-wave integrated circuits. These smaller, highly integrated and low cost circuits have found extensive applications in radar, electronic warfare, and commercial applications.

Solid-state microwave circuits play an important role in communication. High level signals are desirable in a microwave system, because they help to increase the range of propagation and provide reliable and clean signals to the receiver. The need for high power microwave circuits become increasingly important in wireless communication and satellite communication. Transistors based on the gallium arsenide (GaAs) material system have dominated microwave applications over the last two decades in this field. However, engineers have faced difficulties in the implementation of microwave circuits for high power applications using GaAs based technology because of the limited power density available from GaAs devices. In order to achieve higher output power level, large periphery device would be

required. Alternately, power combining techniques can be employed to deliver higher output power using multiple sections of identical circuits. Both of these techniques have drawbacks.

When using a large periphery device, the load line becomes steeper. The optimum load impedance is inverse proportional to the total gate width. This lowered impedance level requires a high impedance transformation ratio from a 50 Ω load. Consequently, matching network design becomes more difficult. Both the bandwidth and the loss of matching networks are functions of the impedance transformation ratio. Uniformity is another challenge for the large periphery devices, since current, phase, and thermal distributions on gate fingers degrade the device performance. Multi-section matching networks could achieve better uniformity in the device performance, but at the cost of requiring higher uniformity in passive components. Additionally, multi-section matching and combining networks are more complex and lossier.

In practice, accurate design depends highly on the accuracy of active devices large-signal models. Distributed effects have to be considered in large periphery devices. A complicated large-signal model is required, making simulations both tedious and time-consuming. One simple way to increase the total gate width is to increase the number of gate fingers. Parasitic elements and iner-finger coupling can cause potential instabilities; generally speaking it is hard to locate and simulate these inner-device instabilities.

Moreover, circuits based on large-periphery devices may require large dc and ac currents. To avoid the failure at high current, passive components on the load side

must have high current handling capacities. Thermal management will be necessary if high efficiency cannot be realized during high output power operation.

Suppliers of RF and microwave power transistors continue to further advances in material science, process techniques, transistor structures, and packaging technologies to drive performance of lateral-diffused metal oxide semiconductor (LDMOS) FETs, GaAs MESFETs, GaAs/InGaP and silicon germanium (SiGe) heterojunction bipolar transistors (HBTs), gallium nitride (GaN) high electron mobility transistors (HEMTs), and silicon carbide (SiC) FETs, to new heights. One important figure of merit which describes the high-frequency power performance of a device is the product of the maximum RF power and f_t, which is referred to as Johnson's figure of merit. It can be approximated by

$$P_{\max} f_t = \frac{\varepsilon w_g v_s^{\ 2} E_{br}^{\ 2}}{32\pi}$$

As seen in Table 1.1, Gallium Nitride (GaN) possesses very attractive features such as a wide energy band-gap (3.4 eV), high breakdown field (330 MV/m) and a high saturation velocity (2.7 x 10^5). Although in practice the power performance does not scale proportionally to the Johnson's figure of merit due to additional effects, it nevertheless remains a clear indicator of GaN's advantage as a material for power devices. GaN has been successfully grown on SiC substrates, which have excellent thermal properties. GaN HEMTs, developed as power devices for microwave applications can deliver a power density over ten times better that of conventional GaAs-based technology. Power density is defined as output power per unit gate width (W/mm). A power density of 32 W/mm has been reported using a

field-plated GaN HEMT. The addition of a field-plate significantly alleviates design and simulation difficulties. GaN HEMTs with similar gate lengths have comparable cut-off frequencies. Thus GaN HEMTs are good candidates for high power microwave and millimeter wave applications.

	Si	GaAs	InP	4H-SiC	GaN
Band-gap energy (eV)	1.12	1.43	1.34	3.26	3.40
Saturation velocity (m/s)	0.6×10^5	10^5	0.9×10^5	2	2.7×10^5
Critical breakdown field (MV/m)	30	40	50	300	330
Relative dielectric constant	11.9	12.8	12.5	9.6	8.9
Thermal conductivity (W/mK)	150	50	69	370	170
Johnson's FOM ratio	1	5	6	896	1800

Table 1.1 Comparison between material parameters for Si, GaAs, InP and GaN at T=300 K

Recent studies have shown that GaN HEMTs also exhibit excellent noise characteristics for LNA circuits. The incorporation of low noise, high breakdown GaN HEMTs in to amplifier front-ends reduce the need for diode limiters as protection against RF overstress. This can reduce the overall LNA noise figure. Additionally, using GaN HEMT technology allows for the fabrication of both low noise and high power circuits on the same wafer.

Barium Strontium Titanate (BST) thin films have been investigated for low cost, frequency agile microwave circuit application. BST thin films have several properties that make them attractive for microwave applications. They include an

electric field dependent permittivity, fast switching speed, wide range of tuning voltages, high tunabilities, compact structures, decent and stable quality factors, and the absence of diode conduction. Monolithic passive microwave BST circuits have been successfully developed and fabricated, but challenges in the loss optimization and the integration of BST films into monolithic process fabrication with active devices still exists, such as loss scaling with geometry-dependence and integration challenges involving in other high temperature process steps. To overcome these difficulties, advanced techniques in device layout design and fabrication are required.

Our main research goal of this work focuses on the development of GaN based MMIsC using novel integrated passive components. This involves process development, device optimization, device modeling and integrated circuit implementation. BST capacitors work as a key passive element in frequency agile microwave circuits with compact layouts. The achievement of this research can also be readily transferred to commercial applications such as wireless communication, satellite communication, etc.

1.2. Outline of the thesis

This work started from the point of MMIC fabrication development. Both active and passive components were monolithically integrated on a single wafer. Discrete components were fabricated and modeled using the developed fabrication process. With RF component modeling, structures of devices were further optimized and stabilized. Finally various microwave circuits were design, fabricated and tested.

The whole work comprises of the initial efforts of fabrication up to implementations of mature integrated circuits. This thesis includes seven chapters, starting from novel passive components, passive integrated circuits, integration of novel passive components with GaN HEMTs and finally GaN HEMT MMICs. The first chapter is the introduction of the thesis, which describes the background and objective of the research. Chapter two describes the design and optimization of passive devices. The modeling and fabrication of BST tunable capacitor, spiral inductor, MIM SiN capacitor and thin film resistor are discussed and analyzed. Chapter two also discusses the optimization of RF BST capacitors. Chapter 3 demonstrates several passive microwave integrated circuits using BST tunable capacitors. Chapter 4 reviews the principle of small-signal and large signal modeling used for GaN HEMT devices. Different field-plate structures are analyzed and compared. Chapter 5 presents the integration of BST thin film capacitor in GaN microwave circuits. The first GaN HEMT oscillator with a BST thin film component is demonstrated. Chapter 6 presents various GaN HEMT based microwave circuits, which include high power and high efficiency class-E power amplifiers, high power and low noise oscillators, high dynamic range and high survivability low noise amplifier and a f_t doubler. These microwave circuits systematically verify the advantages of power and noise performance in GaN HEMTs. Chapter 7 concludes the thesis with the summary of achievements and suggestions for the future work. Appendix A describes the process flow for a field-plated GaN HEMT MMIC. Appendix B summarizes the process flow for a field-plated GaN HEMT MMIC integrated with BST capacitors.

Chapter 2. . Passive devices design and optimation

2.1. RF BST capacitors

$Ba_xSr_{1-x}TiO_3$ (BST) thin films have been investigated for microwave circuit application because of their high dielectric constants, high tunability, relatively low loss, and fast switching speed. A typical C-V curve is shown in Figure 2.1. Recently, a BST film was reported with a tunability as high as 13:1 [1]. This makes BST thin film technology attractive for low cost, frequency agile microwave circuits such as phase shifters, tunable filters, tunable matching network and high tuning range VCO [2][3][4]. Additionally, due to its high dielectric constant, BST is a candidate for very compact MMIC dc blocking capacitors, promising a 100-fold reduction in capacitor area as compared with SiN and SiO_2 capacitors. The high capacitance density also allows for small electrode sizes, making the parasitic inductances lower than typically seen in other capacitor technologies. This increases the self-resonance frequency, therefore allowing for flat capacitances up to very high frequencies.

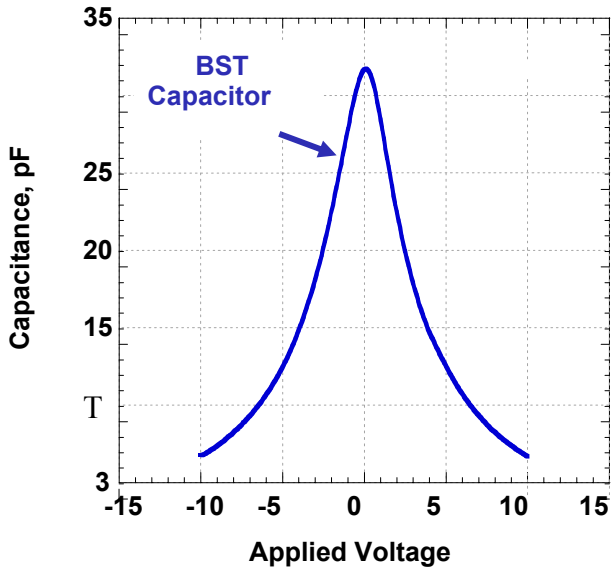
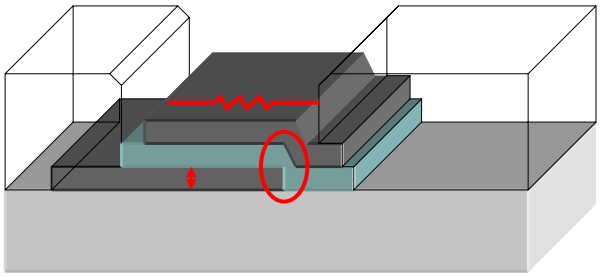


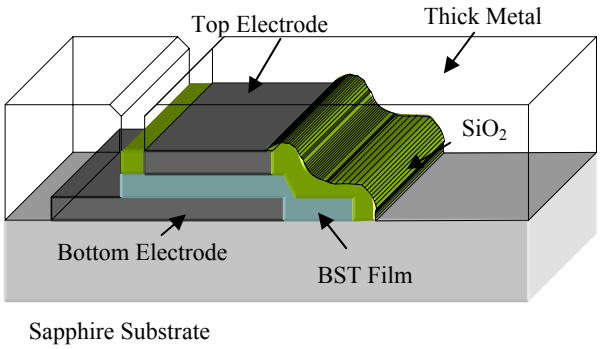
Figure 2.1 Typical CV curve of BST capacitor

Most of the previous work in this area covered material quality, choice of electrodes and processing techniques. Less emphasis has been placed on advanced device designs, leaving room for further improvement. Quality factor, resonace frequency and breakdown voltage are important factors in determining which MMIC applications BST capacitors will work best in. The high-frequency device losses consist of the losses of the thin-film material and the electrode-film interfaces, and the resistive loss on the electrodes. Our previous work uses a simple RF structure, in which a BST film is sandwiched between the bottom and top electrodes [2]. Using this conventional integrated parallel-plate overlay capacitor structure (Figure 2.2a), the thickness of bottom electrodes is constrained by the thickness of the BST film. The loss of the thin bottom electrodes limits the overall quality factor of high frequency BST capacitors. Additionally, the higher electric field between the top and bottom electrodes at the edge of the cross-over may cause premature breakdown

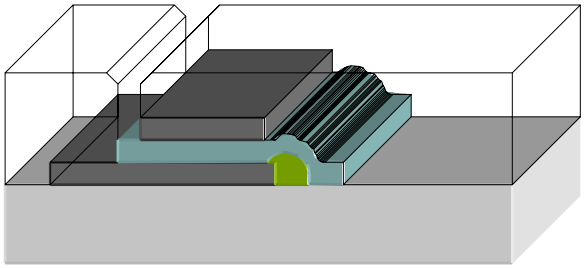
when high bias voltages or large amplitude ac signals are applied to the BST capacitors. The Pt based top electrodes contribute to resistive losses as well. These issues show the need for improvement of the RF device structure.



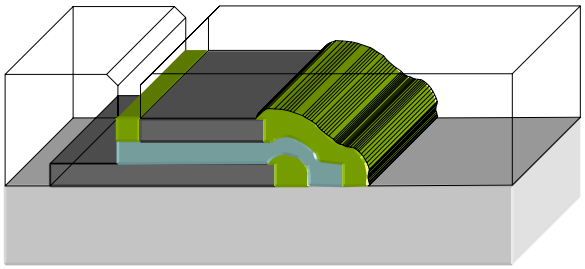
(a)



(b)



(c)



(d)

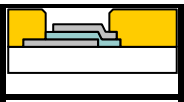
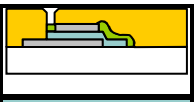
Figure 2.2 (a) Conventional parallel-plate overlay capacitor structure; (b)-(d) improved RF structure with insulating layer

In order to reduce the electrode loss and increase the breakdown voltage, we propose improved structures (Figure 2.2b-d) with one or two dielectric pads under a cross-over bridge. The cross-over thick metal connects the top electrode to the outside pad/interconnect metal. With this structure, the thickness of both the top and bottom electrodes can be increased to further reduce resistive losses. This structure also avoids the premature breakdown at the edge of bottom electrode under the cross-over. The dielectric pad can be made of either SiO_2 or SiN_x insulating material. This layer can also be used to passivate and protect the BST film from damage and contamination during subsequent processing steps. The overlap between the bridge and bottom electrode should be small enough to reduce the parasitic capacitance in the access region.

BST capacitors based on these structures were designed and fabricated. They were fabricated in the same die on the same wafer, so the electrodes and BST film were identical. Table 2.1 compares these four structures using parameters extracted

from measured data at 3 GHz. Their capacitances are close and vary only less 1%. The Q factors of the improved structures are over 20% better than the conventional structure. The improvement comes solely from the thicker top electrodes. With thicker bottom electrodes (3000 Å on this sample), Q factors could be improved further. Additionally, results shows that SiO_2 passivation does not affect the performance of the BST capacitors. Considering easeof fabrication, structure (b) is most favorable, because it requires only one more additional SiO_2 layer to simultaneously cover the edge and passivate the BST, while having the highest resonance frequency among the improved structures.

Table 2.1 Comparison of conventional and improved structures

30x40μm^2				
@ 3GHz	(a)	(b)	(c)	(d)
C(pF)	18.23	18.13	18.32	18.15
Q	9.317	11.565	11.297	11.437
Ls (pH)	3.399	3.644	5.847	6.147
F_{res} (GHz)	19.25	19.25	15.25	14.45

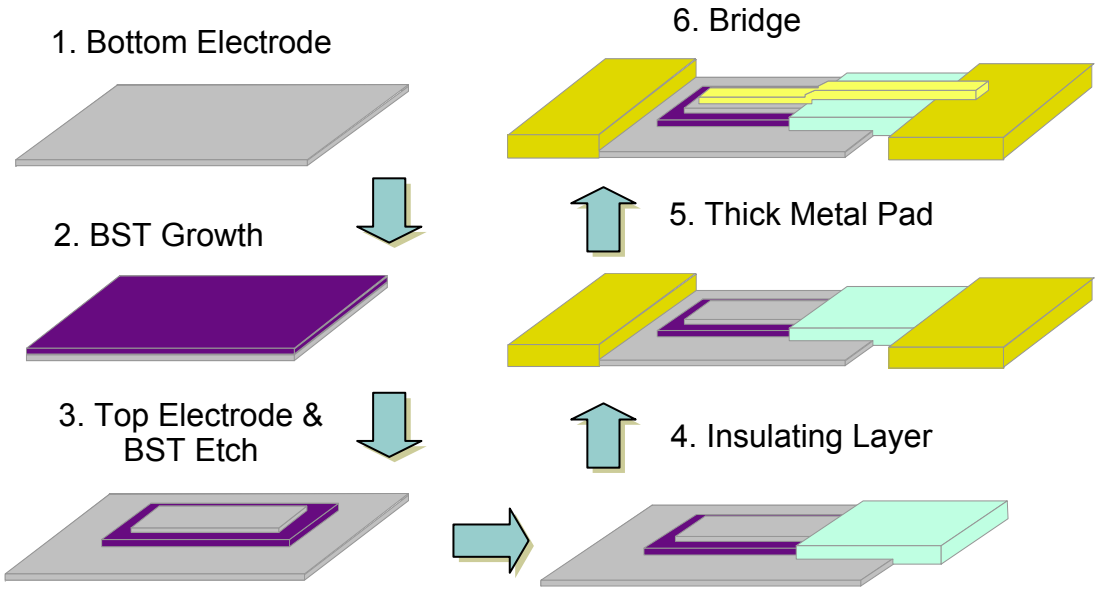


Figure 2.3 Process flow for RF BST capacitors

Figure 2.3 presents a sketch of the process flow for RF BST capacitors. In this work, BST thin films were grown on sapphire substrates with 3000 Å electron-beam evaporated Au/Pt bottom electrodes that were pre-patterned using liftoff. Au metal was incorporated into the bottom electrode to increase the conductivity. The BST films were deposited using RF magnetron sputtering. The film growth conditions were optimized for tunability and microwave loss performance. A capacitance density of 15 fF/μm^2 was chosen for our designs. Pt/Au top electrodes were evaporated followed by a BST etch in 1:1 buffered HF:DI water. A 3000 Å SiO_2 film was electron-beam evaporated as an insulating layer beneath the overpass bridge, which connects the top electrode to a high-conductivity interconnect metal layer. The SiO_2 also functions as a passivation layer for the BST capacitors. The

crossover metal and thick metal pad were e-beam evaporated Au with 1 μm and 3 μm thickness respectively.

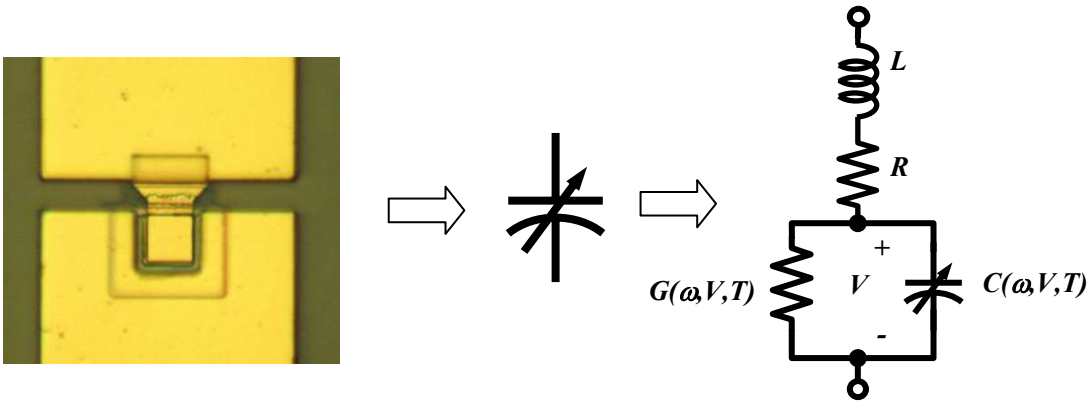


Figure 2.4 Simplified RF lumped-element model

In order to optimize RF devices for ultimate loss performance, a physical equivalent model was required to simulate Q factors with geometry-dependence. Working with EM simulations, the model can helps to determine the lowest loss device layout for MMIC designs. As shown in Figure 2.4, a simplified physical equivalent model was used for this device structure. L is a parasitic series inductance due to RF signal propagation along the electrodes; it determines the self-resonance frequency and increases the effective capacitance. R is the sum of the losses of the electrodes and the interface. G includes intrinsic film conductance, leakage and polarization losses. C is the effective capacitance. Both G and C are dependent on the tuning voltage, frequency and temperature. All parameters scale with device geometry.

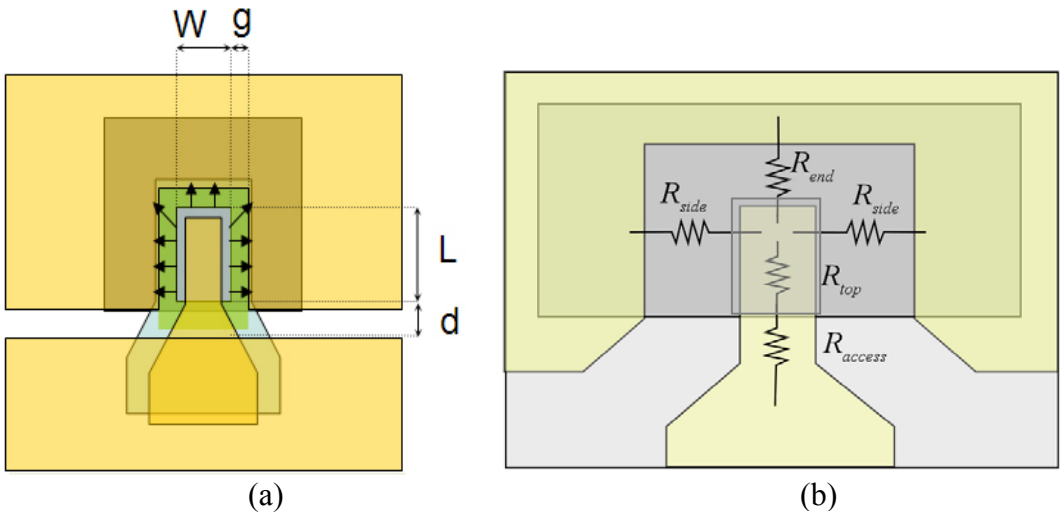


Figure 2.5 (a) Dimension of BST capacitors; (b) Resistive contributions to R

A simplified mask layout is shown in Figure 2.5(a), with critical dimensions as labeled. L and W are the length and width of the active area in the BST capacitor. g is the spacing between the top electrode and the thick metal pad connected to the bottom electrode. d is the length of the crossover metal that connects the top electrode to the thick metal pad in the access region. In the design of the capacitor layout, W and d should be minimized to reduce series resistances in these regions, but their minimum dimensions are set by the process limitations. g is generally chosen to be 2~4 μm, depending on the anticipated difficulty of the BST etch. We modeled all of the metal layers with an associated sheet resistance (Ω/square) and the dielectric film with an associated capacitance density (fF/μm^2). A first order model of resistive loss can be obtained with reference to Figure 2.5(b). The resistance R combines the access resistance on the overpass bridge strip (R_{access}), the

loss on the top electrode (R_{top}) and the loss contributed from the bottom electrode (R_{base}).

$$R = R_{access} + R_{top} + R_{base}$$

With reference to the dimensions in Figure 2.5(a), the resistances for each part can be calculated as following:

$$R_{access} = r_t \frac{d}{W}$$

$$R_{top} = r_t \frac{L}{3W}$$

$$R_{base} \approx \frac{R_{side}}{2} // R_{end}$$

where

$$r_b, r_t : \text{sheet resistance of bottom and top electrodes}$$

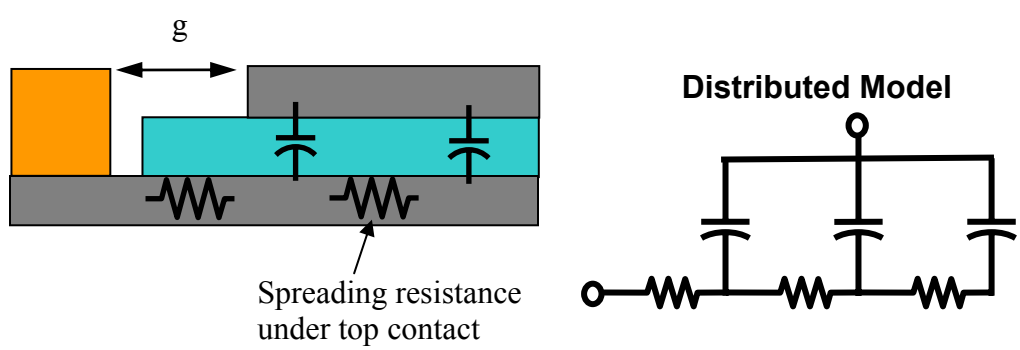


Figure 2.6 Base spreading resistance

The bottom electrode contributes a resistance which includes contributions from the two sides and the end of the device; each of these two contributions consists of a base spreading resistance under the top contact and losses in the gap between the top

electrode and thick metal pad, as shown in Figure 2.6. These contributions can be calculated using the resistivities of the top and bottom metals. The factor of 1/3 comes from the distributed nature of the contact. [5] We obtain the total resistance on the bottom electrode:

$$R_{side} = r_b(\frac{g}{L} + \frac{W}{6L})$$

$$R_{end} = r_b(\frac{g}{W} + \frac{L}{3W})$$

$$R_{base} \approx \frac{R_{side}}{2} // R_{end} = r_b(\frac{g}{2L} + \frac{W}{12L}) // r_b(\frac{g}{W} + \frac{L}{3W})$$

The 1st order skin effect is also incorporated to model high frequency performance accurately. The sheet resistances of the bottom and top electrodes are estimated from the skin depths (λ) of conductor.

$$\lambda = \sqrt{\frac{\rho}{\pi f \mu_0}}$$

$$r = \frac{\rho}{\lambda(1 - e^{-t/\lambda})}$$

where f is the operation frequency, μ_0 is absolute magnetic permeability of the conductor, and t is the thickness of electrode.

The effective total capacitance includes the intrinsic BST capacitance defined by the area (C_{bst}), the access capacitance due to the coupling between bottom electrode and cross-over bridge metal (C_{access}) and the fringing capacitance along the periphery ($C_{fringing}$). G is evaluated from film characterization.

$$C = C_{bst} + C_{access} + C_{fringing}$$

$$G = \frac{\omega C}{Q}$$

where

Q : Q factor from BST film characterization

The BST capacitance is defined by the area of the top electrode. The parasitic access capacitance is calculated from the overlay area between the over-cross metal and bottom electrode with SiO_2 as the dielectric medium; it is defined by the layout of the capacitor structure. An equation developed by v.d. Meijs and Fokkema through function fitting is used to calculate the fringing capacitance [6].

$$C_{bst} = \frac{\varepsilon_{BST} WL}{H}$$

$$C_{access} = \varepsilon_{SiO_2} A_{access}$$

$$C_{fringing} = \varepsilon_{BST}(L+W)\left(0.77 + 1.06\left(\left(\frac{W}{H}\right)^{0.25} + \left(\frac{t}{H}\right)^{0.5}\right)\right)$$

where ε_{BST} and ε_{SiO2} are permittivities of BST and SiO_2, A_{access} is the the overlay area in the access region, t is the thickness of top electrode, and H is the thickness of BST film.

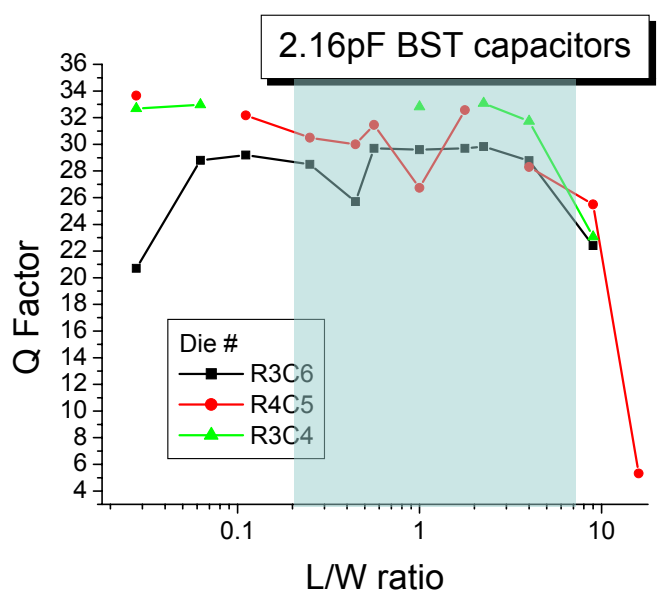
The parasitic C_{access} and $C_{fringing}$ increase the effective capacitance, reducing the tunability of the BST capacitor. This effect becomes significant for small capacitors.

The inductance L can be estimated from the formula for a straight-line inductor [7].

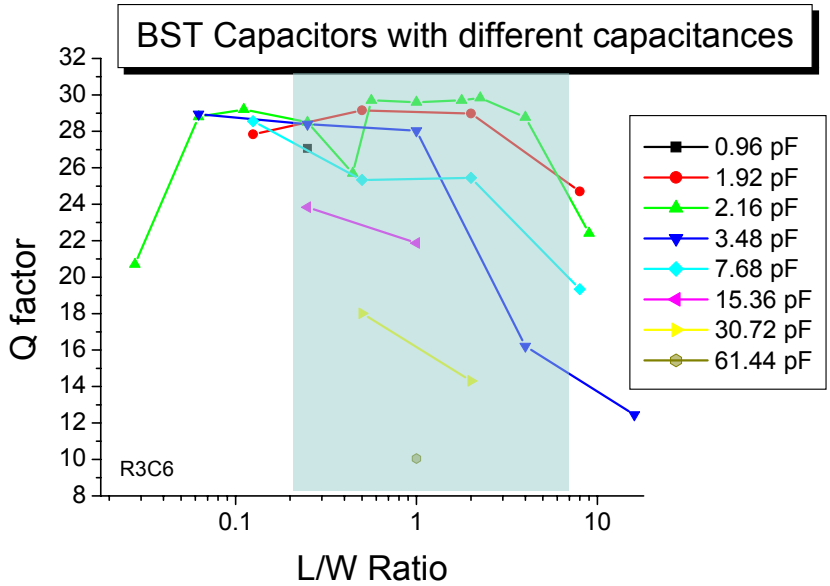
$$L = \frac{\mu_0 L}{4mW} \frac{\sinh(mt) - \sin(mt)}{\cosh(mt) - \cos(mt)}$$

where $m = \sqrt{\pi f \sigma \mu_0}$. σ is the conductivity of metal.

The high frequency properties of BST thin film capacitors with different peripheries are studied. An L/W aspect ratio in the range of 0.2~7 is acceptable, considering both the yield and occupied area. BST capacitors with different sizes and aspect ratios were fabricated based on the structure described above. Q factors at 3 GHz, calculated with resistive losses and effective capacitances, were extracted from measured small signal data. As shown in Figure 2.7 (a), 2.16 pF BST capacitors with different aspect ratios were tested on different dies. The peak Q factors were found on the devices with an aspect ratio of 2.25. Q factors on a series of capacitors with different values were also plotted against their L/W ratios in Figure 2.7 (b). As we can see, Q factor decreases as capacitance increases. Wide layouts are more favorable for large area devices.



(a)



(b)

Figure 2.7 Measured Q factor vs. L/W aspect ratio for BST capacitors

The lumped RF model described above was used to simulate the relationship between Q factor and aspect ratio and to help optimize periphery structure. The simulated results are shown in Figure 2.8. Simulated Q factors are slightly higher than ones from measured data, but they give similar trends and optimized aspect ratios. Finding the optimized physical layout will help to improve the peak performance of integrated circuits.

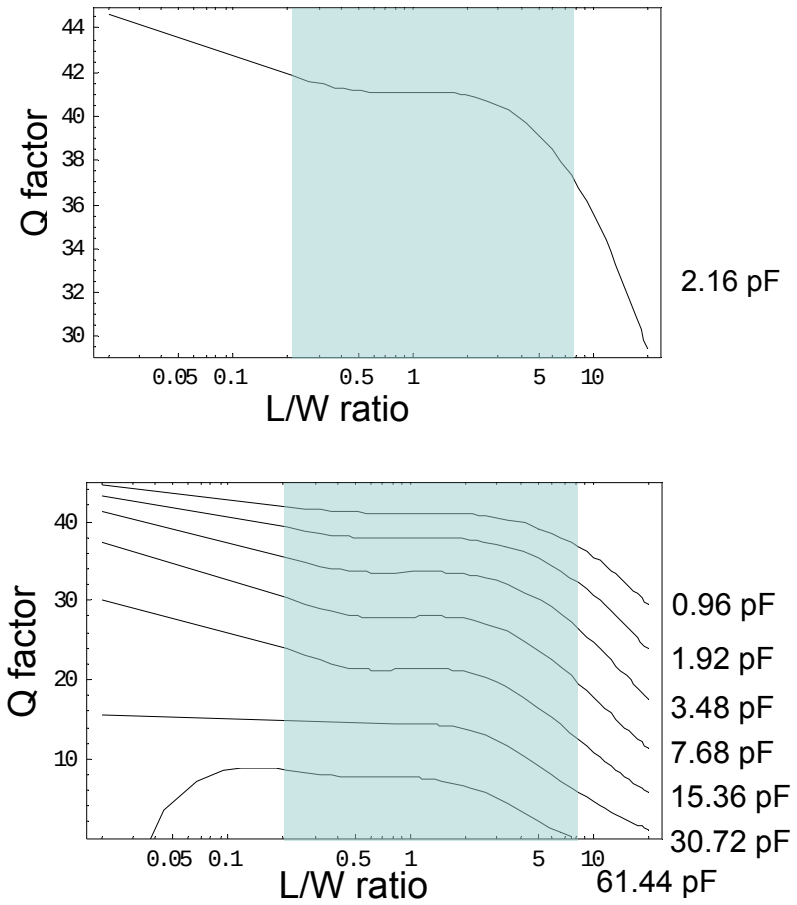


Figure 2.8 Simulated Q factor vs. L/W aspect ratio for BST capacitors

From the perspective of ultimate loss performance in microwave circuits, the BST capacitor itself needs to provide good high frequency performance. The loss contributions from electrodes become significant at high operating frequencies. Q factor variation with geometry is investigated with decent analytical models allowing for optimization. Microwave BST integrated circuits designed based on this optimization technique will be presented in Chapter 3. Compact structures and wide tuning ranges were achieved. Additionally, BST films have also been successfully

integrated in GaN HEMT MMICs. In Chapter 4, a GaN HEMT low noise, high power oscillator integrated with a BST film showed excellent power and noise performance. BST thin film capacitors are a good candidate for frequency agile microwave integrated circuits.

2.2. Spiral inductors

The most widely used on-wafer inductor is the planar spiral inductor. The possible shapes include rectangles, hexagons, octagons and circles. The choice of shape is generally made on the basis of convenience. The losses in spiral inductors primarily come from resistive loss in the conductor and EM dissipation due to the dielectric material and substrate. In other works, methods such as using thick plating of conductors or 3-D structures [8] were developed to obtain higher Q factors. Figure 2.9 shows typical layouts of the rectangular and circular spiral inductors we used in our microwave circuit design. An air-bridge or dielectric cross-over can used to fabricate multi-turn planar spiral inductors.

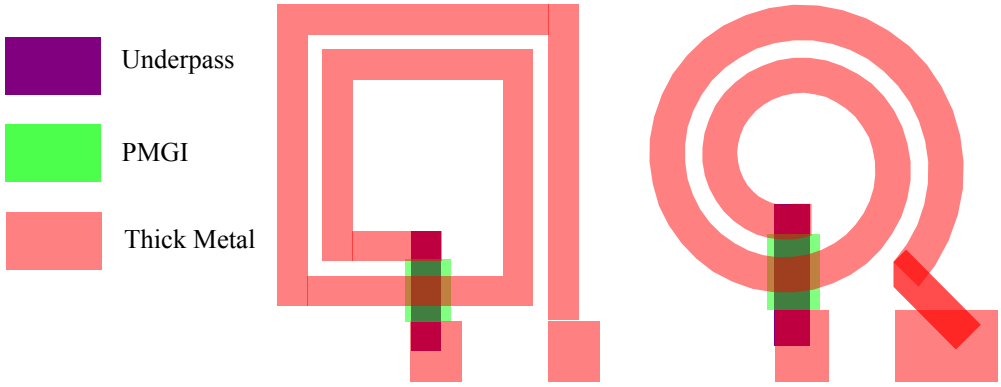


Figure 2.9 Layouts of rectangular and circular spiral inductors

Because of preferred simplicity, our inductor fabrication process includes three layers. The first layer consists of a piece of 1 μm Au underpass metal, which connects the inner end of spiral wire to an outer pad. Instead of using air-bridge or via hole, a PMGI cross-over layer partially covers the underpass metal to make a dielectric bridge for thick metal. A 3 μm Au layer is chosen as the thick metal to reduce resistive losses in the conductor.

The inductance of spiral inductors is primarily determined by number of turns (n), width of the wire (w), space between the turns (s), and the fill factor (ρ). The inductance of planar spirals of all regular shapes can be estimated using a simple unified form [9]:

$$L \approx \frac{\mu_0 n^2 d_{avg} c_1}{2}\left[\ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho^2\right]$$

where the fill factor ρ is defined as:

To investigate the difference between rectangular and circular spiral inductors and also setup design guidelines, over 200 spiral inductors with different parameters were designed and fabricated. Pairs of rectangular and circular spiral inductors with same physical parameters (n, d_{out}, d_{in}, w and s) were characterized correspondingly. Q factors and inductances were measured at 5 GHz. The relationship between Q factor and inductance is plotted in Figure 2.10. The graph shows that rectangular spiral inductors exhibited better Q factors than circular ones, for inductors smaller than 1 nH. Rectangular inductors also have a wider inductance value range. Circular spiral inductors need a larger size to achieve the same inductance as rectangular

ones. Rectangular spiral inductors are much easier to fit in the layout because components can be placed closely.

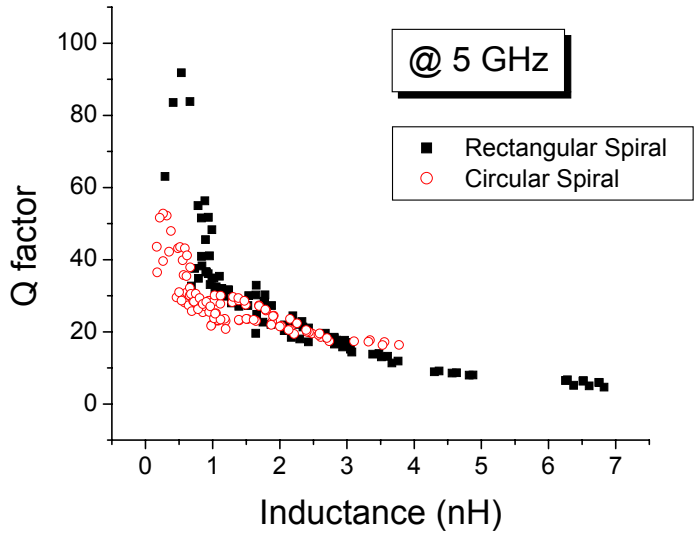


Figure 2.10 Q factors versus inductances of spiral inductors

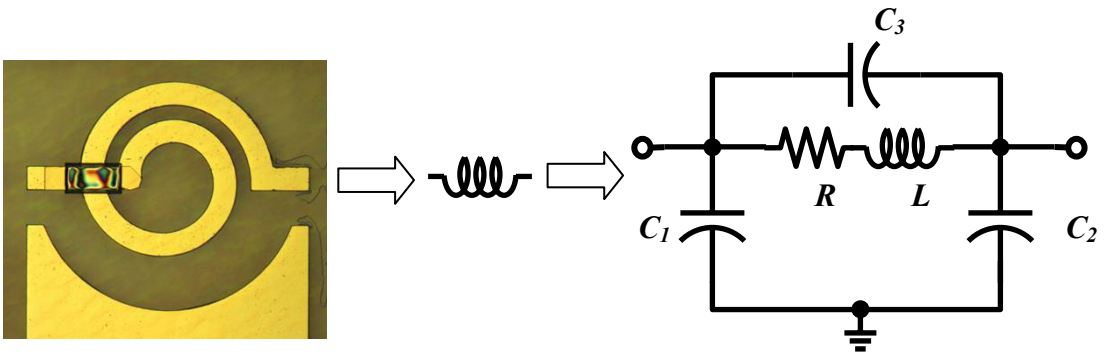


Figure 2.11 Simplified equivalent RF model for spiral inductors

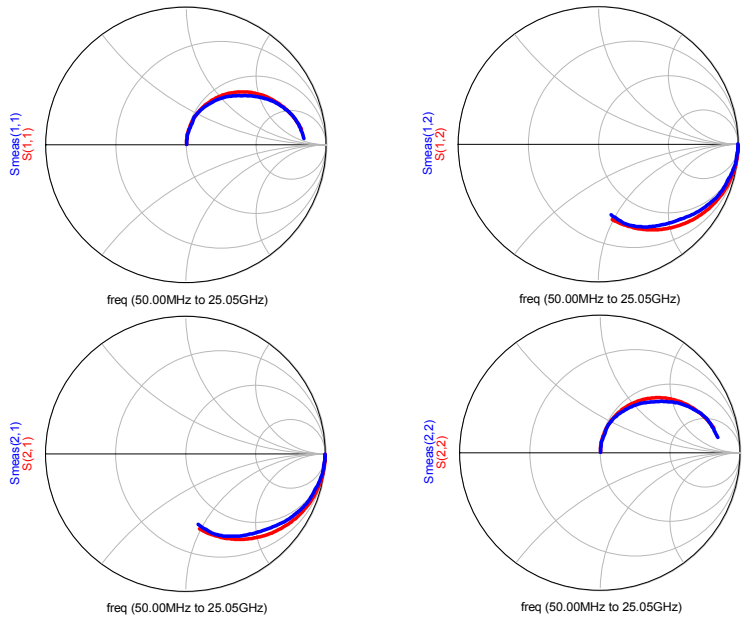


Figure 2.12 Comparison of measured and modeled s-parameters

Our simplified on-chip spiral inductor model (Figure 2.11) includes effective inductance (L), series resistive loss (R), parasitic capacitances (C_1 and C_2) between the ports and the ground, and coupling between the two ports (C_3). Figure 2.12 shows a comparison of a modeled and measured 0.9 nH inductor. Up to 25 GHz, this simplified model achieves relatively good agreement with measurement. The model is symmetrical, even though actual spirals are not. For some applications, such as differential circuits, transformers, and tap inductors, symmetry is very important. Differential or single-turn spiral inductors are widely used in MMIC/RFIC designs, as shown in Figure 2.13.

Figure 2.13 Symmetric layouts of spiral inductors

2.3. Fixed SiN/SiO_2 capacitors and thin film resistors

All of the interconnect layers may be used to make conventional parallel plate capacitors. However, inter-level dielectrics, like PMGI, tend to be rather thick (1-3 μm), making the capacitance density is too small to make useful capacitors in microwave frequency range. In our process, we can use PECVD/sputtered/e-beam evaporated SiO_2 or SiN_x thin films as dielectric layers. Both the BST capacitor and GaN HEMT processes include passivation layers which can be used directly to fabricate fixed capacitors. This saves a few processing steps and reduces process complexity.

Tantalum nitride (TaN) and nickel chromium (NiCr) are widely used in the fabrication of resistors for passive technologies. NiCr has the best temperature coefficient of resistance (TCR) and voltage coefficient of resistance (VCR) and its overall process integration is easier than TaN. However, Ni content controls the film resistivity as well as the NiCr reactivity when exposed to solutions at later processing steps, making complete passivation of the resistors necessary. In addition,

the NiCr has a low current carrying capability due to the poor heat dissipation of the SiO_2 layer upon which the NiCr thin film resistor is built. In our process, a 500 Å thick NiCr thin film is e-beam evaporated to make a 40 Ω per square sheet resistance.

Simplified equivalent RF models for fixed capacitors and thin film resistors are sketched in Figure 2.13 and 2.14 respectively.

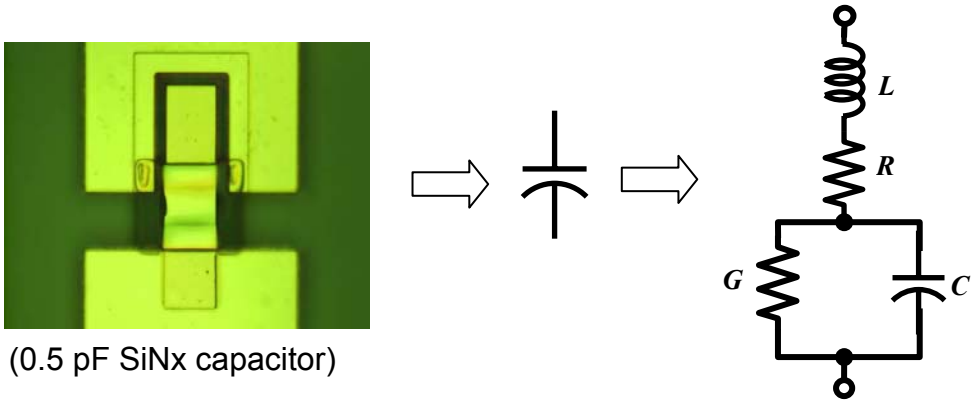


Figure 2.14 Simplified equivalent RF model for fixed capacitors

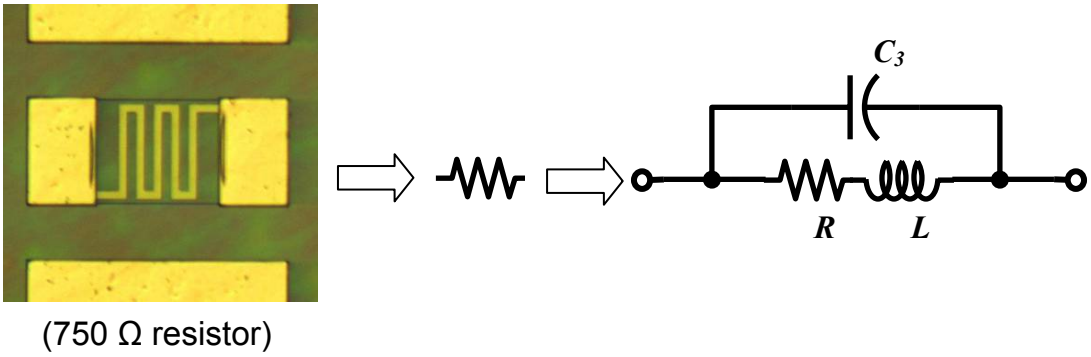


Figure 2.15 Simplified equivalent RF model for thin film resistors

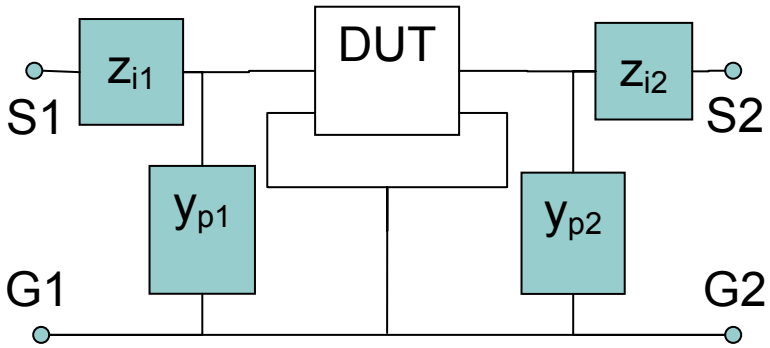
2.4. Open/short de-embedding method for modeling

In order to measure devices, an interface must be established between the device ports and the probe tips. This is done by constructing a fixture for mounting the Device-Under-Test (DUT). This extrinsic structure will not be used in the circuit layout, but it introduces additional parasitics into the raw measurement results. In order to extract value of the intrinsic elements, an open/short de-embedding (OSD) routine is necessary. This method is based on the assumption that the parasitics between the probe and the DUT can be described by a parallel admittance (y_p) and a series impedance (z_i), as shown in Figure 2.15. The required standards are shown in Figure 2.16. In most of cases, symmetry is assumed so that

$$z_i = z_{i,short}$$

$$y_p = 1/(z_{i,open} - z_i)$$

where $z_{i,short}$ and $z_{i,open}$ denote the measured input impedance of the short standard and input impedance of the open standards, respectively. The de-embedding is performed by (i) subtracting the estimated z_i from the measured input and output impedances, (ii) converting the resulting Z-parameters into Y-parameters, and (iii) subtracting y_p as described above.



$$z_i = z_{i,short} \quad y_p = 1/(z_{i,open} - z_i)$$

Figure 2.15 Open/short de-embedding fixture model

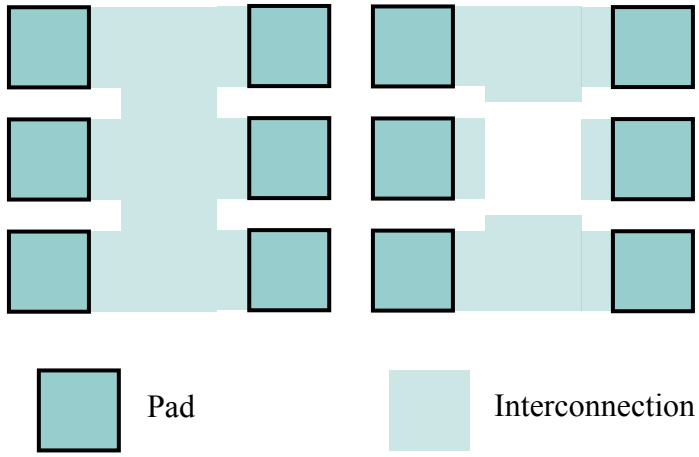


Figure 2.16 Short/Open de-embedding GSG calibration sets

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Chapter 3. Passive integrated circuits in BST technology

3.1. Tunable filters

Tunable filters are widely used in microwave applications for system reconfiguration and optimization [1]. BST tunable filters provide fast tuning speeds and compact sizes with relatively low RF losses [2]. The high dielectric constants of BST films also ensure compact filter designs. To demonstrate the filter applications of BST technology, several tunable filters were designed, fabricated and characterized. The BST capacitors in the circuits were individually optimized.

A simple tunable band-pass filter was realized using a shunt LC parallel resonant circuit. The circuit and die photograph are shown in Figure 3.1. Capacitor C_v is a BST tunable capacitor. The passband frequency is tuned by a DC bias voltage on the BST capacitors, which is applied through port 2 using a bias-tee. A high value BST capacitor is used in the circuit to block DC feeding through the inductor to the ground. The capacitor C is used to isolate feed though between port 1 and port 2 at low frequencies. The insertion loss and return loss of the filter are shown in Figure 3.2. The measurement results show that the center frequency of the passband can be tuned from 4.5 GHz to 6 GHz by biasing the capacitors up to 8 V, which corresponds to 33 % tunability from zero bias. The measured insertion loss within the passband was better than 3.8 dB and the return loss within the passband was better than 10 dB. The losses are reduced as the bias voltage increases. With an 8 V bias, the insert loss and return loss are 2.4 dB and -17 dB, respectively. The

improvement is mainly due to the increase in Q factors of the BST capacitors with higher bias. The circuit has a size of 0.7 mm x 0.5 mm.

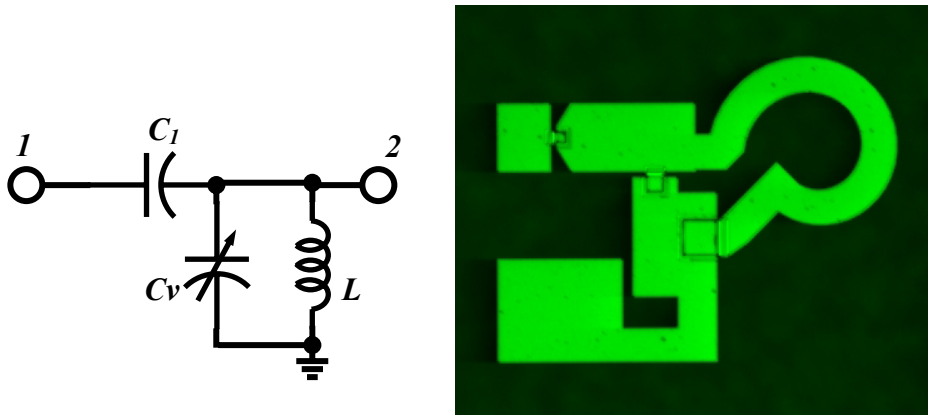

Figure 3.1 Schematic and photograph of 1st order tunable BPF

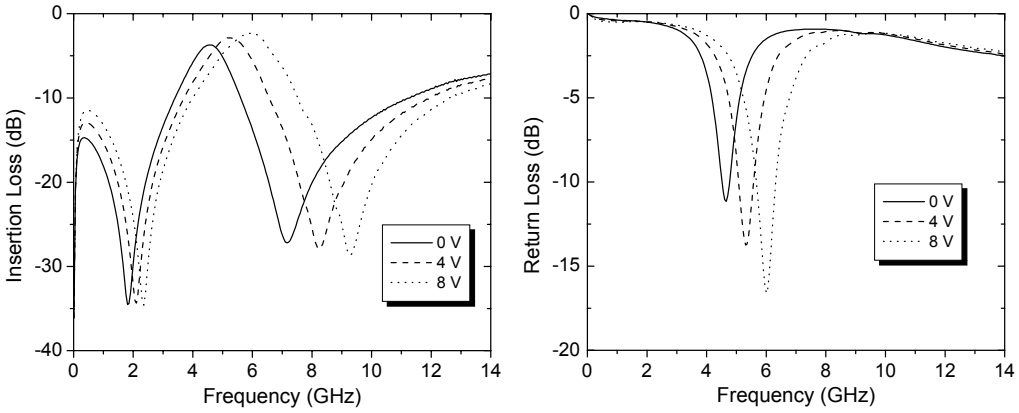

Figure 3.2 Insertion and return losses of 1st order tunable BPF

A high order lumped element tunable band-pass filter was designed and fabricated as shown in Figure 3.3. The series LC resonator in Chebychev band-pass prototype was transformed to a parallel LC circuit using J-inverters. The ground pad is located in the center of the circuit. The inductors in the circuit are implemented

using circular spiral structures which are placed outside around the ground pad to reduce coupling between the components and ground. The DC bias voltage on the BST capacitors was applied through the ports using bias-tees. Large DC block capacitors were employed for each shunt inductors.

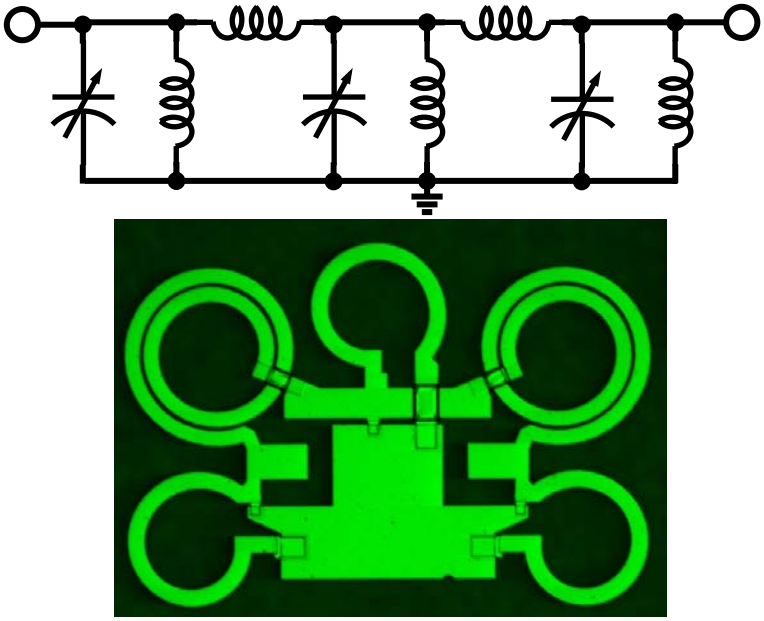

Figure 3.3 Schematic and photograph of BST tunable BPF

The insertion loss and return loss of the filter are shown in Figure 3.4. The center of the passband frequency can be tuned from 3.4 GHz to 4.4 GHz by biasing the capacitors at 6 V, which corresponds to 29 % tunability from zero bias. The measured insertion loss within the passband was better than 13 dB and the return loss within the passband was better than 15 dB. The return loss within the passband is relatively low. The losses in the circuit are mainly due to resistive losses in the passive components. The Q factors of the spiral inductors in this frequency range are typically from 20 to 30. Also the BST film on this wafer was found to be lossier and

leakier than our typical films. As compared with the aforementioned simple 1st order band-pass filter, this circuit demonstrates a well defined bandpass with better rejection. The circuit has a size of 1.4 mm x 1 mm.

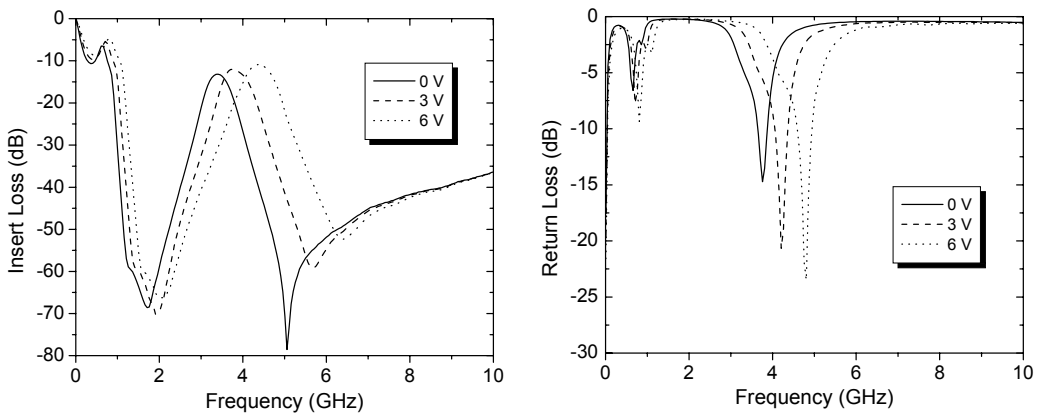

Figure 3.4 Insertion and return losses of BST tunable BPF

A lumped element tunable low-pass filter based on a 3rd order 0.2 dB ripple Chebychev prototype was designed and fabricated as show in Figure 3.5. As with the bandpass filters, the DC bias voltage on the BST capacitors was applied through the ports using external bias-tees. The insertion loss and return loss of the filter are shown in Figure 3.6. The measurement results show that the 3 dB cut-off frequency can be tuned from 9.2 GHz to 12.6 GHz by biasing the capacitors at 10 V, which corresponds to 37 % tunability from zero bias. The measured insertion loss within the passband was better than 0.8 dB and the return loss within the passband was better than 11 dB. The circuit has a size of 0.8 mm x 0.7 mm.

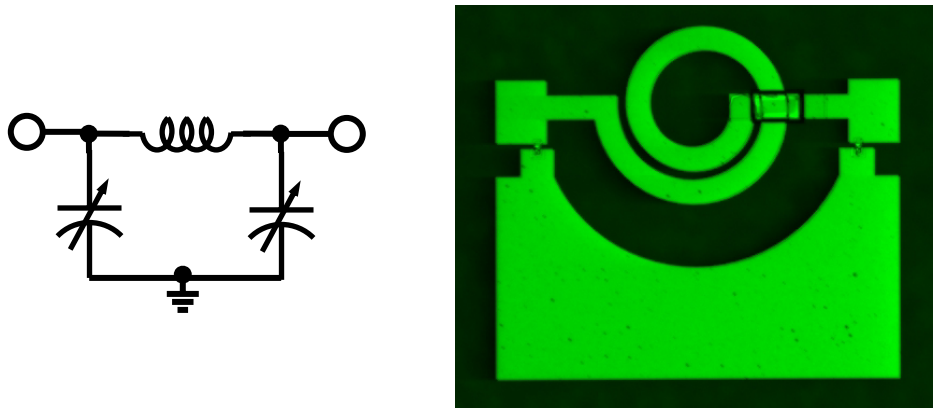

Figure 3.5 Schematic and photograph of 3rd order LPF

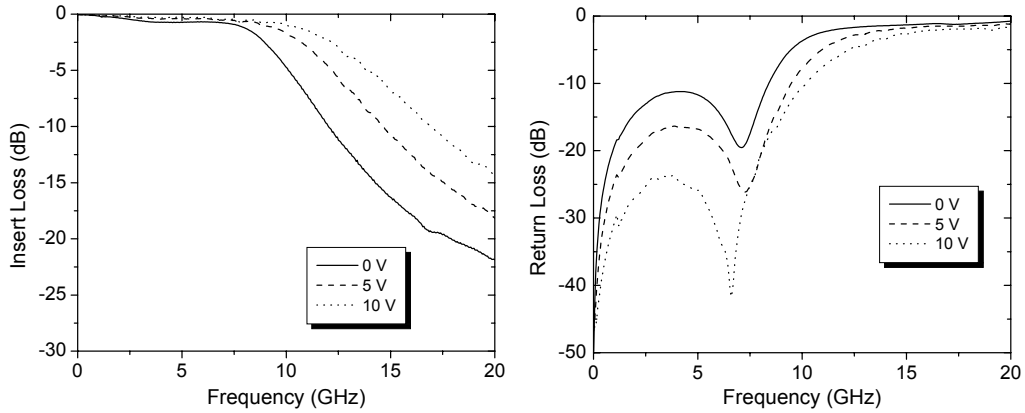

Figure 3.6 Insertion and return losses of 3rd order BST tunable LPF

A 5th order tunable low-pass filter based on a 5th order 0.2 dB ripple Chebychev prototype was also designed and fabricated as shown in Figure 3.7. The DC bias voltage on the BST capacitors was applied through the ports using external bias-tees. The insertion loss and return loss of the filter are shown in Figure 3.8. The filter achieved 56 % tunability under the application of a 16 V dc bias, corresponding to a tuning of the 3 dB cut-off frequency from 6.4 GHz to 10 GHz. The measured

insertion loss within the passband was better than 1 dB and the return loss within the passband was better than 10 dB. The circuit has a size of 1.1mm x 0.7mm.

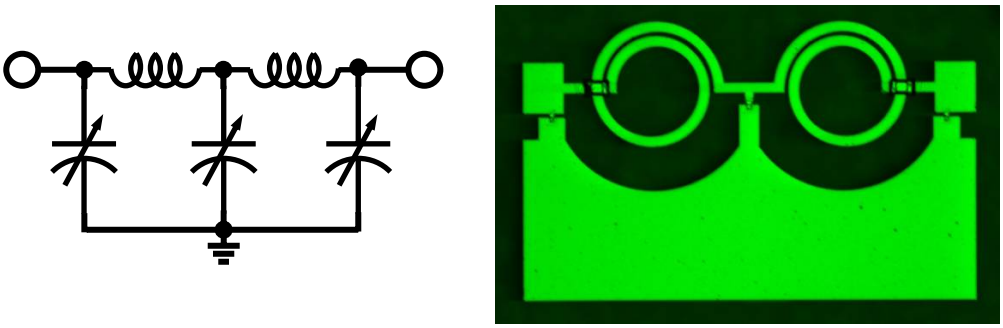

Figure 3.7 Schematic and photograph of 5th order LPF

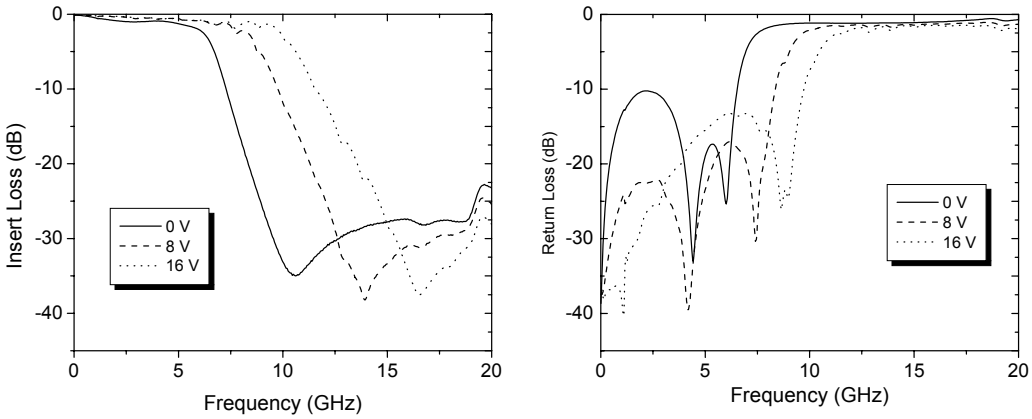

Figure 3.8 Insertion and return losses of BST tunable LPF

3.2. Phase shifters

Phase shifters are devices that provide a variable insertion phase in a microwave signal path without changing the physical path length. They are a key building block in the implementation of phased-array antennas as well as many other radar and

telecommunication applications. Lumped-element phase shifters are superior from the perspective of conserving chip area. Phase shifters using all-pass filter networks were designed and fabricated using the optimization technique described in Chapter 2. These structures provide not only a broadband phase shift design, but also a compact die size [3]. Two types of all-pass networks are shown in Figure 3.9 and 3.11. In Figure 3.9, a highly resistive line is used to bias the top capacitors. The other tunable capacitors are biased through the ports using external bias tees. As we can see in Figure 3.10, the circuit with capacitive shunts (phase shifter I) demonstrated a maximum of 90° differential phase shift at 5.5 GHz. The maximum insertion loss was -1.5 dB and the return loss was better than -15 dB at this frequency. This gives a figure of merit of 60°/dB at the design frequency. Measuring 1.5 mm by 1 mm, its small dimensions demonstrate the advantages of BST circuits with compact all-pass network topologies.

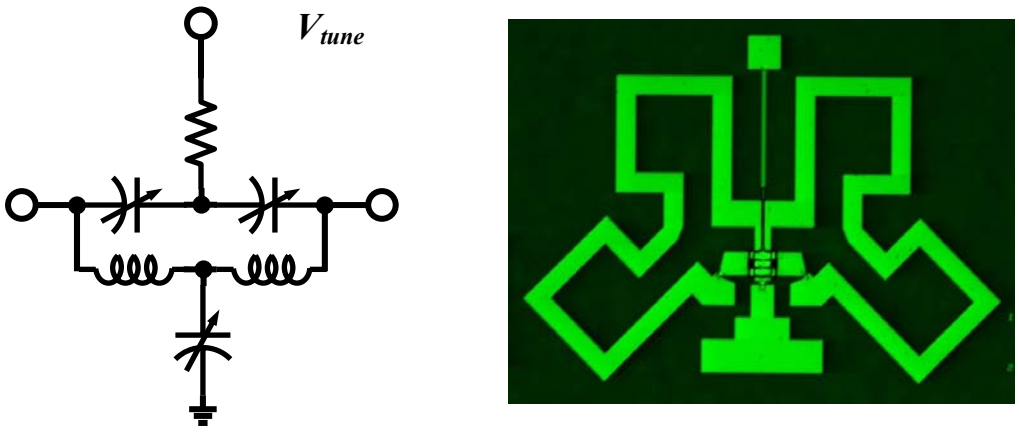

Figure 3.9 Schematic and photograph of phase shifter I

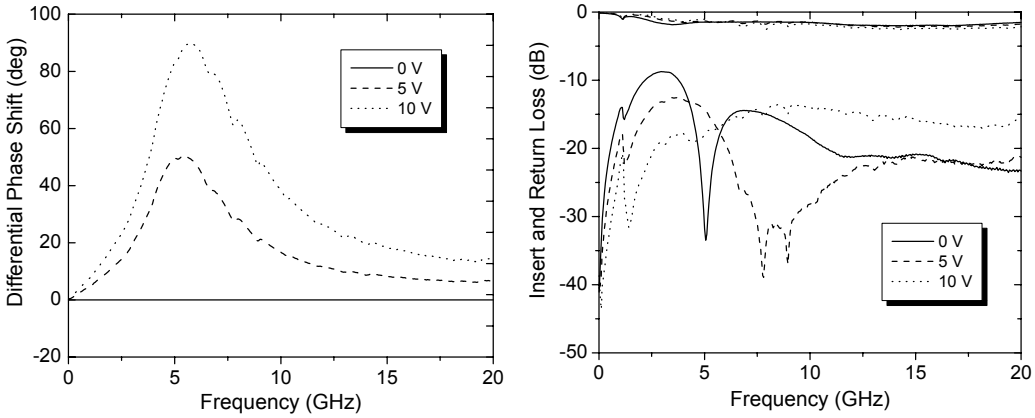

Figure 3.10 Performance of phase shifter I

In Figure 3.12, the measurement results of a phase shifter with inductive shunts (phase shifter II) are presented. The phase shifter exhibits a maximum of 120° differential phase shift at 7.5 GHz. The maximum insertion loss was -2.2 dB, and the return loss was better than -8 dB at this frequency. This gives a figure of merit of 55°/dB at the design frequency. With a slightly smaller size of 1.3 mm by 1 mm, it further proves the advantages of BST technology. With multiple sections, a larger phase shift can be achieved using highly integrated all-pass networks.

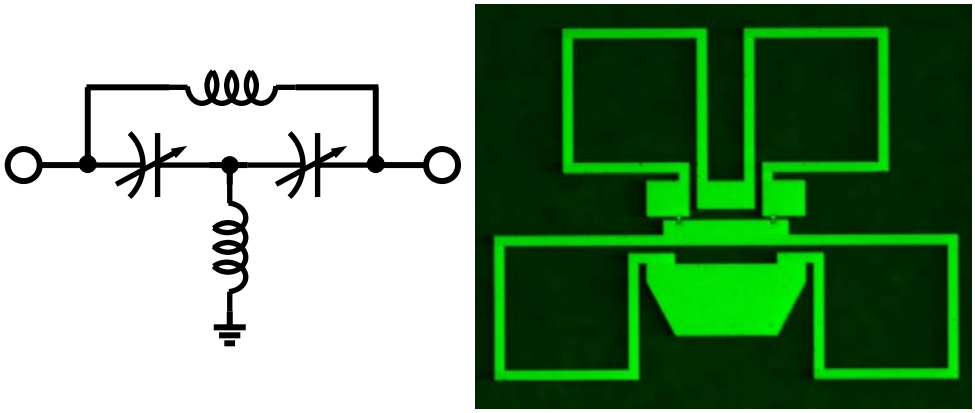

Figure 3.11 Schematic and photograph of phase shifter II

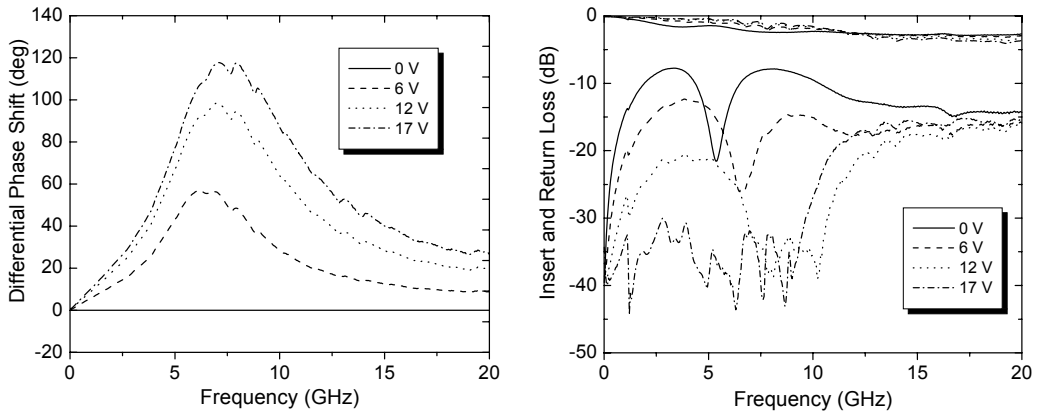

Figure 3.12 Performance of phase shifter II

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Chapter 4. GaN HEMT MMIC integrated with BST films

4.1. Integration of BST thin films with GaN HEMTs

AlGaN/GaN HEMTs have attracted considerable interest as power devices in microwave applications, promising greater than a tenfold increase in power-density as compared with GaAs devices. Similarly, $Ba_xSr_{1-x}TiO_3$ (BST) thin films have been investigated for microwave circuit application because of their high dielectric constant (200-300), high tunability (>3:1), relatively low loss ($\tan\delta < 0.01$), and fast switching speed (sub-nS). Several research groups have exploited the field-dependent dielectric constant of BST in RF varactor circuits [1][2][3]. BST-based varactors are especially attractive for high-power RF circuits since they can sustain relatively large ac fields at low average dc fields, unlike diode technologies. Additionally, due to its high dielectric constant, BST is a candidate for very compact MMIC dc blocking capacitors, promising a 100-fold reduction in capacitor area as compared with SiN and SiO_2 capacitors. The goal of this work was to develop an integration strategy for exploiting the complementary characteristics of GaN HEMTs and BST capacitors in monolithic circuits.

Initial efforts to integrate a standard BST capacitor process with a GaN HEMT process highlighted some key technical challenges. First, early measurements indicated that the AlGaN 2DEG channel was damaged during the RF magnetron sputtering of BST, most likely due to ion damage from the plasma. Secondly, both HEMT and BST devices require high temperature processes which adversely impact

each other. Typical electrode metallurgies for BST capacitors containing Au could not sustain the rapid thermal annealing (RTA) required for the ohmic contacts of the HEMT. Similarly, the ohmic contacts on the GaN HEMT can be adversely affected by the BST deposition process, which typically requires long duration at high substrate temperatures in an oxidizing environment. In this thesis, several experiments for HEMT/capacitor integration are described and analyzed. We show our solutions to these problems, providing a successful method of process integration for future active GaN circuit design and fabrication using BST capacitors.

The HEMT devices tested were grown by metal organic chemical vapor deposition (MOCVD) on sapphire substrates. The epitaxial structure consisted of a semi-insulating Fe-doped GaN base layer [4], followed by a 290 Å thick $Al_{0.35}Ga_{0.65}N$ barrier layer. The room temperature sheet electron concentration and Hall mobility were ~1.5×10^{13} cm^{-2} and ~1170 cm^2/Vs, respectively. The HEMT device fabrication started with ohmic contact formation. Ti/Al/Ni/Au (200/1500/375/500 Å, respectively) were evaporated and annealed at 870 ºC for 30 seconds in N_2. Device mesa isolation was then performed using a Cl_2 reactive ion etch (RIE). TLM measurements showed an average contact resistance of 0.4 Ω·mm, and a sheet resistance $R_{sq} \approx 370$ Ω/□. The gate contact was formed by evaporating Ni/Au/Ni (300/2500/500 Å, respectively). The final processing step was a 170 nm PECVD Si_3N_4 passivation layer, which has been shown to eliminate dc to RF

dispersion [5]. The gate width and length on all the devices tested were 2x75 μm, and 0.7 μm, respectively.

A 3000Å BST thin film was grown on an AlGaN/GaN substrate with 3000Å of electron-beam evaporated Pt that was pre-patterned by liftoff as a bottom electrode for an MIM capacitor. The BST films were deposited using RF magnetron sputtering. The film growth conditions were optimized for tunability and microwave loss performance; typical growth conditions for a ~3000 Å $Ba_{0.5}Sr_{0.5}TiO_3$ film are a substrate temperature of 700 ºC, base pressure of 50 mTorr (90 sccm Ar/10 sccm O_2), and RF power of 150 W on two 3" targets. Pt/Au top electrodes were evaporated followed by a BST etch in 1:1 buffered HF:DI water. The BST capacitors were passivated by a 3000 Å SiO_2 film to prevent contamination during subsequent processing. This passivation layer also functions as an insulating layer beneath the overpass bridge, which connects the top electrodes to a high-conductivity interconnect metal layer.

In this work, both BST capacitors and HEMT devices were fabricated on the same samples. A schematic cross-section of the process and a completed parallel plate capacitor and HEMT device is shown in Figure 4.1.

Reference HEMT devices were fabricated without incorporating the BST film process as an experimental control sample. The HEMT devices were subjected to I-V characterization. Pulsed I-V measurements at 200 ns show the drain current density reaches 1.37 A/mm for V_{gs}=0 V.

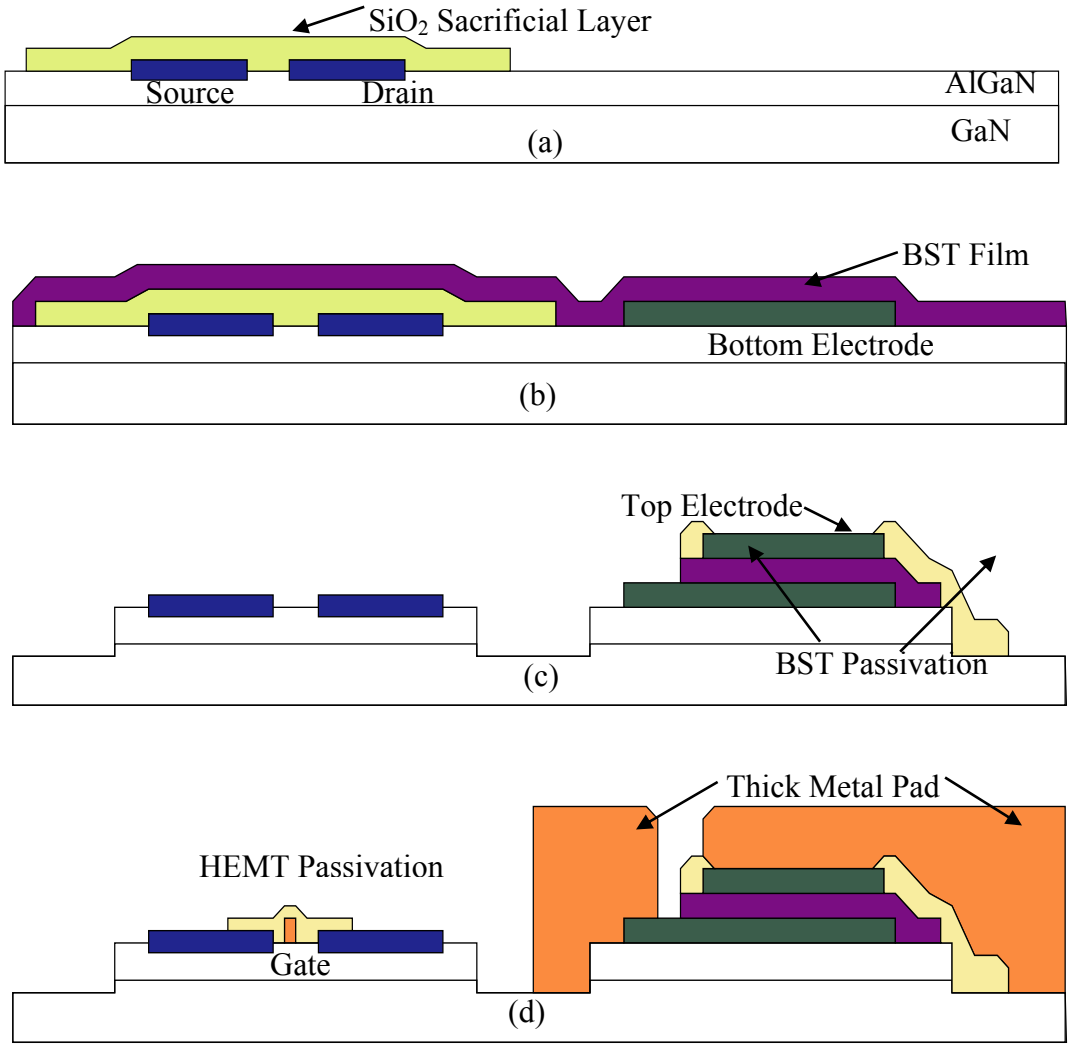

Figure 4.1 Process flow (a) Source/drain ohmic contacts with SiO_2 sacrificial layer; (b) Prepatterned bottom electrodes and BST film deposition; (c) BST pattern etch, top electrodes, mesa isolation and BST film passivation; (d) Gate metallization, HEMT passivation and thick metal pad

BST capacitors were first fabricated directly on the AlGaN surface before the HEMT process. Following the BST deposition, the BST was selectively removed and HEMT devices were fabricated in the area where the BST film was completely

removed. In Figure 4.2, pulsed I-V curves measured at 200 ns on both a control HEMT and a HEMT exposed to the plasma during BST growth are compared. Exposure to the plasma decreased the current density by 28 % and decreased the magnitude of the pinch-off voltage from -7.5 V to -6 V. Further investigation showed that both the sheet electron concentration and Hall mobility were decreased due to plasma damage in the HEMT structure during the BST sputtering [6]. To avoid this damage, a barrier layer is required to protect the 2DEG during BST growth. A thin SiO_2 layer was introduced for this purpose. Because of the stability of group III-nitrides, the SiO_2 layer should not react with the AlGaN. Since it can be wet etched uniformly by the same etchant (buffered HF) as the BST film, the choice of a SiO_2 buffer layer is compatible with both the GaN HEMT and BST capacitor processes.

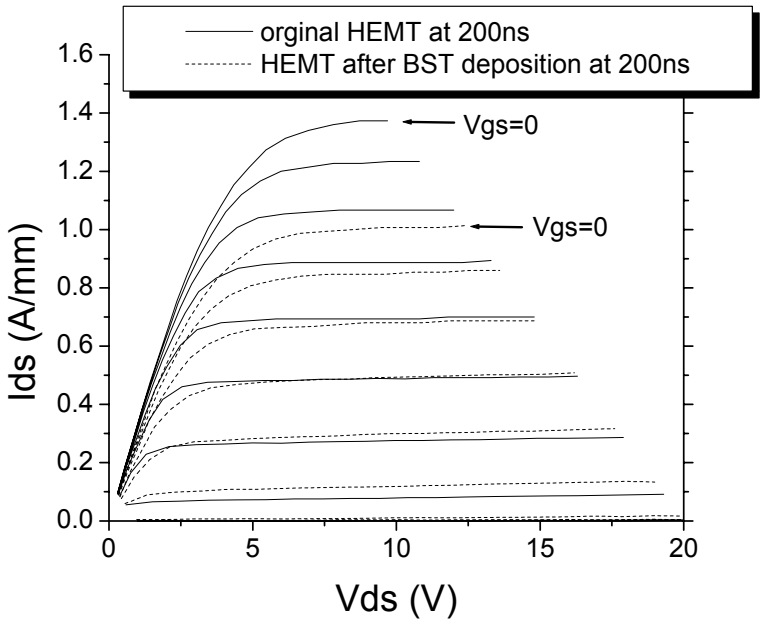

Figure 4.2 200 ns pulsed I-V for HEMT device with BST deposition and control device.

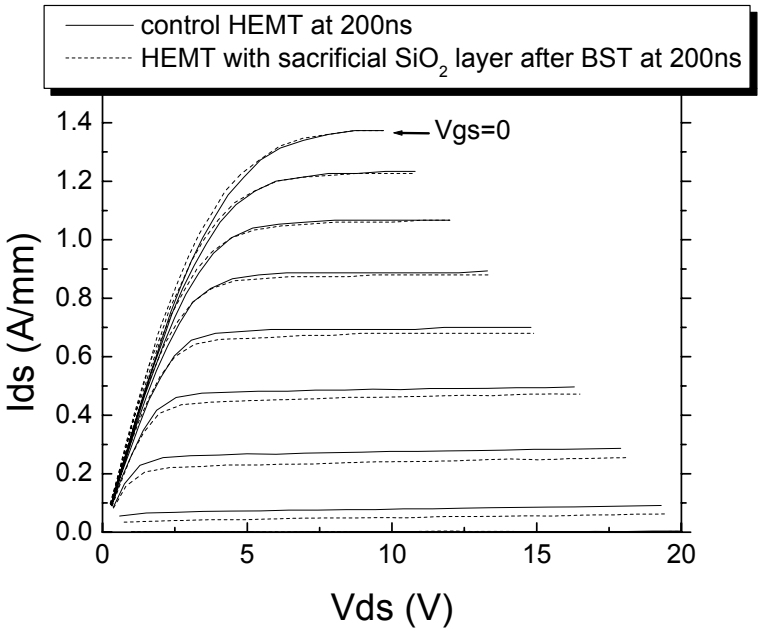

Figure 4.3 200ns pulsed I-V for HEMT device protected by sacrificial SiO_2 with BST deposition and control device.

Based on these initial findings, a 3000 Å S_iO_2 layer was evaporated on the HEMT device area after the bottom electrodes of the BST capacitors were pre-patterned. Following the BST deposition, both the SiO_2 and BST films were etched away from the HEMT device area using buffered HF during the BST pattern definition. In Figure 4.3, pulsed I-V curves at 200 ns on both a control HEMT and a HEMT protected by SiO_2 were compared. The performance of the HEMT was not degraded by exposure to the BST deposition. Thus, a 3000 Å sacrificial SiO_2 layer

efficiently protects the HEMT's 2DEG channel. Additionally, the pinch off voltage did not change and the average ohmic contact resistance was the same as in the control devices, indicating that the SiO_2 did not react with the AlGaN during the approximately 3 hour high temperature BST deposition.

While the sacrificial SiO_2 layer solved one problem, another problem that remained in the integration was that the source/drain annealing caused a reduction in the BST capacitors' breakdown voltage. Before the source/drain annealing, the BST capacitors could sustain the application of more than a 20 V bias, but after the annealing the capacitors broke down at 3 V. Even for BST devices with pure Pt top electrodes, the breakdown voltage was still as low as 7 V. Devices with such low breakdown voltages cannot be used in high power microwave GaN HEMT circuits. To avoid this problem, the sequence of process steps was rearranged. Source and drain ohmic contacts were fabricated first, followed by the e-beam evaporation of a 3000 Å SiO_2 film. The BST capacitors were made following the completion of these two steps, with HEMT device mesa isolation and gate metallization following the BST capacitor fabrication. The complete process flow is depicted in Figure 4.1.

The effect of the heater ramp rate during the BST deposition was also investigated. When the heater ramp rate was 50 ºC/min, the ohmic contact resistance increased from 0.4 Ω·mm to 0.9 Ω·mm after BST deposition. In addition, the source and drain contacts appeared cracked, delaminated and discolored as shown in Figure 4.4. The thermal mismatch between the ohmic contact metals and SiO_2 layer could account for both the metal and SiO_2 layers cracking during the rapid temperature

change due to the heater ramping. Through cracks in the SiO_2 layer, the source and drain contact metals were exposed to O_2 from the sputtering ambient and oxidized. The oxidized metals were then etched and delaminated in the buffered HF during the BST etch. Ohmic contacts protected by intact SiO_2 were not harmed by the buffered HF. With a slower heater ramp rate (20 ºC/min) during BST deposition, no cracking, delamination, or significant discoloration was observed on the source and drain ohmic contacts. The average ohmic contact resistance was 0.4 Ω·mm both before and after the BST deposition. A C-V measurement was performed on BST capacitors manufactured with the integrated GaN/AlGaN HEMT-BST process. The capacitance density at 0V bias was 14.3 fF/μm^2 and the tunability was 3.3:1 with a 20 V bias. The capacitance density is about 50 times that of the usual SiN (2000 Å) MMIC capacitor value, which is typically 0.3 fF/ μm^2. The 1MHz zero-bias Q factor of this film was 85.

In this section, a new method has been developed to incorporate BST thin film capacitors in microwave circuits based on GaN HEMTs has been described. A 3000 Å sacrificial SiO_2 layer protected the AlGaN surface and 2DEG from plasma damage. Reduction of the heater ramp rate to 20 ºC/min during BST growth mitigates damage to the source and drain ohmic contacts, such as cracking and delamination. Using BST thin films, varactors and small area dc blocking capacitors can be integrated into GaN HEMT microwave circuits. High voltage (>20 V) operation and compatibility with a monolithic process are other advantages realized in this work. Higher operating voltages can be achieved by increasing the BST film

thickness or using BST capacitors in series. Compact GaN MMIC circuits, such as power amplifiers, oscillators and VCOs, can be implemented with the integration of BST film to the GaN/AlGaN process.

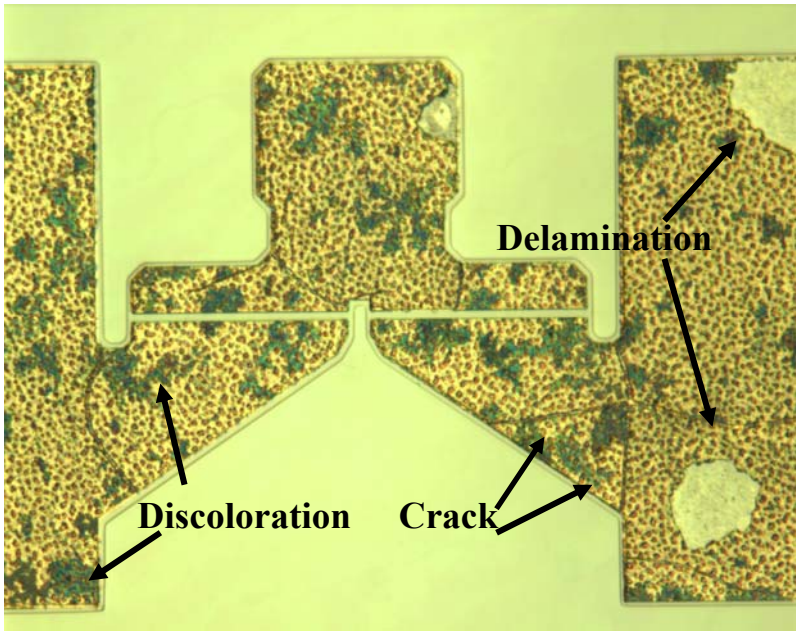

Figure 4.4 Photograph of source and drain ohmic contacts after BST deposition with heater ramp rate of 50ºC/min.

4.2. GaN HEMT Oscillator Integrated with BST Thin Films

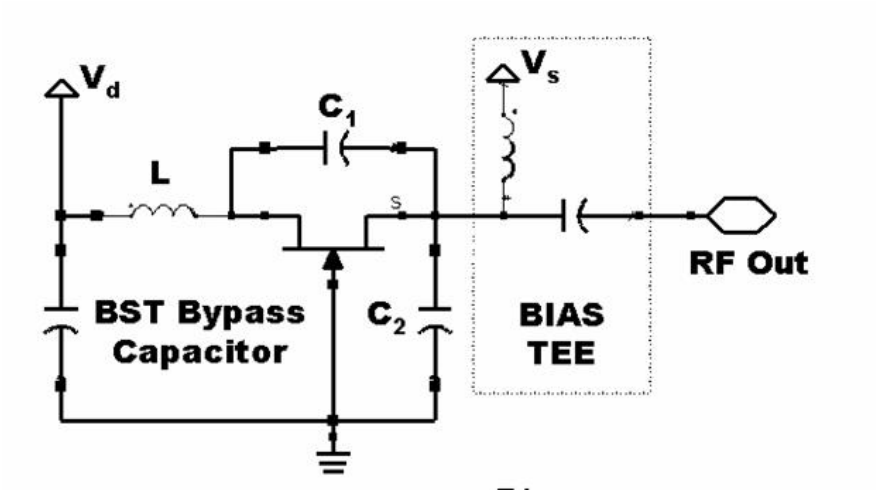

Figure 4.5 Circuit schematic of the GaN oscillator.

The previous section demonstrated a solution for integration of BST capacitors into GaN HEMT microwave circuits which avoids the degradation of both the GaN HEMTs and BST capacitors. In this section, a low-phase noise 5 GHz GaN oscillator integrated with BST capacitors is presented.

A common-gate oscillator structure with an LC resonator on the drain is used. The simplicity of this design makes it easier to control parasitics from the active and passive components during the design process. Also, this LC positive feedback oscillator is considered to be suitable for high-power applications. The bias of the HEMT device was chosen for best linearity and stability of the output signal.

The circuit was designed using ADS as shown in Figure 4.5. To achieve an accurate model, the small-signal properties of the device were characterized in the frequency range from 50 MHz to 25 GHz. The extrinsic parameters were extracted by measuring the small-signal S-parameters for the open and short structures of the

device. The intrinsic parameters were then obtained by de-embedding the extrinsic parameters.

The inductor and capacitors used in the resonator were selected using measurements on fabricated passive components. Special attention was paid to the development of adequate models for the passive components. The average Q factors of the on-wafer spiral inductors and SiN capacitors were 25 and 67 respectively at 5 GHz. Following the typical small-signal design procedure for negative resistance transistor oscillators, the load was designed according to the oscillation conditions as follows:

$$X_L(f_0) = -X_{out}(f_0)$$

$$\text{and } R_L(f_0) = \frac{1}{3}\left|R_{out}(f_0)\right|$$

where $R_{out}(f_0)$ is the real part of negative resistance at the output of the HEMT and $X_{out}(f_0)$ is the imaginary part at the resonance frequency. $R_L(f_0)$ and $X_L(f_0)$ are the real and imaginary parts of the load network with the resonator. f_0 is the resonance frequency.

BST capacitors were used as RF bypass capacitors in the circuit. They significantly reduced the die area of oscillator. Also, since BST capacitors have higher self-resonance frequencies than traditional SiN capacitors with comparably large capacitances, they are easier to model. These properties make them attractive for compact C-band MMIC design. Besides these benefits, the high tunability of BST capacitors allows for more flexibility in various microwave circuits.

Transient and harmonic simulations were done by using the curtice C_FET3 model, which is used to simulate large-signal performance of GaN HEMTs in Agilent ADS software environment. The output power and frequency were verified.

The AlGaN/GaN HEMT devices were grown by MOCVD on sapphire substrates. The epitaxial structure consisted of a semi-insulating Fe-doped GaN base layer, followed by a 290 Å thick $Al_{0.27}Ga_{0.73}N$ barrier layer. The room temperature sheet electron concentration and Hall mobility were ~1.15×10^{13} cm^{-2} and ~1211 cm^2/Vs, respectively. The GaN HEMT device has gate length and width of $L_g = 0.7$ μm and $W_g = 2 \times 100$ μm, current density $I_{dss} = 1$ A/mm at $V_{gs} = 1$ V, and a breakdown voltage larger than 35 V. The measured unity current gain cutoff frequency (f_t) of the device is 20 GHz.

The GaN HEMT MMIC fabrication integrated with BST capacitors started with the formation of source and drain ohmic contacts, followed by the processing of BST capacitors. After that, the HEMT devices were completed with mesa isolation and gate metallization. The GaN HEMT was passivated by a PECVD SiN layer, which was also used as dielectric material in fixed MIM capacitors. Capacitors and spiral inductors with PMGI cross-overs were fabricated in the last steps. A detailed fabrication description and discussion of the integration are presented in Appendix A. The chip size was 1.4 mm x 1.6 mm. As shown in Figure 4.6, the LC resonator tank was at the drain terminal of the HEMT device. The feed-back path between the source and drain was made by SiN MIM capacitors.

The fabricated circuits were characterized on-wafer using air-coplanar probes and an Agilent Spectrum Analyzer E4440 with the phase noise option. Bias feeds for

the gate and drain were provided through off-wafer bias tees for convenience in testing.

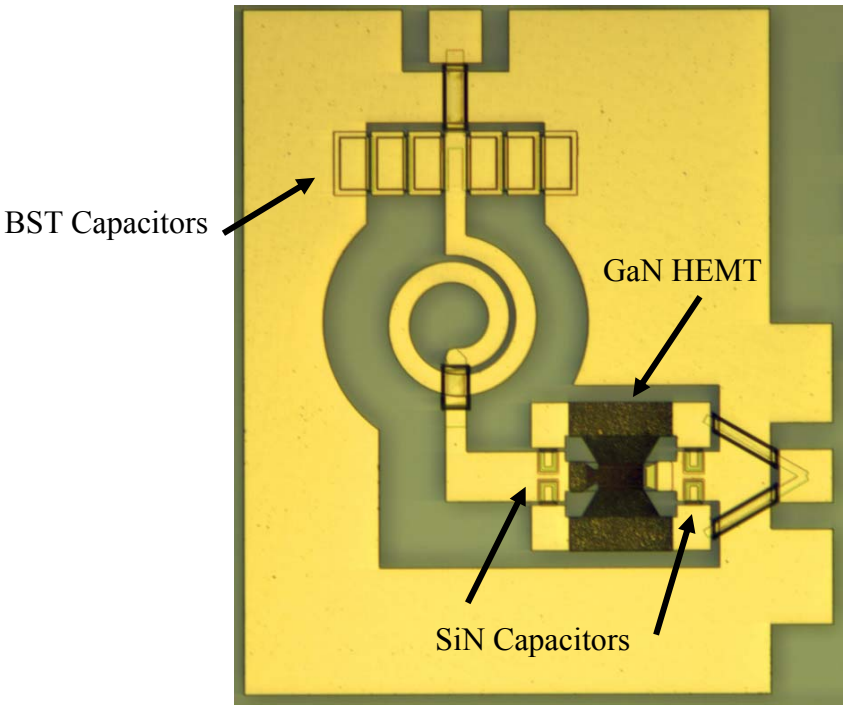

Figure 4.6 Chip photomicrograph of the developed oscillator.

A. Power and efficiency measurements

The output power of the oscillator was measured at different drain bias voltages. The oscillator delivered a maximum of 20.5 dBm at 5.3 GHz into a 50-Ω load when biased at Vds = 15 V and Vgs = -3 V, with a dc-to-RF efficiency of 12.5%. The maximum efficiency of 14.1% occured at Vds = 10 V. The output power and dc-to-RF efficiency as functions of drain voltage are shown in Figure 4.7. The efficiency drops fast as the self-heating effect becomes significant when the drain bias voltage is increased. The output power and efficiency could be improved if circuits were fabricated on a semi-insulating SiC substrate, which has better thermal conductivity.

The second harmonic was measured to be 32 dB below the fundamental signal for all measured drain bias voltages.

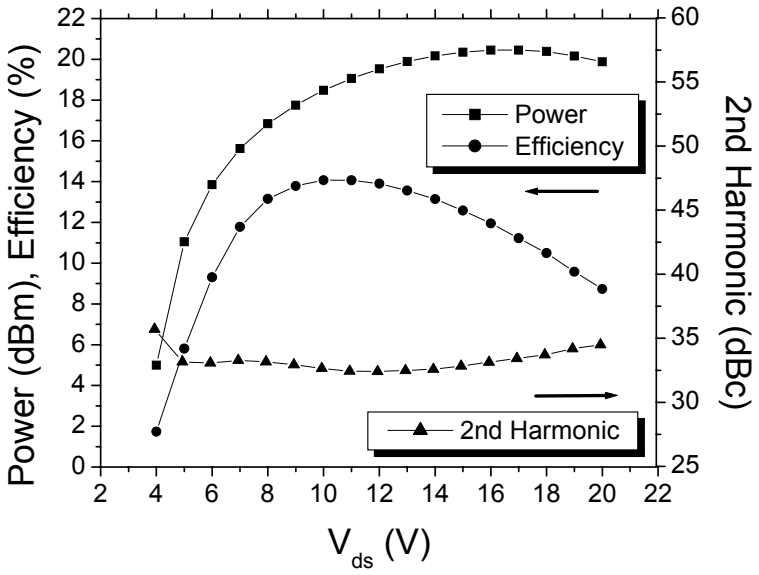

Figure 4.7 Output power, dc-to-RF efficiency and second harmonic as functions of drain bias voltage with V_{gs} = -3 V.

B. Phase noise measurement

The phase noise of the oscillator was measured across an offset frequency range of 100 Hz to 10 MHz. Figure 4.8 shows that the phase noise was -105 dBc/Hz at an 100 kHz offset from a 5.3 GHz carrier. The dependence of phase noise on drain and gate bias voltages were also investigated. The results are given in Figure 4.9. Despite some variations, there did not appear to be any clear dependence of phase noise on the gate bias voltage. Phase noise increased slightly with larger drain bias voltages. According to the Leeson formula:

$$L(f_m) = 10\log\left\{\frac{1}{2}\left[1+\frac{1}{f_m{}^2}\left(\frac{f_0}{2Q_l}\right)^2\right]\frac{FkT}{P_s}\left(1+\frac{f_c}{f_m}\right)\right\}$$

where Q_l is the loaded quality factor, f_0 is the resonant frequency, f_c is the flicker corner frequency of the device, f_m is the offset frequency, P_s is the amplifier's input signal power, F is its noise figure, k is Boltzmann's constant, and T is the temperature.

As the drain bias voltage increases, several factors change simultaneously. These effects have to be investigated in detail and could lead to ways of further understanding and improving the phase noise performance.

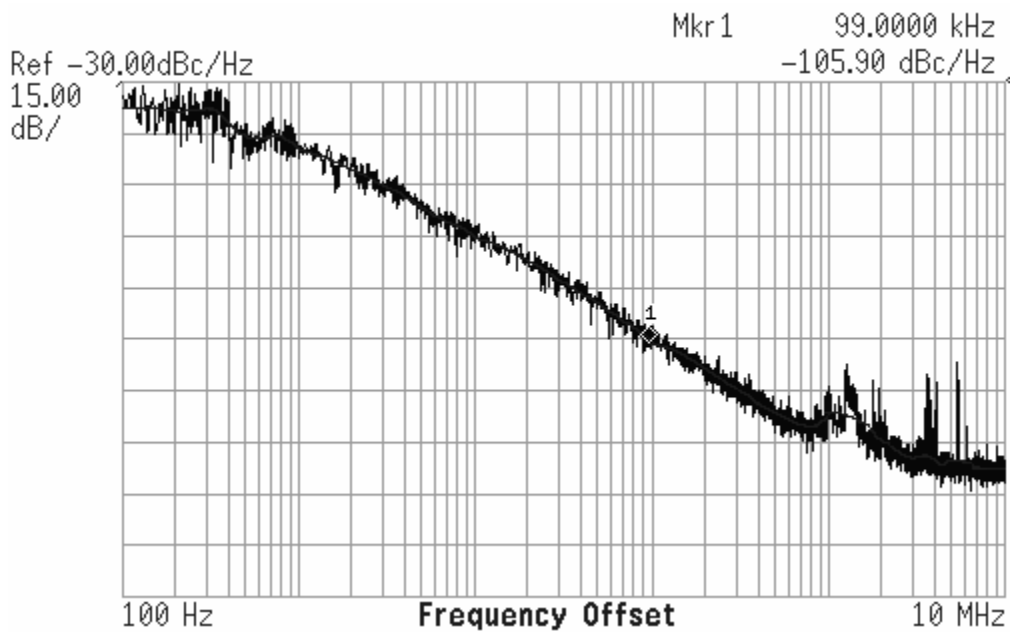

Figure 4.8 Measured phase noise of a GaN HEMT oscillator at a 5.3 GHz carrier with bias of V_{gs} = -3 V and V_{ds} = 15 V.

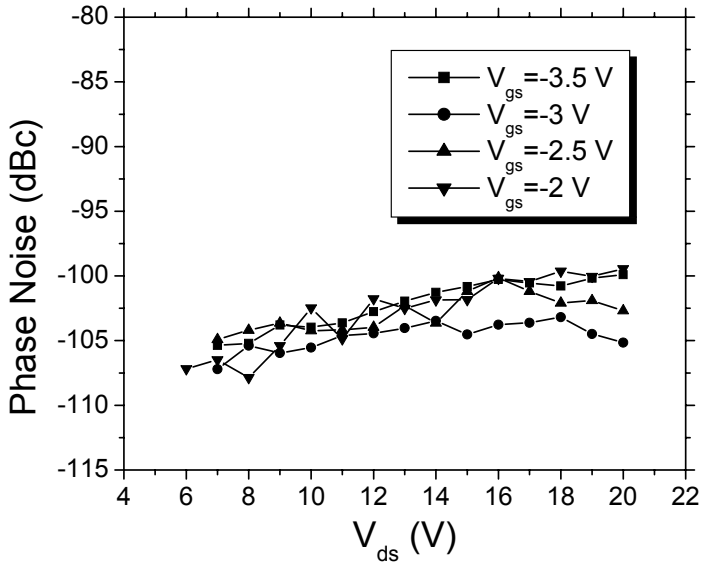

Figure 4.9 Phase noise as a function of drain and gate biases. The results are measured at an offset frequency of 100 kHz from a 5.3 GHz carrier.

In this section, a MMIC GaN HEMT low noise oscillator designed, fabricated, and measured for C-band applications is discussed. In order to reduce the die area, BST capacitors with a high dielectric constant are used for DC block capacitors. The measured phase noise was -105 dBc/Hz at a 100 kHz offset from a 5.3 GHz carrier. The oscillator delivered a single-ended output power of 20.5 dBm with a dc-to-RF efficiency of 12.5%. Thus, it has been demonstrated that a low phase noise and high output power oscillator can be fabricated using GaN HEMT technology.

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Chapter 5. GaN HEMT device modeling and analysis

5.1. Small signal modeling

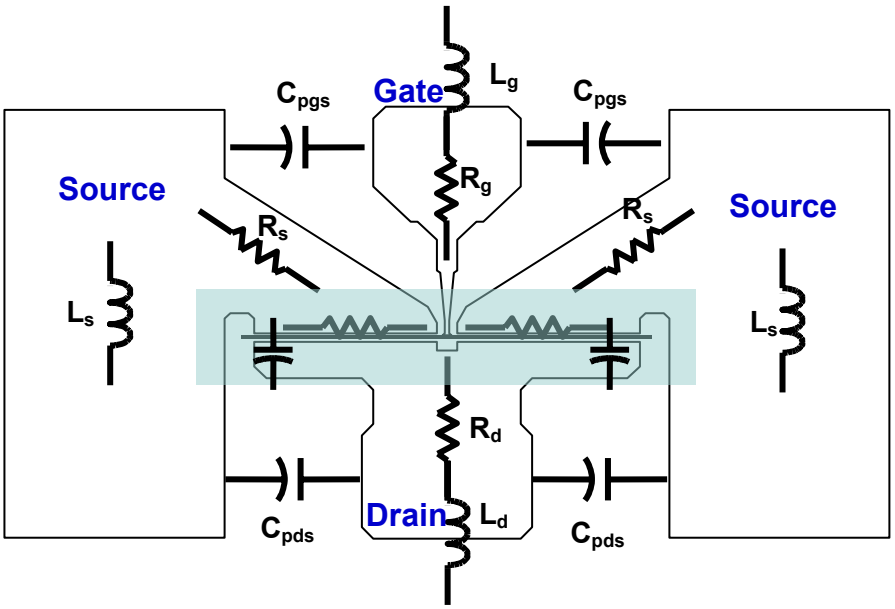


Figure 5.1 HEMT small-signal model showing physical origin of elements

In Figure 5.1, the same equivalent circuit is shown superimposed on a device layout, indicating the physical origin of the equivalent circuit. A fairly standard HEMT equivalent circuit topology is shown in Figure 5.2 [1][2][3]. This topology has the advantage that the elements can be uniquely extracted. A brief discussion follows of each equivalent circuit element and its role in modeling the device physics.

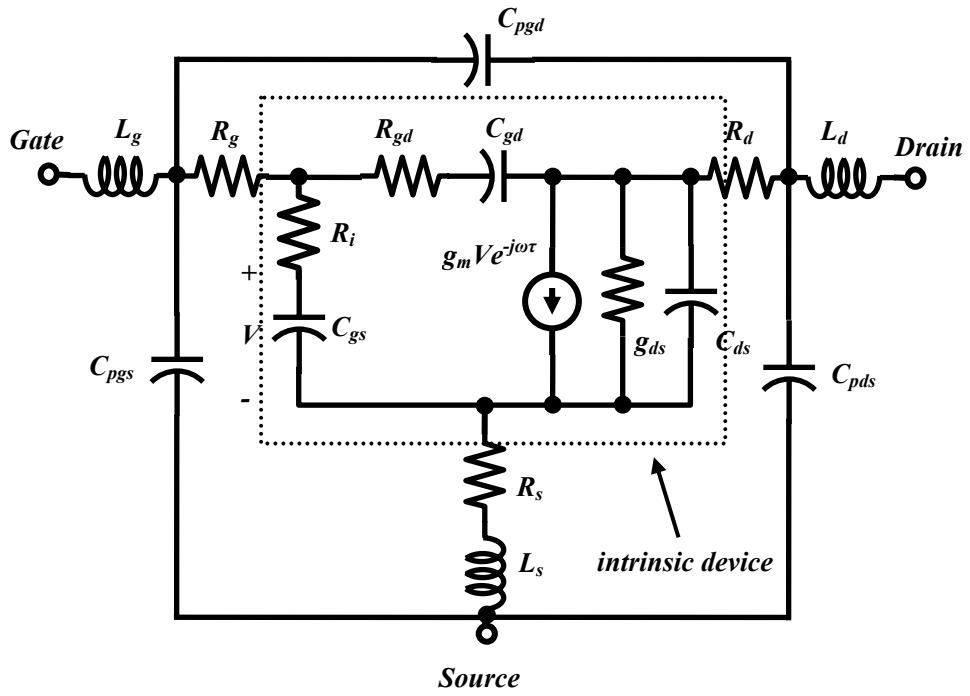


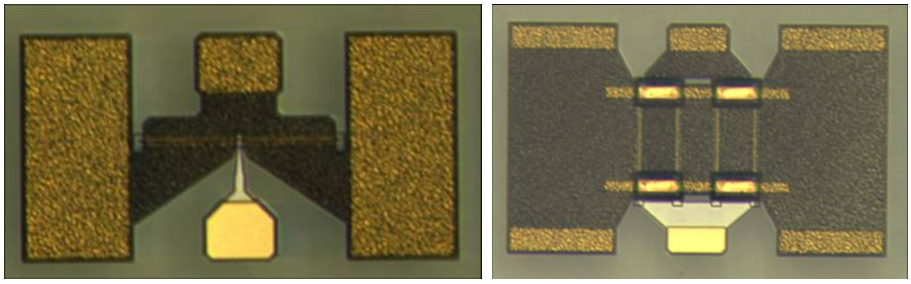
Figure 5.2 HEMT small-signal model including parasitic elements

The parasitic inductances L_g, L_d and L_s arise primarily from metal contact pads deposited on the device surface. For modern short gate length devices, the gate inductance is usually the largest of the three. Typically, L_d is on the order of 5-10 pH. The source inductance is often small, around ~3 pH. For devices utilizing via hole grounds, L_s is even smaller. The parasitic resistances R_s and R_d are included to account for the contact resistance of the ohmic contact as well as any bulk resistance leading up to the active channel. The gate resistance R_g results from the metallization resistance of the gate Schottky contact. All three resistances are on the order of several Ω for modern microwave devices. Although these resistances are slightly bias dependent, they are commonly held constant in large-signal models. The charging resistance R_i is included in the equivalent circuit primarily to improve

the match to S_{11}. R_i is difficult to extract and is of questionable physical significance. The combination of R_g and R_i is generally used to estimate the input resistance. The capacitances C_{gs} and C_{gd} model the change in the depletion charge with respect to the gate-source and gate-drain voltages respectively. Under typical amplifier or oscillator bias conditions, the gate-source capacitance is larger because it models the change in depletion charge resulting from fluctuations in the gate-source voltage. The gate-drain capacitance C_{gd} is considerably smaller in magnitude than C_{gs} but critical to obtaining accurate s-parameter predictions. The drain-source capacitance C_{ds} is included in the equivalent circuit to account for geometric capacitance effects between the source and drain electrodes. C_{gs} and C_{gd} are highly bias dependent, but C_{ds} is usually not considered to be bias dependent. The transconductance g_m is a measure of the incremental change in the output current I_{ds} for a given change in input voltage V_{gs}. The output conductance g_{ds} is a measure of the incremental change in output current I_{ds} with the output voltage V_{ds}. The transconductance cannot respond instantaneously to changes in gate voltage; this delay is described by the transconductance delay τ. Physically, the transconductance delay represents the time it takes for the charge to redistribute itself after a fluctuation of gate voltage. Typical values of τ are on the order of 2 ps. C_{pgs}, C_{pgd} and C_{pds} are the parasitic capacitances of the pads or due to the package. L_s, L_g, L_d, R_s, R_g, R_d, C_{pgs}, C_{pgd} are C_{pds} are the extrinsic elements, which are independent of the biasing conditions. g_m, g_{ds}, C_{gs}, C_{gd}, C_{ds}, R_i and τ are the intrinsic elements, which are functions of the biasing conditions.

Before any device model can be used, values for the model's parameters must be determined. The parameter extraction procedure includes dc and RF measurements,

extrinsic parasitic component de-embedding, equivalent circuit element value calculations and optimization. Two commonly used test structure for GaN HEMT devices are shown in Figure 5.3. A "T" shape structures (Figure 5.3a) are mostly used for device performance characterization, because of their simply layout and fabrication. Parallel, multi-finger, structures (Figure 5.3b) are widely used in MMICs for high power applications, because their gate peripheries can be easily scaled up by increasing the number and width of the gate fingers.



(a) (b)

Figure 5.3 HEMT structures (a) T-shape with 2 gate fingers (b) parallel gate fingers

In order to determine the parasitic resistances (R_g, R_s and R_d) and inductances (L_g, L_s and L_d) accurately, a HEMT structure with a shorted channel was designed. The active channels were covered completely with the same metal layer used for the gate. Gate, source and drain were all shorted by this metal stripe as shown in Figure 5.4. The equivalent circuit for this shorted channel device predicts that in the frequency range below 5 GHz, the contributions of parasitic capacitances are negligible because resistances R_g, R_d and R_s are on the order of 1-10 Ω. In this case,

we can equate the following small-signal parameters with 2 port impedance parameters to be

$$Z_{11} = R_g + R_s + j\omega(L_g + L_s)$$

$$Z_{22} = R_d + R_s + j\omega(L_d + L_s)$$

$$Z_{21} = Z_{12} = R_s + j\omega L_s$$

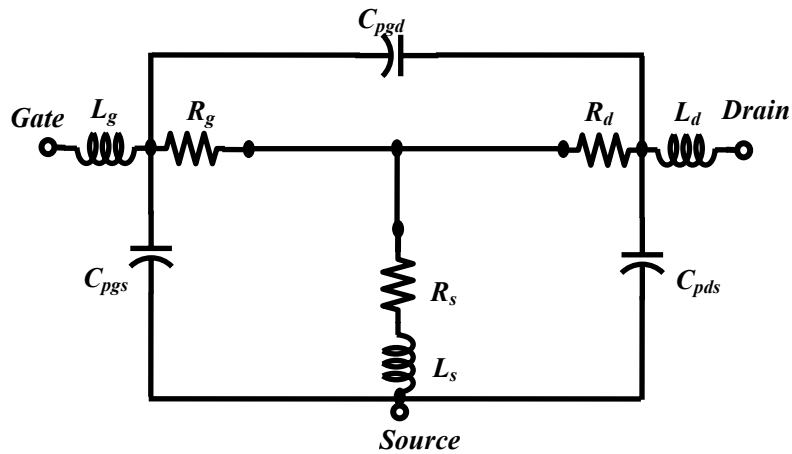


Figure 5.4 HEMT small-signal model for the shorted channel device including parasitic elements

These expressions show that the imaginary part of the Z-parameters increase linearly versus frequency; the real part is frequency independent. The values of the parasitic resistances and inductances can be obtained by using a linear data fit on the Z-parameters.

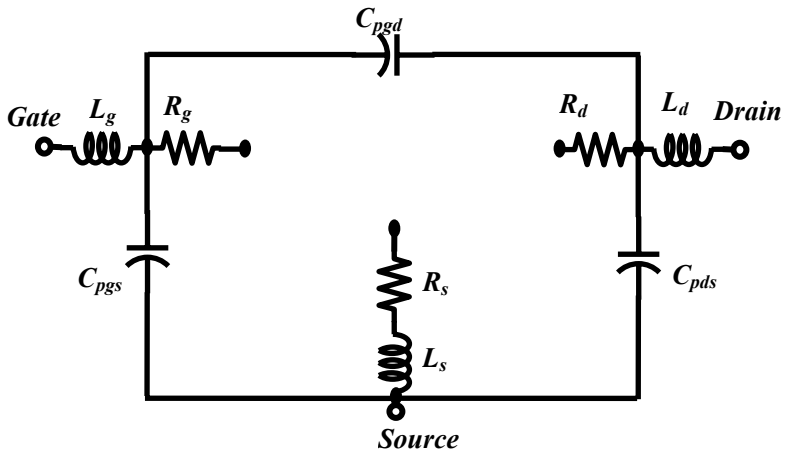


Figure 5.5 HEMT small-signal model for the open device including parasitic elements

Similarly, capacitances (C_{pgs}, C_{pds} and C_{pgd}) were extracted using an open channel structure, on which the active channel was etched using the mesa isolation process step. Thus, the 2DEG does not exist in this open channel test structure. The equivalent circuit is shown in Figure 5.5. Following the same procedure, for frequencies up to 5 GHz, the resistances and inductances have no influence on the imaginary part of the Y-parameters, which can be written as:

$$\mathrm{Im}(Y_{11}) = j\omega(C_{pgs} + C_{pgd})$$

$$\mathrm{Im}(Y_{22}) = j\omega(C_{pds} + C_{pgd})$$

$$\mathrm{Im}(Y_{21}) = \mathrm{Im}(Y_{12}) = j\omega C_{pgd}$$

Thus, the three unknowns C_{pgs}, C_{pgd} and C_{pds} can be calculated using the above expressions.

With all of the extrinsic elements calculated, the next step is to determine the intrinsic elements. Since the intrinsic device exhibits a π topology, it is convenient to use Y-parameters to characterize its frequency dependent properties. The Y-parameters are:

$$y_{11} = \frac{R_i C_{gs}{}^2 \omega^2}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right)$$

$$y_{12} = -j\omega C_{gd}$$

$$y_{21} = \frac{g_m \exp(-j\omega\tau)}{1 + jR_i C_{gs}\omega} - j\omega C_{gd}$$

$$y_{22} = g_{ds} + j\omega(C_{ds} + C_{gd})$$

where $D = 1 + R_i^2 C_{gs}{}^2 \omega^2$.

For a typical low-noise device like a GaN HEMT, the term $R_i^2 C_{gs}{}^2 \omega^2 << 1$ and $D = 1$ constitutes a good approximation. Also, assuming, $\omega\tau << 1$, we have

$$y_{11} = R_i C_{gs}{}^2 \omega^2 + j\omega(C_{gs} + C_{gd})$$

$$y_{12} = -j\omega C_{gd}$$

$$y_{21} = g_m - j\omega(C_{gd} + g_m(R_i C_{gs} + \tau))$$

$$y_{22} = g_{ds} + j\omega(C_{ds} + C_{gd})$$

The expressions above show that the intrinsic small-signal elements can be deduced from the Y-parameters as follows: C_{gd} from y_{12}, C_{gs} and R_i from y_{11}, g_m and τ from y_{21}, and, lastly, g_d and C_{ds} from y_{22}.

To determine the Y matrix of the intrinsic device from the experimental data, all of the extrinsic elements have to be de-embedded. This can be carried out using the following procedure (Figure 5.6):

1) Measure S-parameters of the device with extrinsic elements
2) Transform S-parameters into Z-parameters and subtract series L_g and L_d
3) Transform resultant Z-parameters into Y-parameters and subtract parallel C_{pgs}, C_{pds} and C_{pgd}
4) Transform resultant Y-parameters back into Z-parameters and subtract series R_g, R_s, R_d and L_s
5) Transform final Z-parameters into Y-parameters to calculate intrinsic elements

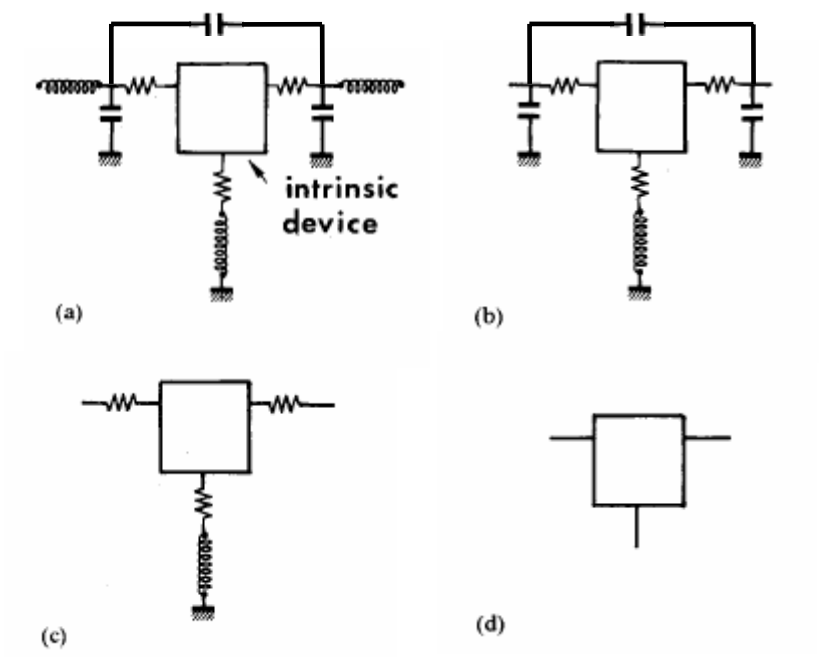


Figure 5.6 Extrinsic elements de-embedding procedure

Finally, the intrinsic parameters can be calculated from the expression derived above. Following a parameter optimization (if necessary), a small-signal model can be obtained with less than 5% error.

5.2. Large signal modeling

The empirical and physical parameters contained in large-signal device models are rarely known when devices are fabricated or acquired by the circuit or device designer. These parameters define the electrical characteristics unique to an individual device and must be extracted from measurements for use in large-signal circuit simulations. The parameter values are defined by fitting measured data to a model. The measured data can include physical parameters such as device geometry, electrical parameters such as I-V characteristics and S-parameters over a varied bias range. Also harmonic content in the output signal can be used for a better prediction [4].

Various large-signal parameter extraction methods exist for determination of the large-signal model parameters for HEMTs. Parameter extraction using large-signal power or spectrum measurements has been implemented. A more efficient method, however, is to use dc and small-signal S-parameter measurements to determine the large-signal device behavior. The method of predicting nonlinear behavior in GaAs MESFET devices by determining the bias and frequency dependence of S-parameters was originally proposed by Willing et al. [5].

In the small-signal model of a HEMT, C_{gs}, g_m, C_{gd} and g_{ds} are the dominant nonlinear elements. These nonlinear element values can be determined by the direct

extraction method presented in section 5.1. The large-signal device behavior is approximated by measuring the S-parameters over many bias voltages from the linear through the saturation regions of device operation. Static dc measurements are also made at the bias points where the S-parameters are measured. The nonlinear equivalent circuit element values are extracted at all bias voltages, thereby creating an equivalent circuit for the device at each bias point. The choice of bias levels to use with this technique is determined by the applications. This technique offers several advantages over many other large-signal parameter extraction methods. It does not require time-consuming or expensive measurements. Load-pull, transient, or harmonic output power measurements require significant expenditures of time, capital or labor. The dc and S-parameter data required in this method are easily taken using equipments typically available in any microwave laboratory.

In Agilent's ADS simulation tool, a model, EE_HEMT1, has been developed just for HEMT devices. It is an empirical analytic model for the express purpose of fitting measured electrical large-signal behavior of HEMTs. Bias-dependent non-linear models of g_m and C_{gs} are incorporated in the model. Use of bias-dependent equivalent circuit values instead of directly measured S-parameter can reduce the computational requirements and improve accuracy because more data can be considered. In the EE_HEMT1 model, an accurate breakdown model describes gate leakage current as a function of both V_{gs} and V_{ds}. The EE_HEMT1 model can also include self-heating correction and dispersion modeling, which are useful for GaN HEMT high power applications. Another advantage of this model is its scalability of this model. Scaling of the intrinsic components is accomplished through the

definition of the unit gate finger width (Ugw) and the number of gate fingers (N) in the device parameters. The new EE_HEMT1 parameters are then calculated internally by the simulator according to the scaling rules. Other extrinsic components must be added externally. A detailed description and discussion can be found in Agilent's technical notes or through the help function in the ADS software.

The essence of this large-signal extraction method, based on characterization using dc and S-parameter measurements, is its optimization routine. An efficient and practical procedure is described here:

1) Measure dc and pulsed I-V curves. Estimate saturated current I_{dss}, threshold voltage V_{th} and knee voltage. Check for dispersion effects such as knee walk-out and current collapse to make sure use well passivated devices for modeling.

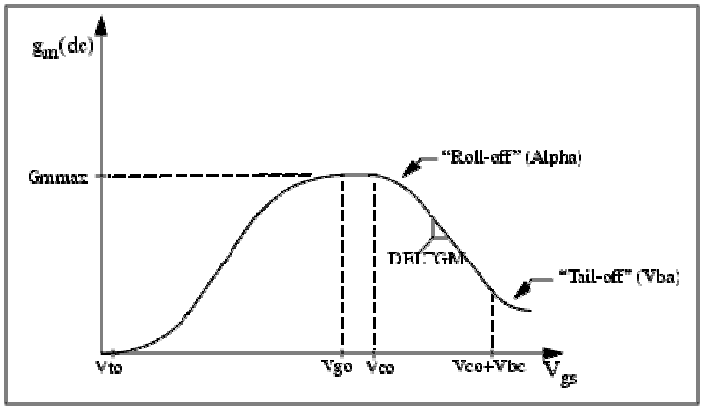


Figure 5.7 EE_HEMT1 g_m-V_{gs} model parameters (ADS technical notes)

2) From I-V curves, choose a feasible drain bias voltage, Vdso for the application. Measure g_m versus Vgs curves for this output voltage. Extract Vto, Vgo,

Gmmax, Vco, Vba, Vbc, Deltgm and Alpha from a plot of gm(dc)-Vgs, as indicated in Figure 5.7.

3) Measure S-parameters under a bias of Vdso and Vgo, where g_m reaches Gmmax. Extract small-signal model parameters at this bias. Use these initial parameters as seeds to further optimize dc parameters for I-V curve fitting.

4) Measure S-parameters with a sweep of Vgs at Vdso. Extract small-signal parameters from experimental data. A plot of input capacitance C11 versus Vgs can be obtained as shown in Figure 5.8. Accurate Vinfl and Deltgs are key factors in modeling the non-linearity of C11 with Vgs.

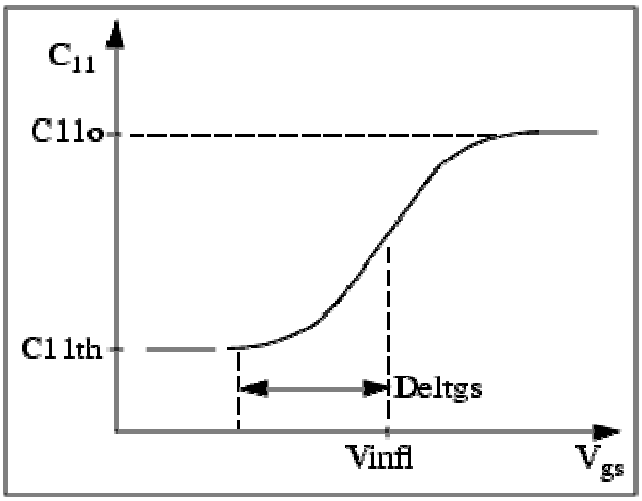


Figure 5.8 EE_HEMT1 C_{11}-V_{gs} model parameters (ADS technical notes)

4) Final optimizations are required to fit both dc and RF modeled data to measurement data simultaneously. Better accuracy can be obtained by fitting measured S-parameters over a wider bias range.

5) Self-heating, dispersion effects and leakage effects can also be modeled with additional corresponding characterization. In this study, self-heating and dispersion

effects were not included for simplicity of simulation. The gate leakage was modeled using a two-terminal breakdown voltage.

A GaN HEMT model with unit gate finger width of 125 μm and 4 gate fingers is extracted using this methodology. This model can be scaled up to 10 fingers without significant differences between measurement data and both dc and RF performance.

5.3. Field-plated device analysis

AlGaN/GaN HEMTs have attracted considerable interest as power devices in microwave applications. However, device performance is known to be often limited by the "dc-to-RF dispersion" phenomenon. Surface traps prevent proper device operation, reducing the available current swing as well as degrading the knee voltage [6]. Recently, the power capacity of AlGaN/GaN HEMTs was dramatically improved by though the application of field-plates, which not only increase the device breakdown voltage, but also reduce the high-field trapping effect. This method was successfully applied by Asano *et al.* on AlGaAs/GaAs HFETs to improve power densities as high as 1.7 W/mm at 1.5 GHz [7]. This structure was first used by Zhang *et al.* with GaN HEMTs for high-voltage switching applications [8]. Following this, Ando *et al*. used a similar structure with smaller gate dimensions and demonstrated excellent performance of 10.3 W/mm output power at 2 GHz on SiC substrate [9]. Chini *et al.* obtained a 12 W/mm at 4 GHz from a 150-μm-wide device on sapphire substrate with a different design [10]. Using field-plate optimization, AlGaN/GaN HEMTs with a CW power density of 32.2 W/mm at 4 GHz were reported by Wu *et al.* [11]. AlGaN/GaN HEMTs have not only been

identified as a promising technology for high power applications, but they have also shown excellent noise properties in LNA circuits. However, noise characterization of field-plated GaN HEMTs has not been well studied yet; it is important to characterize and analyze the noise performance on field-plated GaN HEMTs. Another possible benefit of these structures is that the high survivability of field-plated GaN HEMT allows the reduction or elimination of front-end protection, and the fabrication of both low noise and high power circuits on the same wafer.

Two different gate-terminated field-plate structures have been reported previously. One is a conventional field-plate structure as in [11], with the field-plate sitting on the SiN passivation layer and connected to the gate through the common path of the gate and gate feeder in the extrinsic device region (Figure 5.9). The other is an intimately connected field-plate structure as shown in Figure 5.10 [9]. The intimately connected field-plate is made as follows. An opening for the gate metallization was etched through the SiN passivation layer. The gate and field-plate metal were deposited by a single metallization step and are electrically connected everywhere along the gate fingers. In order to compare them side by side, these two different field-plate GaN HEMT structures have been designed and fabricated on a same substrate. Both devices have gate fingers of L_g = 0.7 μm and W_g= 150 μm. Devices with various field-plate lengths from 0.5 μm to 1.1 μm were fabricated for the study. The AlGaN/GaN HEMT devices were grown by MOCVD on SiC substrates. The epitaxial structure consisted of a semi-insulating Fe-doped GaN base layer, followed by a 290 Å thick $Al_{0.27}Ga_{0.73}N$ barrier layer. The room temperature sheet electron concentration and Hall mobility were ~9.96×10^{12} cm^{-2} and ~1450

cm^2/Vs, respectively. They were fabricated using UCSB standard process described in Appendix A. Conventional and intimately connected field-plate structures with the same field-plate extensions (0.7 μm) to the drain will be compared and discussed in this section.

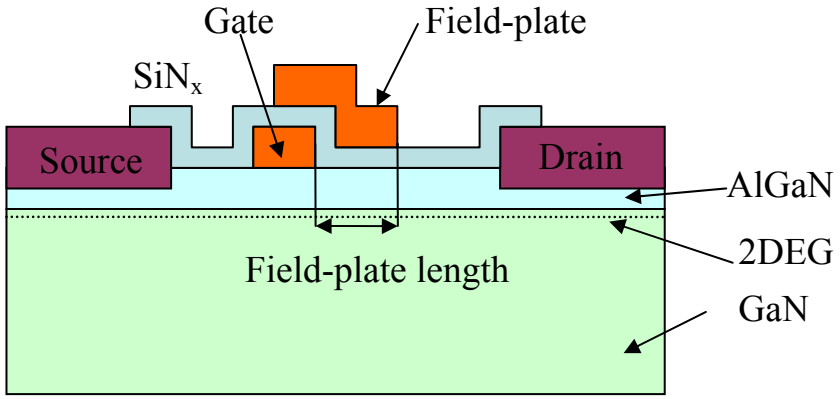


Figure 5.9 Field-plated GaN HEMT device

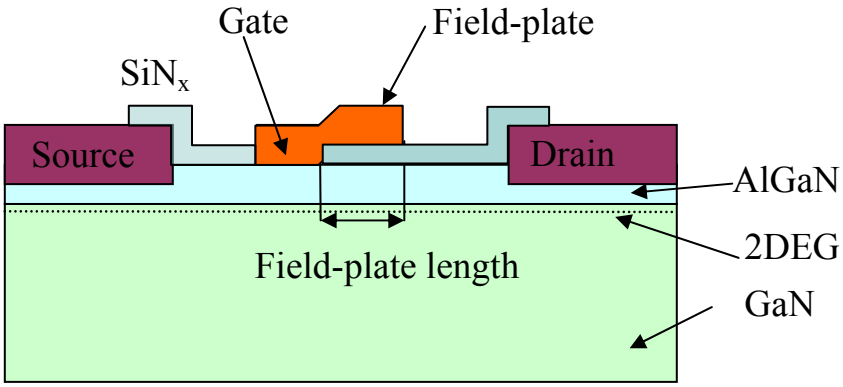


Figure 5.10 Intimately connected field-plated GaN HEMT device

Pulsed I-V and small-signal measurements were carried out on these two devices. In Figure 5.11, the output I-V characteristics, obtained using pulsed measurement (200 ns wide pulses) are shown. Passivated devices were capable of

reaching a current density of I_{dss} = 1.25 A/mm at V_{gs} = 1 V. The different field-plated devices had very similar I_{dss}, but the intimately connected field-plated device has slightly higher pinch-off voltage. This indicates that the 2DEG underneath the barrier layer is untouched after SiN etch, but the AlGaN/gate interface might be slightly etched from BCl3 cleaning step during RIE. Also no knee walk-out or current collapse is observed in pulsed I-V curves, thus the dispersion effects were well reduced by the SiN_x passivation layer.

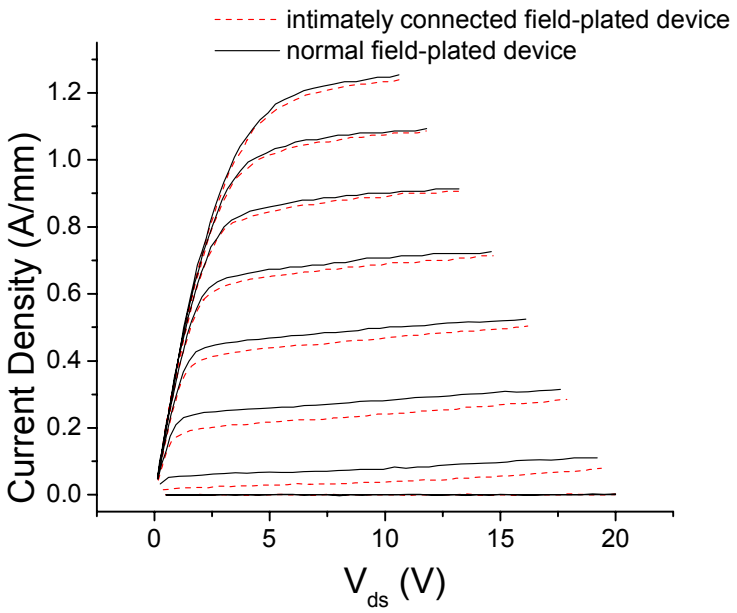


Figure 5.11 200ns pulsed I-V curves of field-plated GaN HEMTs

S-parameters were measured at a bias of V_{ds} = 20 V and I_{ds} = 200 mA/mm. As shown in Figure 5.12, both devices have similar f_t of 18 GHz, but f_{max} of intimately connected field-plated device has dropped to 40 GHz, comparing to a conventional field-plated device having 51 GHz. For the conventional field-plate structure, the

signal coupling between the gate and drain occurs indirectly though the field-plate. But for the intimately connected field-plate structure, the field-plate and the gate use the same conductor, so any coupling between the field-plate and the drain are directly transmitted to the gate. Thus, the equivalent gate-to-drain capacitance (C_{gd}) in the intimately connected field-plate structure is higher than the conventional field-plate structure. This increment in C_{gd} causes the reduction of f_{max}.

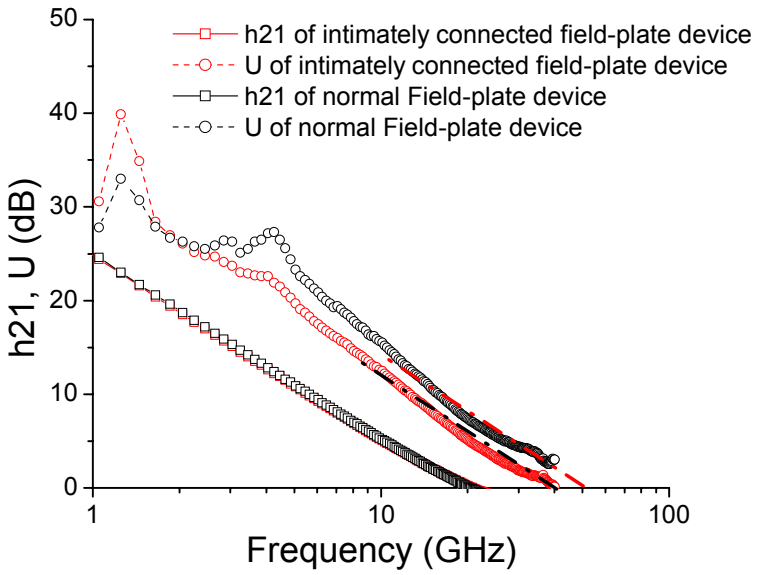


Figure 5.12 Small-signal characterization of field-plated GaN HEMTs

Single-tone power measurements were done at 4 GHz. Biased at Vds =40 V and Ids = 33 mA/mm, the saturated output power of a conventional device with a 0.7 µm field-plate length was 10.1 W/mm while the peak PAE was 70.9 % (Figure 5.13). With the same bias and field-plate length, the saturated output power of an intimately connected field-plated device was 12.9 W/mm with a peak PAE of 60 % (Figure 5.14).

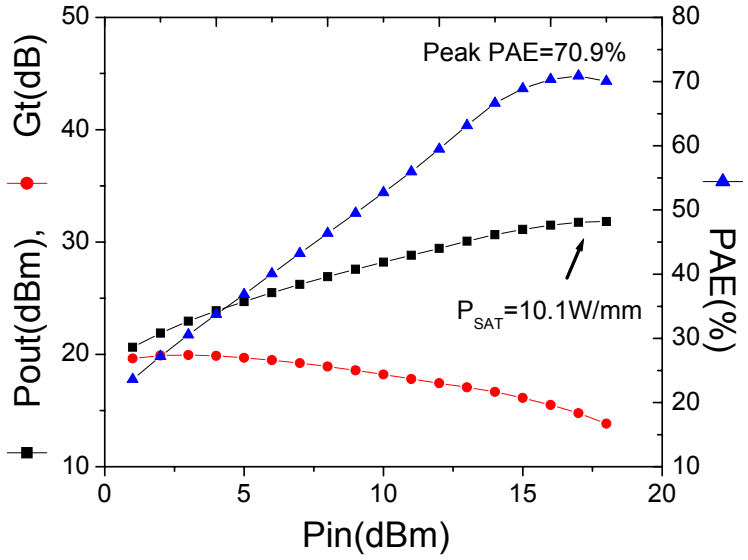


Figure 5.13 Single-tone power measurement of a conventional field-plate device with 0.7 μm field-plate length at 4 GHz.

These results show that the intimately connection device has a better saturated power density, but with a lower peak PAE. As explained above, the larger C_{gd} decreases the power gain and, therefore, lowers the PAE. But in order to understand the improvement of power density, an analysis on the resistance and the current distribution on the gate fingers are performed.

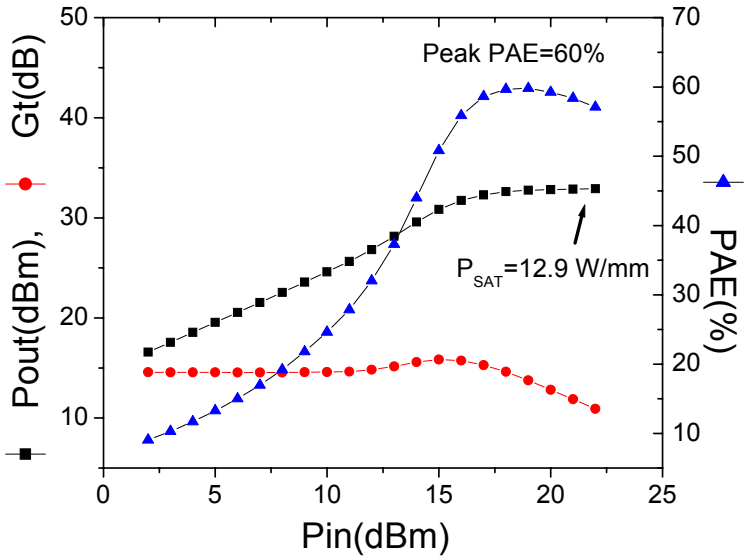


Figure 5.14 Single-tone power measurement of intimately connected field-plate device with 0.7 µm field-plate length at 4 GHz.

Figure 5.15 shows the gate structure used in the analysis of the distributed gate resistance. The input gate current flows through the metal and diverts into the semiconductor through the gate capacitances. At low frequency, the real part of input impedance R_g is:

$$R_g = \frac{1}{3} R_{sh} \frac{W}{L}$$

where R_{sh} is the gate sheet resistance in Ω/square. It is equal to the gate metal's resistivity divided by the metal thickness. The factor 1/3 accounts for the distributed nature of the current conduction.

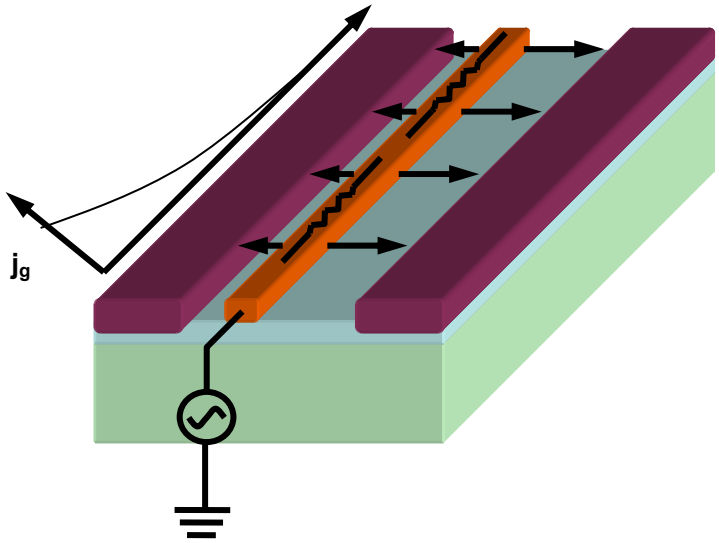


Figure 5.15 Schematic diagram depicting the gate structure

Generally, we intuitively tend to think that a device's performance degrades over frequency because of higher input resistance. However, the input resistance decreases with frequency with increasing frequency after a certain limit. This is because as the frequency gets higher, less and less signal travels through the entire width of the gate before diverting to the channel. As shown in Figure 5.15, the current density decreases along the gate finger and goes to zero at the end. When only a certain portion of the width is accessible to the input signal, the effective width decreases, hence the input resistance decreases. A good device requires both lower input resistance and uniform gate current distribution.

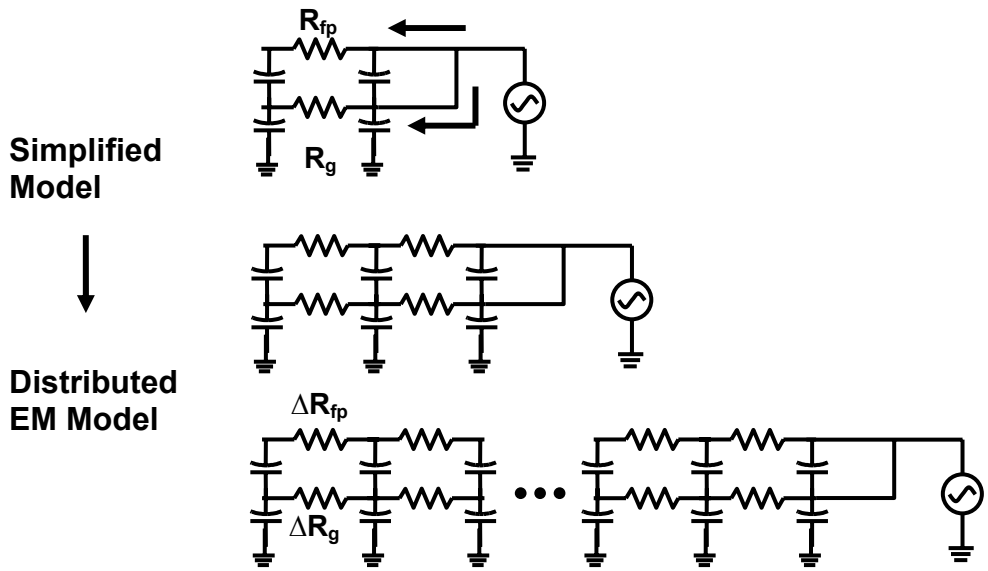


Figure 5.16 Equivalent models for the field-plated gate structure

The field-plate and the gate are connected at the input. The capacitors between them represent the signal coupling along the gate finger. At high frequency, the distributed model or EM simulation is the best way to characterize the input resistance as shown in Figure 5.16. EM simulations on both field-plate structures were performed at 4 GHz using Sonnet 2D EM simulator. The ac current density distributions on gate and field-plate are plotted in Figure 5.17. Obviously, the ac current is distributed more uniformly on both gate finger and field-plate for the intimately connected field-plated device, while most current is congested at the input in normal field-plated device. Also the difference of ac current distributions on the field-plates indicates that the field-plate in normal field-plated device does not carry much ac current. Therefore, it doesn't provide a significant contribution to the input resistance reduction. For a 75 μm gate finger, the simulated input resistances are 1.6 Ω and 1.33 Ω for normal and intimately connected field-plate structures respectively

at 4 GHz. Channel resistance, source/drain contact resistances and pad/feeder resistance are not included in the simulation. From the analysis, the improvements on input resistance and current distribution enhance the power performance of intimately connected field-plated devices.

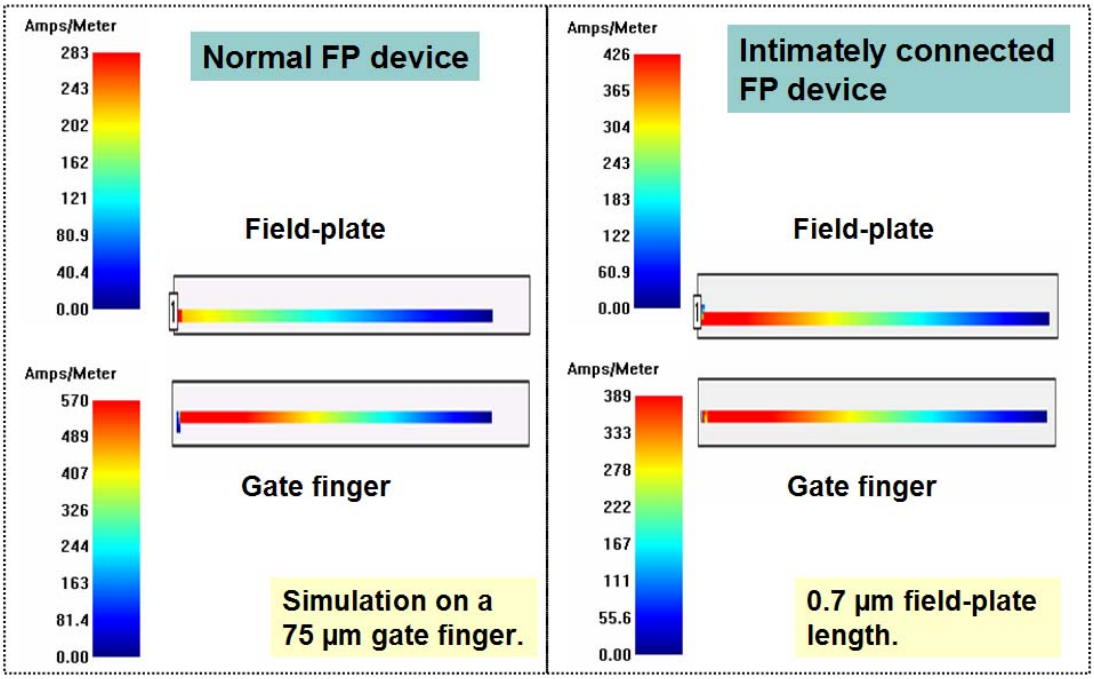


Figure 5.17 Current distribution on gate and field-plate

High frequency noise measurements were also done between 4 to 12 GHz. The optimum biasing point was found for each device by sweeping drain voltages and drain currents. In Figure 5.18, noise of an intimately connected field-plated device with a field-plate length of 0.7 µm is plotted. Compared to a conventional field-plate device with the same device structure, the noise figure of the intimately connected field-plated device is better because of lower gate resistance. The associated gain is also lower because of larger gate to drain capacitance. The power and noise results

show devices with an intimately connected field-plate structure exhibit higher power density and better noise figure, while the peak PAE and associated gain were lower than conventional field-plate devices.

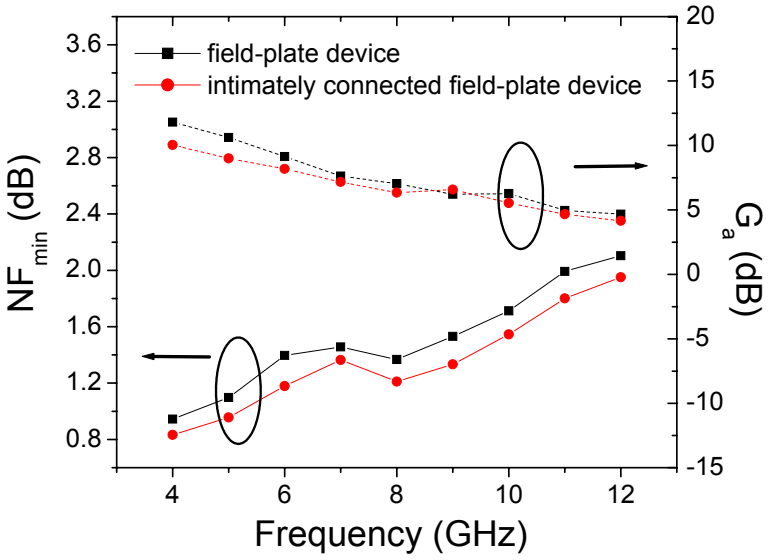


Figure 5.18 Noise performance comparison between two field-plated devices

In a conventional field-plate structure, the difference in the phase of an RF signal between the gate and field-plate could weaken the benefits of a field-plate. This is especially true when the gate finger width is comparable to the signal wavelength. Even though intimately connected field-plated GaN HEMT structures exhibitsboth better power and noise performance, the corresponding power gain and PAE are degraded because of stronger coupling between the gate and the drain. Also this structure involves more complicated and riskier RIE etching of SiN. Here we present an improved structure that shorts the field-plate to the gate at the ends of the gate fingers (Figure 5.19). SiN_x, which covered the gate at the ends of the fingers, was

etched away while patterning the passivation layer for bond metal. The field-plate metal and the exposed gate metal are then electrically connected at the ends by standard metal evaporation. The active area was still protected completely by the SiN_x passivation layer to reduce the high frequency dispersion.

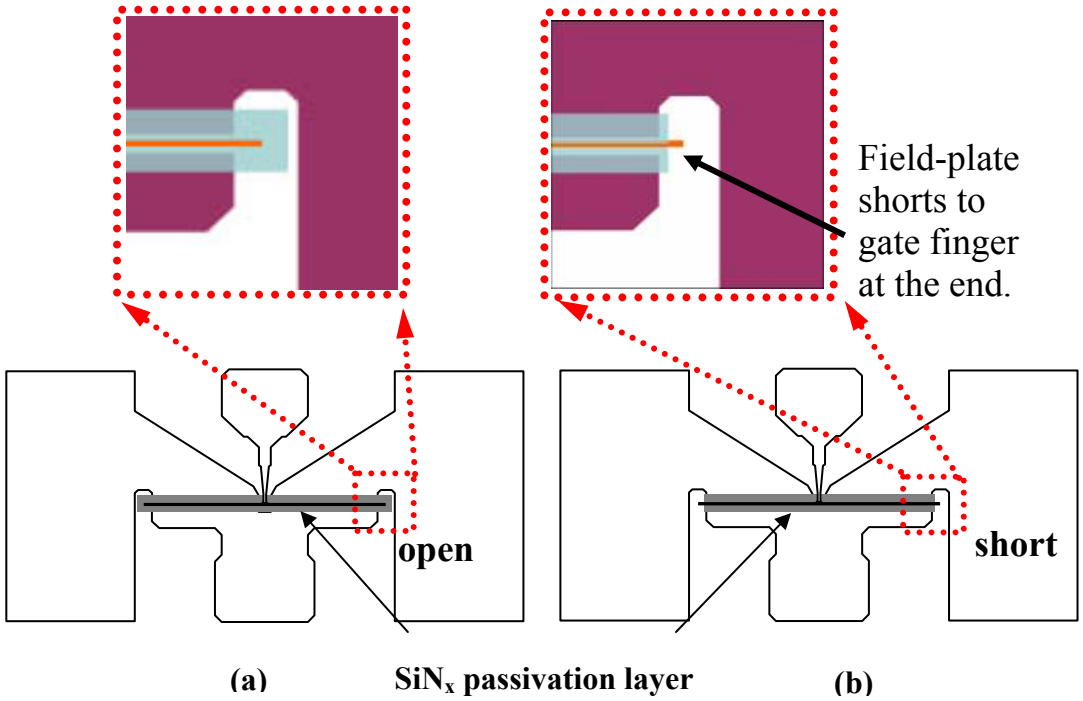


Figure 5.19 (a) Conventional field-plate structure; (b) new field-plated structure with field-plates shorted to their gates at the ends of gate fingers.

Following the gate current analysis above, it is known that in normal field-plated devices, field-plates do not improve the current distribution and nor reduce the input resistance significantly. The ac current density peaks at the feed-in point and dies off to zero at the end. But if the gate and field-plate are connected at both ends on a gate finger, since field-plate is generally wider than the gate length, more ac current can flow through the field-plate metal. Partial ac current from the field-plate flows back

into the gate at the other end and the gate current goes to zero at a point between two ends on the gate, as indicated in Figure 5.20.

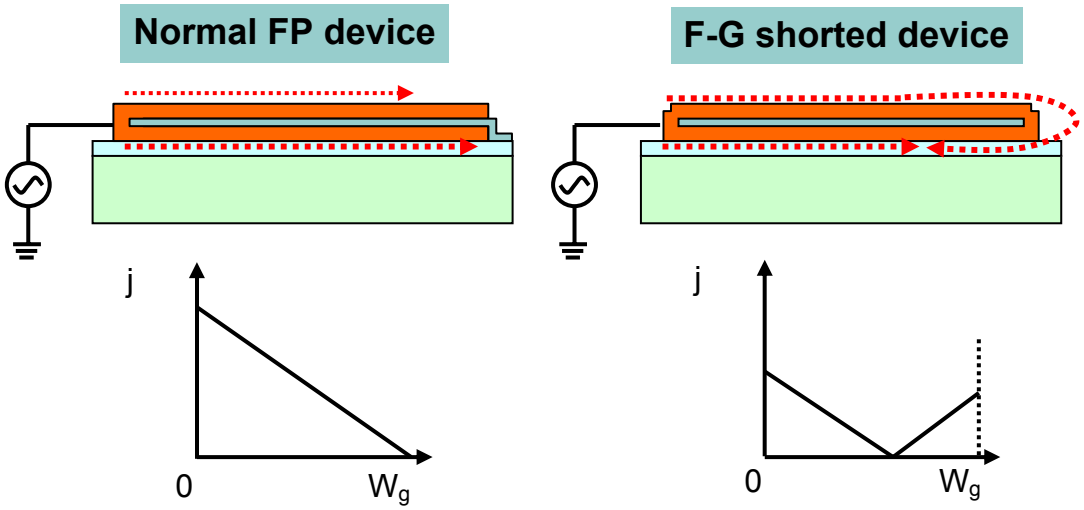


Figure 5.20 Current density distributions in (a) Conventional field-plate structure; (b) new field-plated structure

These behaviors are verified by EM simulation. Simulations on this new field-plate structure were also performed at 4 GHz using Sonnet 2D EM simulator. The ac current density distributions on the gate and field-plate of both normal field-plate and new field-plate structures are plotted in Figure 5.21. For the device with gates and field-plate shorted on both ends, the input ac currents are almost equally distributed. The ac current on field-plate continues to flow back to the gate finger and is zero at a point 5/6th of gate finger width away from the feed-in side for a 75 μm gate finger. The simulated input resistance is 1.3 Ω for these new devices, meaning a 19% improvement in the gate resistance.

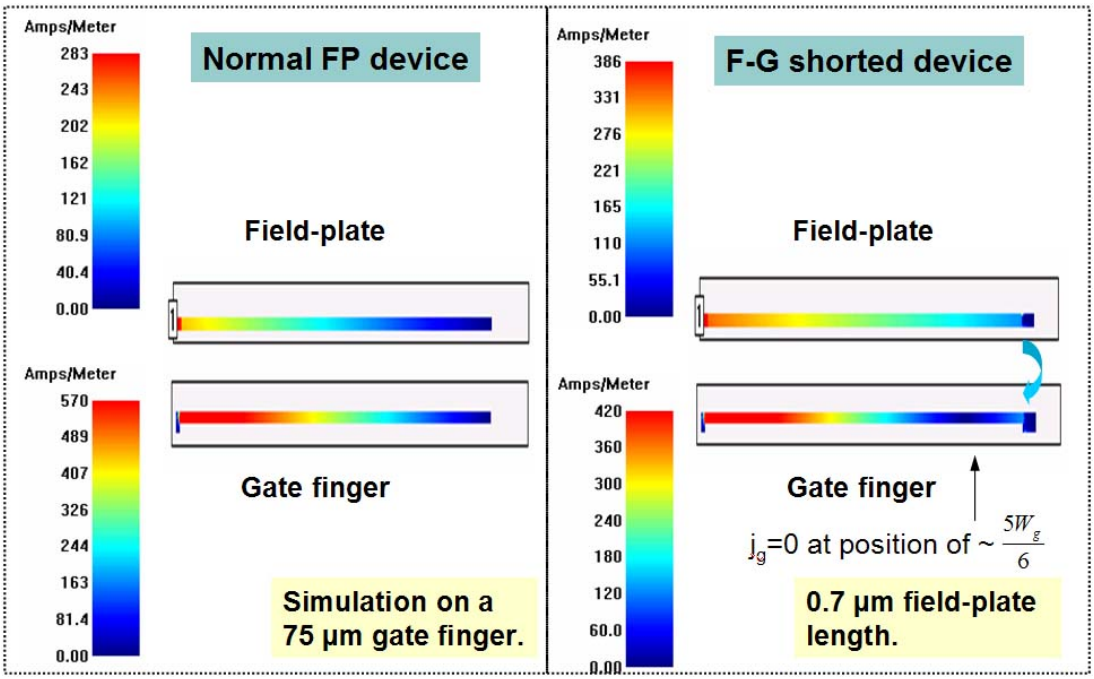


Figure 5.21 Current distribution on gate and field-plate

In order to understand the impact of this new structure, conventional field-plated devices and new field-plated devices were designed and fabricated on the same sample with an identical gate length and width of L_g = 0.7 µm and W_g = 2x75 µm. Conventional and new structures with the same field-plate extensions (0.7 µm) to the drain will be compared and discussed in this section. The fabricated devices were subjected to pulsed I-V and small-signal measurements. In Figure 5.22, the output I-V characteristics obtained with a pulsed width of 200 ns are shown. Passivated devices were capable of reaching a current density of I_{ds} = 1.25 A/mm at V_{gs} = 1 V. The different field-plated devices had very similar pulsed I-V curves, thus the dispersion effects were well reduced by the SiN_x passivation layer. S-parameters

were measured at a bias of V_{ds} = 20 V and I_{ds} = 200 mA/mm. As shown in Figure 5.23, the two kinds of devices had a similar f_t of 18 GHz and f_{max} of 51 GHz.

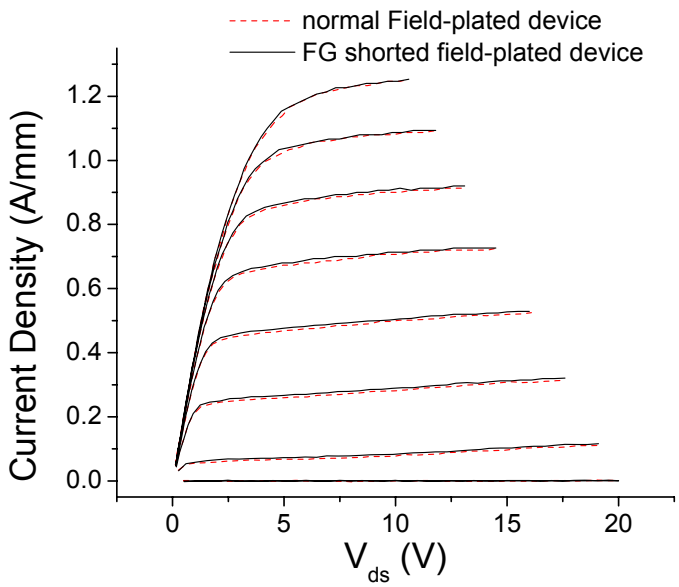


Figure 5.22 200 ns pulsed I-V curves of field-plated GaN HEMTs

Single-tone power measurements were done at 4 GHz. During the measurement, conventional field-plated devices failed to sustain high RF power with drain bias over 50 V, while devices with new structure worked up to 90 V. The uniformity of current on the gate could account for the improvement of the ac breakdown voltage. With additional reduction of the gate resistance, both saturated power and PAE were improved slightly.

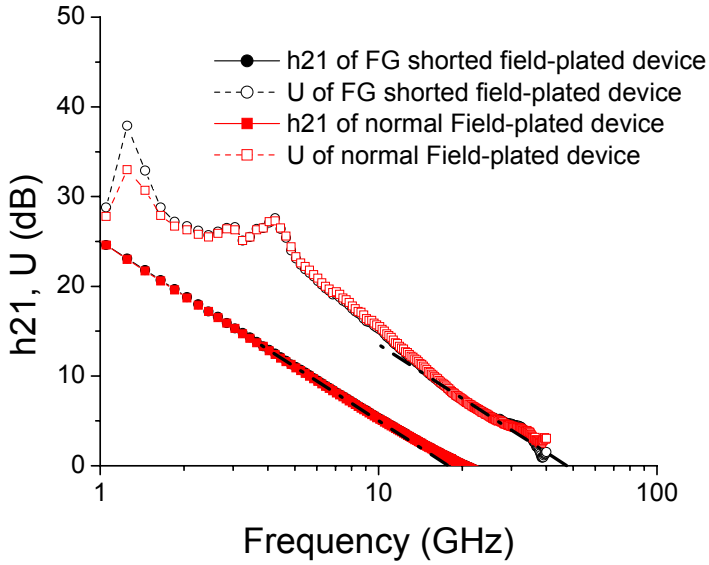


Figure 5.23 Small-signal characterization of field-plated GaN HEMTs

Biased at V_{ds} = 30 V and I_{ds} = 38 mA/mm, the saturated output power was 7.2 W/mm while peak PAE was 75.6 % (Figure 5.24). The output power density at peak PAE was 6.6 W/mm. With a higher drain bias of V_{ds} = 80 V and I_{ds} = 38 mA/mm, the saturated output power was 23.3 W/mm, while the peak PAE was 53.8 % (Figure 5.25). Both output power density and PAE were improved from previous reported results with similar drain voltages. Figure 5.26 shows measured saturated output powers and PAEs at different drain biases. The saturated output power kept increasing from 7.2 W/mm at 30 V drain voltage to 23.3 W/mm at 80 V drain voltage. But at 90 V drain voltage, the saturated output power dropped back slightly to 22.7 W/mm. PAE decreased almost linearly from 75 % to 46 % as the drain voltage increased from 30 V to 90 V.

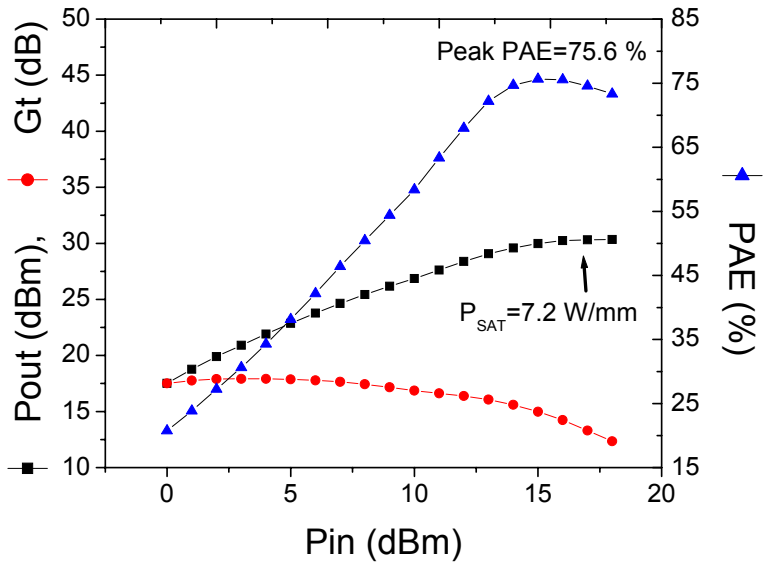


Figure 5.24 Single-tone power measurement of the new field-plated device with 0.7 µm field-plate length at 4 GHz. (V_{ds} = 30 V)

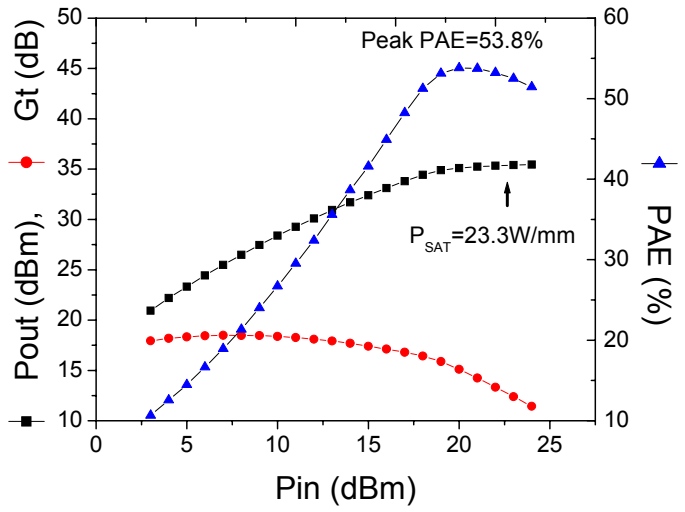


Figure 5.25 Single-tone power measurement of the new field-plated device with 0.7 µm field-plate length at 4 GHz. (V_{ds} = 80 V)

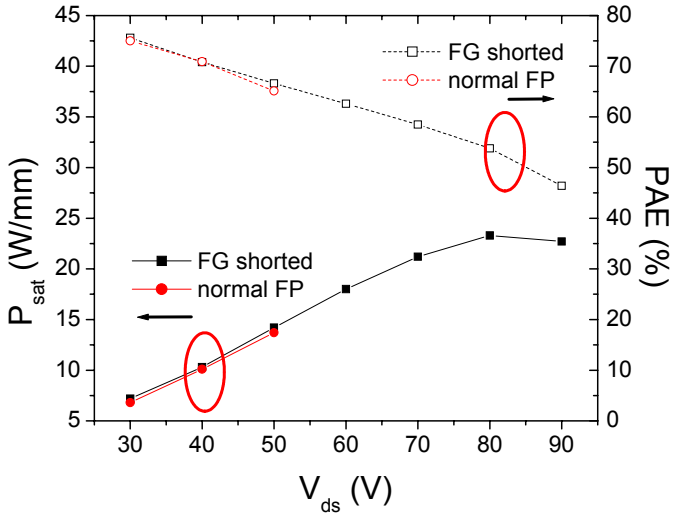


Figure 5.26 4 GHz saturated output power and PAE measurements of normal and new field-plated devices.

To further understand the impact of field-plates on the noise performance, a non-field-plate device with the same structure and on the same sample was tested with these two field-plated devices. High frequency noise measurements were done from 4 to 12 GHz. The optimum biasing point was found for each device by sweeping drain voltages and drain currents. In Figure 5.27, both field-plated devices were found to have lower minimum noise figures, possibly because of lower gate resistances for field-plated devices. The associated gains of field-plated devices are lower because of larger gate to drain capacitances. Devices with field-plates shorted to their gates exhibit slightly better noise figure and gain than conventional field-plated devices, since the gate resistance is further reduced.

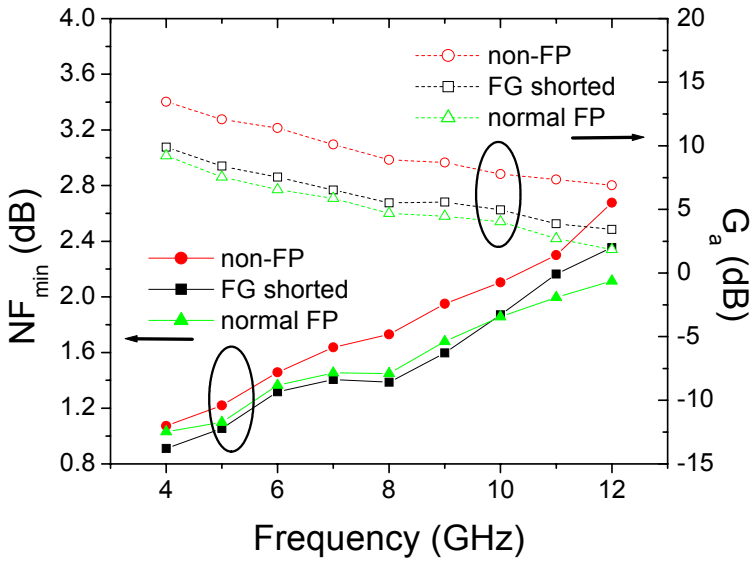


Figure 5.27 Noise performance of non-field-plated devices, normal field-plated devices and devices with field-plates shorted to their gates at ends.

A set of conventional field-plated devices with different field-plate lengths was measured and compared as shown in Figure 5.28. As the field-plate length increases, the associated gain drops. The minimum noise figure peaks with a 0.7 μm field-plate length. Devices with shorter or longer field-plate length exhibit better noise figure. The noise performance of field-plated devices is not well understood yet. Further studies are underway at UCSB.

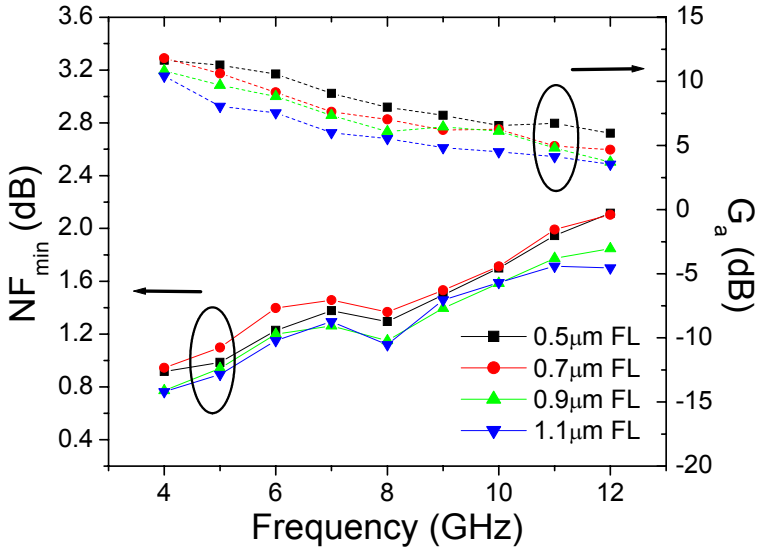


Figure 5.28 Noise performance of field-plate devices with different field-plate lengths.

To further compare the three different field-plate structures (normal field-plate/gate one end connected structure, two end connected structure and intimately connected structure), small-signal parameters of these three devices were extracted from S-parameters measurements as in section 5.1. All three devices were biased at the same condition. The charging resistance R_i is included in the equivalent circuit primarily to improve the match to S_{11}. The sum of R_g and R_i represented the gate parasitic resistance and channel resistance between the gate and the source. The simulated parameters were optimized by curve fitting. Simulation errors of S-parameters for both types of devices are less than 1 %. The simulated small-signal parameters are listed in Table 5.1. From the table, we see the feedback capacitance C_{gd} is not affected by the shorted-ends field-plated structure, but it increases 50% for

intimately connected field-plate structure. The sum of R_g and R_i is calculated as total the input resistances, R_{in}, for these three devices in Table 5.2. It changes from 8.1 Ω to 7 Ω by the shorted-ends field-plate structure from the normal field-plate structure. In the standard field-plated device, the resistance of the gate fingers is in parallel with the resistance of the field-plate. When the field-plate metal is connected at the two ends of the gate fingers, the effective gate parasitic resistance is reduced. In the intimately connected field-plate device, the input resistance is 9.1 Ω, which is higher than the other two structures. This is because the field-plate and the gate are formed by one metal layer, while the field-plate and the gate are deposited by two metal layers in the other two field-plate structures. If the thickness of the field-plate/gate metal was doubled for the intimately connected field-plate structure, the input resistance could be ~4.6 Ω, which should be the lowest one among these three structures. Also the ac current flows in the gate from both sides of each finger in the shorted-ends field-plate device. It helps to improve the uniformity of the ac current on the gate. The intimately connected field-plate structure also exhibits better ac current uniformity than normal field-plate structure.

In this section, we have tested and analyzed three different field-plate structures. A new field-plated GaN HEMT structure with the field-plate shorted to the gate at the finger ends is demonstrated with the same process steps as the conventional structure. Using this new structure, the operation bias voltage of field-plated devices increased from 60 V to 100 V. At 4 GHz, field-plated GaN HEMT devices exhibited a saturated output power of 23.3 W/mm with a peak PAE of 53.8 % with a drain voltage of 90 V. Both PAE and saturated output power are slightly higher because of

the reduction of the gate resistance. Also, with this new field-plated structure, the minimum noise figure and associated gain are improved simultaneously. These results show that this new GaN HEMT structure improves both power and noise performance without additional processing and only a slight change to one photolithography mask.

Table 5.1 Simulated small-signal parameters of the field-plated HEMTs

	R_i (Ω)	R_{ds} (Ω)	R_{gd} (Ω)	C_{gd} (fF)	C_{ds} (fF)
Normal FP device	7.178	1297.6	22.882	45.497	14.842
FG shorted FP device	6.068	1327.3	22.357	47.431	15.220
Intimately connected FP device	8.276	960.0	15.374	70.885	16.340
	C_{gs} (fF)	g_m (S)	R_s (Ω)	R_g (Ω)	R_d (Ω)
Normal FP device	270.7	0.040	6.531	0.924	5.503
FG shorted FP device	265.0	0.040	6.519	0.907	5.443
Intimately connected FP device	246.0	0.040	4.830	0.782	5.423

Table 5.2 Simulated input resistances of field-plated HEMTs

	$R_{in} = R_i + R_g$(Ω)
Normal FP device	8.102
F-G shorted FP device	6.975
Intimately connected FP device	9.058*

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Chapter 6. GaN HEMT MMIC design and performance

6.1. GaN class-E power amplifiers

Power amplifiers (PA) are typically the most power-consuming building blocks of RF transceivers. Therefore, high-efficiency MMIC power amplifiers are desirable for reduced dc power consumption, simple thermal management, and longer operating lifetime. High-efficiency amplifier configurations have long been studied. The class-E amplifier has a maximum theoretical efficiency of 100%. The class-E amplifier topology is an attractive choice for simultaneous high efficiency and high output power [1]. In recent years several class-E MMIC power amplifiers using GaAs MESFET, InP DHBT, LDMOS and CMOS technologies have been reported [2][3][4][6]. In this section, two GaN HEMT based class-E MMIC PAs are presented. AlGaN/GaN HEMTs have a superior power-density compared with other technologies due to an inherently larger breakdown field, with cutoff frequencies that are comparable to GaAs-based FETs or HEMTs at similar gate lengths. Using GaN HEMT technology, class-E power amplifiers can achieve high-power and high-efficiency simultaneously. In the class-E power amplifier topology the device is used as a switch at the driving frequency, and hence must have a high impedance in the "off" state and a low impedance in the "on" state. The passive load network is designed to minimize the drain (or collector if a bipolar technology is being used) voltage and current waveforms from overlapping, which minimizes the output power dissipation. High efficiency is achieved by tailoring the drain voltage and current

waveforms to minimize losses at the switching instants. A typical class-E amplifier circuit is shown in Figure 6.1. It consists of a switch, a bias RF choke, a shunt capacitor C, a fundamental frequency resonator L_0-C_0, and a load R_L with an excessive reactance jX. The circuit design in this work is based on the theory described in [6] for an idealized class-E amplifier with a 50% duty cycle and zero voltage and zero derivative at the switching instant. The switch has zero "on" resistances and infinity "off" resistance. The RF chock, the resonator, and other components in the load network are assumed to be ideal, lossless and linear.

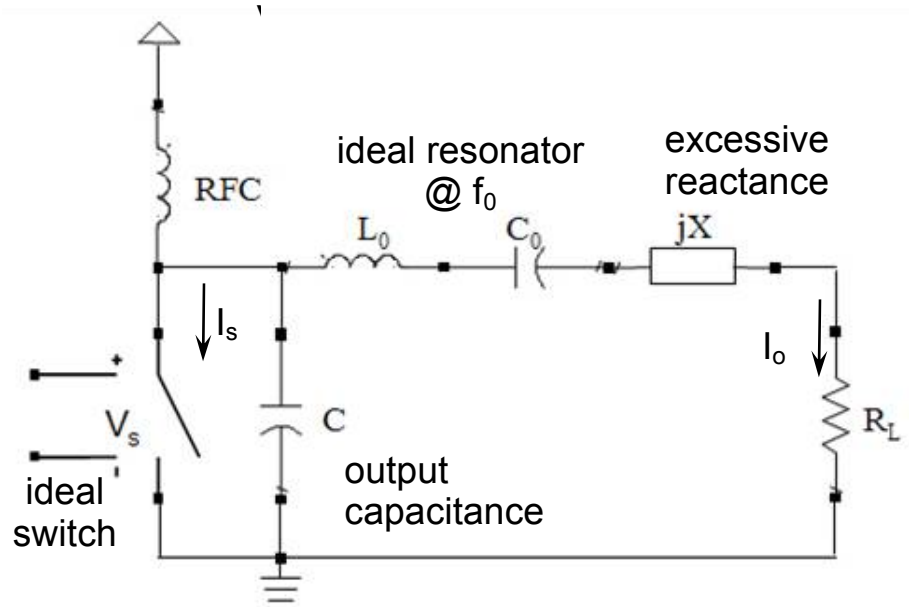


Figure 6.1 Equivalent circuit of a class-E amplifier

The analysis of the class-E amplifiers has been reported in several papers. In an ideal class-E power amplifier, the transistor operates as a switch, which is turned on and off periodically at the design frequency. The waveforms of Vs and Is are shown in Figure 6.2. By appropriately choosing values of the output network, the overlap

between drain voltage and drain current is minimized, leading to minimum power dissipation in the switch. Since only signals at the fundamental frequency can pass though the resonator, the output current I_0 is an ideal sine wave.

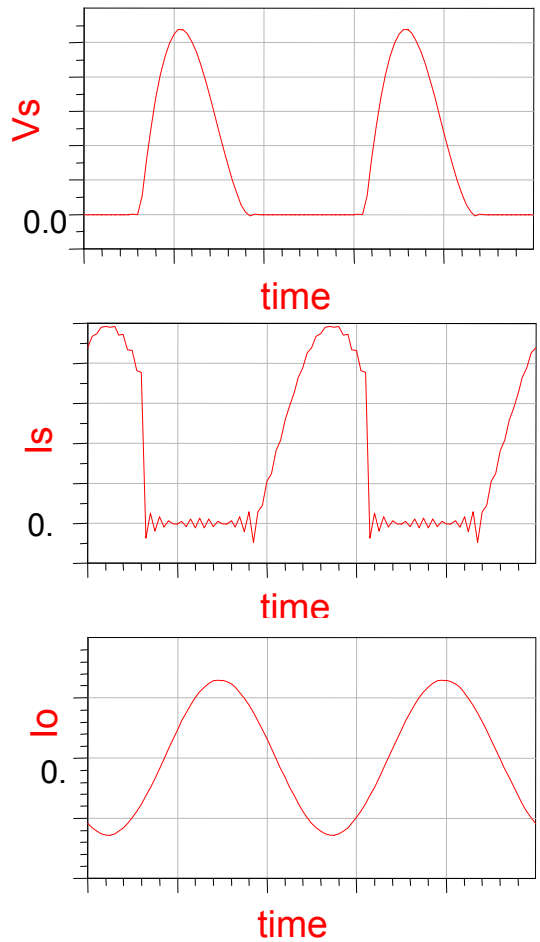


Figure 6.2 Ideal class-E voltage and current waveforms

Based on the circuit theory in [6], there is a set of equations that provide a good starting point for design. These equations are:

Output power: $$P_o = \frac{V_{dc}^{\ 2}}{R_{dc}}$$

Equivalent dc resistance: $R_{dc} = 1.7337 R_L$

Shunt susceptance: $B = \omega C = \dfrac{1}{5.4466 R_L}$

Load angle (inductive): $\psi = 49.052^o$

Load network impedance: $Z = R_L + jX$

Excessive reactance: $X = R_L \tan\psi = 1.152 R_L$

Peak switch voltage: $V_{s\max} = 3.56 V_{dc}$

Peak switch current: $I_{s\max} = 2.84 I_{dc}$

Maximum frequency: $f_{\max} = \dfrac{I_{dc}}{2\pi^2 C_{ds} V_{dc}} \approx \dfrac{I_{\max}}{56.5 C_{ds} V_{dc}}$

Following these expressions, component values can be estimated initially. For a certain device technology, the peak switching voltage V_{smax} and current I_{smax} are limited by the breakdown voltage and the maximum saturated current. Therefore, device periphery should be chosen based on these two factors and the expected output power P_o. Also for this switch mode amplifier topology, the maximum frequency is constrained by the output capacitance C_{ds}. For high power application, the large gate periphery and high drain bias voltage limit the maximum operating frequency.

Two L-band class-E amplifiers are implemented in this section using a modest a modest 0.7 μm AlGaN/GaN process, with a field-plated gate structure to increase the breakdown voltage. One of them is a single-stage PA and the other is a two-stage PA

with a class-F driver. Both amplifiers presented here were designed for 2 GHz applications.

A. Single-stage class-E GaN HEMT power amplifier

Because of the narrow range of component values that can be realized in our MMIC process, the usual series LC network at the output is replaced by an L-match network as shown in Figure 6.3 (L_1, C_1). The output L-network transforms a 50 Ω load to the desired optimum load and also provides some harmonic suppression [7]. The drain capacitance C_{ds} of the transistor, together with an external capacitance C_p, functions as the output capacitance for class-E operation. A second order harmonic trap (L_{g2}, C_{g2}) at the gate is employed to improve the input waveforms, so that the transistor can be switched on and off efficiently, as required in class-E mode operation. As the device is potentially unstable, a stability circuit (R_{s1}, C_{s1} and R_{s2}) is also added at the input. The circuit was simulated using Agilent's ADS. A bias-dependent and scalable large-signal EEHEMT1 model was used to simulate output power and efficiency. Passive lumped components and parasitics were simulated using the ADS Momentum EM simulator.

Figure 6.4 shows the simulated waveforms of drain voltage and current, as well as the voltage waveforms at the load. The load voltage waveform is close to sinusoidal indicating good suppression of harmonic components. However, the simulated drain voltage and current waveforms are clearly not the ideal class-E drain voltage/current waveforms. This is partly due to the inherent non-idealities of the device as a switch, but also a consequence of the non-optimal output network that was used because of passive component realization constraints. The low Q-factors of

the spiral inductors and loss from the stability circuit also contribute to a degradation in efficiency. These issues are common to MMIC amplifiers and explain why most MMIC class-E amplifiers suffer lower efficiency than hybrid implementations.

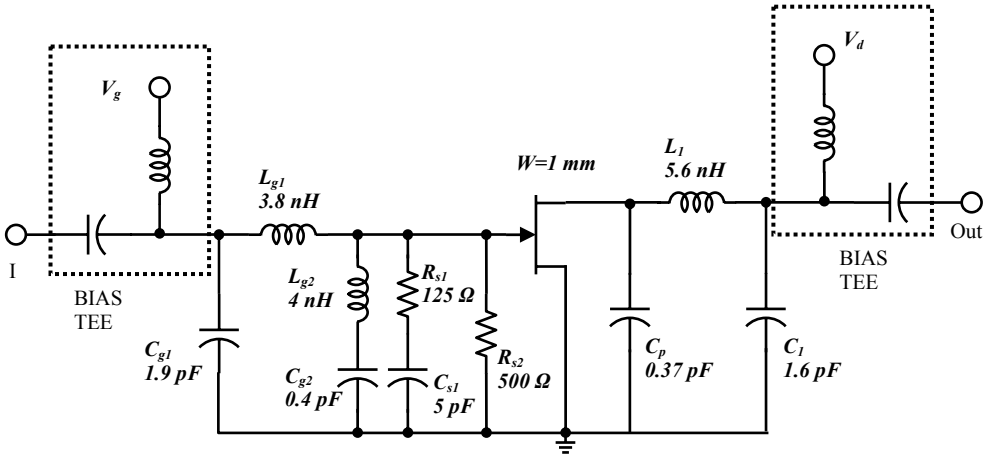


Figure 6.3 Circuit schematic of the class-E power amplifier

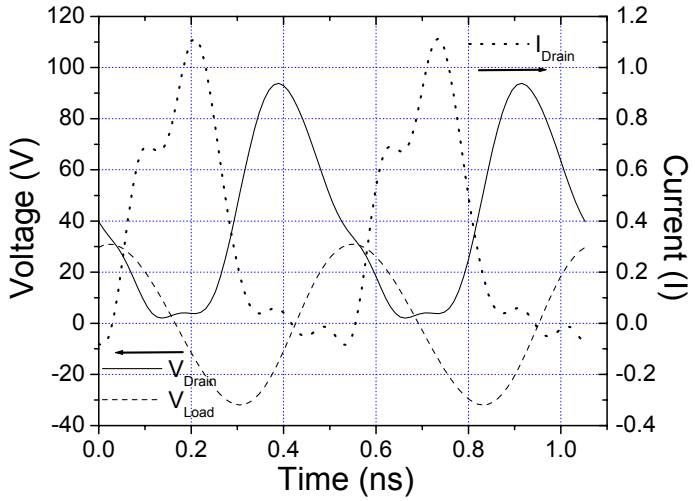


Figure 6.4 Simulated voltage and current wave form of the GaN

The class-E power amplifier was fabricated on a SiC substrate. The AlGaN/GaN epitaxial layers were grown by MOCVD. The detailed epitaxial structure consisted of a semi-insulating Fe-doped GaN base layer, followed by a 290 Å thick $Al_{0.27}Ga_{0.73}N$ barrier layer. The room temperature sheet electron concentration and Hall mobility were ~1.12×10^{13} cm^{-2} and ~1430 cm^2/Vs, respectively. The device featured a field-plated gate structure, with a 0.7 μm gate length, 8x125 μm gate width and 0.7 μm field-plate length. The field-plated GaN HEMT device has a breakdown voltage greater than 100 V and I_{dss}=1 A/mm. The measured unity current gain cutoff frequency (f_t) of the device is 18 GHz.

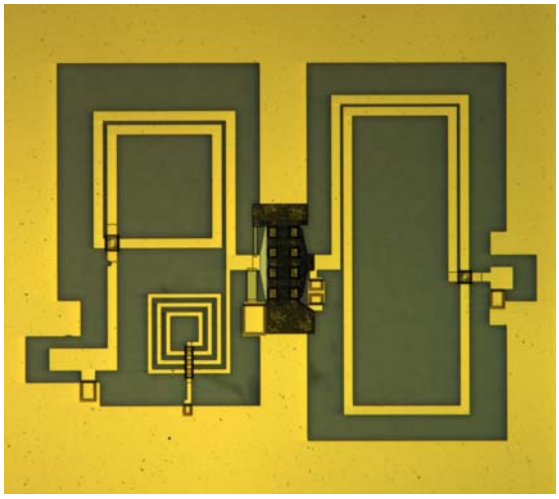
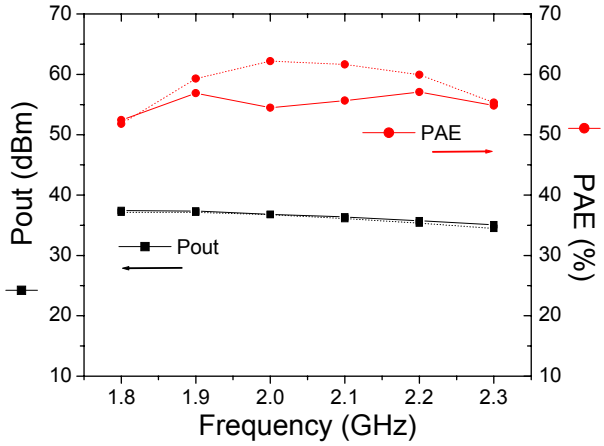


Figure 6.5 Chip photograph of the amplifier (2.4 mm x 2.2 mm)

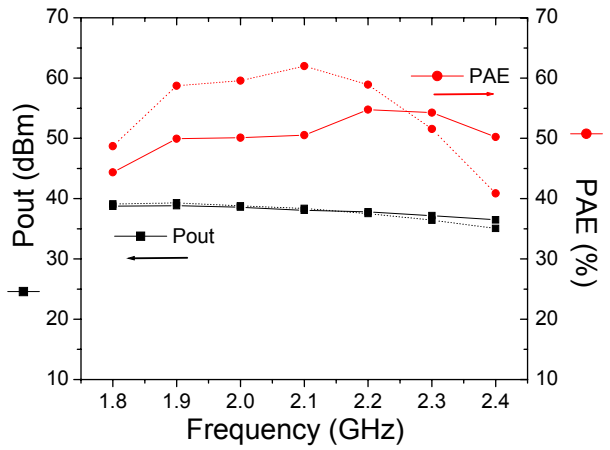
Figure 6.5 is a photo of the completed circuit, which occupies an area of 2.4 mm by 2.2 mm, clearly dominated by the spiral inductor areas. There are no vias in our process, so all ground connections are made on the top side with CPW I/O ports. The complete MMIC process begins with a standard HEMT process with SiN passivation, followed by device isolation and steps to create the passive lumped

components. Lumped component fabrication included NiCr thin film resistors, metal-insulator-metal (MIM) SiN capacitors and spiral inductors with PMGI cross-overs.

All input and output matching and tuning networks are on chip. Bias feeds for gate and drain are provided through off-wafer bias tees for convenience in testing. The sample was vacuum-held on a 2-inch copper wafer chuck during testing. There was no additional thermal management. Figure 6.6(a) shows the measured results of output power and PAE performances. The drain voltage bias is at 30 V in this case. A maximum power level of 37.2 dBm is achieved at 1.9 GHz, corresponding to 5.25 W/mm in output power density. In the 500 MHz bandwidth from 1.8 GHz to 2.3 GHz, the PAE is above 52% for an input power of 27 dBm. The highest PAEs are measured as 57% at 1.9 GHz and 2.2 GHz respectively.



(a)



(b)

Figure 6.6 Measured (solid lines) and simulated (dotted lines) maximum output power and peak PAE of the power amplifier versus frequency at a drain bias of (a) 30 V and (b) 40 V

The measured results of output power and PAE performances versus frequency at a drain voltage bias of 40 V are shown in Figure 6.6(b). In this case the power amplifier delivers a maximum output power level of 38.7 dBm at 1.9 GHz, and the power density increases to 7.4 W/mm. A peak PAE of 55% is measured at 2.2 GHz, and the PAE is above 50% within the frequency range from 1.9 GHz to 2.4 GHz for an input power of 28 dBm.

Simulated results are also presented as dotted lines in Figure 6.6 for comparison. A relatively good agreement between simulated and measured output power results is observed. The discrepancy between simulated and measured PAE results may be due to an inaccuracy of the nonlinear device model, EM simulation, process variation and device self-heating.

The measured results of output power, gain, and PAE performances of the amplifier at different input power levels at 1.9 GHz and a 30 V drain bias are shown in Figure 6.7. The power-added efficiency of the transistor reaches 57% with a 10 dB gain. The corresponding drain efficiency is 63%.

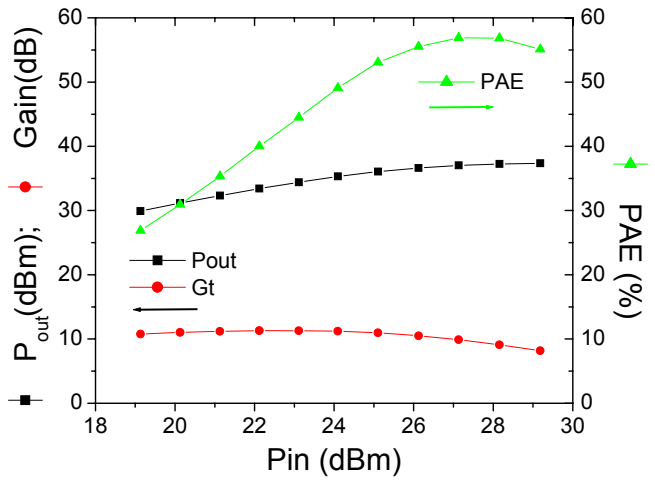


Figure 6.7 Measured output power, gain and PAE of the power amplifier versus input power level at 1.9 GHz with a 30 V drain bias

B. Two-stage class-E GaN HEMT power amplifier

To operate the transistor as a switch, it has been commonly recognized that a rectangular voltage waveform is ideal for the input waveform of the class-E amplifier, so that the transistor can be switched on and off at the design frequency [1][6]. In the two-stage power amplifier, a class-F amplifier is used as a driver stage, so that a rectangular voltage waveform can be formed at the output of the class-F amplifier, *i.e.*, the input of the class-E power stage [2]. Figure 6.8 shows the circuit schematic of the two-stage power amplifier. The design of the output network in the power stage is similar as the single-stage class-E amplifier. An "L" network (C_{11}, L_7)

is used as the output network of class-E amplifier, so that a 50 Ω load can be transformed to the optimum RF load. At the output of the power stage, the drain capacitance C_{ds} and an external lumped capacitor together form the output capacitance C_{10} for class-E operation. At the class-F driver stage, two resonant circuits, including one at the design frequency (C_5,L_5) and the other one (C_4,L_4) at the third harmonic frequency, are used to terminate the harmonics. As the devices used are potentially unstable, two stabilization circuits are used: one at the class-F driver stage (R_1, C_3, R_2 and L_3), and the other one at the class-E power stage. To do simulations, a bias-dependent and scalable large-signal EEHEMT1 model of the device is incorporated into the Harmonic Balance Simulator of ADS. Table 1 lists the values of all the components in Figure 6.8.

Figure 6.9(a) shows the simulated results of drain voltage and current at the output of the class-F driver stage, and Figure 6.9(b) shows the simulated results of drain voltage and current at the output of the class-E power stage. It is seen that neither the ideal class-F voltage waveforms at the driver stage nor the ideal class-E voltage waveforms at the power stage are realized. The reasons include the limited values of components realizable from the MMIC process, finite Q values of the components from the MMIC process, and similar reasons as listed previously. Another important reason is that the transistor is not an ideal switch. These discrepancies lead to degraded efficiency performances as shown below.

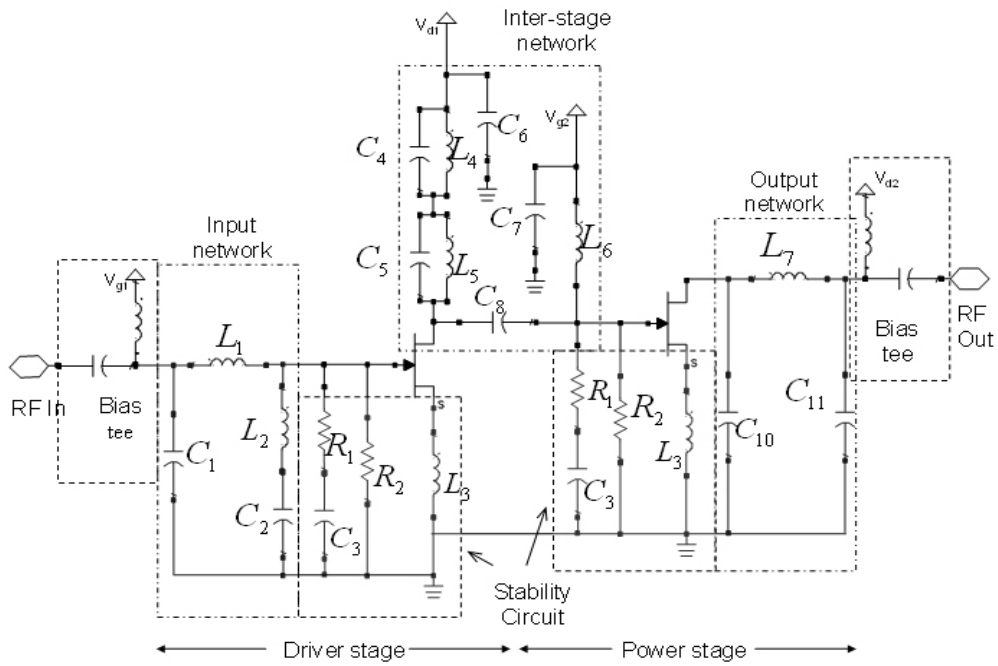


Figure 6.8 Schematic of the two-stage class-E amplifier

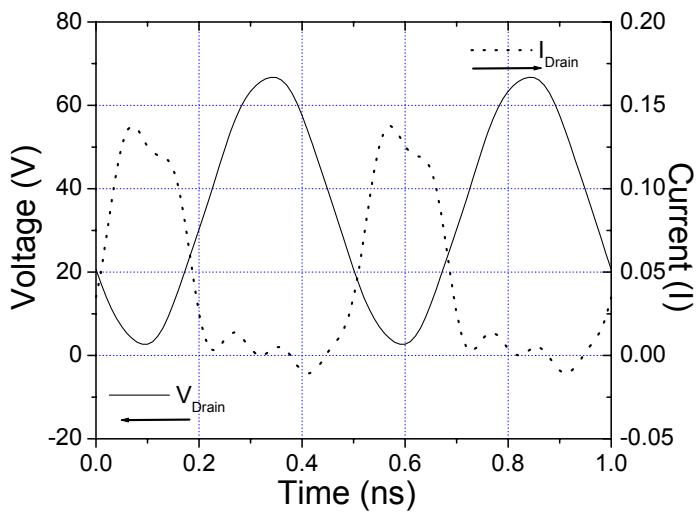
Table 6.1 Component values of the 2-stage PA (Figure 6.8)

C_1 (pF)	C_2 (pF)	C_3 (pF)	C_4 (pF)	C_5 (pF)	C_6 (pF)	C_7 (pF)
0.42	0.4	5.0	0.7	1.2	20	10
C_8 (pF)	C_9 (pF)	C_{10} (pF)	L_1 (nH)	L_2 (nH)	L_3 (nH)	L_4 (nH)
0.8	0.4	1.6	2.6	4	0.1	1
L_5 (nH)	L_6 (nH)	L_7 (nH)	R_1 (Ω)	R_2 (Ω)		
3	7.9	5.6	125	500		

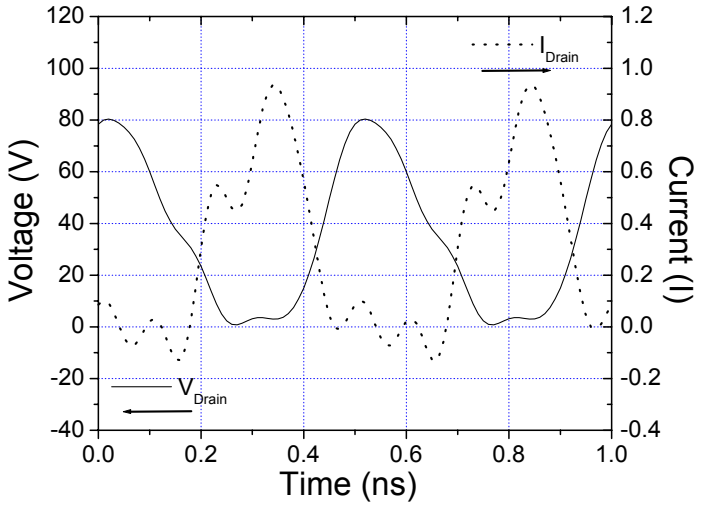
The two-stage MMIC class-E amplifier is fabricated on a SiC substrate in GaN HEMT technology. Two field-plated AlGaN/GaN HEMT devices, one having 0.7

μm gate length and 2x125 μm gate width, and the other one having 0.7 μm gate length and 8x125 μm gate width, are used for the driver stage and the power stage, respectively.

Figure 6.10 shows a photograph of the amplifier, which has a size of 3.4 mm x 2.2 mm. The input network of the driver stage, the inter-stage network, and output network of the power stage are all on chip. Both the input and the output ports are designed for a standard 50 Ω environment. Off-chip bias tees are used to provide dc bias, for the convenience of testing. The device fabrication process is the same as the single-stage class-E amplifier.



(a)



(b)

Figure 6.9 Drain voltage and current waveforms: (a) Driver stage; (b) Power stage.

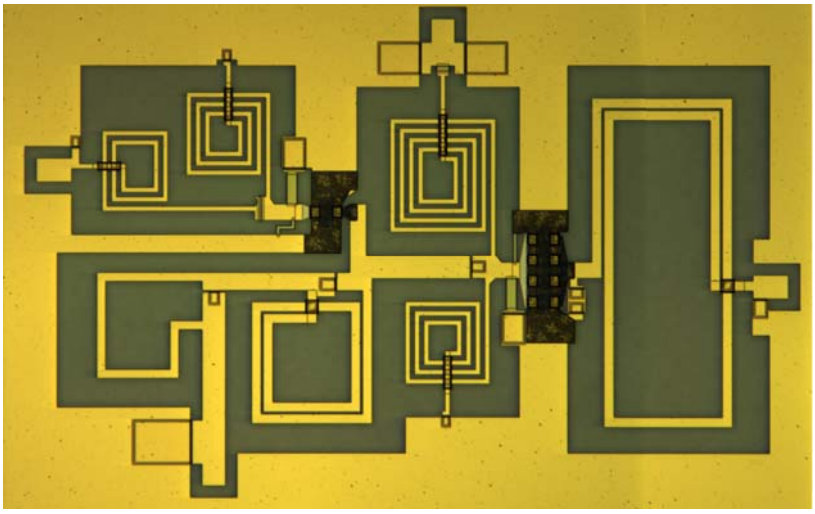


Figure 6.10 Photo of the Chip (3.4 mm x 2.2 mm)

Figure 6.11 shows both the measured and simulated results of output power and PAE versus frequency when the drain bias is 30 V. The two-stage amplifier achieves

a PAE of 50.4 %, a 36.3 dB output power into a 50 Ω load, and a power density of 4.3 W/mm. It can be seen from the figure that the PAE is over 49% within the frequency range between 1.9 GHz and 2.1 GHz. The simulation results of output power are in good agreement with the measured results, while a maximum discrepancy of about 7% is observed between measured and simulated PAE. Possible reasons include the inaccuracy of the device model for large-signal operations, and process variation.

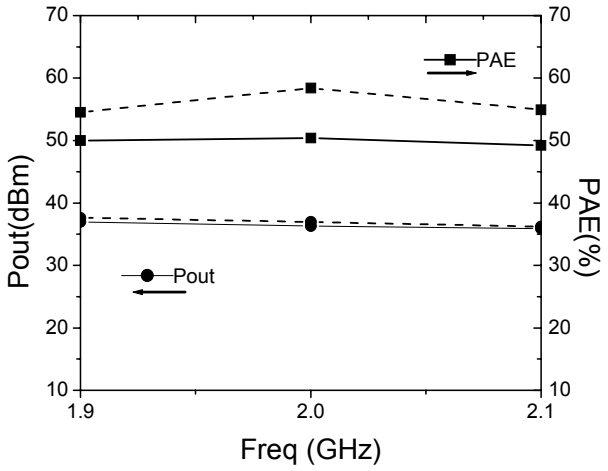


Figure 6.11 Output power and PAE versus frequency at V_{ds}=30 V,

Solid line: measured: dashed line: simulated.

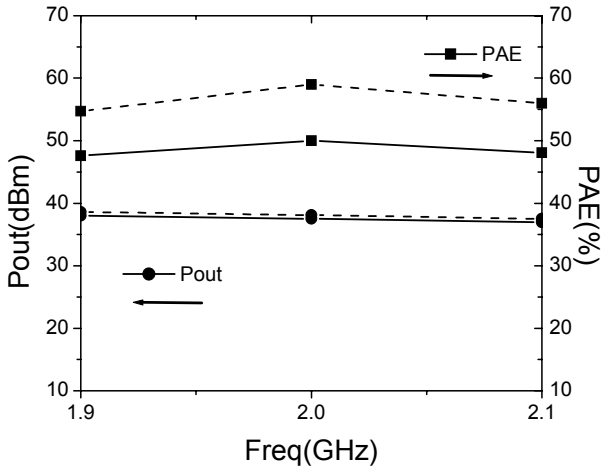


Figure 6.12 Output power and PAE versus frequency at V_{ds}=35 V, Solid line: measured; dashed line: simulated.

In Figure 6.12, the measured and simulated results of output power and PAE versus frequency at 35 V drain bias are shown. In this case, it achieves a PAE of 50%, a 37.5 dB output power into a 50 Ω load, and a power density of 5.6 W/mm. Within the frequency range between 1.9 GHz and 2.1 GHz, the PAE is over 47%. Again, a good agreement between measured and simulated results of output power is observed.

Figure 6.13 shows the measured output power, gain and PAE versus input power, which is measured at 2 GHz with a 35 V drain bias. At an input power level of 19.3 dBm, it achieves a PAE of 50 %, with a gain of 18.2 dB. Higher gain about 20 dB is achievable at lower input power levels.

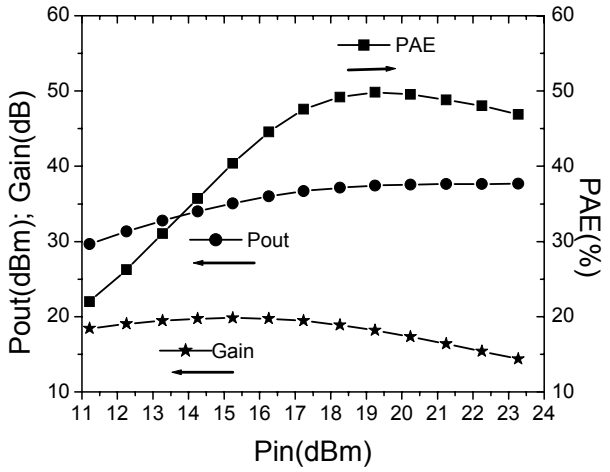


Figure 6.13 Measured output power, gain, and PAE versus input power: f_0= 2 GHz, V_{ds}=35 V

We have presented two class-E MMIC power amplifiers in GaN HEMT technology, taking advantage of the high-power density of GaN devices and the high-efficiency of the class-E PA topology. Using a field-plated AlGaN/GaN HEMT device, the single-stage circuit achieved a maximum power-added-efficiency of 57% and an output power of 37.2 dBm at 1.9 GHz and 30 V drain bias. The power density reaches 5.25 W/mm at 30 V drain bias and 7.4 W/mm at 40 V drain bias. The two-stage amplifier achieves an output power of 37.5 dBm into a 50 Ω load, a PAE of 50%, a gain of 18.2 dB, and a power density of 5.6 W/mm. In Table 6.2, class-E amplifiers based on different technologies are listed and compared. The output power and the power density from GaN HEMTs are much higher than other technologies. Comparing this GaN HEMT class-E amplifier with other technologies, the power amplifier exhibits state-of-the-art efficiency performance with significant

improvement in output power and power-density. Future mobile communication systems would require both high efficiency and high linearity. To achieve these, the GaN-based class-E amplifier could be employed in more advanced architectures such as linear amplification using nonlinear components (LINC), or envelope elimination and restoration (EER), etc.

Table 6.2 Compare class-E amplifiers in different technologies

	Technology	Freq. (GHz)	Vdc (V)	Pout (dBm)	PAE (%)	Area (mm2)	Device width (mm)	Power density (W/mm)	# of Stages
Ref. [2]	GaAs MESFET (0.8)	0.835	2.5	24	50	8.37	4	0.063	2
Ref. [8]	GaAs MESFET (0.8)	1.8	2.4	23	57	5.7	5	0.04	2
Ref. [3]	InP DHBT	10	4	22	65	4.4	180 (μm2)	n/a	1
Ref. [5]	LDMOS SOI	0.9	5	23	49	6	4.8	0.04	2
Ref. [4]	CMOS (0.35)	0.7	2.3	30.0	62	2.6	n/a	n/a	2
Ref. [9]	CMOS (0.25)	0.9	2.5	29.5	41	4.0	15	0.06	2
Ref. [10]	CMOS (0.35)	1.9	2.0	30.0	48	0.6	n/a	n/a	2
Ref. [11]	CMOS (0.18)	1.9	2.0	16.3	70	2.0	0.4	0.107	2
This work	GaN HEMT	1.9	30	37.2	57	5.28	1	5.248	1
	GaN HEMT	2	35	37.5	50	7.7	1	5.623	2

6.2. GaN low noise amplifiers

I. INTRODUCTION

As stated before, AlGaN/GaN HEMTs have not only been identified as the technology of choice for next generation high-power, high frequency applications but have also shown excellent noise characteristics for LNA circuits [12][13][14][15]. Typical receiver configurations include additional circuitry to protect the system from damaging signals, increasing complexity and introducing additional noise to the receiver system. Low-noise, high breakdown GaN HEMTs in amplifier front-ends reduce the need for diode limiters as protection against RF overstress. The high power capability directly translates into the ability to handle a high input power or energy spike without failure in a receiver front-end. This can reduce the overall LNA noise figure by 1dB [14]. In this section, we will demonstrate our noise figure and linearity of robust LNAs using GaN HEMT technology.

Our first GaN HEMT LNA circuit was designed using Agilent Advanced Design System (ADS) as show in Figure 6.14. To achieve accurate modeling, the small signal and noise properties of the transistors were characterized for circuit design. Noise parameters were measured using a Maury ATS load-pull system. A single stage low noise amplifier was designed with the input and output-matching network using only on-wafer spiral inductors. The amplifier input circuitry transformed the 50 Ω input load into a complex impedance, varying with frequency, that was as close as possible to the measured optimum noise matching of the transistors. The

measured and simulated input matching points from 4 to 8 GHz are shown in Figure 6.15. The output-matching circuit was optimized for maximum gain, gain flatness, and output matching using a small signal model extracted from s-parameter measurements. Special attention was paid to stabilized the circuit and develop adequate models of the passive components. The average Q factor of these on-wafer spiral inductors is 20 at 6 GHz. The LNA design avoids the use of metal-insulator-metal capacitors and thin-film resistors. The elimination of these components improves yield, reduces die area and lowers the cost of the chip fabrication.

The AlGaN/GaN HEMT devices were grown by MOCVD on sapphire substrates. The epitaxial structure is similar to what was used earlier in this work, which consisted of a semi-insulating Fe-doped GaN base layer, followed by a 290 Å thick $Al_{0.27}Ga_{0.73}N$ barrier layer. The room temperature sheet electron concentration and Hall mobility were ~1.15×10^{13} cm^{-2} and ~1211 cm^2/Vs, respectively. The GaN HEMT device has a gate length and width of Lg=0.7 μm and W_g=2x100 μm, a current density of I_{dss}=1 A/mm at 1V V_{gs}, and a breakdown voltage larger than 35 V. The device is not field-plated. The measured unity current gain cutoff frequency (f_t) of the device is 20 GHz.

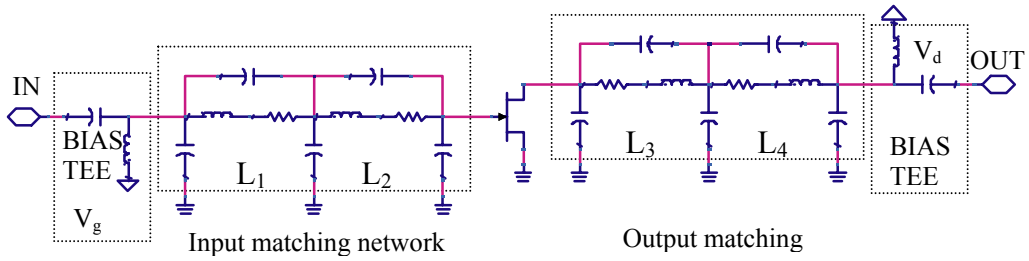


Figure 6.14 Circuit schematic of the low noise amplifier

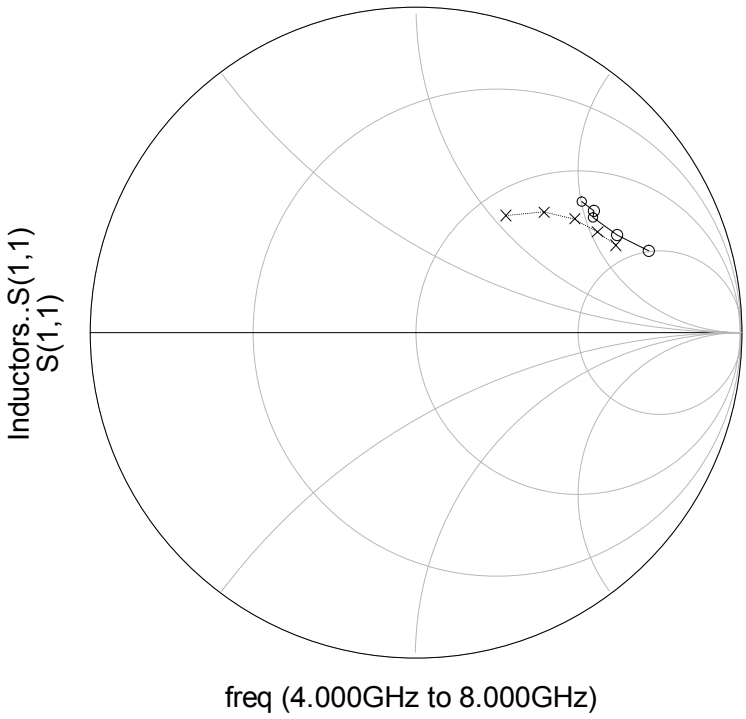


Figure 6.15 Measured (o) and simulated (x) input matching points

Since there are no SiN MIM capacitors or NiCr thin film resistors, the GaN HEMT LNA fabrication started with UCSB's standard HEMT process, then a spiral inductor process with PMGI cross-overs. The chip size is 3.1 mm x 1.25 mm. As shown in Figure 6.16, all input and output networks are on wafer. Circuit characterization was also done on a Maury ATS system from 4-8 GHz with a bias condition of V_{gs}=-3.5 V (~15% I_{dss}) and V_{ds}=4 V. Bias feeds for gate and drain were provided through off-wafer bias tees for convenience in testing.

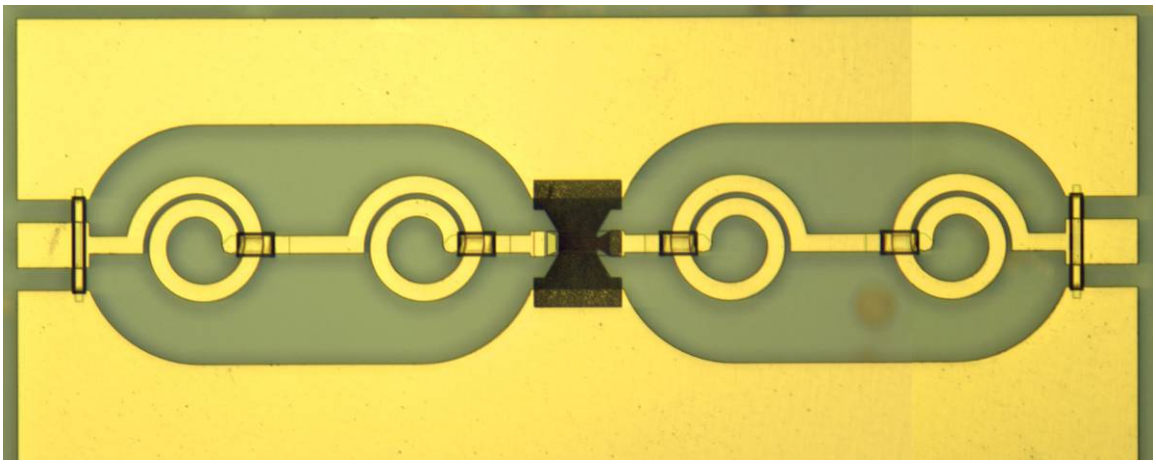


Figure 6.16 Chip photomicrograph of the developed LNA

The noise and gain performance of the LNA is shown in Figure 6.17. The LNA has a noise figure of 1.6 dB and a gain of 10.9 dB at 6 GHz. Moreover, it exhibits broadband operation. From 4-8 GHz, the noise figure is less than 1.9 dB. The DC power consumption of the amplifier is 120 mW. We have investigated the non-linear behavior of the amplifier by 1 dB compression point and third order intermodulation distortion measurements. In Figure 6.18, the single tone power measurement at 6 GHz shows a P_{1dB}=12.8 dBm.

The IM3 characterization was performed using a two-tone signal at 6 GHz with an offset frequency of 100 kHz. In Figure 6.19, the IIP3 of the LNA is 13 dBm in the linear region. The LNA shows very high dynamic range with decent gain and noise figure.

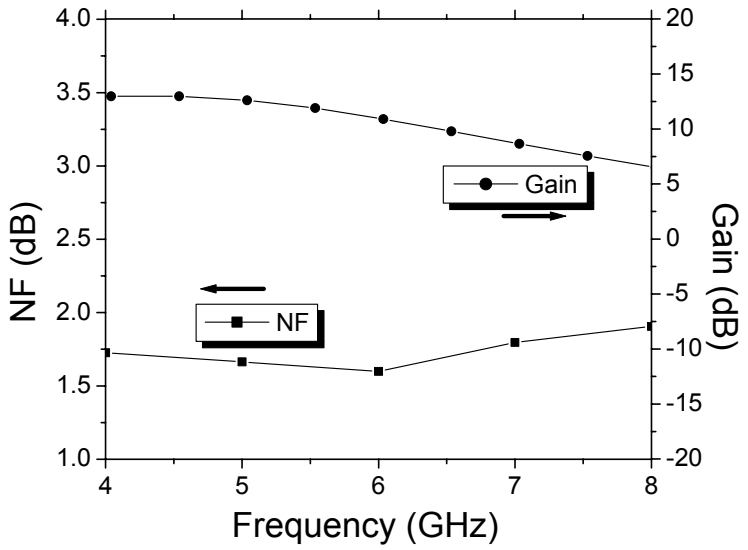


Figure 6.17 Noise figure and gain vs. frequency of LNA

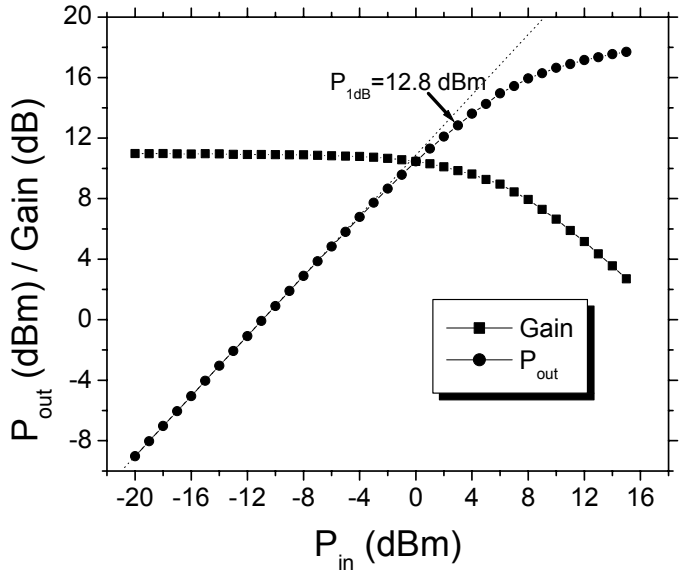


Figure 6.18 Single tone output power and gain of LNA at 6 GHz

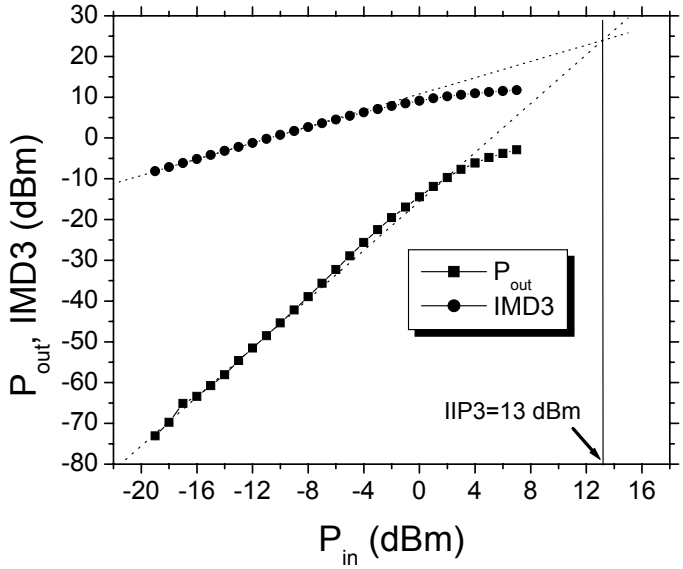


Figure 6.19 Linearity measurement at 6 GHz

Survivability characterization was performed on the LNA for sustaining high input power without failure. We drove the LNA with increasing CW input power until failure. In Figure 6.20, the LNA shows an input survivability of 31 dBm. For input power levels larger than 20 dBm, the device gate diode is partially forward biased during each RF cycle. As the driver level increases, the forward gate current increases, resulting in device burn-out when it reaches a ~400 mA/mm level (i.e. at a 31 dBm input power level). 20 dBm was the safe maximum input power level for CW input, since a slight performance degradation was observed for larger input power levels. However, the circuit was capable of handling up to 31 dBm input power before experiencing a catastrophic failure.

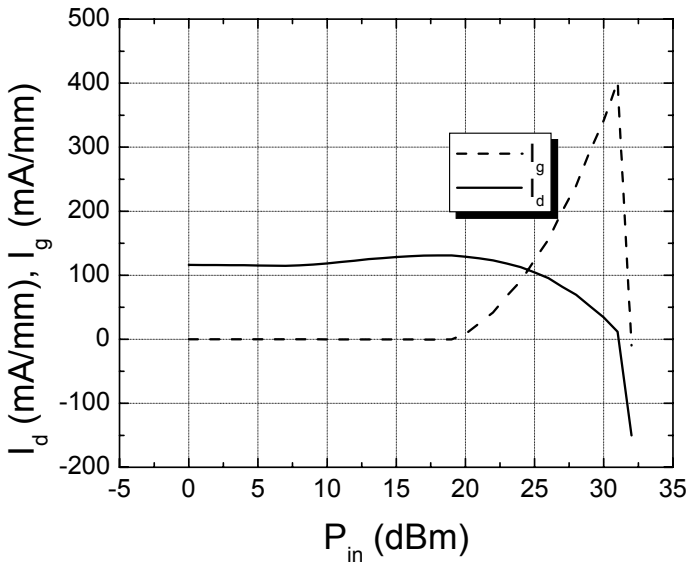


Figure 6.20 Survival test of LNA at 6 GHz

Even thought the noise and linearity performance look promising, but the input impedance is not well matched, because the optimized noise matching point, S_{opt}, is generally unrelated to the conditions that maximized power transfer. The return losses at the input and the output ports are less than -2.3 dB and -21.1 dB, respectively at 6 GHz (Figure 6.21). Providing a good match to a 50 Ω source without degrading noise performance would appear to be difficult. Several approaches to providing a resistive input impedance are used to improve the power and noise match simultaneously. But most of them require shunt-series resistors or feedback. They will add thermal noise of their own and attenuate the signal ahead of the transistor. A better method is to employ inductive source degeneration. With

such an inductance, current flow lags behind an applied gate voltage and it creates a resistive input impedance without the noise of real resistors.

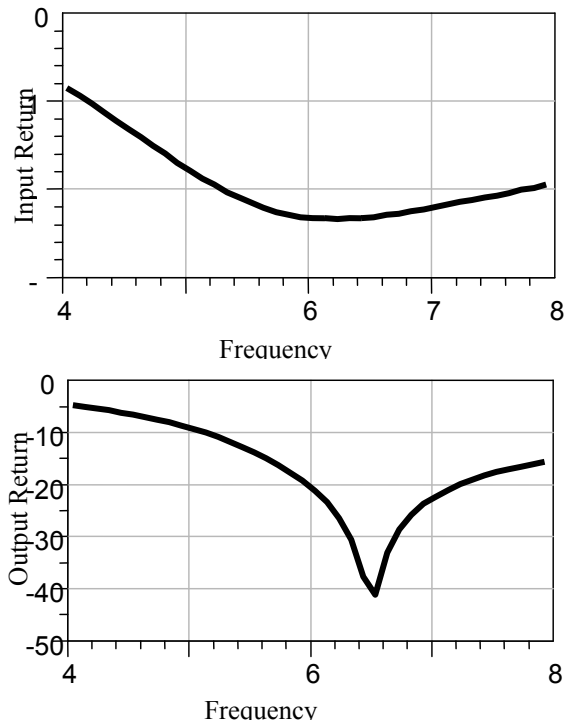
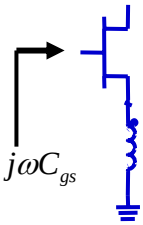


Figure 6.21 Input and output return loss of LNA

To simplify the analysis, consider a device model that includes only a transconductance g_m and a gate-source capacitance C_{gs}. In that case, it is easy to show that the input impedance has the following form:

$$Z_{in} \cong R_i + L_s g_m / C_{gs} + j\omega L_s + 1/ j\omega C_{gs}$$



Therefore, the input impedance is a series RLC network, with a resistive term that is directly proportional to the inductance value. With this resistive term, it is important to emphasize that it does not bring with it the thermal noise of an ordinary resistor because a pure reactance is noiseless. Even though the series inductor helps to match power and noise simultaneously, it also provides negative feedback that reduces the power gain, especially at high frequency. The real part of the optimum noise impedance is preferred to be close to 50 Ω, so that the required value of L_s is relatively small.

Empirical noise parameter relationships:

$$F_{\min} = 1 + k_1 f C_{gs} \left(\frac{R_g + R_s}{g_m} \right)^{1/2}$$

$$R_n = k_2 / g_m$$

$$R_{opt} = \frac{k_3}{g_m} \left(\frac{1}{4 g_m} + R_s + R_g \right)$$

$$X_{opt} = \frac{k_4}{f C_{gs}}$$

Scaled circuit parameter:

$$R_s' = R_s / s_1$$

$$g_m' = g_m s_1$$

$$C_{gs}' = C_{gs} s_1$$

$$R_g' = R_g s_2$$

Device scaled factors:

$$s_1 = \frac{W'_g}{W_g} \qquad s_2 = \frac{W'_g / N'^2}{W_g / N^2} \qquad s_1 s_2 = \frac{\left(W'_g / N'\right)^2}{\left(W_g / N\right)^2} = \left(\frac{U_{gw}'}{U_{gw}} \right)^2$$

N: The number of gate fingers; $\mathbf{W_g}$: Total gate width; $\mathbf{U_{gw}}$: Unit gate finger width.

N'; $\mathbf{W_g'}$; $\mathbf{U_{gw}'}$: parameters of scaled devices.

It is clear that one possible method is to modify the device periphery in order to enable the real part of the optimum noise impedance close to the input impedance. The above empirically derived relationships are found to reliably predict the noise characteristics [16]. Thus, with scaling factor s_1 and s_2, for a constant drain current,

when noise parameters for a HEMT of width W_g are known, the scaled noise parameters for width W_g' are obtained by substituting the scaled circuit parameters into empirical noise parameters. The resultant equations allow prediction of noise parameters as a function of gate width. These equations are shown in Figure 6.22. The scalability of this model to predict noise parameters is also further verified by measurements.

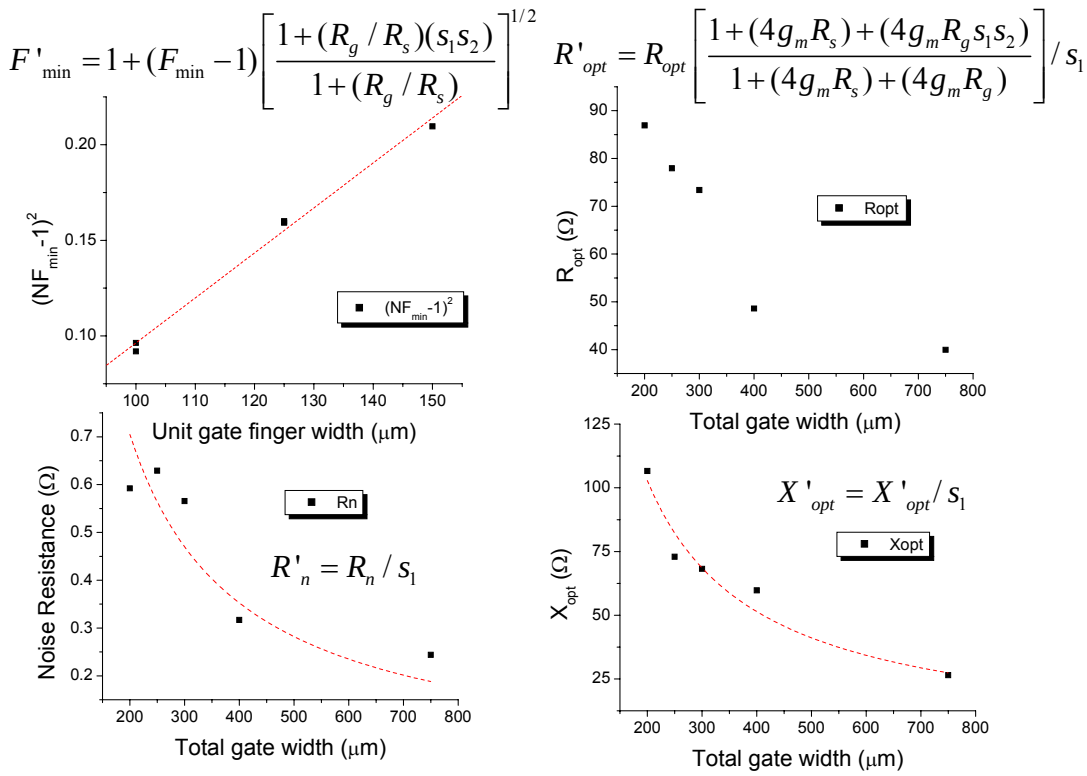


Figure 6.22 Scaled noise parameters

Based on these discussions, a new LNA was design using the topology with a series source inductor. Initially, a GaN HEMT with 0.7 μm gate length and total 360 μm gate width on 4 fingers was chosen to have a real part of the optimum noise

impedance close to 50 Ω. A noise model was setup for this device. Using this model, passive components L_g and L_s match noise and input impedance simultaneously. Then, an output matching network for power gain and gain flatness was designed. Finally, the complete circuit is optimized to provide input and output matching with the lowest possible degradation of the overall noise figure and gain. The circuit schematic of the new LNA is shown in Figure 6.23. Equivalent models of inductors are used in the circuit simulation. The output matching network consists of a series spiral inductor and a shunt capacitor at the drain. The GaN HEMT device in the circuit is bias at 5 V V_d and 45 mA I_d. The AlGaN/GaN HEMT devices have the same epitaxial structure and Al composition as the previous LNA.

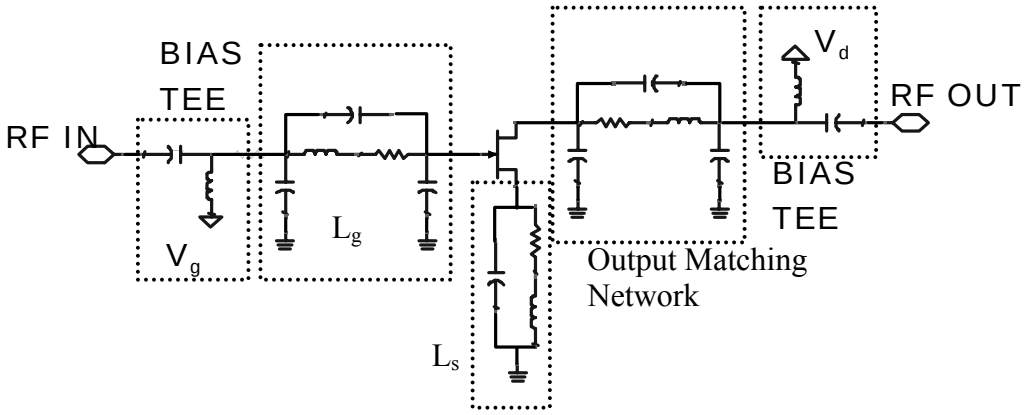


Figure 6.23 Circuit schematic of the improved low noise amplifier

The chip size is 0.9 mm x 1 mm, which is 4 times smaller than the previously designed LNA. As shown in Figure 6.24, all input and output networks are on wafer. The circuit was characterized on a Maury ATS system with external bias tees.

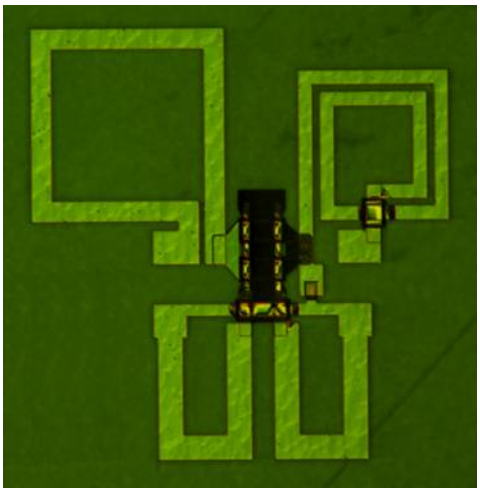


Figure 6.24 Circuit schematic of new low noise amplifier

The return losses at the input and the output ports are shown in Figure 6.25. The input return loss is improved 3.5 dB from the first design to -6 dB at 6 GHz, while the output return loss is still relatively low.

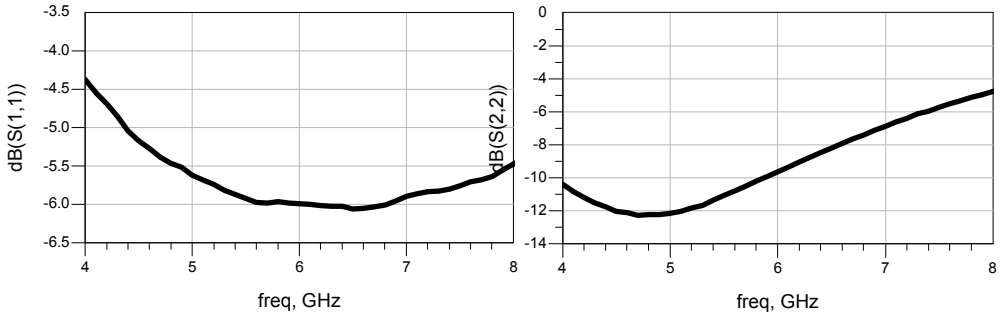


Figure 6.25 Input and output return loss of the new LNA

Noise, linearity and survivability results are shown in Figure 6.26. Also, as a comparison, the performance of both LNAs were summarized and listed in Table 6.3.

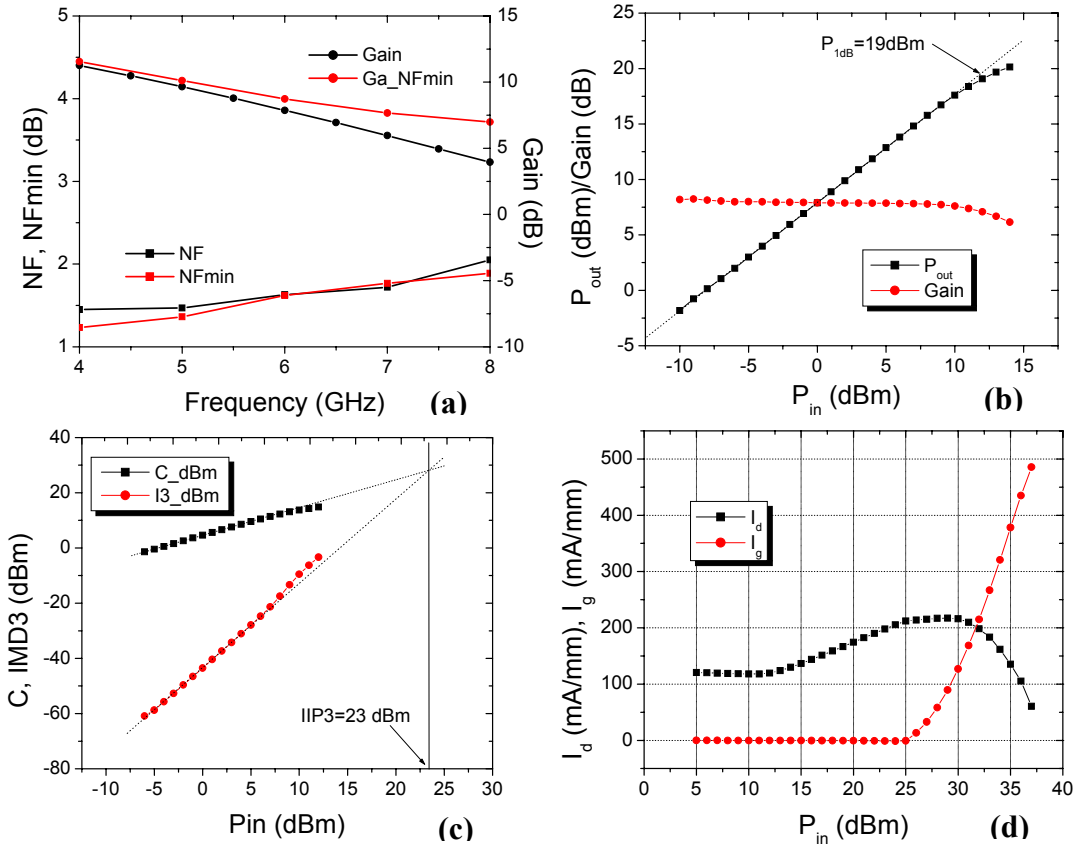


Figure 6.26 (a) Noise, (b)&(c) linearity and (d)survivability performance of the new LNA

Both GaN HEMT LNAs exhibit similar noise figure at 6 GHz. But the gain of the new LNA is 3 dB lower than the previous one. This is primarily because of the series degeneration source inductor. But the new LNA shows better input matching, linearity and survivability. The predicted cost of the new LNA is also reduced by the compact layout.

We have presented the performance of LNAs based on GaN HEMT technology and demonstrated that the GaN HEMT is an attractive candidate for low noise application. With respect to other technologies, it has comparable noise specifications with higher dynamic range and survivability. Moreover, using GaN HEMT technology allows the reduction or elimination of front-end protection, and the fabrication of both low noise and high power circuits on the same wafer.

Table 6.3 Performance comparison of GaN HEMT LNAs

	New LNA	Previous LNA
Frequency	6 GHz	6 GHz
NF	1.6 dB	1.6 dB
Gain	7.9 dB	10.9 dB
P1dB	19 dBm	12.8 dBm
IIP3	23 dBm @100 kHz	13 dBm @100 kHz
Survivability	>37 dBm	>31 dBm
Input Return Loss	-6 dB	-2.3 dB
Output Return Loss	-9.7 dB	-21 dB
Chip Size	0.9 mm x 1 mm	3.1 mm x 1.25 mm
Broadband NF	4-8 GHz (NF<2 dB)	4-8 GHz (NF<2 dB)

6.3. GaN oscillators

Limited by their low power capacity, most current GaAs microwave systems require a power amplifier to follow an oscillator in order to deliver a higher-power signal source. Studies of low-frequency noise show that GaN HEMTs offer comparable noise levels to conventional GaAs devices [17]; this indicates the

possibility of the use of GaN HEMTs to simultaneously achieve both high power and low phase noise performance in a single oscillator circuit [18][19]. In this section a study of the effect of field-plate dimensions on the output power, dc-to-RF efficiency and phase noise is presented. Through field-plate optimization, dramatic power and efficiency improvements were achieved over the previous state-of-the-art design.

The structure and analysis of the field-plated devices have been discussed in section 5.3. To study and optimize the effect of field-plates, the field-plate length of GaN HEMTs used in the oscillator circuits of this section was varied from 0 to 1.1 μm, while the circuit structure and other components remained fixed.

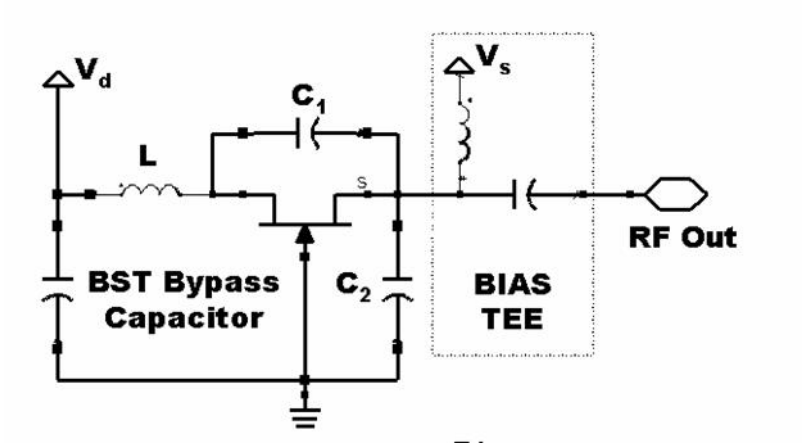


Figure 6.27 Circuit schematic of the oscillator

The oscillator circuit used a single-end Colpitts topology with a common-gate structure (Figure 6.27). The resonator was formed by lumped LC components. This simple structure helps to control parasitics from both active and passive components,

reduces the fabrication process variation, and allows us to accurately analyze the impact of field-plates on the circuit performance.

The design procedure was similar to the GaN/BST oscillator in Chapter 4. The small-signal properties of devices were characterized in the frequency range from 50 MHz to 25 GHz. The small-signal model parameters were extracted by using ADS-based parameter extraction routines. The model incorporated dominant parasitics and losses. The circuit was optimized to achieve maximum available output power, while keeping reasonable phase noise and linearity performance. An ADS EEHEMT1 scalable non-linear large-signal model was used to simulate transient and harmonic performance. The output power and frequency were also verified.

Instead of using spiral inductors, a metal stripline was used to make a high quality factor inductor. Unlike spiral inductors, striplines avoid ac current coupling between sections. They therefore exhibit better Q factors and higher self-resonant frequencies. The EM simulated Q factor of the 1.1 nH inductor used in the circuit was 39 at 5 GHz. Special attention was paid to make a compact circuit layout and avoid parasitic coupling between components.

The AlGaN/GaN HEMT devices were grown by MOCVD on SiC substrates. The epitaxial structure consisted of a semi-insulating Fe-doped GaN base layer, followed by a 290 Å thick $Al_{0.27}Ga_{0.73}N$ barrier layer. The room temperature sheet electron concentration and Hall mobility were ~9.96×10^{12} cm^{-2} and ~1450 cm^2/Vs, respectively. The circuits were fabricated using our standard MMIC process described in Appendix A. The GaN HEMT device has a gate length of $L_g = 0.7$ μm and width of $W_g = 4 \times 125$ μm. The channel is pinched off at a gate-source bias of -

5.3 V and the saturated drain current density was 1 A/mm at zero gate bias. With a drain bias of 20 V and drain current density of 200 mA/mm, the measured unity current gain cutoff frequency (f_t) decreased from 21 to 15 GHz for devices with field-plate lengths ranging from 0 to 1.1 μm. A detailed discussion on small-signal performance of field-plated HEMT devices can be found in Chapter 5. The chip size was 0.72 mm x 0.7 mm. As shown in Figure 6.28, The LC resonator tank is at the drain terminal of the HEMT device. The feed-back path between the source and drain is made by SiN_x MIM capacitors.

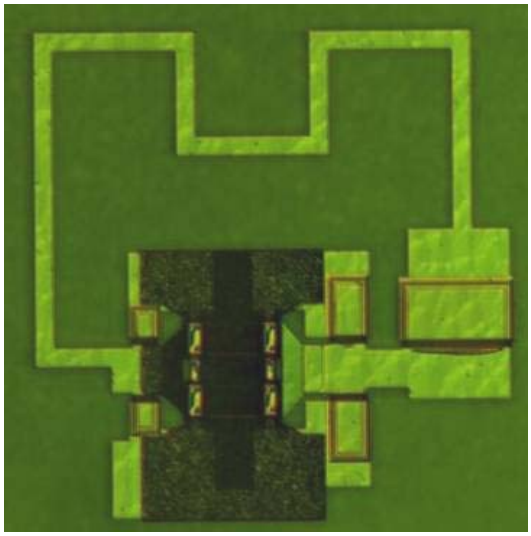


Figure 6.28 Chip photomicrograph of the developed oscillator

Circuits were characterized on-wafer using air-coplanar probes and an Agilent E4440 Spectrum Analyzer with phase noise option. Bias feeds for the gate and drain were provided through off-wafer bias tees for convenience during testing.

For comparison purposes, all oscillators were characterized at a bias of 40 V drain-to-source voltage and -4.5 V gate-to-source voltage. Output power and dc-to-

RF efficiencies for oscillators with HEMT devices using different field-plate lengths are shown in Figure 6.29. The output power increases from 28.4 to 32.8 dBm as L_F is increased from 0 to 1.1 μm. dc-to-RF efficiency exhibited a similar trend; increasing from 11 to 21.5%. As discussed in Chapter 5, the field-plated structure helps to reduce the knee-voltage and RF drain current dispersion of the devices. With 40 V drain voltage, the enhancement by the field-plate becomes more significant, but as the output power approaches maximum the saturated power level, the signal becomes more compressed. The 2nd harmonic distortion drops from 26.6 to 22.4 dBc as the field-plate length increases.

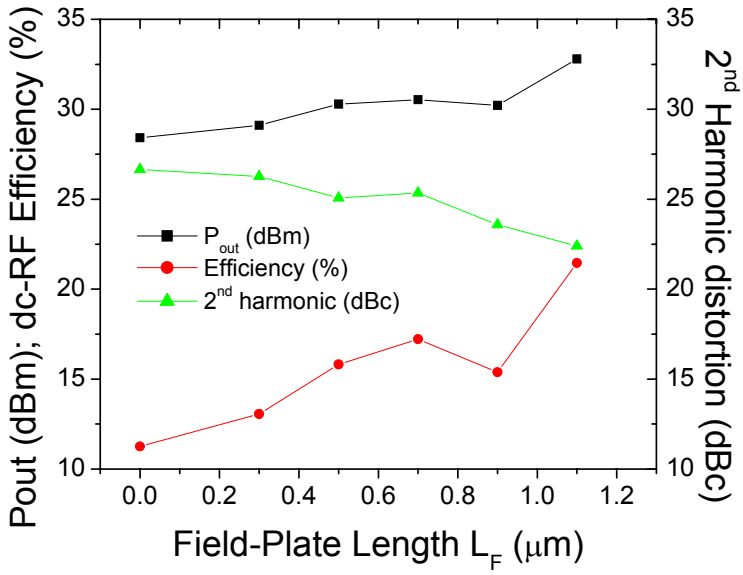


Figure 6.29 Output power, dc-to-RF efficiency and second harmonic vs. L_F

As seen from small-signal analysis, the gate-drain capacitance of field-plated devices increases as the field-plate length increases because of stronger gate-to-drain coupling. In oscillator circuits, this lowers the carrier frequency because the effective

capacitance in the LC tank increases. Figure 6.30 shows this carrier frequency shift, approximately 4% with a 1.1 μm change of field-plate length. This effect can be reduced by using an LC tank with a larger capacitance. Figure 6.30 also demonstrates that the oscillator power density improved dramatically with the field-plated structure. With a 1.1 μm field-plate length, the output power density reached 3.8 W/mm. Output power and dc-to-RF efficiency of this oscillator are shown as functions of drain voltage in Figure 6.31. The oscillator delivers a maximum of 30 dBm at 5 GHz into a 50-Ω load with a peak dc-to-RF efficiency of 24%.

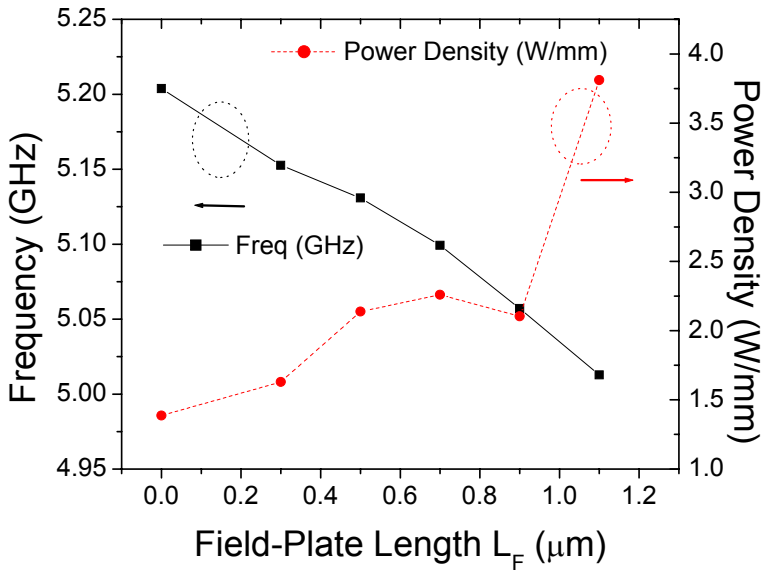


Figure 6.30 Carrier frequency and power density vs. L_F

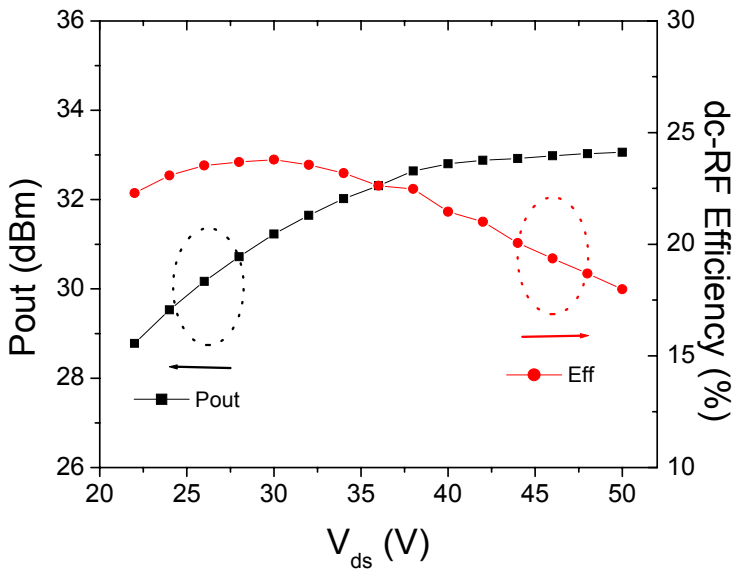


Figure 6.31 Output power and dc-to-RF efficiency of the oscillator with a 1.1-µm-long field-plate

The phase noise of the oscillator was measured across the offset frequency range of 10 kHz to 10 MHz. Figure 6.32 summarizes the measurement results at V_{ds} = 40 V and V_{gs} = -4.5 V. According to the Leeson formula:

$$L(f_m) = 10\log\left\{\frac{1}{2}\left[1+\frac{1}{f_m{}^2}\left(\frac{f_0}{2Q_l}\right)^2\right]\frac{FkT}{P_s}\left(1+\frac{f_c}{f_m}\right)\right\}$$

where Q_l is the loaded quality factor, f_0 is the resonant frequency, f_c is the flicker corner frequency of the device, f_m is the offset frequency, P_s is the amplifier's input signal power, F is its noise figure, k is Boltzman's constant, and T is the temperature. It can be seen that phase noise is inversely proportional to output power, the loaded quality factor, and noise figure. Since the passive

components were kept same for all of the oscillators, Q_l has a fixed impact on the phase noise for different field-plate lengths. It is known that with an identical peripheral dimension, the noise figure of field-plated devices is generally better than devices without a field-plate (L_F = 0). But among all field-plated devices, noise figure becomes worst with a 0.7-µm-long field-plate [20][21]. Phase noise measurements in Figure 6.32 showed a similar shape with phase noise increased for L_F = 0.7 µm. Phase noise drops fast for devices with larger L_F because of higher output power. 1/f baseband noise also plays an important role in phase noise. Further low frequency noise measurements on field-plated devices are required to understand the impact of field-plates on 1/f noise.

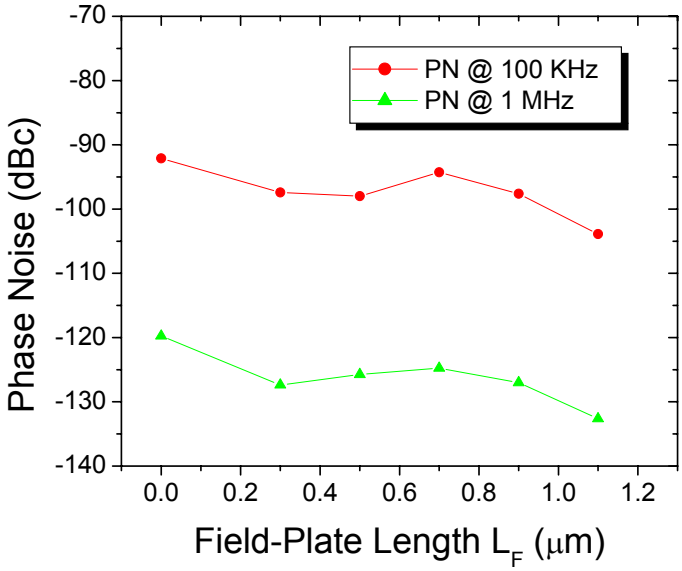


Figure 6.32 Phase noise at 100 kHz and 1 MHz offsets vs. L_F

The measured phase noise performance for the device with a 1.1 μm field-plate length is given in Figure 6.33. The phase noise is -103 and -132 dBc/Hz at offset frequencies of 100 kHz and 1 MHz respectively from 5 GHz carriers.

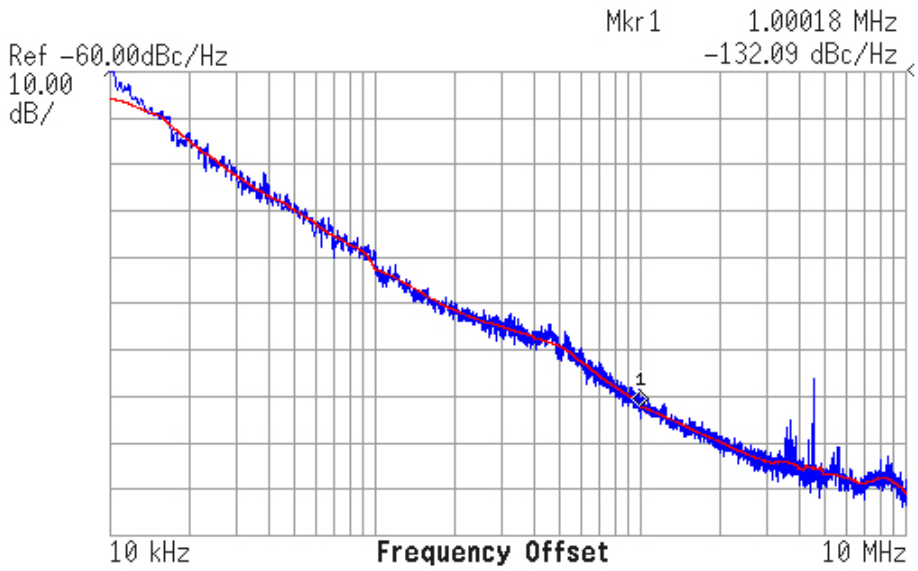


Figure 6.33 Measured phase noise of oscillator with a 1.1-μm-long field-plate

Dependences of the oscillation frequency on the gate and drain bias voltages are referred to as a pulling figure, which describes oscillation frequency sensitivity on power-supply variation. Frequency shifts as a function of the bias voltage change are shown in Figure 6.34. The observed change in oscillation frequency is less than 1% within a 1 V voltage variation from the initial bias condition.

One reason for using a buffer amplifier along with an oscillator is to provide a constant load impedance to the oscillation, and thus ensure that the oscillation frequency is not being affected by the rest of the system. A high power oscillator can be considered an alternative to a low power oscillator with buffer amplifier, only if it is capable of having very low sensitivity to changes in the load impedance. This

sensitivity is typically characterized by a pulling figure. The pulling figure measures the frequency shift as a function of the output reflection coefficient phase for a constant return loss of -12 dB. This measurement has been performed with a Maury ATS load-pull system, and the results are show in Figure 6.34. If these specifications meet system requirements, this high power oscillator can be used in a microwave system directly without a buffer amplifier. If not, the pulling figure has to be improved by inserting a buffer amplifier or an on-chip passive attenuator.

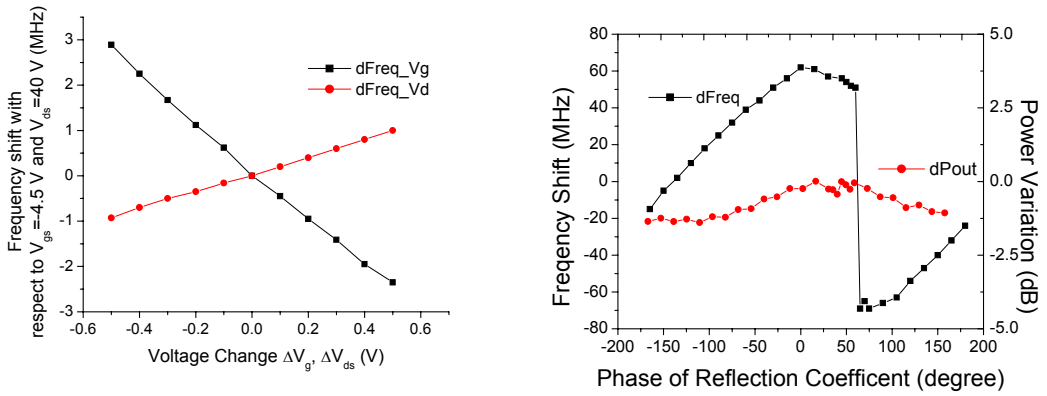


Figure 6.34 Pushing and pulling factors of the oscillator with a 1.1-µm L_F

It has been shown that at 5 GHz the field-plate offers enhancement of both power and noise properities. With a 1.1-µm-long field-plate, the oscillator delivered 32.8 dBm output power with 21% dc-to RF efficiency, corresponding to an output power density of 3.8 W/mm at 40 V drain voltage. But from the characterization of individual field-plated GaN HEMTs, the power density reaches over 10 W/mm at a 40 V bias and over 6 W/mm at a 30 V bias. The power densities from these oscillators obviously are much lower than expected. This indicates that large amount

of power are dissipated in the device and the LC tank. RF power is not efficiently delivered to the load. One principle reason is the small source resistance in the common gate structure. The equivalent resistance from the source of the transistor is

$$r_s = \frac{1}{g_m}$$

It is inverse proportional to the total gate width. For a 0.5 mm wide GaN HEMT, r_s is on the order of 8 Ω, which is significantly less than a 50 Ω load. Figure 6.35 shows the equivalent load network for a common gate Colpitts oscillator.

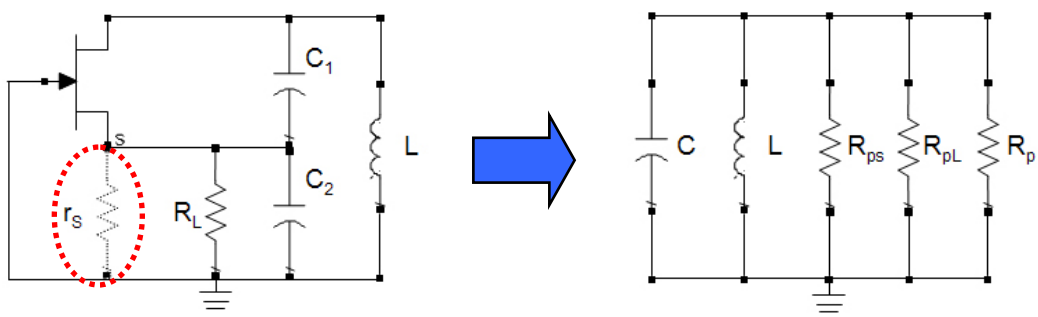


Figure 6.35 Equivalent load network for common gate oscillator

The values of components in the load networks are estimated from following expressions.

$$N = \frac{C_1 + C_2}{C_1} \qquad R_{ps} = N^2 r_s = \frac{N^2}{g_m}$$

$$C = \frac{C_1 C_2}{C_1 + C_2} \qquad R_{pL} = N^2 R_L$$

R_p : The sum result of R_{ds}, R_{gd} and unloaded Q

From the oscillation condition, N is calculated from the close loop gain.

$$CloseLoopGain = g_m \left(\frac{N^2}{g_m} // R_L N^2 // R_p\right) \frac{1}{N} \cong \frac{R_L}{r_s + R_L} N \cong 1$$

$$N \cong 1 + \frac{r_s}{R_L}$$

Thus, we have the load resistance and the dc-to-RF efficiency as follows:

$$Load = r_s N^2 // R_L N^2 // R_p \cong r_s (1 + \frac{r_s}{R_L})$$

$$Eff = \frac{r_s N^2 // R_L N^2 // R_p}{R_L N^2} Eff_{drain} \cong \frac{Eff_{drain}}{1 + \frac{R_L}{r_s}}$$

The expressions above imply that the load line is constrained by r_s, since r_s is generally smaller than the load resistance R_L. This is especially true for high power oscillators, because high current and large periphery make r_s even smaller, while a high resistive load line is required to achieve better power density and efficiency for large drain bias. To overcome this issue, the load R_L should be parallel connected to a high input resistance terminal, like the gate of a HEMT. A feedback common source oscillator structure is proposed to solve this problem. As required for this positive feedback oscillator structure, a π network is used to transform a high impedance, Z, at the gate to the Z_{in} at the load as shown in the Figure 6.36, while a 180 degree phase shift is obtained simultaneously. The impedance Z_{in} and voltage transfer function for this network are:

$$Z_{in} = \frac{Z(1-\omega^2 LC) + j\omega L}{(1-\omega^2 LC) + j\omega ZC(2-\omega^2 LC)}$$

$$\frac{V_o}{V_i} = \frac{Z}{Z(1-\omega^2 LC) + j\omega L}$$

If the values of L and C are properly chosen so that $\omega^2 LC = 2$, we have

$$Z_{in} = \frac{-Z + j\omega L}{-1} = Z - j\omega L$$

$$\frac{V_o}{V_i} = \frac{1}{-1 + \frac{j\omega L}{Z}}$$

If $j\omega L << Z$, $Z_{in} \approx Z$, the gate resistance Z is transformed to the input at the load. Also $\frac{V_o}{V_i} \approx -1$, this indicates a 180 degree phase shift. The required oscillation conditions are met without a degradation of the output power or efficiency, if $Z_{in} >> R_L$. Also since R_L is an external circuit component, the 50 Ω load Z_o can be easily transformed to a high resistance using appropriate impedance transformer circuits.

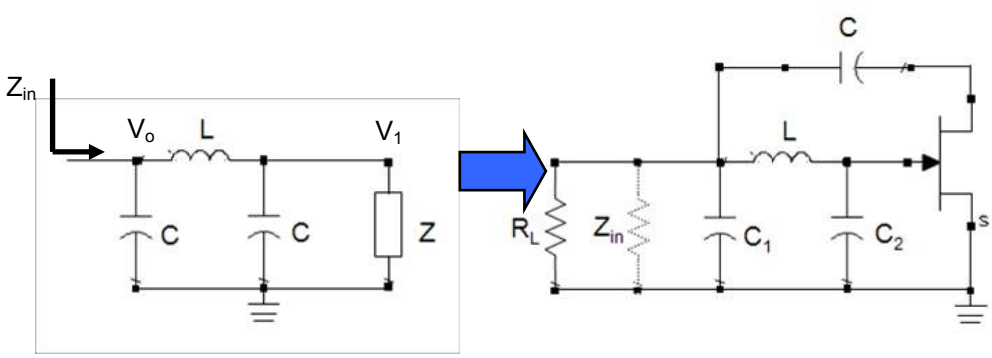


Figure 6.36 Network at the gate for the phase shift and impedance transform

A common source oscillator was designed and fabricated based on the analysis above. The circuit schematic and photograph are shown in Figure 6.37. The chip size of the circuit is 0.6 mm by 1.3 mm. The GaN HEMT material structure and circuit

fabrication are the same as the common gate structure before. The GaN HEMT device in the circuit has a 0.7 μm gate length and a 2x125 μm gate width with 0.7 μm field-plate length. The measured carrier frequency is 4.6 GHz.

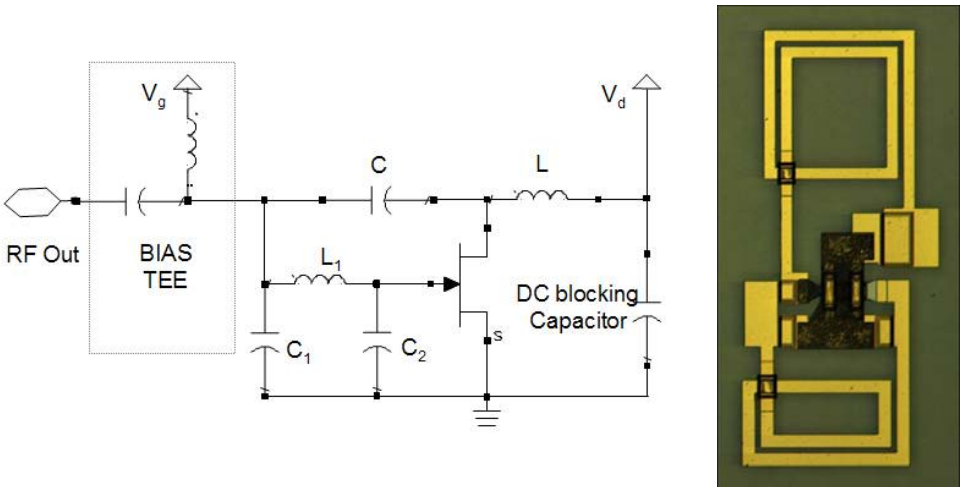


Figure 6.37 Circuit schematic and photograph of the common-source oscillator

Power, efficiency and linearity results are summarized in Figure 6.38. As we can see, the oscillator delivers 1 W output RF power, which corresponds to 4 W/mm at 25 V drain bias. The peak dc-to-RF efficiency is 30%, and keeps above 29 % with the bias range from 15 V to 25 V. Also the 2nd harmonic distortion is better than 32 dBc in this bias range. These results are significantly better than these typical ones in the common gate Colpitts oscillators. The power density achieved in this oscillator is also approaching the highest available power level from characterizations on individual field-plated GaN HEMTs with the same drain bias.

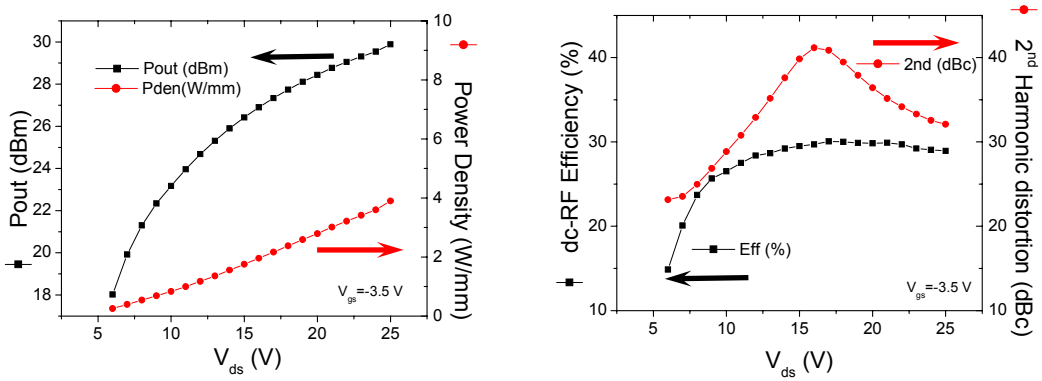


Figure 6.38 Power, efficiency and linearity of the common source oscillator

The noise performance is also characterized using a E4440 Spectrum Analyzer with phase noise option. The phase-noise was measured to be -99.99 dBc/Hz and -130.5 dBc/Hz at 100 kHz and 1 MHz offset respectively (Figure 6.39). It is 6 dB better than the common gate field-plated GaN HEMT oscillator with similar output power for the same field-plate length.

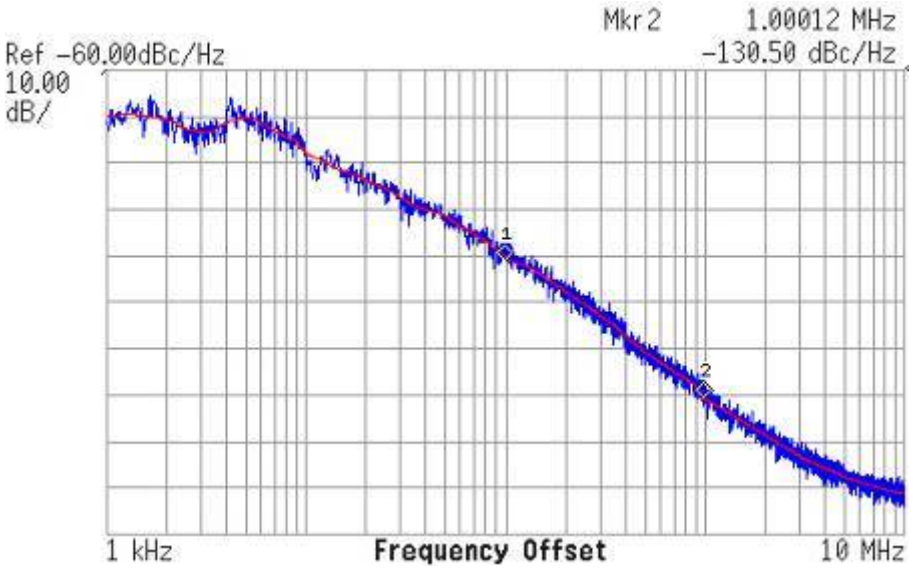


Figure 6.39 Phase-noise of common source oscillator

The power and noise performance of oscillators based on field-plated GaN HEMTs were investigated in this section. Such high power densities suggest the possibility of making ultra compact high power oscillators. Meanwhile, the high dc-to-RF efficiency will ease the requirements of thermal management. The field-plate devices also exhibit better phase noise than devices without field-plates. It has been demonstrated that with these improvements of power and noise performance, GaN HEMTs will be an ideal candidate in microwave source applications as next-generation microwave power devices.

6.4. GaN HEMT f_t doubler

Generally, the gain-bandwidth of an amplifier is limited by f_t, the unity current gain cutoff frequency. While the bandwidth of an amplifier need not be a strong function of f_t, it remains true that a higher f_t increases it, all other things equal. Device f_t is bounded within a given technology, so it would seem that once biasing conditions that maximize f_t have been established, the designer has done all that can be done to widen the andwidth. However, f_t would increase if the input decreases increases without decreasing transconductance. It can be done by a topological way.

The f_t doubler consists of transistors arranged with their drains summed together to increase the ac output signal current. The single-ended version is shown in Figure 6.40. With this arrangement, assuming both HEMTs to be of equal gate width and identical transcanductances, the output current is doubled. M1 acts as a source follower with the source resistor chosen to be $1/g_m$ so that the input signal evenly splits between the two transistors. The effective input capacitance is halved, while

the transconductance for the whole structure is still g_m. The effective ft for the ft doubler becomes $2\pi f_t = \frac{2g_m}{C_{gs}}$, which is two times that of a single transistor. A disadvantage of the ft doubler is a more complicated biasing scheme is needed. Also at higher frequency, the phase delay in M2 can cause distortion problems.

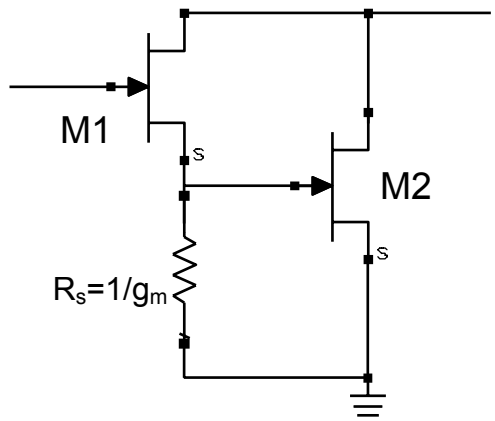


Figure 6.40 Single-ended f_t doubler cell

A GaN HEMT f_t doubler was designed and fabricated using two identical non-field-plated transistors with 0.7 μm gate length and 2x75 μm gate width. Since the peak f_t is normally measured with a 200 mA/mm drain current for GaN HEMTs, R_s is chosen as 25 Ω to meet the requirement of $1/g_m$ for the f_t doubler. The circuit schematic is shown in Figure 6.41. A 175 Ω self-biasing resistor is used to bias both transistors at the same operation condition. A 6-pF RF bypass capacitor is in parallel with the self-biasing resistor to ensure that the source of the HEMT in the second stage is RF grounded.

The AlGaN/GaN HEMT material was grown by MOCVD on SiC substrates. The epitaxial structure consisted of a semi-insulating Fe-doped GaN base layer, followed by a 290 Å thick $Al_{0.27}Ga_{0.73}N$ barrier layer. The ft doubler was fabricated using our

standard GaN HEM TMMIC process as described in Appenix A. The size of the circuit is 0.3 mm by 0.42 mm (Figure 6.42). The circuit is characterized as a single "transistor" using GSG ACP probes with bias tees at the input and output ports.

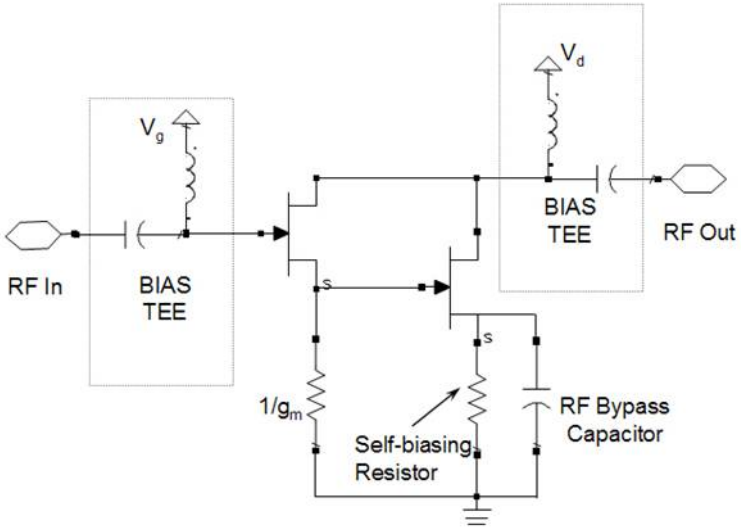


Figure 6.41 Circuit schematic of the GaN HEMT ft doubler

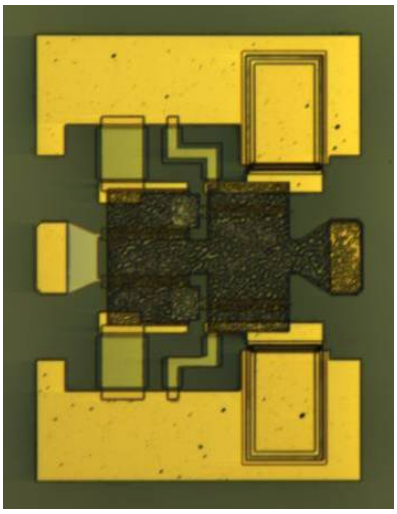


Figure 6.42 Chip photograph of the GaN HEMT ft doubler

The current gain (H_{21}) is extracted from measured S-parameters with a 20 V drain bias. A single 2x75 μm wide GaN HEMT is fabricated as a control device on the same die. Since the measured H_{21} versus frequency doesn't have a perfect 20 dB/dec slope, H_{21} data between 5 dB to 10 dB are used to calculated f_t by fitting a straight line with a 20 dB/dec slope. Measured results are shown in Figure 6.42. The f_t of the f_t doubler is measured as 43.5 GHz, which is 69% better than 25.5 GHz f_t from a single HEMT device.

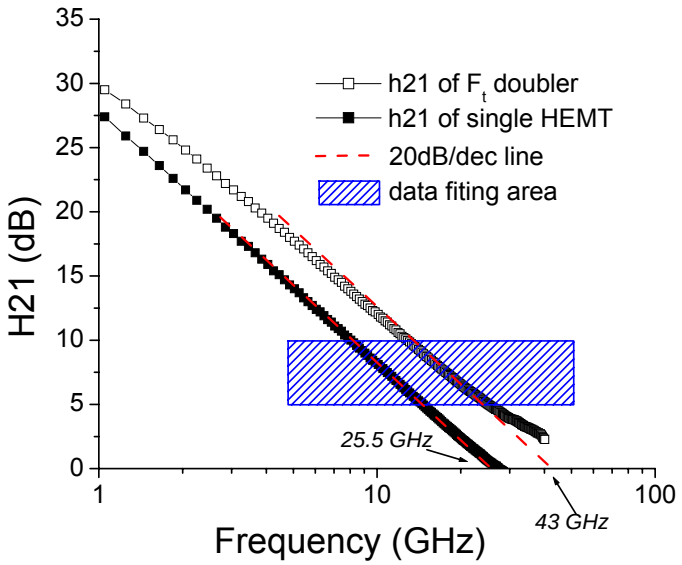


Figure 6.43 H_{21} versus frequency for single HEMT and f_t doubler

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Chapter 7. Summary and suggested future work

At UCSB, we have world leading material groups and device groups. Our work takes advantage of cutting-edge, newly developed device technologies. Both BST thin film and GaN epitaxial layer are being optimized and maturing for devices used for MMICs.

BST RF tunable capacitors, as a compact frequency agile component, have been investigated for years. In this work, an improved structure was proposed to increase its breakdown voltage and Q factor. Based on an analytical model, an optimization technique of the device periphery was developed. The peak RF performance of BST capacitors can be realized without changing device fabrication procedure or growth conditions. This technique has been validated by measurement results. Using this optimization routine, several tunable MMICs were designed and fabricated. Tunable BST thin-film based filters exhibit wide tuning range with relatively low losses. Two C-band phase shifters, using all-pass networks, showed very attractive figures of merit (phase shift per dB loss). Also their layouts are much smaller than circuits developed before, benefiting from device optimization and new circuit topologies.

Besides use in passive MMICs, BST thin films were successfully integrated with GaN HEMT circuits. A valid integration technique has been developed and tested with both circuit components and oscillators. Using a 3000 Å SiO_2 sacrificial layer, the AlGaN surface and 2DEG are protected from plasma damage during BST film growth. A slow ramping rate overcame the difficulty of using two unavoidable high temperature steps, which adversely affect each other. A 5 GHz GaN/BST oscillator

was demonstrated in Chapter 4. BST capacitors were used as RF bypass capacitors, which can significantly reduce die area. With the integration of both advance technologies, high power and low noise microwave source were obtained.

AlGaN/GaN HEMTs, as superior microwave power devices, have achieved tremendous progress in the last decade. Because the field-plate was employed in the GaN HEMT structure, power density has increased dramatically. In Chapter 5, we systematically compared two different field-plate structures from fabrication, simulation and measurement. A new field-plate structure is also proposed to achieve better power capacity and efficiency. Using this field-plate structure, both power and noise performances were improved.

Small and large-signal modelings are very critical to the circuit design. In Chapter 5, a small-signal modeling technique was described using an extrinsic element de-embedding process. A Large-signal modeling procedure was developed using optimization routine to fit dc curves and bias dependent RF parameters. The established small-signal models and large-signal models were used directly for the MMIC design.

Following development on GaN HEMT, passive components, fabrication and modeling, three major microwave components (PAs, LNAs and oscillators) were realized in GaN HEMT MMICs. GaN HEMT class-E power amplifiers using a field-plate structure were presented. A 1.9 GHz single-stage class-E PA delivers 5.25 W of output power with 57 % peak PAE. A two-stage class-E PA using a class-F driven stage delivers 5.6 W output power with 50% PAE. GaN HEMT LNAs show an attractive 1.6 dB noise figure at 6 GHz with a modest 0.7 μm gate length. Because of

the high power capacity of GaN HEMTs, LNAs have very high dynamic range and survivability. GaN HEMT oscillators were designed and fabricated to investigate low frequency noise properties of GaN field-plated devices. Oscillators with different field-plate extensions were compared for power, efficiency and phase-noise. The results were consistent with characterization and analysis from devices. In order to improve power capacity and efficiency, a common source feedback oscillator was designed and measured. It delivers 4 W/mm of output power with 30% of dc-to-RF efficiency at a 30 V drain bias. GaN HEMT technology can provide the possibility to integrate both high power and low noise microwave components on a single wafer.

In this work, MMICs based on BST thin film and GaN HEMT have been presented. Many problems remain unsolved. Some important aspects of future work are suggested below.

1) For field-plated devices, the noise figure is better than that in non-field-plate devices. Additionally, from measurement results, the dependence of noise figure on field-plate length is not straight forward. One possible reason is because of the trade-off between drain to gate capacitance C_{gd} and gate resistance R_g. But why and how field-plates impact noise figure is still not fully understood from a physical analysis. Also the phase-noise in oscillators showed a similar relationship with field-plate length. Low frequency noise characterization of field-plated devices is required to understand it. Once the causes behind these phenomena have been found,

we can use them to optimize noise properties from the material and device level. It will boost the ultimate noise performance in MMICs.

2) BST capacitors, as a frequency agile component, can be used in many applications, especially with active devices like GaN HEMTs. Some interesting circuits would be large tuning range VCOs, pre-distortion networks for PA, tunable matching networks or active antenna.

3) As the desired frequency for radar, satellite and wireless communication moves into the millimeter wave band, GaN HEMTs are also attractive for millimeter wave high power applications. One method to employ GaN HEMTs is directly using device with deep sub-micron gate lengths of 0.1-0.2 um. The other way is applying advanced circuit topologies to multiply the fundamental frequency. MIMICs design can start with f_t doublers, frequency multipliers and push-push oscillators. The availability of high quality integrated passive components in this frequency range is a big challenge.

4) Since we have developed various microwave components (PAs, oscillators, LNAs and filters), it would be very interesting to implement a more sophisticated subsystem by integrating these circuits and adding a few standard microwave components, like mixers, combiners or even antennas.

Appendix A. Process Flow of Field-plated GaN HEMT MMIC

1 Source and Drain Ohmics

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern

(2 layer resist process using OCG825 and SPR 950 ~ 0.8 µm)

Apply OCG 825 30 sec @ 5 krpm
Softbake OCG 825 1 min @ 95 °C (hotplate)
Cool down 1 min
Apply SPR 950 30 sec @ 3.5 krpm
Softbake SPR 950 1 min @ 90 °C (hotplate)
Cool down 1 min
Expose1.7 sec
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
MF 701:DI 200mL:100mL 1min 20 sec
DI Rinse 1 min
Nitrogren dry

Evaporate Ti/Al/Ni/Au

Using E-Beam #4

O2 Descum 15 sec @ 100 W, 300 mT
HCl:DI 1:3 30 sec
Evaporate Ti/Al/Ni/Au 200 A/1200 A/300 A/500 A

Liftoff Ohmic Metal

Liftoff 15 min soak in ACE
2 min UltraSonic in ACE,
(use small beaker, sample face down)
2 min UltraSonic in ISO,
(use small beaker, sample face down)
3 min UltraSonic in ACE
3 min UltraSonic in ISO
2 min DI Rinse
Nitrogren dry

RTA

RTA 30 sec @ 870 °C in N2
Check contacts on curve tracer

2 Mesa Isolation

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern

(2 layer resist process using SPR 950 and CEM 365 ~ 0.8 µm)

Apply SPR 950 30 sec @ 3.5 krpm
Softbake SPR 950 1 min @ 90 °C (hotplate)
Cool down 1 min
Apply CEM 365 30 sec @ 3.5 krpm
Remove PR on back
Expose 1.7 sec
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
DI Rinse 1 min
Develop in MF 701 2 min 20 sec
DI Rinse 1 min
Nitrogren dry

RIE #5 Etch

O2 Descum 15 sec @ 100 W, 300 mT
HCl:DI 1:3 30 sec
DI Rinse 1 min 30 sec
Nitrogren dry
BCl3 15W 10 sccm 10 mT 1 min
Cl2 100 W 10 sccm 5 mT 2 min

Resist Removal

Resist Removal 3 min UltraSonic in ACE
3 min UltraSonic in ISO
2 min DI Rinse
Nitrogren dry
Check isolation on curve tracer

3 Gate

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern

(2 layer resist process using OCG825 and SPR 950 ~ 0.8 µm)

Apply OCG 825 30 sec @ 5 krpm
Softbake OCG 825 1 min @ 95 °C (hotplate)
Cool down 1 min

Apply SPR 950 30 sec @ 3.5 krpm
Softbake SPR 950 1 min @ 90 °C (hotplate)
Cool down 1 min
Expose3 sec
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
MF 701:DI 200mL:100mL 1min 20 sec
DI Rinse 1 min
Nitrogren dry

Evaporate Ni/Au/Ni

Using E-Beam #4

O2 Descum 15 sec @ 100 W, 300 mT
HCl:DI 1:3 30 sec
DI Rinse 1 min 30 sec
Nitrogen dry
Evaporate Ni/Au/Ni 300 A/2500 A/500 A (rates are 2 A/ 3 A/ 2 A)

Liftoff Gate Metal

Liftoff 15 min soak in ACE
2 min UltraSonic in ACE,
(use small beaker, sample face down)

2 min UltraSonic in ISO,
(use small beaker, sample face down)
3 min UltraSonic in ACE
3 min UltraSonic in ISO
2 min DI Rinse
Nitrogren dry

4 Resistor

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern

(2 layer resist process using SPR 950 and CEM 365 ~ 0.8 µm)

Apply SPR 950 30 sec @ 3.5 krpm
Softbake SPR 950 1 min @ 90 °C (hotplate)
Cool down 1 min
Apply CEM 365 30 sec @ 3.5 krpm
Remove PR on back
Expose1.7 sec
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
DI Rinse 1 min

Develop in MF 701 2 min 20 sec
DI Rinse 1 min
Nitrogren dry

Evaporate Ti/SiO2/NiCr

Using E-Beam #1

O2 Descum 15 sec @ 100 W, 300 mT
HCl:DI 1:3 30 sec
DI Rinse 1 min 30 sec
Nitrogen dry
Evaporate Ti/SiO2/NiCr 25 A/300 A/500 A (rates are <0.5 A/ 2 A/ 1 A)
Be careful while melting NiCr. Be patient and keep low rate.
Keep observing and checking. Don't let ebeam damage the crucible. Better use bazooka for NiCr.

Liftoff Resistor Metal

Liftoff soak in ACE until metal start peeling off
3 min UltraSonic in ACE
3 min UltraSonic in ISO
2 min DI Rinse
Nitrogren dry

5 SiN Passivation

Chamber Preperation

Chamber ISO wipe
PECVD Process CHIN_A01
(When SiN depositing, Voltage should be 53 to 56V)

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry

PECVD SiN

(SiN thickness should be 1700 to 1800 A)

O2 Descum 15 sec @ 100 W, 300 mT
HCl:DI 1:3 30 sec
DI rinse 1 min 30 sec
Nitrogen dry
PECVD Process CHIN_A09

6 SiN Etching

Clean sample

ACE, ISO 3 min each
DI rinse 2 min
Nitrogen dry
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern

Apply SPR950 30 sec @ 3.5 krpm

Softbake SPR950 1 min @ 90 °C (hotplate)
Remove PR on back
Expose1.7 sec
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
Develop in MF 701 2 min 20 sec
DI Rinse 1 min
Nitrogren dry

Plasma Etch

O2 Clean without sample 10 min @ 300 W, 300 mT
CF4 etch 2 min @ 200 W, 300 mT
O2 Clean without sample 10 min @ 300 W, 300 mT

PR removal

ACE, ISO 3 min each
DI rinse 2 min
Nitrogen dry

7 Field Plate

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern

(2 layer resist process using OCG825 and SPR 950 ~ 0.8 µm)

Apply OCG 825 30 sec @ 5 krpm
Softbake OCG 825 1 min @ 95 °C (hotplate)
Cool down 1 min
Apply SPR 950 30 sec @ 3.5 krpm
Softbake SPR 950 1 min @ 90 °C (hotplate)
Cool down 1 min
Expose3 sec
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
MF 701:DI 200mL:100mL 1min 20 sec
DI Rinse 1 min
Nitrogren dry

Evaporate Ni/Au/Ni

Using E-Beam #4

O2 Descum 15 sec @ 100 W, 300 mT
HCl:DI 1:3 30 sec
DI Rinse 1 min 30 sec
Nitrogen dry
Evaporate Ni/Au/Ni 300 A/2500 A/500 A (rates are 2 A/ 3 A/ 2 A)

Liftoff Field-Plate Metal

Liftoff 15 min soak in ACE
2 min UltraSonic in ACE,
(use small beaker, sample face down)
2 min UltraSonic in ISO,
(use small beaker, sample face down)
3 min UltraSonic in ACE
3 min UltraSonic in ISO
2 min DI Rinse
Nitrogren dry

8 Underpass Bridge Metal

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern

(3 layer resist process using OCG 825, SPR 950 and CEM 365 > 2 µm)

Apply OCG 825 30 sec @ 3.5 krpm
Softbake OCG 825 1 min @ 95 °C (hotplate)
Cool down 1 min
Apply SPR 950 30 sec @ 3.5 krpm
Softbake SPR 950 1 min @ 90 °C (hotplate)
Cool down 1 min
Apply CEM 365 30 sec @ 3.5 krpm
Remove PR on back
Expose1.7 sec (increase focus offset by 8)
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
DI Rinse 1 min
Develop in MF 701 1min 50 sec
DI Rinse 1 min
Nitrogren dry

Evaporate Ti/Au

Using E-Beam #3 or #1

O2 Descum 15 sec @ 100 W, 300 mT
HCl:DI 1:3 30 sec
DI Rinse 1 min 30 sec
Nitrogen dry
Evaporate Ti/Au 200 A/10000 A (rates are 2 A/ 5~7 A)

Liftoff Bridge Metal

Liftoff soak in ACE until metal start peeling off
2 min UltraSonic in ACE,
2 min UltraSonic in ISO,
3 min UltraSonic in ACE

3 min UltraSonic in ISO
2 min DI Rinse
Nitrogren dry

9 PMGI

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern

(PMGI thickness of ~3 µm)

Apply PMGI SF15 40 sec @ 2 krpm
Softbake PMGI 3 min @ 200 °C (hotplate)
Cool down 3 min
Apply IR 5214 30 sec @ 4 krpm

Softbake IR 5214 1 min 15 sec @ 95 °C (hotplate)
Remove PR on back
Expose.38 sec, focus offset +16
Postbake 1 min 30 sec @ 105 °C (hotplate)
Flood expose 1 min
Develop in AZ400:DI 1:5.5 55 sec
DI Rinse 2 min
Nitrogren dry
Check lithography
Deep UV 3 min 20 sec
Develop in SAL101 1 min 15 sec
DI rinse 2 min
Nitrogen dry
Repeat last four steps 3 or 4 times (4 times is better)
Check lithography

PR removal

ACE, ISO 3 min each
DI rinse 2 min
Nitrogen dry
Do not soak in ACE for long time!

PMGI reflow

(You don't need to do cleaning if do reflow right after the liftoff.)

ACE, ISO 3 min each
DI rinse 2 min
Nitrogen dry
Reflow15 min @ 210 °C (hotplate)

10 Thich Metal

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry
Do not soak in ACE for long time!
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern

(3 layer resist process giving ~4 µm thickness)

Apply OCG 825 80 sec @ 1 krpm
Softbake OCG 825 2 min @ 95 °C (hotplate)
Cool down 1 min
Apply SPR 950 30 sec @ 3.5 krpm
Softbake SPR 950 1 min @ 90 °C (hotplate)
Cool down 1 min
Apply CEM 365 30 sec @ 3.5 krpm
Remove PR on back
Expose1.7 sec, focus offset +8
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
DI rinse 1 min
Develop in MF 701 1min 50 sec
DI Rinse 1 min
Nitrogren dry

Evaporate Ti/Au

Using E-Beam #1

Fill and melt Au source
Lower the holder to 28.3 cm from the source (27 cm from the platform)
Refill the Au source again to make sure it is enough to deposit 3 µm Au
Load sample on a holder with rotation
O2 Descum 20 sec @ 100 W, 300 mT
Nitrogen dry
Evaporate Ti/Au 300 A/30000 A (reading 150 A/15000 A)
rates are 2 A / 10 A (reading 1 A/5 A)

Liftoff Thick Metal

Liftoff soak in ACE for 20 min
3 min UltraSonic in ACE
3 min UltraSonic in ISO
2 min DI Rinse
Nitrogren dry

Appendix B. Process Flow of GaN HEMT MMIC integrated with BST capacitors

1 Source and Drain Ohmics

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern

(2 layer resist process using OCG825 and SPR 950 ~ 0.8 μm)

Apply OCG 825 30 sec @ 5 krpm
Softbake OCG 825 1 min @ 95 °C (hotplate)
Cool down 1 min
Apply SPR 950 30 sec @ 3.5 krpm
Softbake SPR 950 1 min @ 90 °C (hotplate)
Cool down 1 min
Expose1.7 sec
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
MF 701:DI 200mL:100mL 1min 20 sec
DI Rinse 1 min
Nitrogren dry

Evaporate Ti/Al/Ni/Au

Using E-Beam #4

O2 Descum 15 sec @ 100 W, 300 mT
HCl:DI 1:3 30 sec
Evaporate Ti/Al/Ni/Au 200 A/1200 A/300 A/500 A

Liftoff Ohmic Metal

Liftoff 15 min soak in ACE
2 min UltraSonic in ACE,
(use small beaker, sample face down)
2 min UltraSonic in ISO,
(use small beaker, sample face down)
3 min UltraSonic in ACE
3 min UltraSonic in ISO
2 min DI Rinse
Nitrogren dry

RTA

RTA 30 sec @ 870 °C in N2
Check contacts on curve tracer

2 Bottom Electrodes (BE) of BST Capacitors

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern

(2 layer resist process using SPR 950 and CEM 365 ~ 0.8 µm)

Apply SPR 950 30 sec @ 3.5 krpm
Softbake SPR 950 1 min @ 90 °C (hotplate)
Cool down 1 min
Apply CEM 365 30 sec @ 3.5 krpm
Remove PR on back
Expose 1.7 sec
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
DI Rinse 1 min
Develop in MF 701 2 min 20 sec
DI Rinse 1 min
Nitrogren dry

Evaporate Ti/Au/Pt

Using E-Beam #4

O2 Descum 30 sec @ 100 W, 300 mT
HCl:DI 1:3 30 sec
Evaporate Ti/Au/Pt 35 A/2000 A/1000 A (rates are 0.5 A/2.5 A/1.5A)

Liftoff BE Metal

Liftoff soak in ACE for 20 min
3 min UltraSonic in ACE
3 min UltraSonic in ISO
2 min DI Rinse
Nitrogren dry

3 SiO_2 Sacrificial Layer

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern

(2 layer resist process using SPR 950 and CEM 365 ~ 0.8 µm)

Apply SPR 950 30 sec @ 3.5 krpm
Softbake SPR 950 1 min @ 90 °C (hotplate)
Cool down 1 min
Apply CEM 365 30 sec @ 3.5 krpm

Remove PR on back
Expose 1.7 sec
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
DI Rinse 1 min
Develop in MF 701 2 min 20 sec
DI Rinse 1 min
Nitrogren dry

Evaporate SiO_2

Using E-Beam #2

O2 Descum 15 sec @ 100 W, 300 mT
HCl:DI 1:3 30 sec
Evaporate SiO_2 3000 A (rate is 3A)

Liftoff SiO_2 Layer

Liftoff soak in ACE for 10 min
3 min UltraSonic in ACE
3 min UltraSonic in ISO
2 min DI Rinse
Nitrogren dry

>> Sputtering BST film with a ramping rate of <u>20°C/min</u> <<

4 Top Electrodes (TE) of BST Capacitors

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern

(2 layer resist process using SPR 950 and CEM 365 ~ 0.8 μm)

Apply SPR 950 30 sec @ 3.5 krpm
Softbake SPR 950 1 min @ 90 °C (hotplate)
Cool down 1 min
Apply CEM 365 30 sec @ 3.5 krpm
Remove PR on back
Expose 1.7 sec
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
DI Rinse 1 min
Develop in MF 701 2 min 20 sec
DI Rinse 1 min
Nitrogren dry

Evaporate Pt/Au

Using E-Beam #4

O2 Descum 30 sec @ 100 W, 300 mT

HCl:DI 1:3 30 sec

Evaporate Pt/Au 1000 A/3000 A (rates are 1 A/2.5 A)

Liftoff TE Metal

Liftoff soak in ACE for 20 min

3 min UltraSonic in ACE

3 min UltraSonic in ISO

2 min DI Rinse

Nitrogren dry

5 BST etch

Clean sample

ACE, then ISO 3 min each

DI rinse 2 min

Nitrogen dry

Dehydration bake 3 min @ 120 °C (hotplate)

Cool down 3 min

Pattern

(PR thickness of ~1.4 µm)

Apply IR 5214 30 sec @ 4 krpm

Softbake IR 5214 1 min 15 sec @ 95 °C (hotplate)

Remove PR on back

Expose.38 sec, focus offset +16

Postbake 1 min 30 sec @ 105 °C (hotplate)

Flood expose 1 min

Develop in AZ400:DI 1:5.5 55 sec

DI Rinse 2 min

Nitrogren dry

Bake 15min @ 90 °C (oven)

BST etch

Buffer HF:DI H_20 3 min

Check under microscope. Repeat last step if the etch isn't complete.

Over etch 1~2 µm. Make sure BST & SiO_2 are removed completely.

PR removal

ACE, ISO 3 min each

DI rinse 2 min

Nitrogen dry

6 Mesa Isolation

Clean sample

ACE, then ISO 3 min each

DI rinse 2 min

Nitrogen dry

Dehydration bake 3 min @ 120 °C (hotplate)

Cool down 3 min

Pattern
(2 layer resist process using SPR 950 and CEM 365 ~ 0.8 µm)

Apply SPR 950 30 sec @ 3.5 krpm
Softbake SPR 950 1 min @ 90 °C (hotplate)
Cool down 1 min
Apply CEM 365 30 sec @ 3.5 krpm
Remove PR on back
Expose 1.7 sec
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
DI Rinse 1 min
Develop in MF 701 2 min 20 sec
DI Rinse 1 min
Nitrogren dry

RIE #5 Etch

O2 Descum 15 sec @ 100 W, 300 mT
HCl:DI 1:3 30 sec
DI Rinse 1 min 30 sec
Nitrogren dry
BCl3 15W 10 sccm 10 mT 1 min
Cl2 100 W 10 sccm 5 mT 2 min

Resist Removal

Resist Removal 3 min UltraSonic in ACE
3 min UltraSonic in ISO
2 min DI Rinse
Nitrogren dry
Check isolation on curve tracer

7 SiO_2 BST Crossover and Passivation Layer

Clean sample

ACE, then ISO 3 min each
DI rinse 2 min
Nitrogen dry
Dehydration bake 3 min @ 120 °C (hotplate)
Cool down 3 min

Pattern
(2 layer resist process using SPR 950 and CEM 365 ~ 0.8 µm)

Apply SPR 950 30 sec @ 3.5 krpm
Softbake SPR 950 1 min @ 90 °C (hotplate)
Cool down 1 min
Apply CEM 365 30 sec @ 3.5 krpm
Remove PR on back
Expose 1.7 sec
Postbake 2 min @ 100 °C (hotplate)
Cool down 1 min
DI Rinse 1 min

Develop in MF 701 2 min 20 sec
DI Rinse 1 min
Nitrogren dry

Evaporate SiO_2

Using E-Beam #2

O2 Descum 15 sec @ 100 W, 300 mT
HCl:DI 1:3 30 sec
Evaporate SiO_2 3000 A (rate is 3A)

Liftoff SiO_2 Layer

Liftoff soak in ACE for 10 min
3 min UltraSonic in ACE
3 min UltraSonic in ISO
2 min DI Rinse
Nitrogren dry

>> Follow steps 3-10 in Appendix A to complete the rest process <<