Waveguide-Based Spatial Power Combiners

A dissertation submitted in partial satisfaction of the requirements for the degree of Doctor of Philosophy in Electrical and Computer Engineering by Nai-Shuo Cheng

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ABSTRACT

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Spatial power combining technique provides a viable solution to the realization of solid-state power sources and amplifiers at microwave and millimeter-wave frequencies, with RF power levels that currently can not be achieved by a single solid-state device. Spatially-fed/spatially-combined arrays have been the focus of much research activity during the past decade. Most of the work has centered on planar arrays with normally incident or outgoing beams. Such arrays generally have limited bandwidths and also present difficult challenges in thermal management and efficient power collection. A waveguide-based spatially-combined solid-state power amplifier has been developed to address these issues.

The waveguide-based combiner systems use stacked trays of broadband tapered-slot antennas integrated with commercial MMIC amplifiers, housed in a waveguide environment that is operated in the dominant $TE_{10}$ mode. Each antenna is then essentially a waveguide-to-transmission line transformer that couples energy from the waveguide mode to a set of power amplifiers. Power enters and leaves the system in a single well-defined mode, and therefore power distribution and collection is simplified. The hybrid circuit configuration not only enables circuit designers with flexibility of choosing different device technologies, but also presents excellent thermal management. Higher power output can be achieved by increasing the number of trays and active devices per tray and using high-performance devices. In addition, the modular architecture allows easy maintenance, variable power output and potential medium-scale fabrication. A maximum 150-Watt result at X-band in an over-moded waveguide was achieved, suggesting that our combiner system is a promising candidate to challenge the dominant vacuum-tube technology such as traveling-wave tube amplifiers (TWTA) in wireless communication applications.
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Chapter 1

Introduction

Power combining techniques provide a viable solution to the realization of solid-state power sources at microwave and millimeter-wave frequencies, with RF power levels that currently can not be achieved by a single solid-state device. Traditional quasi-optical and/or spatial power combining circuits based on tile architecture have seen tremendous developmental progress; however, fail to render broadband characteristics and efficient thermal management, particularly for large arrays. This thesis presents the research work regarding the development of waveguide-based spatial power combiners with high-power capability (> 100 Watts at X-band), broadband characteristics and verified heat-sinking property.

1.1 Motivation

There has been a constant unsatisfied need in microwave industry for high power solid-state sources and amplifiers at microwave and millimeter-wave frequencies [1]. Solid-state electronics is a mature technology, which is in general favored over its vacuum-tube-based counterpart in terms of size, weight, integration capability, operating voltage and reliability. However, solid-state devices, which have limited power-handling capability along with an inverse dependence on frequency, are popular but only find applications at low frequency and/or low power. As the applications gear towards higher frequency and/or higher power, the vacuum-tube electronics claims a dominantly leading position. Even with the advent of promising high-power solid-state devices based on wide-bandgap semiconductor materials such as gallium nitride (GaN) and silicon carbide (SiC) [2, 3], it is still difficult and costly at the present time to realize significant RF output power at a single device level. Consequently, power combining techniques have been
widely adopted since high power at microwave/millimeter-wave frequencies can be achieved by coherently collecting the output power from a large number of solid-state devices.

![Graph showing available technologies for power sources and amplifiers](image)

*Figure 1-1: Available technologies for power sources and amplifiers (at a single-device level) at microwave and millimeter-wave frequencies [4].*

Corporate combining techniques have been very popular and often used in planar circuits, due to design simplicity and ease of implementation. As shown in Figure 1-2(a), Wilkinson combiners, for example, consist of one or several stages of binary adders, which are used to successively combine the outputs from a number of active devices. However, the loss associated with each stage quickly adds up as the array size increases; therefore, they are only suitable for small-scale integration. In the case of spatial/quasi-optical power combining, as shown in Figure 1-2(b), all the devices are operated in parallel with each other, with the combining process typically taking place in free space. As a result, the combining loss remains constant as the number of active element increases. A comparison between two (corporate and spatial) schemes is shown in Figure 1-3. It is obvious to see why spatial combining technique is favored over its corporate counterpart in high power applications, where a large number of active elements are present. Recently, spatial/quasi-
optical power combining techniques have witnessed tremendous technological advances in terms of power performance and functionality [1, 5-7].

Figure 1-2: Circuit topology for (a) corporate and (b) spatial/quasi-optical power combining networks

Figure 1-3: A comparison between corporate and spatial power combining schemes, assuming that the gain and power-added efficiency of the amplifiers being combined are 10 dB and 50%, respectively.
For spatial/quasi-optical power combining circuits consisting of large array of active elements, sub-systems of smaller array can be used, which can be implemented by using either "tile" or "tray" architecture [7]. In the "tile" architecture, as shown in Fig. 1-4(a), planar antennas are of resonant-type and have broadside radiation characteristics. This approach is very popular because of its simplicity and possible monolithic fabrication; however, it suffers from narrow bandwidth and potential thermal problems since the waste heat can only be removed inefficiently from the edges of the two-dimensional arrays. Another approach is the "tray" architecture, as shown in Fig. 1-4(b), where antennas with endfire radiation characteristics can be utilized, which render a wide-band property. In addition, this approach provides much better heat-sinking environment and modular architecture. As a result, the "tray" architecture is more suitable than the "tile" architecture if broadband high-power amplifiers/sources are desired.

![Figure 1-4: Two architectures, (a) tile and (b) tray, used to implement active antenna arrays in spatial combining circuits.](image)

The U.S. Department of Defense (DoD) has initiated several research and developmental programs over the years to develop a solid-state-based technology capable of high output power and new functionality for advanced system applications at microwave/millimeter-wave frequencies [8]. This thesis presents the work regarding the design and analysis of waveguide-based solid-state amplifiers using spatial power combining technique, which was sponsored by the Defense Advanced Research Project Agency (DARPA) through a sub-contract from HRL Laboratories, LLC. The ultimate goal
of the project was to realize a broadband solid-state source at X-band capable of >100 Watts of output power.

A prototype circuit using dense tapered antenna arrays in waveguide was initially developed by Alexanian and York, which achieved 10 Watts of maximum output power at X-band [9, 10]. Although the concept was outstanding, the implementation of the combiner circuit was immature and plagued with many technical problems, including low combining efficiency (about 50%), poor thermal property, mediocre bandwidth characteristics, and complicated/low-yield fabrication procedure. In addition, the circuit architecture was not physically robust, resulting in frequent circuit breakage problems during measurements. Furthermore, the design of the passive antenna arrays was basically semi-empirical, whereas an optimized design procedure is desired. The aforementioned problems provided impetus for additional research into such combining circuits, which will be covered by this thesis.

1.2 Thesis Outline

In the following chapter, a finite-difference (FD) numerical technique is developed to study the propagation characteristics of finline arrays. Using the method, the eigen matrices corresponding to a wave-guiding structure with specific geometric parameters can be derived from the finite difference equations along with the applied boundary conditions. The eigenvalues (propagation constant) and eigenvectors (longitudinal magnetic field) can successively solved by using ARPACK, an eigen matrix solver which is capable of treating large non-symmetric sparse matrices with efficient usage of computer resources, in terms of memory and time.

In Chapter 3, we establish the design procedure and equations for the realization of broadband non-TEM wave-guiding structures. The theory of Klopfenstein taper, which was originally proposed for broadband TEM impedance transformer, was modified and applied to finline arrays, which is quasi-TE in nature. With the essential design information (propagation characteristics) established in Chapter 2, the shape of the finline arrays can be determined and optimized so as to minimize the return loss within the entire
frequency band of interest. Design examples will be provided and verified with measurement results.

Chapter 4 presents a new version of combining circuits based on dense finline arrays, which not only addresses the issues that limited the performance of the previous design but also is capable of delivering >100 Watts output power as well. Details such as design considerations, circuit topology, and assembly procedure will be discussed. In addition, the performance of the passive structure of the combining circuits will be studied, in terms of combining efficiency, return loss characteristics and thermal property. Furthermore, the impacts on combiner performance due to non-ideal effects such as bondwire parasitics and non-uniform illumination will be studied.

In the following chapter, combining circuits based on 4×2, 6×4 and 8×4 active antenna arrays, either in standard or oversized waveguide environment will be covered. Characterization and optimization of GaAs MMIC power amplifiers will also be investigated with an attempt to enhance combiner performance. The combiner performance will be evaluated, in terms of RF output power, gain, power-added efficiency (PAE) and graceful degradation property. Various results including a 150-Watt maximum power output with gain variation less than ±1.9 dB within the entire band of interest will also be presented. In addition, an oscillation problem that plagued the combiner performance will be studied.

More design effort can be made for further performance improvement, including measures to reduce bondwire parasitics, eliminate oscillation problems and enable uniform illumination, will all be presented in Chapter 6.

References


Chapter 2

FDFD Analysis of Finline Arrays

Finline is a planar structure that has been widely used to realize millimeter-wave integrated circuits, mainly due to its low-loss and wide-band properties [1, 2]. Arrays of finline, or slotline in rectangular waveguides, have been used to implement spatial power combining circuits due to their compatibility with tapered slot antennas and rectangular waveguides. A finite-difference frequency-domain (FDFD) technique was applied in order to study the dispersion characteristics of two-dimensional finline arrays. Not only that FDFD is capable of analyzing complex structure with multiple dielectrics and irregular geometry, but also that the field distributions can be obtained directly as well, making the derivation of physical parameters such as characteristic impedance straightforward. ARPACK, a free software available from Internet and consisting a collection of Fortran 77 subroutines, was used to solve large-scale, non-symmetric and sparse-matrix eigenvalue problems that were derived from the finite difference equations.

2.1 Problem-Solving Procedure

The two-dimensional FDFD technique has been widely used to study the dispersion property of a variety of inhomogeneous and/or anisotropic wave-guiding structures, such as dielectric-loaded waveguides and optical/dielectric waveguides [3-9]. Several features have made FDFD a popular numerical technique both for practical applications and academic interests. The mathematical formulation is straightforward in that the finite difference equations are derived directly from the Maxwell equations. In addition, complex structures with multiple dielectric regions can be treated relatively easily and structure variation does not necessarily translate into significant revision of computer codes. Furthermore, the field components can be obtained directly so that certain physical
parameters such as characteristic impedance, power density, field components and current distribution can be derived quite easily. A typical problem-solving procedure used in FDFD analysis is outlined in Figure 2-1, including four major steps.

![Diagram of problem solving procedure](image)

Figure 2-1: Procedure of problem solving used in FDFD analysis.

First, a computation domain is defined, which represents the cross section of a wave-guiding structure with all the geometric parameters and material properties determined. A grid of nodes, with proper indexing, is set up by dividing the computation domain into mesh of unit cells, based on either non-uniform or uniform grid approach. When the aspect ratio of the geometric dimensions is large, a non-uniform grid is usually used in that the grid size can be greatly reduced. The boundary properties have to be properly assigned so that boundary conditions can later be implemented accordingly. It cannot be over-emphasized to make use of symmetry property of the wave-guiding structure whenever possible, with the consideration of the propagating mode of interest. Significant reduction in domain size and computation time is almost guaranteed with such move. Consequently, fictitious boundaries such as perfect electric conductor (PEC) or
perfect magnetic conductor (PMC) are used so that FDFD analysis is only required to simulate part of the original structure.

After the computation domain is set up properly, the corresponding finite-difference (FD) equations at all the nodes are derived from the governing electromagnetic equations, which are second-order partial differential equations. In general, a hybrid-mode problem requires two unknowns at every node in the computation domain. In certain special cases, where TE or TM modes are present, only one unknown per node is needed. For the nodes residing on the boundary, such as PEC or PMC wall, proper boundary conditions have to be implemented in the FD equations.

Subsequently, all the FD equations can be combined collectively and transformed into a standard matrix eigenvalue problem, since the unknowns at a particular node are related to the unknowns at other adjacent nodes in every FD equation. The resulting eigenvalues and eigenvector are associated with the propagation constant and the unknown field components at all the nodes in the entire computation domain, respectively. The major effort involved here is the construction of the eigenmatrix, which contains the all the important information that is derived from the FD equations and boundary conditions.

The final step of the problem-solving procedure involves in the application of a non-commercial eigenmatrix solver (ARPACK), which is specialized in treating large-scale sparse-matrix eigenvalue problems. The size of the eigenmatrix directly depends on the size of the computation domain and the number of unknowns at each node. Often the computation domain and the eigenmatrix are both large in size. Consequently the latter contains a lot of zero elements, which becomes a large sparse matrix. As a result, a large grid size in the computation domain can be used to analyze more complicated structures and yield more accurate results.

2.2 Definition of Computation Domain

In our waveguide-based spatial power combining circuits, as briefly introduced in the previous chapter, a tapered slot antenna array is made up of sections of finline array with varying slot width. In order to minimize the return loss and insertion loss of the tapered slot antennas, optimization in the taper shape is required but can not be realized
without knowing the propagation characteristics of the finline structure, which can be analyzed by using FDFD techniques.

Figure 2-2: Cross section of a 2x2 finline array and the corresponding computation domain for FDFD analysis.

To show how a typical computation domain is defined in FDFD analysis, a 2x2 finline array is used here as an example, as shown in Figure 2-2. Only two dissimilar media exist in the structure, including air and dielectric slabs, which correspond to the aluminum nitride substrates. Metal strips are shown on one side of the dielectric slabs. Three important tasks required to set up a computation domain are (1) looking for symmetry so as to reduce domain size whenever possible, (2) defining boundary property and (3) indexing mesh points. Since the desired propagation mode is quasi-TE, the profile of the tangential E field is illustrated accordingly in the plot. Due to the symmetry possessed by the field profile and the geometrical structure, the computation domain can be greatly reduced and only one quarter of the original structure is necessary, with the introduction of two artificial conducting walls. Consequently, the boundary property of the new computation domain can be determined, including three PEC walls (two for the actual
waveguide walls) and one PMC wall. A grid of nodes can be set up according to the new structure, in a way that there are nodes right on the boundary, air-dielectric interface and edges of the metal strips on the dielectric substrates. Either uniform or non-uniform grid approach can be used, depending on applications. In this particular case, where the slots and dielectric slabs are relatively small, a non-uniform grid is used for more accurate results. Each node is assigned with an index number, as shown in Figure 2-3.

![Diagram of a grid of nodes](image)

Figure 2-3: Illustration of a computation domain consisting of a two-dimensional grid of nodes, where each node is labeled with an index number.

### 2.3 Finite Difference Equations

#### 2.3.1 Governing Differential Equations

For a wave-guiding structure with a uniform cross section, the transverse field components $E_x$, $E_y$, $H_x$ and $H_y$ can be expressed in terms of the longitudinal field components $E_z$ and $H_z$ [10]. As a result, all of the field components can be derived by solving the homogeneous scalar Helmholtz's equations for $E_z$ and $H_z$. Further simplification can be made if the guided wave operates in a TE mode, in which the longitudinal electric field does not exist ($E_z = 0$) and only the longitudinal magnetic field
component $H_z$ needs to be solved. For TM mode operation, $H_z = 0$ and $E_z$ is the unknown to be solved.

In this thesis work, the wave-guiding structure of interest are the finline arrays. A longitudinal electric field component must exist, but it is much smaller than the other transverse components; therefore, the dominant mode for a finline structure is quasi-TE by nature. To simplify the mathematical formulation, TE-mode operation is assumed in the analysis of the dispersion characteristics of finline structures. Therefore, only one unknown ($H_z$) at each nodal point in the computation domain is required in constructing the finite-difference equations.

In a source-free loss-less medium, the homogeneous scalar Helmholtz’s equation [10] is written as

$$\nabla^2 \Phi + k^2 \Phi = 0$$  \hspace{1cm} (2.1)

where $k$ is the wave number in the medium, $k^2 = \omega^2 \mu \varepsilon = (\omega / \nu)^2$ and $\Phi$ represents the longitudinal magnetic field component $H_z$. Assume that a wave-guiding structure, which consists of isotropic, source-free and loss-less dielectric media, is uniform in the propagating (z) direction, equation (2.1) can be modified and rewritten as

$$\nabla^2 \Phi + k_c^2 \Phi = 0$$  \hspace{1cm} (2.2)

where $k_c^2 = k^2 - \beta^2 = \omega^2 \mu \varepsilon - \beta^2$ and $\beta$ is the propagation constant associated with the wave-guiding structure. In a rectangular coordinate system, the cross section of the wave-guiding structure lies within the $x$-$y$ plane and $\Phi$ is a function only dependent on coordinates $x$ and $y$. As a result, equation (2.2) can be further modified and rewritten as

$$\frac{\partial^2 \Phi}{\partial x^2} + \frac{\partial^2 \Phi}{\partial y^2} + k_c^2 \Phi = 0$$  \hspace{1cm} (2.3)

### 2.3.2 Generic Finite-Difference Equations

In order to solve equation (2.3) numerically, the derivatives are approximated and replaced by applying the finite-difference schemes, in this case a central-difference formula
and Taylor's expansion [12]. Consequently, the aforementioned second-order partial differential equation is transformed into a finite-difference equation. A five-point finite-difference representation [4], as illustrated in Figure 2-4, is applied during the transformation process. The graded mesh consists of in general four unequal side lengths \( n, e, s \) and \( w \) and at most two dissimilar media (represented by \( \varepsilon_1 \) and \( \varepsilon_2 \)) at node \( C \), which complies with the actual finline structures used in the spatial power combining circuits, as discussed in the previous section.

![Diagram](image)

Figure 2-4: Illustration of a graded mesh of the five-point representation used in finite-difference method.

The derivative term \( \frac{\partial^2 \Phi}{\partial x^2} \) in equation (2.3) can be approximated (with the use of central-difference formula) by the following expressions for region 1 and 2, respectively

\[
\left. \frac{\partial^2 \Phi}{\partial x^2} \right|_1 = \frac{2}{e \cdot (e + w)} \cdot \Phi_E + \frac{2}{w \cdot (e + w)} \cdot \Phi_W - \frac{2}{e \cdot w} \cdot \Phi_C 
\]  

(2.4)

\[
\left. \frac{\partial^2 \Phi}{\partial x^2} \right|_2 = \frac{2}{e \cdot (e + w)} \cdot \Phi_E + \frac{2}{w \cdot (e + w)} \cdot \Phi_W - \frac{2}{e \cdot w} \cdot \Phi_C 
\]  

(2.5)
and the $\frac{\partial^2 \Phi}{\partial y^2}$ term can be approximated (with the use of Taylor expansion\(^1\)) by the following expressions for region 1 and 2, respectively

$$\left. \frac{\partial^2 \Phi}{\partial y^2} \right|_1 = \frac{2}{n^2} \cdot \Phi_N - \frac{2}{n^2} \cdot \Phi_C - \frac{2}{n} \cdot \frac{\partial \Phi}{\partial y} \right|_1 \quad (2.6)$$

$$\left. \frac{\partial^2 \Phi}{\partial y^2} \right|_2 = \frac{2}{s^2} \cdot \Phi_N - \frac{2}{s^2} \cdot \Phi_C + \frac{2}{s} \cdot \frac{\partial \Phi}{\partial y} \right|_2 \quad (2.7)$$

Since there are two dissimilar media existing in the computation domain, the inhomogeneous cross section leads to two coupled finite-difference equations (of region 1 and 2) for the unknown $\Phi$ (or $H_2$) corresponding to the node at the interface of two dissimilar dielectrics. By applying equations (2.4), (2.5), (2.6) and (2.7) to equation (2.3), two coupled equations can be derived for region 1 and 2, respectively

$$\frac{2}{e \cdot (e + w)} \cdot \Phi_E + \frac{2}{w \cdot (e + w)} \cdot \Phi_W - \left( \frac{2}{e \cdot w} + \frac{2}{n^2} \right) \cdot \Phi_C + \frac{2}{n^2} \cdot \Phi_N$$

$$\left. -\frac{2}{n} \cdot \frac{\partial \Phi}{\partial y} \right|_1 + k_1^2 \cdot \Phi_C = 0 \quad (2.8)$$

$$\frac{2}{e \cdot (e + w)} \cdot \Phi_E + \frac{2}{w \cdot (e + w)} \cdot \Phi_W - \left( \frac{2}{e \cdot w} + \frac{2}{s^2} \right) \cdot \Phi_C + \frac{2}{s^2} \cdot \Phi_S$$

$$\left. + \frac{2}{s} \cdot \frac{\partial \Phi}{\partial y} \right|_2 + k_2^2 \cdot \Phi_C = 0 \quad (2.9)$$

---

\(^1\) The field strengths at points $N$ and $S$, are expressed in Taylor series (truncation at the second-order term): $\Phi_N = \Phi_C + n \cdot \frac{\partial \Phi}{\partial y} \right|_1 + \frac{1}{2} \cdot n^2 \cdot \frac{\partial^2 \Phi}{\partial y^2} \right|_1$ and $\Phi_S = \Phi_C - s \cdot \frac{\partial \Phi}{\partial y} \right|_2 + \frac{1}{2} \cdot s^2 \cdot \frac{\partial^2 \Phi}{\partial y^2} \right|_2$, respectively [5].

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where $k_1^2 = \omega^2 \mu_0 \varepsilon_0 \varepsilon_1 - \beta^2$ and $k_2^2 = \omega^2 \mu_0 \varepsilon_0 \varepsilon_2 - \beta^2$. Since the tangential electric field is continuous across the interface between two dissimilar materials

$$E_x|_1 = E_x|_2$$  \hspace{1cm} (2.10)

which can be further formulated as

$$k_2^2 \frac{\partial \Phi}{\partial y}|_1 = k_1^2 \frac{\partial \Phi}{\partial y}|_2$$  \hspace{1cm} (2.11)

This boundary condition, as shown in equation (2.11), is satisfactory to properly continue the finite-difference wave equation from region 1 to region 2. By applying equation (2.11) to equations (2.8) and (2.9), the terms $\frac{\partial \Phi}{\partial y}|_1$ and $\frac{\partial \Phi}{\partial y}|_2$ can both be eliminated and all three equations can be reduced to one finite-difference equation,

$$-\frac{2}{e \cdot (e + w)} \frac{n + t \cdot s}{n + s} \cdot \Phi_E - \frac{2}{w \cdot (e + w)} \frac{n + t \cdot s}{n + s} \cdot \Phi_W - \frac{2}{n \cdot (n + s)} \cdot \Phi_N$$

$$= -\frac{2 \cdot t}{s \cdot (n + s)} \cdot \Phi_S + \frac{2}{n + s} \left[ \frac{n + t \cdot s}{e \cdot w} + \frac{t}{s} + \frac{1}{n} \right] \cdot \Phi_C = k_1^2 \cdot \Phi_C$$  \hspace{1cm} (2.12)

where $t = \frac{k_1^2}{k_2^2} = \frac{\omega^2 \mu_0 \varepsilon_0 \varepsilon_1 - \beta^2}{\omega^2 \mu_0 \varepsilon_0 \varepsilon_2 - \beta^2}$. Equation (2.12) is the generic governing finite-difference equation that is applicable to every node in the computation domain.

2.3.3 Finite-Difference Equations for Nodes at Particular Locations

The aforementioned FD equation can be more specific in formulation if the location for the node of interest can be identified. A node can locate in one of the four possible locations in the computation domain as shown in Figure 2-2, which can be (1) totally in the air, (2) totally in the dielectric, (3) right at the air-dielectric interface, or (4) right at the dielectric-air interface. In the following sub-sections, equation (2-12) will be modified accordingly so that a standard format of
\[ C_E \cdot \Phi_E + C_w \cdot \Phi_w + C_N \cdot \Phi_N + C_s \cdot \Phi_s + C_C \cdot \Phi_C = k_a^2 \cdot \Phi_C \] 

(2.13)

can be applied to each of the four aforementioned cases. \( C_E, C_w, C_N, C_s \) and \( C_C \) are the coefficient constants and \( k_a^2 = \omega^2 \mu_0 \varepsilon_0 - \beta^2 \).

2.3.3.1 Finite-Difference Equation for Nodes in Air Region

\[ - \frac{2}{e \cdot (e + w)} \cdot \Phi_E - \frac{2}{w \cdot (e + w)} \cdot \Phi_w - \frac{2}{n \cdot (n + s)} \cdot \Phi_N - \frac{2}{s \cdot (n + s)} \cdot \Phi_s + \left[ \frac{2}{e \cdot w} + \frac{2}{n \cdot s} \right] \cdot \Phi_C = k_a^2 \cdot \Phi_C \] 

(2.14)

2.3.3.2 Finite-Difference Equation for Nodes in Dielectric Region

\[ - \frac{2 \cdot \tau}{e \cdot (e + w)} \cdot \Phi_E - \frac{2 \cdot \tau}{w \cdot (e + w)} \cdot \Phi_w - \frac{2 \cdot \tau}{n \cdot (n + s)} \cdot \Phi_N - \frac{2 \cdot \tau}{s \cdot (n + s)} \cdot \Phi_s + \left[ \frac{2 \cdot \tau}{e \cdot w} + \frac{2 \cdot \tau}{n \cdot s} \right] \cdot \Phi_C = k_a^2 \cdot \Phi_C \] 

(2.15)

2.3.3.3 Finite-Difference Equation for Nodes at Air-Dielectric Interface

\[ - \frac{2}{e \cdot (e + w)} \cdot \frac{n + \tau \cdot s}{n + s} \cdot \Phi_E - \frac{2}{w \cdot (e + w)} \cdot \frac{n + \tau \cdot s}{n + s} \cdot \Phi_w - \frac{2}{n \cdot (n + s)} \cdot \Phi_N \]

\[ - \frac{2 \cdot \tau}{s \cdot (n + s)} \cdot \Phi_s + \frac{2}{n + s} \cdot \left[ \frac{n + \tau \cdot s}{e \cdot w} + \frac{\tau}{s} + \frac{1}{n} \right] \cdot \Phi_C = k_a^2 \cdot \Phi_C \] 

(2.16)

2.3.3.4 Finite-Difference Equation for Nodes at Dielectric-Air Interface

\[ - \frac{2}{e \cdot (e + w)} \cdot \frac{\tau \cdot n + s}{n + s} \cdot \Phi_E - \frac{2}{w \cdot (e + w)} \cdot \frac{\tau \cdot n + s}{n + s} \cdot \Phi_w - \frac{2 \cdot \tau}{n \cdot (n + s)} \cdot \Phi_N \]
\[-\frac{2}{s \cdot (n + s)} \cdot \Phi_s + \frac{2}{n + s} \left[ \frac{\tau \cdot n + s}{e \cdot w} + \frac{1}{s} \cdot \frac{\tau}{n} \right] \cdot \Phi_C = k_a^2 \cdot \Phi_c \quad (2.17)\]

where \(\tau = \frac{k_a^2}{k_d^2} = \frac{\omega^2 \mu_0 \varepsilon_0 - \beta^2}{\omega^2 \mu_0 \varepsilon_0 \varepsilon_d - \beta^2}\) and \(\varepsilon_d\) is the dielectric constant of the substrate material.

Now that the expression for the finite-difference equation associated with any particular node in the computation domain is established. However, for the nodes located right at the electric or magnetic walls, the boundary conditions \(\partial H / \partial n = 0\) and \(H = 0\), respectively, have to be satisfied (\(\vec{n}\) represents the unit vector normal to the electric walls). As a result, modifications to the finite-difference equations have to be made accordingly.

**2.4 Matrix Eigenvalue Problems**

The relationship between the unknown field components at an arbitrary node (C) and at the adjacent nodes (E, W, N and S) is embedded in the finite-difference equation, as manifested in equation (2.13). With \(N\) nodes specified in the computation domain, there are \(N\) corresponding finite-difference equations and \(N+1\) unknowns need to be solved. The unknowns include the longitudinal magnetic field components \(H_z\) at all the nodes and the corresponding propagation constant \(\beta\), of which \(k_1^2\) and \(k_2^2\) are the implicit functions, as shown in equation (2.12). Collectively, \(N\) sets of finite-difference equations (with the modification made to comply to the boundary conditions at the electric/magnetic walls) can be transformed into a standard eigenvalue problem with the form of

\[\overline{A} \cdot \overline{\Phi} = k_a^2 \cdot \overline{\Phi} \quad (2.13)\]

where \(k_a^2 = \omega^2 \mu_0 \varepsilon_0 - \beta^2\), both of the eigenvalue \(k_a^2\) and the eigenvector \(\overline{\Phi} = [\Phi_1, \Phi_2, \ldots, \Phi_N]\) can be solved accordingly.

However, the parameter \(\tau\) shown in equations (2.15), (2.16) and (2.17) has to be tuned during the computation process. \(k_a^2\) is first solved based on \(\tau\) with an initial guess.
in value. A new $\tau$ is then calculated and updated and $k_a^2$ is solved again. The same procedure is repeated until the value of $\tau$ converges. Therefore, an iterative process is involved when solving $k_a^2$ and $\Phi$. Usually, the initial value of $\tau$ is chosen to be 0.1.

The content of the matrix $\overrightarrow{A}$ in equation (2.13) is revealed in Figure 2-5, which also illustrates the sparse characteristic of the matrix $\overrightarrow{A}$. For $N$ unknowns, the size of matrix $\overrightarrow{A}$ is $N \times N$. Each row in matrix $\overrightarrow{A}$ only possesses at most five non-zero elements, including one diagonal and four off-diagonal terms. As a result, matrix $\overrightarrow{A}$ is sparse in nature, which contains a lot of zero elements. When the number of unknowns is large, the problem as shown in equation (2.13) becomes a large-scale sparse-matrix eigenvalue problem.

$$\begin{bmatrix}
\bullet & \bullet & 0 & 0 & 0 \\
\bullet & \bullet & 0 & 0 & 0 \\
0 & \bullet & 0 & 0 & 0 \\
0 & 0 & \bullet & 0 & 0 \\
0 & 0 & 0 & \bullet & 0 \\
0 & 0 & 0 & 0 & \bullet \\
\bullet & \bullet & \bullet & \bullet & \bullet \\
\end{bmatrix}
\begin{bmatrix}
\Phi_1 \\
\Phi_2 \\
\Phi_3 \\
\Phi_4 \\
\Phi_5 \\
\Phi_6 \\
\Phi_7 \\
\end{bmatrix}
= k_a^2
\begin{bmatrix}
\bullet & \bullet & \bullet & \bullet & \bullet \\
\end{bmatrix}
\begin{bmatrix}
\Phi_1 \\
\Phi_2 \\
\Phi_3 \\
\Phi_4 \\
\Phi_5 \\
\Phi_6 \\
\Phi_7 \\
\end{bmatrix}
$$

$\bullet$...$C_C$, $\bullet$...$C_N$, $\bullet$...$C_S$, $\bullet$...$C_E$, $\bigcirc$...$C_W$

Figure 2-5: Illustration of the large sparse-matrix eigenvalue problem.

For example, if a $50 \times 50$ mesh is used in the computation domain, the corresponding number of unknowns is $(50+1) \times (50+1)$, or 2,601. Therefore, the size of the matrix $\overrightarrow{A}$ will be $2,601 \times 2,601$, which consists of 6,765,201 elements. Assume that each row of matrix $\overrightarrow{A}$ has 5 non-zero elements, there will be $(2601-5) \times 2601$, or 6,752,196 zero element in matrix $\overrightarrow{A}$, which is about 99.8% of the total matrix elements.
2.5 Solution to Large-Scale Sparse-Matrix Problems

Iterative methods, such as Jacobi, Gauss-Seidel and successive over-relaxation (SOR), have been used to solve a large-scale matrix eigenvalue problems, in which a first approximation is used to calculate a second approximation, and so on. [12]. Although the iterative methods are limited in their usefulness because they require a large computer memory, these methods have been applied to simple structures [9, 11, 12]. Convergence problems such as non-convergence and slow convergence have been reported [8], especially when the matrices are neither symmetric nor diagonally dominant. Alternatively, direct methods are applied and triangularization is involved in the problem-solving process [8]. Although straightforward, the direct methods require the storage of the all the corresponding matrices and, therefore, are usually restricted to limited number of nodes in the computation domain if the size of computer memory is limited.

Commercial software and free shareware, such as MATLAB, EISPACK and LAPACK, are available for solving standard eigenvalue problems. However, they are not suitable for solving large-scale eigenvalue problems as described in this thesis work. Fortunately, a computer program, ARPACK\(^2\), is available over Internet and is extremely powerful in attacking large-scale sparse-matrix eigenvalue problems. ARPACK is a collection of Fortran 77 subroutines, which was designed to compute a few eigenvalues and the corresponding eigenvectors of a general \(N \times N\) matrix \(A\).

The template of a particular driver (dnrv1.f) in ARPACK has been modified. A FDFD code was then developed for solving the eigenvalue problems, as the one shown in equation (2.13), with an \(N \times N\) matrix \(A\). Matrix \(A\) is banded, which is a direct consequence of properly indexing the grid of nodes. Matrix \(A\) is also non-symmetric, due to the nature of non-uniform grid and the implementation of boundary conditions. The modification made to the driver template has mainly been the construction of matrix \(A\).

\(^2\) ARPACK has been developed by the researchers at the Department of Computational & Applied Mathematics at Rice University, Houston, TX 77251, USA. The software is free and can be downloaded from Internet via http://www.caam.rice.edu/software/ARPACK.
which is derived from the finite-difference equations and stored in a compact matrix format (LAPACK format), particularly devised for storing large sparse matrices. The desired number of eigenvalues can be specified in the FDFD code and particular types of eigenvalues can be computed, with the choices such as largest real value (LR), largest magnitude (LM), smallest real value (SR), and smallest magnitude (SM).

2.6 Design Example I – Rectangular Waveguide

An air-filled homogeneous X-band rectangular waveguide was used as an example to verify the validity of the FDFD code. As shown in Figure 2-6, the waveguide has a 10.16 mm × 22.86 mm (0.4 in. × 0.9 in.) cross section. Based on the prior knowledge of the electric field orientation for the dominant TE_{10} mode, two fictitious symmetry walls (one PEC and one PMC) were used so that only one quarter of the actual waveguide cross section was analyzed. The operating frequency was arbitrarily chosen to be 55 GHz and a uniform 50 × 50 grid were used in this particular case. The simulation time was only about 10 seconds on a HP 9000 Unix workstation, thanks to the powerful capability provided by ARPACK.

Figure 2-6: A standard X-band rectangular waveguide.

The eigenvalue to be solved is $k_a^2$ and for a rectangular waveguide, it has a analytical expression [10] and its value for the dominant TE_{10} mode can be calculated.
\[ k_a^2 = \left( \frac{n \cdot \pi}{L_y} \right)^2 = \left( \frac{1 \cdot \pi}{22.86 \times 10^{-3}} \right)^2 = 1.8886 \times 10^4 \text{ (rad / m)}^2 \] (2.14)

where \( n \) and \( L_y \) represent the mode number and dimension of the waveguide opening in the \( y \) direction.

The computed value for \( k_a^2 \) was \( 1.8884 \times 10^4 \text{ (rad / m)}^2 \) and the field distribution of \( E_x \) for the dominant mode across the entire waveguide cross section is shown in Figure 2-7. These simulation results agree very well with the analytical results and therefore present a confidence check on the FDFD code.

![Figure 2-7: The field distribution of \( E_x \) for the dominant TE\(_{10} \) mode in a rectangular waveguide.](image)

2.7 Design Example II – Single-Sided 2×2 Finline Array

FDFD Analysis has been performed for unilateral finline arrays, which is the building block of the spatial power combining circuits. The configuration of a 2×2 finline array, as shown in Figure 2-8, was studied due to its relative simple design. The rectangular boundary, which was assumed to be PEC walls, corresponds to a standard X-
band waveguide aperture, with dimensions as specified in Figure 2-5. By taking advantage of the symmetry of the tangential electrical field, only one-quarter of the actual cross section was simulated by applying two fictitious conducting walls, including a PMC and a PEC wall. Since the field was expected to be concentrated near the slots and the dielectric, 30 units of grid were allocated for both of the slot width and the thickness of the dielectric. Each side of the metal had 10 units and the air regions above and beneath the dielectric had 20 and 10 units, respectively. As a result, the total grid size for the computation domain was $60 \times 50$ (for $x$ and $y$).

![Figure 2-8: Configuration of a unilaterial 2×2 finline array.](image)

A simulation was performed, with the slot width and operating frequency set at 1000 μm and 10 GHz, respectively. The substrate thickness and the separation between two substrates are 254 μm and 4 mm, respectively. The eigenvalue and eigenvector corresponding to the dominant mode were calculated and by using a MATLAB code the post data processing was performed, from which all the field components, power density, current distribution and characteristic impedance were derived. The power density distribution across the entire cross section of the wave-guiding structure is shown in Figure
2-9, where the inset plot provides the orientation of the computation domain. It can be seen that power is highly concentrated and peaks at the slot regions. Moreover, power is much more concentrated at the metal side of the substrate, since the current only exists on the metal. The current distribution is shown in Figure 2-10, suggesting that the current peaks near the slot region and from which it gradually tapered off. It can also be seen that the current flows simultaneously in the opposite directions at the two sides of the slotline.

The dispersion characteristic of a unilaterally 2×2 finline array was computed, as shown in Figure 2-11. The corresponding gap size was 1 mm wide. A 50 × 60 grid was adopted, with 30 units allocated in the gap/slot region and dielectric region, respectively, where the field is mostly concentrated. The effective dielectric constant of the dominant mode, which is defined as

\[
\varepsilon_{r,\text{eff}} = \frac{\beta^2}{k_0^2} = \frac{\beta^2}{\omega^2 \mu_0 \varepsilon_0 - \beta^2}
\]  

(2.15)

gradually increases as the frequency increases. The rate of change in the effective dielectric constant decreases as the frequency increases, eventually to zero when the effective dielectric constant reaches a upper limit of about 1.0.

Figure 2-9: Power density distribution for a unilaterally 2×2 finline array.
Figure 2-10: Current distribution for a unilateral 2×2 finline array.

Figure 2-11: Dispersion characteristic in terms of effective dielectric constant vs. frequency for a unilateral 2 × 2 finline array with a gap size of 1000 μm.
Figure 2-11: Calculated characteristic impedance and effective dielectric constant vs. slot width for a unilaterial 2×2 finline array.

Simulations were also performed, by varying the slot width from 450 μm to 20 μm with frequency fixed at 10 GHz. The corresponding characteristic impedance was calculated, as shown in Figure 2-11, by using the power-voltage definition [13], which can be expressed by

$$Z = \frac{V_{\text{slot}}^2}{2 \cdot P}$$

(2.16)
since the power and voltage are easy to define for slotlines. $V_{\text{slot}}$ represents the slot voltage, derived by performing a line integration of electric field in the slot.

According to Figure 2-11, as the slot width decreases, the characteristic impedance and the effective dielectric constant of the finline array gradually decreases and increases, respectively, which is the typical trend observed for finline array [2]. For a 50-μm slot, the impedance is about 110 Ω. The effective dielectric constant was also computed, which is defined by the following expression,
\[ \varepsilon_{r,\text{eff}} = \frac{\beta^2}{\omega^2 \mu_0 \varepsilon_0} \]  

(2.17)

References


Chapter 3

Optimal Taper Design

One important aspect involved in the development of the spatial power combining circuits discussed in this thesis work is the requirement for broadband characteristics. Although a wide-band property may not be necessary for some system planners and wireless architects, it does extend the flexibility for the circuit designers should the passive combiner structure provide such a feature. Power amplifiers based on different device technology and operating frequency can then be chosen with great flexibility but with much less concern about the frequency limitation imposed by the combiner circuits. A design procedure for optimal tapers was established by extending and applying the Klopfenstein taper design to non-TEM wave-guiding structures. The corresponding design theory, which is based on the well-known theory of small reflections, will also be discussed. Several design examples will be examined and validated by measurement results. As will be shown in this chapter, the optimization in the passive combiner structure is the stepping stone to an excellent combiner performance, mainly due to the improvement in combining efficiency.

3.1 Design Problems

In general, a spatial power combining circuit is implemented by integrating the power amplifiers with input/output antenna arrays, which distribute and combine power, in free space, to and from all the active elements. Tapered slot antenna arrays are appealing to combiner designers mainly due to their broadband characteristics. Optimization in the taper shape is possible and can result in minimization of return loss over a frequency range of interest, which will directly enhance combiner efficiency. From a different point of view, in terms of circuit terminology, a broadband impedance transformer that transforms
the impedance from free space to 50 Ω at the MMIC input is realized via the optimization process. However, the fact that finline is a non-TEM wave-guiding structure complicates the design problem, particularly in the optimization of tapered slot antenna arrays.

The design problem of interest is shown in Figure 3-1, where two input antennas along with two MMIC amplifiers are present and are part of a 4×2 combiner circuit. The goal of the design problem is to optimize the shape of the tapered slot so that return loss is greater than a designated level, i.e. 20 dB, over a frequency band of interest. The input gap size is determined by the waveguide opening and the number of antennas that fit in the waveguide. In this case, there are two antennas and the waveguide opening is 0.4 inch. As a result, the input gap size is 0.2 inch. The output gap size is determined by the impedance value required at the input of the MMIC amplifier.

Figure 3-1: Design problem – the optimization of finline arrays used in power combining circuits.

3.2 Optimal Taper for TEM Structures

Quarter-wavelength transformers are very popular in microwave circuit design in that it provides a simple and efficient way to achieve impedance transformation at a
particular frequency. However, a single quarter-wavelength transformer has narrow bandwidth of about 10 – 15 %. The use of a multi-section impedance can extend bandwidth and better performance can be achieved as the number of section increases. In the limit of an infinite number of sections, a gradual impedance taper is realized, which has a lower frequency cutoff set by its length, but no upper frequency cutoff.

3.2.1 Theory of Small Reflections

The well-known theory of small reflections [1] states that the reflection coefficient of a gradual impedance taper, as shown in Figure 3-2, can be determined and expressed as

\[ \Gamma(\theta) = \frac{1}{2} \left( \frac{Z}{Z_0} \right) \left( \frac{d}{dz} \ln \left( \frac{Z}{Z_0} \right) \right) \cdot dz \]  

(3.1)

where \( Z_0 \) represents the reference impedance at the input end of the taper upon which the reflection coefficient is defined, \( z \) is the position along the taper, \( L \) is the taper length, \( \theta \) stands for the round-trip phase delay from position 0 to \( z \) and \( \theta = \int_0^z 2\beta \cdot dz' \). In another words, if the impedance value at each point along the taper can be specified, the reflection coefficient can be determined based on equation (3.1).

![Figure 3-2: A gradual impedance taper structure.](image)

3.2.2 Klopfenstein Taper

In 1956, Klopfenstein was able to invert equation (3.1) so that an optimized impedance taper for TEM wave-guiding structures can be designed so that the reflection
coefficient for the taper structure is minimized in the passband [2]. With pre-designated minimum reflection coefficient in the passband $\Gamma_m$, taper length $L$, input impedance $Z_0$ and output impedance $Z_L$, the logarithm of the characteristic impedance variation for the Klopfenstein taper is given by

$$\ln\left(\frac{Z(z)}{Z_0}\right) = \frac{1}{2} \ln\left(\frac{Z_L}{Z_0}\right) + \Gamma_m A^2 \phi\left(\frac{2z}{L} - 1, A\right)$$

(3.2.1)

where

$$\Gamma_0 = \frac{1}{2} \ln\left(\frac{Z_L}{Z_0}\right)$$

(3.2.2)

$$A = \cosh^{-1}\left(\frac{\Gamma_0}{\Gamma_m}\right)$$

(3.2.3)

$$\phi(x, A) = -\phi(-x, A) = \int_0^x \frac{I_1(A\sqrt{1-y^2})}{A\sqrt{1-y^2}} \cdot dy$$

(3.2.4)

$I_1(x)$ is the modified Bessel function of the first kind and first order and the passband is defined as $\beta L \geq A$. The resulting reflection coefficient is given by

$$\Gamma(\theta) = \Gamma_0 e^{-j\beta L} \frac{\cos \sqrt{(\beta L)^2 - A^2}}{\cosh A}, \text{ for } \beta L > A$$

(3.3)

A few observations can be made for the Klopfenstein taper design. There is a lower-end cutoff frequency at the passband, as implicitly defined in the relationship of $\beta L \geq A$, while no upper-end cutoff frequency exists. The cutoff frequency decreases when either the taper length increases, which may not be desired for microwave circuit design, or the value of factor $A$ decreases. As illustrated in equations (3.2.2) and (3.2.3), the larger the ratio of impedance transformation $Z_L / Z_0$ and the smaller the minimum reflection coefficient $\Gamma_m$, the higher the cutoff frequency $f_c$ since the factor $A$ becomes larger. These factors, including impedance tranformation ratio $Z_L / Z_0$, taper length $L$, minimum
reflection coefficient $\Gamma_m$ and cutoff frequency $f_c$, in general act against each other; therefore, one factor may have to compromise in order to achieve the other for certain desired performance.

3.2.3 Design Example – A Broadband 100Ω-to-50Ω Impedance Transformer

A continuous microstrip taper was designed to verify the concept of Klopfenstein taper. The design goal is to devise a broadband impedance transformer to match a 100Ω load to a 50Ω source with a reflection coefficient better than 20 dB in the passband, with a cutoff frequency of 1GHz. By following the aforementioned design equations, a microstrip taper was designed and constructed with twenty sections. The total length of the tapered line was chosen to be 5 cm, since a commercial 2"×2" aluminum nitride substrate was used to realize the circuit.

A simple Mathematica code was written to calculate the characteristic impedance for each section of the microstrip taper, with all the design criteria satisfied. A look-up table relating the impedance value and microstrip width was set up and incorporated in the code. As a result, the corresponding widths for the tapered line sections can be interpolated and extracted from the table. The calculated values of the tapered line widths were rounded up to the closest even integers, due to the constraint of the minimum tolerance supported by the mask manufacturer. Simulations using EEsof were performed to compute the reflection coefficient of the twenty-section tapered line, which was terminated with a 100Ω load.

Several microstrip tapers were fabricated by using a 10-mil thick aluminum nitride substrate with about 3.8-μm gold layer on top and a relative dielectric constant of 8.6. Undesired lateral etch occurred during the etching process; moreover, non-uniform etching across substrate was observed, due to the large size of the substrate. However, the lateral etch is about 5μm from prior experience and the value was taken into consideration when designing the mask. 100Ω chip resistors were used as terminations and epoxy-attached to the substrate, with 1-mil bondwires used as interconnection between the taper line and the 100Ω load.
A return loss (S11) measurement was performed with the circuit mounted onto a universal test fixture. The measurement result (in dotted line) is shown in Figure 3-3, along with the simulation result (in solid line). The return loss is greater than 22dB throughout the whole frequency band, ranging from 0.5 to 10.5GHz, and the cutoff frequency is below 1GHz. The result shows that not only the design goal was successfully achieved, but also pretty good agreement exists between the simulation and measurement results as well.

![Return Loss Graph](image)

Figure 3-3: Comparison between simulation and measurement results of a microstrip taper designed for a 100Ω-to-50Ω impedance transformation.

### 3.3 Optimal Taper for Non-TEM Structures

Although powerful in designing broadband impedance transformers, Klopfenstein taper was proposed with intended applications in TEM wave-guiding structures, where the propagation constant $\beta$ is non-dispersive and the characteristic impedance is well defined. For non-TEM structures such as finlines, modifications have to be made in order to make
use of the concept of Klopfenstein taper, since the corresponding relationship between characteristic impedance and gap size usually is not available. However, the concept of Klopfenstein taper can be extended and applied to non-TEM structures, by using wave impedance instead of characteristic impedance.

For non-TEM wave-guiding structure, the design equations in (3.2) are rewritten as the following

\[
\ln \left( \frac{Z(\theta)}{Z_0} \right) = \frac{1}{2} \ln \left( \frac{Z_L}{Z_0} \right) + \Gamma_n A^2 \phi \left( \frac{2\theta}{\theta} - 1, A \right) \tag{3.4.1}
\]

where

\[
\theta(f, z) = \int_0^z 2\beta(f, z') \, dz' \tag{3.4.1}
\]

is the round-trip phase delay to a point \( z \) along the taper and \( \theta_i = \theta(f, L) \). \( Z(\theta) \) represents the wave impedance at certain point \( z \) along the non-TEM taper structure, at which point \( \theta \) and \( z \) are related via equation (3.4.1). In non-TEM structure, the propagation constant \( \beta \) becomes dispersive and the round-trip phase delay \( \theta \) is no longer a linear function of \( \beta \) and \( z \).

Since the dominant mode for finline is quasi-TE in nature, the following relationship can be approximately assumed between wave impedance and propagation constant

\[
Z = \frac{\omega \mu}{\beta} \tag{3.5}
\]

Equation (3.4.1) can now be rewritten in term of \( \beta \) as follows

\[
\beta(f, z) = \sqrt{\beta_L \beta_0} \exp \left[ -\Gamma_n A^2 \phi \left( \frac{2\theta(f, z)}{\theta} - 1, A \right) \right] \tag{3.6}
\]

where \( \beta, \beta_L \) and \( \beta_0 \) correspond to \( Z, Z_L \) and \( Z_0 \), respectively.

With the prior knowledge of the relationship between the propagation constant and the geometrical parameters of the finline, most importantly the slot width, an optimized
taper structure in finline can be derived based on equation (3.6). However, the evaluation of the propagation constant at each point along the taper structure involves an iterative process, because $\beta$ and $\theta$ are mutually related as revealed in equations (3.4.1) and (3.6).

![Diagram showing taper structure and phase delay](image)

Figure 3-4: A taper is divided into N sections so as to estimate the round-trip phase delay $\theta$ by approximation.

Consequently, the taper structure is first divided into N sections of length $\Delta z = L / N$, as shown in Figure 3-4, and $\theta$ can be estimated by

$$
\theta(z_i) = \sum_{k=0}^{i-1} 2\beta(z_k) \Delta z = \theta(z_{i-1}) + 2\beta(z_{i-1}) \Delta z
$$

(3.7)

where $N$ has to be large enough to ensure good approximation.

With an initial guess of $\theta_i$ and $\theta(z_0) = 0$, $\beta(z_0)$ can be calculated from equation (3.6). Subsequently, $\theta(z_i)$ can be determined from equation (3.7) based on the knowledge of $\theta(z_0)$ and $\beta(z_0)$. By repeating the same process, all the values of $\theta(z_i)$ and $\beta(z_i)$ with $i = 1$ to $N$ can be computed. Then $\theta_i$ can be re-evaluated and updated via equation (3.4.1), so that a new set of $\theta$ and $\beta$ can be calculated. The iterative process continues until the solution set of $\beta$ converges and the shape of the optimal taper can subsequently determined.

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3.4 Optimized 2×2 Finline Arrays

A 2×2 finline array, as shown in Figure 3-5, was designed to verify the concept of non-TEM optimal taper. Physically it corresponds to two 10-mil thick aluminum nitride substrates, with a separation of c = 5 mm, placed in an X-band (WR-90) waveguide (a = 0.9 in., b = 0.4 in.). Symmetries along the major axes were used to minimize the size of computation domain. With the normalized gap (2g/b) as a variable, the corresponding effective dielectric constant, \((\beta / k_0)^2\), was computed by using Spectral Domain Method (SDM) at various frequencies, and a family of curves are shown in Fig. 3-6. Based on this information, an optimal tapered finline array was designed and a profile of normalized gap width vs. position along the taper line was computed and shown in Figure 3-7.

The characteristic impedance at each end of a taper line was calculated, with approximation, based on Hoffmann’s formula [3] for double-strip coplanar waveguide with infinitely wide ground conductors. A different physical taper is required for each different frequency due to the frequency dependence of the propagation constant, which is obviously impossible to implement. Therefore, the center frequency at the band of interest was chosen to be the operating frequency.

![Diagram](image)

Figure 3-5: The cross section of a 2×2 finline array in a standard X-band waveguide environment.
Figure 3-6: Effective dielectric constant vs. normalized slot width at various frequencies for a 2x2 finline array.

Figure 3-7: The shape of the optimized taper structure for a 2x2 finline array.
Figure 3-8: The optimized finline tapers terminated with chip resistors as terminations.

Figure 3-9: Comparison between measurement and simulation results for optimized taper structure for a 2×2 finline array.
An optimal tapered finline array was fabricated on 10-mil thick aluminum nitride substrates. Multi-section tapers were used to realize the ideal continuous tapers. The taper length was chosen to be 17.5mm and 50 sections (350μm each) were used for each taper. All the tapered finlines were terminated with 100Ω single wrap-around chip resistors by using 1-mil gold wires, as shown in Figure 3-8. Measurement was performed for a 2×2 finline array with the use of HP 11644A X-band waveguide calibration kits. The measured results, as shown in Figure 3-9, agree very well with the simulation result. A return loss better than 19dB was observed within the entire frequency band from 7.5 to 12.5 GHz, suggesting a very broadband characteristic which was a direct result of the optimal taper structure.

![Graph](image)

Figure 3-10: Measurement results for the optimized taper structure for a 2×2 finline array, terminated with various chip resistors.

It should be noted that good agreement occurred when 100Ω chip resistors were used as matched terminations. As shown in Figure 3-10, several measurements were performed for the finline arrays terminated with chip resistors with different values,
ranging from 30Ω to 100Ω, with 100Ω yielding the best return loss, suggesting that the slotline dimensions at the end of the taper yielded a characteristic impedance close to 100Ω. This is related to an uncertainty in the characteristic impedance of the slotline. There is very little accurate design information for slotline, and our system is further complicated by the proximity of the cards to each other and the surrounding metallic waveguide walls. The optimal taper theory can be used to compute an optimum transition from the waveguide mode to some target slotline width, but does not actually tell what that slotline width should be. The theoretical curve in Figure 3-9 merely assumes that the transition has been terminated with a matched load, whatever that may be. A slot dimension was chosen based on a formula in [3] to achieve a 50-Ω impedance, but the experiments confirmed that the transition ends in a 100-Ω impedance.

Since the experimental results suggest that the characteristic impedance at the narrow end of the taper structure is 100Ω instead of 50Ω, an additional microstrip taper was designed and incorporated into the existing circuitry to serve as a 100-to-50 Ω impedance transformer, as shown in Figure 3-11.

![Diagram](image)

Figure 3-11: An extra microstrip taper is inserted between the taper slot antenna and the termination (MMIC) to serve as impedance transformer.
Return loss measurements were performed for performance verification, with the optimized $2 \times 2$ finline array and the $100\Omega$-to-$50\Omega$ microstrip transformer terminated with $50\Omega$ chip resistor. The measured return loss, as shown in Figure 3-12, is better than 15 dB for the entire waveguide band, which was sufficiently close to the design goal for this work. It is worth noting that theoretically there is no upper limit for the bandwidth of the gradual taper, and as a result the bandwidth is currently limited by the waveguide and the active elements.

![Return loss measurement graph](image)

**Figure 3-12:** Return loss measurements for an optimized $2 \times 2$ finline array, with the end of microstrip taper terminated with $50\Omega$ chip resistor.

These results suggest that the concept of Klopfenstein taper has been successfully extended and applied to optimal design of finline arrays, which are non-TEM waveguiding structure. The results of return loss measurements show very good agreement with the simulation results, presenting broadband frequency response and excellent return loss characteristics.
References

Chapter 4

Combining Circuit Design

During the development of a broadband combiner circuit capable of high power output at X-band, several important issues have been carefully addressed and incorporated into the design procedure, which will be covered in this chapter. Besides the challenge of achieving the program goal of >100-Watt power output, much effort has been devoted to solve the technical problems that plagued a previous version of combiner circuit, which not only had limited power performance but also presented a low-yield problem as well. The performance of the passive combiner structure will be evaluated, along with the fabrication procedure discussed in details. Also examined were the influences on combiner performance resulting from the bondwire parasitics, non-uniform field illumination, groove and side-wall effects.

4.1 Circuit Concept

Alexanian and York originally proposed the “first generation” of the waveguide-based spatial power combiners [1,2], from which the new combiner system was derived. The combiner circuit consisted of a two-dimensional array of active antennas, where broadband tapered slot antennas were wire-bonded with high-power MMIC amplifiers via a slotline-to-microstrip transition, as shown in Fig. 4-1. A 4×2 active antenna array was constructed in a rectangular waveguide environment, which guided the incoming and outgoing waves with exceptionally low loss and provided a natural heat-sinking reservoir. The energy of the input and output signals had the spatial distribution corresponding to a dominant waveguide (TE_{10}) mode, which was distributed and collected from a dense array of amplifiers.
The actual circuit setup of the "first-generation" waveguide-based spatial combiner is shown in Fig. 4-2. Ten-mil thick aluminum nitride (AlN) substrates, which have high thermal conductivity, with single-sided metallization were used to realize the planar antenna structure and carry MMIC amplifiers. The patterns of tapered slot antenna were photo-etched on the metallization layer by using the standard photolithography processes and two MMIC power amplifiers were mounted on each aluminum nitride substrate with the use of conducting epoxy. Each antenna card was machined so that the input and output ends fitted into the openings of waveguide adapters and held in position after being clamped between two I-shaped metal bars made of aluminum.

With this particular setup, a maximum 20-Watt CW result has been achieved [3], with corresponding gain and combining efficiency of 9 dB and 50%, respectively. Eight GaAs MMIC power amplifier (Texas Instruments TGA8286-EEU) were used, each with 5-Watt output power and 37% power-added efficiency at 2 to 3-dB gain compression. No thermally induced degradation in output power was observed during the measurements, indicating acceptable heat-sinking property of the combiner. Although this combiner circuit presented an extraordinary 50% increase in term of power level, advancing from 10 to 20 Watts, a great deal of improvement could be made with an effort to achieve higher
performance, mainly in terms of output power capacity, combining efficiency, thermal management and manufacturing yield.

![Diagram of X-Band waveguides, Grooves, Array, and Heat sink](image)

Figure 4-2: The circuit setup for the “first-generation” waveguide-based spatial power combining circuit.

### 4.2 Focuses for New Combiner Design

Several problems have been observed in the aforementioned “first-generation” combiner circuit, which limited the circuit performance and functionality. First of all, the fabrication of antenna cards required a laborious and time-consuming grinding/machining process, resulting in a low-yield problem due to the recurring card breakage. Secondly, since the antenna cards were machined to fit exactly into the waveguide openings and make good contact with the waveguide walls, card breakage frequently occurred during measurements with slight movement of the waveguides, especially if the waveguide adapters were not initially in good alignment with the antenna cards. Moreover, the penetration depth of antenna cards into the waveguide adapters was found to greatly affect the combiner performance; however, this phenomenon could not be quantified because it was difficult to properly model this particular combiner structure.
For the implementation of high-power spatial combiners, where the output power is at the level of tens or hundreds of Watts, several important issues have to be incorporated into the design of combining circuits to achieve desired performance. When dealing with a large number of solid-state high-power devices, thermal management is extremely important since device performance degrades drastically if waste heat can not be removed efficiently. In addition, the combiner must be compact but large enough (physically and thermally) to accommodate the desired number of MMIC amplifiers. Minimizing output combiner losses is also critical as far as combiner efficiency is concerned. A well-designed combiner should ideally exhibit broadband characteristics, i.e. a frequency independent 50Ω environment, so that the performance of the individual (isolated) MMIC amplifiers can be retained and the combiner system is also device independent.

4.3 Circuit Topology for New Combiner Design

4.3.1 40-Watt Combiner System Based on 4×2 Arrays

A new design of a spatial power combiner targeted at 40 Watts based on a 4×2 active antenna array is shown in Figure 4-3, with three major objectives including high-power capability, good thermal property and broadband characteristics. The test fixture adopted a modular tray architecture with four identical “trays” and each tray was mounted with active devices and antennas. By increasing the number of trays and amplifiers per tray, the power capacity of the combiner can be greatly increased. With the MMIC amplifiers attached directly on to the test fixture, the thermal resistance underneath the MMIC is minimized, resulting in an excellent thermal property for the combiner. Tapered slot antennas can be used and incorporated in the test fixture, which renders the combiner with a broadband characteristic.

An active antenna array was constructed in a waveguide environment with standard waveguide openings, after the trays and the top/bottom covers were stacked and bolted together, as shown in the top figure of Figure 4-3. Alignment pins were used to hold the fixture in exact position, which avoided the previous card breakage problem.
resulting from misalignment of antenna cards. The prototype design was constructed from aluminum for ease of fabrication, however copper is preferred due to its lower thermal resistance.

![Diagram of test fixture]

**Figure 4-3**: The top figure shows a schematic plot of the test fixture. Bottom figure depicts the layout on a single tray.

The circuit layout on a single tray is shown with details in the bottom figure of Figure 4-3. Two tapered slot antennas were mounted on a "H"-shaped tray (see also Figure 4-8), both at input and output, and rested in grooved channels so that the antenna surface was flush with the tray surface. The MMICs, the associated RF feed and DC bias circuitry were mounted directly onto the metal crossbar of the tray. Bondwires were used to make connections between antennas and MMIC amplifiers, resulting in a crude but effective slotline-to-microstrip transition. At each side of the test fixture there were
notched openings on each tray which allow for distribution of DC bias to the MMIC amplifiers from an external power supply. The completely enclosed structure not only eliminates radiation loss in the system but also provides a well-defined boundary value problem for analysis, enabling more accurate modeling of the antenna/wave-guiding structure.

The commercially available MMIC GaAs power amplifiers (Texas Instruments TGA9083-EEU) used in this work were individually attached to a heat-spreader by the manufacturer using vacuum-reflow eutectic soldering techniques. Subsequently, the MMICs could be easily attached directly onto the test fixture with the use of conducting silver epoxy. As a result, the thermal resistance between the MMIC amplifiers and the test fixture was minimized, creating an efficient thermal path for waste heat removal.

![Diagram with labels](image)

Figure 4-4: Shape of the taper slot antenna structure has to be determined to minimize return loss and provide proper impedance transformation between MMIC amplifiers and the waveguide.

Tapered slot antennas are broadband in nature and therefore attractive for this combiner system. Ten-mil thick aluminum nitride (AlN) substrates with single-sided
metallization were used to realize the antennas. By using standard photolithographic processes, the antenna pattern was defined and etched in a 3.4-μm-thick gold layer. Aluminum nitride substrate was initially chosen due to its high thermal conductivity, which was a desired feature in the "first-generation" power combiner circuits where the MMIC amplifiers were mounted directly on to aluminum nitride substrates. Although other inexpensive substrates with lower dielectric constants could be used in the new combiner design, aluminum nitride substrates were still used because of the switching barriers such as existing design information and established process flow.

![Diagram of circuit layout](image)

Figure 4-5: Overview of the circuit layout on a single tray for the 40-Watt system.

As shown in Figure 4-4, the taper shape of the finline structure was optimized to minimize the return loss and, therefore, increase the combining efficiency. Ideally, an optimized tapered finline structure is desired to provide a broadband impedance transformation from the waveguide to MMIC amplifiers, which were internally matched to a 50-Ω environment. However, it was practically impossible to realize a finline array with the slot size that corresponded to a characteristic impedance of 50Ω, as explained in Chapter 3. It turned out that for the chosen slot size (of 52 μm) at the MMIC end, the
corresponding characteristic impedance was about 100 Ω. As a result, another microstrip taper structure was used to provide a broadband impedance transformation, from 100 Ω to 50 Ω, as shown in Figure 4-4. A photo of a single tray with two MMIC amplifiers is shown in Figure 4-5.

4.3.2 100-Watt Combiner System Based on 6×4 Arrays

One unique feature of the aforementioned new combiner design is that more MMIC amplifiers can be laterally added to the space adjacent to the existing amplifiers, increasing the number of devices per tray. In addition, the number of trays could also be increased so that more active element can be integrated into the combiner circuit, resulting in a larger array. With the success witnessed in the 40-Watt combiner system, another combiner system aiming at 100-Watt output power was made based on a larger, 6×4 array, as illustrated in Figure 4-6.

Four input/output antennas and MMIC amplifiers were used on each tray. For convenience, the antenna design in the 40-Watt system was scaled and applied to the 100-Watt system, with the slot width along the taper halved in value. The resulting slot size (at the MMIC end) was 26 μm, of which the corresponding characteristic impedance was experimentally verified to be 70 Ω. Therefore, a tapered microstrip transformer was used to achieve a broadband impedance transformation from 70 Ω to 50 Ω. The shape of the microstrip taper was meander so as to equalize the electrical lengths among different channels since the MMIC amplifiers were spread out to a distance wider than the width of the waveguide opening. The top view of the circuit layout of a single tray was shown in Figure 4-7.

In order to increase the number of trays and in the mean time keep the size of the overall array the same, the tray thickness was reduced to 4 mm, which was two third of the original thickness as in the 40-Watt system. Consequently, all the active elements were clustered towards the center of waveguide, which was an attempt to minimize the effect of non-uniform illumination. Since the total tray thickness remained unchanged, the waveguide openings still corresponded to a standard X-band waveguide (WR-90) environment. It is worth mentioning that the size of the active antenna arrays can keep on
increasing, while an oversize waveguide environment may be needed. Figure 4-8 shows
the assembled 100-Watt system mounted on an air-cooled heat sink.

Figure 4-6: A new design for a larger array with four MMIC amplifiers per tray.
The rectangular boxes located around the MMIC amplifiers are the DC bias capacitors.

Figure 4-7: Top view of the circuit layout on a single tray for the 100-Watt system.
4.6 Fabrication Procedure

The spatial power combining circuits were realized by using a hybrid approach, where standard assembly procedure for the fabrication of microwave integrated circuits (MIC) was used. Since combiner performance is highly contingent on the quality of circuit assembly, in this section, technical details and practical issues involved in the fabrication procedure will be examined for potential future references. As outlined in Figure 4-9, the procedure consisted of five major steps, including photolithography, etching, dicing, die attachment, and wire-bonding, which are typically used in MIC fabrication. The performance of combiner circuits was contingent on the successful execution of the fabrication procedure.

First, a standard photolithography process was used to defined patterns on photoresist for tapered slot antennas, microstrip transformers, and DC bias pads on 10-mil aluminum nitride (AlN) substrates, supplied by Film Microelectronic Inc.. The AlN
substrate was deposited with either single- or double-sided 0.15-mil. or 3.81-µm. gold layers, on top of a thin titanium layer, which served as a diffusion barrier. Subsequently, potassium iodine (KI) and hydrogen peroxide (H₂O₂) was used to etch away the unwanted portions of gold and titanium. Since the AlN substrate was large in size (2 in. by 2 in.), sufficient stirring was essential during the etching process to minimize non-uniform etching across the substrate surface. In general, smaller substrates and/or pattern with less unwanted area achieved better uniformity in etching. Etch time for gold ranged from 3 to 10 minutes for a single run, depending on the weariness of KI etchant, which could be reused for about 50 runs. Sidewall etch was approximately 5 µm each side and had to be accounted for in the mask design process to reduce fabrication error.

Figure 4-9: The typical fabrication procedure for spatial combiner circuits.

After the pattern was defined on the gold layer of an AlN substrate, the sample was then cut into desired shapes by using an automatic dicing saw. The AlN substrate had to be mounted on a silicon wafer by using crystal wax (which melts at about 150 °C) for adhesion. The 2.050-4B-22RU7 dicing blades (from Thermocarbon Inc.) were used to dice
up AlN substrates. The dicing blades usually could endure more than 100 cuts before being replaced. The resulting cut/street was usually between 250 to 400 µm wide, depending on the type and weariness of dicing saw that was used. Upon completion, standard cleaning procedure (acetone, ISO, and DI water) was used to clean the after-cut substrates.

After the passive components (tapered slot antennas, microstrip tapers and DC biasing pads) were fabricated, they were attached onto the test fixture, along with the MMIC amplifiers and chip capacitors. Non-conducting silver epoxy (from Epotek) was used for adhesion. The microstrip taper section was first attached to the antenna section to realize the RF feed, which consisted of a slotline-to-microstrip transition, for MMIC amplifiers. Subsequently, the input and output RF feeds were mounted on the test fixture, with epoxy applied only to the bottom of microstrip taper sections. The MMIC amplifiers and the chip capacitors were tweezer-mounted on the designated locations on the test fixture, where epoxy was pre-painted.

Ultra caution was taken to prevent from using excessive epoxy, which might cause electrical shorting. The attachment of MMIC power amplifiers required uniform application of epoxy with appropriate amount, so that voids would not be formed underneath the MMICs, which might result in heat spots and cause device burnout. The epoxy was cured at 175 °C for 45 seconds on a hot plate.1

After all the components were mounted on the test fixture, bondwires with one-mil diameter were placed at proper locations to make interconnections for purposes such as RF feeds, slotline-to-microstrip transition, and DC bias setup. Figure 4-10 illustrates a typical bondwire interconnections for RF feeds and DC bypass capacitors and Figure 4-11 for slotline-to-microstrip transition. In order to minimize the parasitic inductance resulted from the bondwires, multiple bondwires and minimal loop height were intentionally used. The bondwire parasitic effects will be examined in details in section 4.7.2. As many as

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1 Shorter (longer) curing time is possible but higher (lower) curing temperature is required. Also, temperature-controlled oven can be used in stead of hot plate. In industry, it seems that longer curing time (about one hour typically) and oven are preferred for die-attachment.
260 bondwires were required on every single tray, with four MMICs per tray (for the 100-Watt system).

Figure 4-10: Bondwire interconnections for DC bypass capacitors and RF feeds (for the 40-Watt combiner system). A MMIC power amplifier is located in the center, with seven 100pF chip capacitors at various locations.

Figure 4-11: Illustration of bondwire interconnections for slotline-to-microstrip transition (for the 40-Watt combiner system), with a microstrip at the left and a slotline at the right of the photo.
4.5 Passive Antenna Arrays

In order to obtain a broadband characteristic for the combiner systems, the passive structures, including the tapered slot antennas and microstrip transformers, were optimized by properly determining the taper shapes, as described in the previous chapter. Both return loss and through measurements were performed to verify the taper design for the 40-Watt system based on 4×2 active antenna arrays.

For convenience, a return loss measurement was performed for a 2×2 passive array, which consisted of two trays with two RF feeds (tapered slot antenna and microstrip transformer) per tray. Each RF feed was terminated with a 50Ω chip resistors (instead of a MMIC amplifier), which was flip-chip-mounted and epoxy-attached in order to eliminate the bondwire connections. The bondwire parasitics was found to severely impact the performance of optimal taper design (see section 4.7.2).

![Figure 4-12: Return loss of the RF feed for a 2×2 array, designed for a 40-Watt combiner system.](image-url)
The measured return loss was better than $-15$ dB for the entire waveguide band, as shown in Figure 4-12, indicating a 40% instantaneous bandwidth centered at 10 GHz. The design work for the passive array was proven to be successful, considering the measurement result was sufficiently close to the design goal ($-20$ dB). It is worth mentioning that theoretically there is no upper limit on the bandwidth of the optimized taper structure, and therefore the combiner bandwidth is currently limited by the waveguide and MMIC amplifiers.

![Return Loss vs Frequency Graph](image)

**Figure 4-13:** Return loss of the RF feed for a 6×4 array, designed for a 100-Watt combiner system.

Another return loss measurement, as shown in Figure 4-13, was performed for a 6×4 passive array for the 100-Watt combiner system with RF feeds terminated with 50Ω chip resistors. A better than -10 dB of return loss property was observed within the entire band of interest, which was satisfactory considering the fact that the antenna design used for the 6×4 array was not optimized but scaled from the design used in the 4×2 array.
Figure 4-14: The layout of the test circuit for the through measurements.

Through measurements were performed for the 100-Watt system to examine the insertion loss characteristics. The layout of the test circuit is shown in Figure 4-14, consisting of a back-to-back configuration of splitting/combining structure (tapered slot antennas and microstrip transformers) with 50Ω microstrip lines used as through elements. The interconnections were made by using 1-mil bondwires to emulate the actual circuit setup, except the length of the bondwires between the through element and microstrip taper was actually much shorter. Two\(^2\) (4×2) and six-tray (6×4) measurements were made, as shown in Figure 4-14. The average insertion losses, represented by the solid curves, were −1.38 dB and −1.74 dB for two-tray and six-tray cases, respectively, within the frequency range from 8.2 to 12.4 GHz. The results suggested the properties of wide band and low insertion loss possessed by the 100-Watt combining system.

\(^2\) Four empty trays were used in the two-tray measurement.
Figure 4-15: Measured insertion losses for the 2x4 and 6x4 arrays based on the 100-Watt system, with 50Ω microstrip lines used as through elements. Measured radiation and conductor losses are also shown.

The solid curves in Figure 4-15 stand for the combined losses of radiation loss and conductor loss, which is defined as $|S_{11}|^2 + |S_{21}|^2$. The curves for both of the two-tray and six-tray cases were tracking each other within about 0.5 dB range, representing the best return loss that can be achieved if return loss is totally eliminated. The preceding statement is made under the assumption that the lengths of the taper structures remain fixed. The resemblance between the two solid curves also confirms that the combining efficiency is basically independent of the number of trays/active elements in the combiner system, which is an important feature of spatial power combining.

The degree of disparity between insertion loss (dotted curve) and radiation and conductor loss (solid curve) suggests the degree of impedance mismatch, where more impedance mismatch corresponds to greater disparity. Therefore, better impedance match can be observed in the two-tray case than in the six-tray case, which was a direct effect due
to the fact that the antenna structure was originally optimized for a 2×2 configuration in a 40-Watt system.

4.6 Thermal Property

Thermal management presents a tremendous challenge for the design of power amplifiers with significant output power. For combiner circuits based on the more popular tile architecture, as previously shown in Figure 1-4 (b), waste heat has to be removed from the edge of the active antenna arrays, which is very inefficient and thus more complicated heat-dissipating measures have to be employed. The combiner circuits presented in this thesis adopt a tray architecture, in which the active elements are located close to the heatsinking structure and better thermal management can be achieved. Most importantly, the MMIC amplifiers were attached directly to the metallic test fixture instead of non-metallic substrates such as ceramics; the thermal resistance between the MMICs and test fixture was greatly reduced. In addition, since the test fixture was constructed in a waveguide format, the waveguide wall provides a natural heat-sinking environment.

Figure 4-16: Thermal simulation for the 40-Watt combiner system, based on a 4×2 active antenna array.
With the use of a thermal simulator from Tanner Research, thermal simulations were performed for the combiner systems to insure that the MMICs would be operating below their rated maximum operating temperature. It was assumed that each MMIC renders 5 Watts of output power at 30% PAE, and a copper fixture with a base temperature held at 25 °C. Two simulated temperature distributions for the 40-Watt and the 100-Watt combiner systems are shown in Figures 4-16 and 4-17, respectively. The maximum temperature rise occurs beneath the MMICs on the top tray, and is approximately 60 °C, or 35 °C above ambient for the 40-Watt system and 77 °C, or 52 °C above ambient for the 100-Watt system. This is within acceptable limits for this MMIC technology, indicating an excellent thermal property of the combiner circuits, which is mainly due to the direct attachment of MMIC amplifiers to the test fixture.

![Figure 4-17: Thermal simulation for the 100-Watt combiner system, based on a 6x4 active antenna array.](image)

During power measurements, thermocouples were used and attached to various positions on the body of test fixture for temperature measurement. For the 40-Watt system, about 41 °C of temperature difference existed between the bottom surface of metal carrier right underneath the MMIC amplifiers and the base plate, which was about 25 °C.
In addition, the measured temperature at the top cover was about 45 °C for the 100-Watt system and 55°C for the 40-Watt system. These numbers agreed quite well with the simulation, suggesting that the waste heat was removed efficiently during the combiner operations.

4.7 Non-Ideal Factors and Parasitic Effects

4.7.1 Non-Uniform Illumination and Coupling Losses

Since the waveguide operates in the dominant $TE_{10}$ mode, there is a non-uniform excitation of the trays. The MMIC amplifiers that are located close to the center of the waveguide receive more incident RF power than the ones at the outer positions. This should lead to some degradation in output power for a given input power, especially when MMIC amplifiers operate at or near saturation, which adversely affects the combining efficiency and PAE. Although it was difficult to quantify this analytically without performing detailed electromagnetic analysis, a coarse calculation has been done to understand more about the impact of the non-uniform illumination on the 40-Watt combiner system. Assumptions were made so that all the MMIC amplifiers were considered identical and each could render 7 Watts of saturated power and 20 dB of linear gain. The output RF power was modeled by using the following expression [5].

$$P_{OUT,i} = P_{SAT,i} (1 - \exp\left(-\frac{P_{IN,i} G_i}{P_{SAT,i}}\right)$$  \hspace{1cm} (4.1)

where $P_{OUT,i}$, $P_{SAT,i}$, $P_{IN,i}$, and $G_i$ represent the output power, saturated power, input power and linear gain, respectively, for the $i$-th MMIC amplifier in the combiner circuit. The input power to each MMIC was estimated by assuming a $TE_{10}$ mode excitation and accounting for the location of each tray in the waveguide (see inset of Figure 4-19). The calculations based on these assumptions indicated that the two center trays jointly receive about 67 % of the total incident power, while the two outer trays jointly receive about 33 % of the total incident power.

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The total output power was calculated by summing up all the output power from each MMIC amplifier,

$$P_{OUT} = \sum_{i=1}^{8} P_{OUT,i}$$  \hspace{1cm} (4.2)

and the percentage of loss in available power, due to non-uniform illumination, was calculated, as shown in Figure 4-18, by using

$$LOSS = \frac{P_{OUT,Uniform} - P_{OUT,non-uniform}}{P_{OUT,Uniform}}$$  \hspace{1cm} (4.3)

Somewhat surprisingly, the loss peaks at only \(-3.8\%\) at \(Pin = 0.95\) Watt, suggesting that the non-uniform field distribution of the incident RF power does not seriously impact the RF power level available from the MMIC amplifiers in this particular combining structure. This is a result of clustering the cards towards the center of the waveguide.

![Figure 4-18: Losses due to mode-mismatch and non-uniform illumination.](image)

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Figure 4-19: Effect of non-uniform illumination of incident power on output power. The inset plot outlines the actual positions of the trays with each supports two MMIC amplifiers. Sinusoidal field distribution is assumed for the non-uniform case.

We also need to consider the coupling loss, caused by the mismatch between the waveguide mode profile and the output field distribution from the MMIC amplifiers. This effect is important only when the MMIC amplifiers operate in or near saturation. The coupling factor between two mode profiles can be calculated based on the following expression,

\[ \eta = \iint \phi \psi \, ds \]  

(4.4)

The output field distribution, calculated by using Equations (4.1) and (4.2), and the waveguide mode profile, shown in the inset of Figure 4-19, were represented by \( \phi \) and \( \psi \), respectively. Both of \( \phi \) and \( \psi \), were normalized and the integration was performed over the entire waveguide cross section. The estimated coupling loss was derived, as shown in
Figure 4-18, suggesting that the coupling loss increases as the incident RF power increases. The coupling loss peaks at $-1.3\%$ (Pin = 3 Watts) where all the MMIC amplifiers saturate and each outputs the same amount of power. The total loss, accounting for losses due to mode mismatch and non-uniform illumination, is about $-4.2\%$ at Pin = 1 Watt. Figure 4-19 shows the curves for available power from the MMICs and the actual power coupled to the waveguide. At Pin = 1 Watt, the available power was 46.6 Watts and the actual power was 44.6 Watts, with a loss of about 2 Watts, or 4.2% of available power.

### 4.7.2 Bondwire Parasitics

The use of bondwires enables interconnections for RF signals; however, it also introduces unwanted parasitic inductance, which may greatly degrade combiner performance. Effort has been made to model the parasitic effect so that the resulting impact could be understood and even reduced. During the return loss measurement, as presented in section 4.5.1, chip resistors were used to terminate the RF feeds. Not surprisingly, it was found that two dramatically different measurement results were obtained if the chip resistors were terminated in two different fashions, bondwire or flip-chip, as shown in Figure 4-20. On average, about 8 dB of difference in return loss was observed in the entire frequency band from 8.2 to 10.4 GHz, as shown in Figure 4-21.

![Single wrap-around chip resistors](image)

**Figure 4-20:** Circuit setup for return loss measurements. Chip resistor was used as termination with two different types of interconnections, flip-chip and wire-bonding.
Figure 4-21: Different measured return loss properties due to the effect of bondwire parasitics.

In order to quantify the parasitic inductance resulting from the bondwire, return loss measurements were performed for a test circuit, which consisted of a 100Ω-to-50Ω microstrip transformer terminated with a 50Ω chip resistor via a bondwire connection. The test circuit was mounted on a universal test fixture and one-port measurements were made by a vector network analyzer. An equivalent circuit, as shown in Figure 4-22, was used in EEsof to model the test circuit. The “round wire” model in EEsof was used to represent the bondwire. The simulation and measurement results agreed very well, also shown in Figure 4-22, suggesting that the parasitic effect can be modeled with great accuracy and incorporated in the design process.
Figure 4-22: Comparison between measurement and simulation results for the return loss characteristics of a test circuit, which is shown above the results.

References


Chapter 5

Combining Circuit Performance

Traditional circuit-based power combining approach encounters difficulties when a large array is required for high power applications. On the other hand, the spatial power combining approach, which is supposed to enjoy the major advantage of fixed loss when the array size increases, has not been able to realize significant RF power. In this chapter, the performance of the proposed waveguide-based combiner systems with various array sizes will be examined, including a 150-Watt result at X-band. The UCSB/HRL combiner systems presented not only a high-power capability but also broadband characteristics as well, thanks to the design work implemented in the test fixture and the passive antenna arrays. Important issues such as graceful degradation and oscillation problems will also be discussed.

5.1 Measurement Setup and Calibration Procedure

5.1.1 Generic Measurement Setup

Figure 5.1 shows a typical setup for power measurements. A sweeper followed by a traveling-wave tube (TWT) amplifier was used to generate RF signal with power level ranging from 5 dBm to 40 dBm. The TWT amplifier had an average gain of 50 dB at X-band with maximum output power of about 10 Watts. Attenuators were placed before the TWT amplifier so that the desired RF power level could be obtained. Two power sensors were used to monitor the power levels at the input and output ports of the device-under-test (DUT), which could be either a single MMIC amplifier or a combiner system. Three directional couplers were used to sample the RF signals and the sampled signals were readily fed to the power sensors and the spectrum analyzer, which was utilized to check for
oscillations. When power measurements were performed for MMIC amplifiers, all the couplers were microstrip-based. If a combiner circuit was the DUT, then a waveguide directional coupler was used (for coupler #2) because of its high-power handling capability. A high-power 50Ω load with 300-Watt rating was used as the load for the DUT, since power level greater than 100 Watts was expected.

![Diagram of power measurement setup]

Figure 5-1: A typical setup for power measurement.

An eight-channel power supply was used for DC biasing. Each channel was capable of supplying DC bias up to 10 Volts and 15 Amperes. The power supply also had a remote-sensing capability so that the voltage drop along each bias line could be properly compensated, providing exact bias voltage to the DUT. It is worth mentioning that the voltage drop on a bias line with a seemingly negligible resistance of 0.2Ω at 10 Amperes is
a significant 2 Volts, which corresponds to a 25% drop if 8 Volts of drain voltage is desired. The output power and power-added efficiency of the DUT will be adversely affected should this drop problem exists.

The power supply, the sweeper and the power meter were interfaced to a personal computer, on which a window-based, user-interactive computer program was developed and employed for automatic instrumentation control and data acquisition. Based on the readings from the sensors and the power supply, important data such as input/output RF power, gain and power-added efficiency could be recorded with great ease. All the components employed in the measurement setup, active or passive, were all subject to a maximum power rating for RF signals. Extreme caution had to be taken by carefully calculating the power level at every location in the setup to avoid potential instrument damage and measurement errors.

5.1.2 Power Sensors

Particular attention has been paid to the power sensors, since the input/output power level was determined based on the readings from the sensors. The power meter had to be properly calibrated before meaningful measurements could be made. The calibration data stored in the power meter tends to drift over a period of time and changes if the ambient temperature varies. As a result, the calibration procedure for power meter should be repeated whenever necessary. The accuracy of the reading from a power sensor is contingent upon two main factors: the sensor's dynamic range and sensitivity.

The received RF power has to fall within the dynamic range of power sensors, typically ranging from -30 dBm to 20 dBm, by properly setting the insertion loss and the coupling coefficients of attenuators and directional couplers, respectively, in the measurement setup. Also important, if not much more so, is the sensitivity of the power sensors. The lower the power level, the longer the settling time for a power sensor to respond. In addition, it was noticed that a few seconds elapsed before a reading appeared when the power meter was commanded to switch from one channel to the other, under the condition that both sensors received signals with sufficiently high power. Therefore, it is also very important to allow enough "delay time" before the computer fetches data from the power meter.
5.1.3 Calibration Procedure

The power levels for the RF signals presented at the input and output ports of the DUT were derived from the readings of the power sensors, based on two sets of calibration data established in a calibration procedure performed prior to power measurements. The accuracy of measured results greatly relies on the quality of the calibration procedure. When the power level is high, half a dB of measurement error in output power may cause a measured result to vary from 100 Watts (50.0 dBm) to 112 Watts (50.5 dBm), corresponding to a 12% change in output power on a linear power scale. Therefore, it is very important to obtain a good calibration before an accurate measurement can be made.

Figure 5.2 outlines the three major steps involved in the calibration procedure. Two sensors, designated as A and B, were used and a frequency sweep was performed in each step. In the step (a), the difference between the coupling end and the output end of the coupler #1 can be calculated and the first set of calibration data is generated, based on which the power at sensor B can be derived from sensor A. The setup in step (b) is the same as in step (a) except that a set of back-to-back adapters\(^1\) is added. Step (b) is meant for characterizing the insertion loss of a single adapter, assuming that the adapters are identical. In step (b), the difference between two sensors is again calculated and another data set is created. Based on the two data sets established in steps (a) and (b), the “input set of calibration data” can be derived and from which the incident RF power at DUT, as shown in Figure 5-1, can be determined from the power received at sensor A.

Now the input end of the measurement setup is “calibrated,” and the output end will be “calibrated” after step (c) is completed. The setup in step (c) is exactly the same as what in Figure 5-1 except that the DUT is removed. Once again, the difference between two sensors is calculated and the third data set is generated, from which the “output set of calibration data” can be created. With this new piece of information, the output power from DUT, as shown in Figure 5-1, can be determined based on the power received at sensor B. As a result, two (input and output) sets of calibration data are established after a

\(^{1}\) RF probes and waveguide adapters were used for MMIC and combiner measurements, respectively.
complete 3-step calibration procedure is completed. Through measurements based on the setup in step (c) should be performed at various power level to verify the quality of calibration procedure. Typically, a calibration procedure is considered good if the maximum deviation is within ± 0.02 dB, corresponding to a ± 5% of variation.

Figure 5-2: The calibration procedure for power measurement.
5.2 MMIC Characterization and Optimization

5.2.1 MMIC Screening

The MMIC amplifier (TGA9083-EEU) used in this work was commercially available from Texas Instruments (Now TriQuint-TI) and classified as an engineering evaluation unit. The MMICs were individually pre-mounted on metal carriers by manufacturer for better handling and attachment. However, the vacuum-reflow eutectic soldering process had contributed to certain device failure problems, such as cracking and electrical shorting, as witnessed in several occasions. It was also found that about 50% of MMICs survived after the soldering process. Therefore, a screening process was conducted by visually inspecting the MMICs under high-resolution microscope, attempting to eliminate the problematic MMICs before they were attached to the combiner circuits. In addition, DC-IV measurements were made to further identify the normalcy of the MMICs. These screening steps were proven very effectual to prevent the mysterious MMIC failures that occurred during previous power measurements from repeating.

5.2.2 MMIC Characterization

This particular MMIC amplifier provides a nominal 5 Watts of output power when biased at 7 Volts, 6 Watts at 8 Volts and 8 Watts at 9 Volts, covering the frequency band from 6.5 to 11 GHz. However, it was found that the MMIC amplifier became unstable and often burnout when biased at 9 Volts. The power-added efficiency (PAE) is 40% and 35% at 7 and 9 Volts, respectively. Typical small signal gain is 19 dB and, as suggested on the manufacturer's data sheet, the MMIC amplifier is recommended to operate at the 3-dB gain compression point.

In order to verify the MMIC performance, power measurements were made to characterize several MMIC amplifiers individually. With the measurement setup as

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2 The MMIC amplifiers were purchased from the manufacturer at a greatly reduced prices ($300 per unit instead of $900) but all marked with "DC GOOD / VISUALLY BAD."

3 The MMIC amplifiers were only tested under the condition of low drain current (up to 150 milli-Amperes) and low drain voltage (up to 3 Volts).
described in Section 5.1, eight MMIC amplifiers were tested by using two Cascade GS/SIGRF probes, since the MMIC was implemented in a microstrip format. Figure 5-3 shows a plot of Pout (output RF power) vs. frequency on a linear scale, when the MMICs were biased at 9 Volts with Pin = 21 dBm. Quite a dramatic difference on output power was observed not only among the amplifiers but also at different sweep frequency. Figure 5-4 shows a plot of Pout vs. Pin measurements with the MMIC operated at 9 GHz and Vd = 9 Volts, which also indicated other differences among MMICs in terms of saturated power and linear gain. On average, the actual maximum output RF power from a single MMIC was about 6.9 Watts when the MMIC was biased at 9 Volts and driven into saturation. It should be noted that usually the MMIC was biased at 8 or 8.5 Volts when the combiner circuits operated.

![Graph showing output RF power vs. frequency](image)

**Figure 5-3:** Power measurements for individual MMIC amplifiers. Output power was measured at Vd = 9 Volts and Pin = 21 dBm. The plot is shown on a linear scale.

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4 These MMIC amplifiers were already die-attached to the test fixture for a 40-Watt (4x2 array) combiner system, with all bondwire connections set up except for input/output RF feeds.

5 G and S are the acronyms for ground and signal.
5.2.3 MMIC Optimization

The TGA9083-EEU MMIC amplifiers offers either standard gate biasing of an on-chip active gate bias (AGB) circuit which simplifies gate biasing. The former option requires gate biasing at two sides of the MMIC chip, which enables the application of different gate voltages for different MMICs but at the expense of complicating the circuit layout design. The AGB option requires a supply of −5 Volts, which powers up an internal current source along with a resistive ladder network. With the choice of five bonding (gold) pads, which are electrically connected to five different locations along the resistive ladder and located on top of the MMIC chip, five different bias voltages can be applied to the gate pad via a bondwire connection. As a result, the MMIC amplifier can be tested at as much as five different gate voltages so that output power, PAE and consumed drain current at different bias conditions can be measured. Based on this information, each MMIC amplifier can be optimized and hence operates under certain optimal condition, such as maximizing output power or PAE, or minimizing drain current.
Figure 5-5: Variation on drain current existed among eight MMICs, which were tested at $V_d = 9$ Volts and $f = 9$ GHz.

Another possible distinction among MMIC amplifiers, other than the ones mentioned in Section 5.3.2, could be the drain current. As shown in Figure 5-5, when biased at the same condition ($V_d = 9$ Volts), eight tested MMIC amplifiers all consumed different amount of drain current, which in general increased monotonically as the input RF power increased. At $P_{in} = 21$ dBm, the average current was about 2.3 Amperes and the maximum variation was 0.75 Ampere. An optimization attempt was made to equalize the current level among all the MMICs before they were wired with RF feeds in an effort to eliminate a previously observed oscillation problem. Another eight MMICs were tested (at 8.1 GHz with $V_d = 7$ Volts and $P_{in} = 21$ dBm) and proper gate voltage was determined (out of the five available choices) for each MMIC. Table 5-1 shows the drain current, output power and the corresponding bias pad for each MMIC amplifier after the optimization study was performed. The average current was about 1.75 Amperes and the maximum variation was 0.22 Ampere, a seemingly uniform distribution of drain current among the MMICs. The average output power was about 5.13 Watts and the maximum
variation was 0.69 Watts. Half of the MMICs used pad #4 for gate bias and the other half used pad #3.

<table>
<thead>
<tr>
<th>MMIC</th>
<th>Drain Current</th>
<th>Output Power</th>
<th>Bias Pad</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>1.86 A</td>
<td>5.47 W</td>
<td>#4</td>
</tr>
<tr>
<td>#2</td>
<td>1.80 A</td>
<td>5.11 W</td>
<td>#4</td>
</tr>
<tr>
<td>#3</td>
<td>1.76 A</td>
<td>5.24 W</td>
<td>#4</td>
</tr>
<tr>
<td>#4</td>
<td>1.81 A</td>
<td>5.41 W</td>
<td>#4</td>
</tr>
<tr>
<td>#5</td>
<td>1.69 A</td>
<td>4.83 W</td>
<td>#3</td>
</tr>
<tr>
<td>#6</td>
<td>1.64 A</td>
<td>4.92 W</td>
<td>#3</td>
</tr>
<tr>
<td>#7</td>
<td>1.76 A</td>
<td>4.78 W</td>
<td>#3</td>
</tr>
<tr>
<td>#8</td>
<td>1.64 A</td>
<td>5.26 W</td>
<td>#3</td>
</tr>
</tbody>
</table>

Table 5-1: The drain current, output power, and the corresponding bias pad for each MMIC, after eight of them were optimized so as to equalize the drain current. The MMICs were biased at 7 Volts and tested at $f = 8.1$ GHz with $P_{in} = 21$ dBm.

5.3 Power Performance

5.3.1 40-Watt Combiner System Based on A 4x2 Array

Power measurements were performed for a 40-Watt combiner system based on a 4x2 active antenna array, with the measurement setup shown as in Figure 5-1. Two SMA-to-waveguide adapters were used to create a coaxial environment for measurement. A maximum output power of about 41 Watts was observed at 8.7 GHz, with a corresponding gain of about 16.5 dB, as shown in Figure 5-6. The gain varied within the range from 13.8 to 16.5 dB, indicating a remarkably broadband characteristic, with only less than $\pm 1.4$ dB of gain variation. The PAE of the combiner circuit fluctuated, in the range from 17 to 27 %, as the frequency varies. About 150 Watts of DC power and 17 Amperes of drain current on average were consumed by a total of eight MMIC amplifiers when the combiner was in operation.
Figure 5-6: Measured power performance for the 40-Watt combiner system based on a 4×2 array at Pin = 30 dBm.

Measurements were also made to characterize the Pout vs. Pin property of the combiner system at 8.7 GHz, as shown in Figure 5-7. Saturated power of 43.1 Watts and linear gain of 18.2 dB were observed during the measurement. The measured linear gain was very close to the nominal small signal gain (19 dB) of the MMIC amplifier, indicating the combiner efficiency was very high, at least at this particular frequency. Based on the measured compressed-gain curve, it can be easily derived that the combiner operates at the 2 dB gain compression point if Pin = 30 dBm.

By adding an extra directional coupler at the input port of the combiner circuit, the return loss characteristics were measured under the same operation condition. As shown in Figure 5-7, the return loss was better than −10 dB for the entire frequency band, confirming the successful effort that was dedicated to the passive array design. It can be seen that Figures 5-7 and Figure 4-12 both show results with similar shaped curves, indicating that the combiner circuit presented a consistent return loss characteristic as expected for the passive/tapered structure.
Figure 5-7: Pout vs. Pin result for the 40-Watt combiner system based on a 4x2 array at 8.7 GHz.

Figure 5-8: Return loss characteristics for the 40-Watt combiner system.
An effort was made to determine the efficiency of the 40-Watt combiner system. To begin to address the issue experimentally, measurements were made using a two-tray system based on a 2×2 array. Ideally each MMIC amplifier should receive the same amount of incident RF power due to the location symmetry, and a simple estimate of combining efficiency can be made using earlier measurements of the individual MMIC performance. As shown in Figure 5-9, the combining efficiency was calculated by dividing the actual saturated power from the combiner by the total saturated power from all the MMIC amplifiers, resulting in an averaged combining efficiency of about 77%. Since this is essentially a measure of output losses in each tray, this number sets an upper limit on the combining efficiency of the 4-tray system.

![Combining Efficiency Graph](image)

*Figure 5-9: Combining efficiency of the combiner circuit, based on a 2×2 array.*

### 5.3.2 100-Watt Combiner System Based on A 6×4 Array

With twenty-four MMIC amplifiers, instead of eight used in the 40-Watt case, a 100-Watt combiner system was designed based on a 6×4 active antenna array. For better thermal management, the test fixture was mounted on a dedicated heat sink, equipped with a rotary fan and multiple metal fins, as shown in Figure 4-8. Thermal grease was applied
in appropriate amount between adjacent trays and top/bottom covers to further facilitate waste heat removal during combiner operations. Power measurements were performed when the MMICs were biased at 8 Volts with Pin = 38 dBm. As shown in Figure 5-10, a maximum output power of 126 Watts was observed at 8.1 GHz, with a corresponding gain of about 13.1 dB. The gain varied within the range from 9.3 to 13.1 dB, resulting in a gain variation of less than ±1.9 dB. The PAE of the combiner circuit fluctuated, in the range from 14 to 34 %, as the frequency varies. Average speaking, about 350 Watts of DC power and 43 Amperes of drain current were consumed the twenty-four MMIC amplifiers when the combiner was in operation. The variation on drain current among trays is shown in Figure 5-11. Maximum difference occurred at 10.8 GHz, where tray #4 and tray #1 consumed about 8.7 and 4.2 Amperes of drain current, respectively. The Pout vs. Pin measurements were performed on another 100-Watt system, as shown in Figure 5-12. The saturated power was about 50.1 dBm, or 103 Watts, and the linear gain was about 14 dBm, when the combiner operated at 8.1 GHz.

![Graph](image)

Figure 5-10: Measured power performance for the 100-Watt combiner system based on a 6×4 array at Pin = 38 dBm.

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Figure 5-11: Drain current consumed by each of the six trays for the 100-Watt combiner system based on a 6x4 array at Pin = 38 dBm.

Figure 5-12: Pout vs. Pin result for another 100-Watt combiner system based on a 6x4 array at 8.1 GHz.
5.3.3 150-Watt Combiner System Based on An 8x4 Array

In the previous two cases, the 40-Watt and 100-Watt combiner systems were both implemented in a standard waveguide environment. By hosting an 8-tray system based on an 8x4 array in an oversized waveguide environment, a 150-Watt combiner system was realized based on exactly the same circuit topology as in the 100-Watt system, as shown in Figure 5-13. It can be seen that two waveguide taper sections made of aluminum were placed at the input and output ports of the 8-tray combiner system, providing a linear transition from an oversized to a standard waveguide environment. Small-signal measurements were performed to characterize the return loss and insertion loss of two waveguide taper sections placed back-to-back against each other, as shown in Figure 5-14. Insertion loss was almost non-existent and return loss was better than −35 dB covering the entire X-band from 8.2 to 12.4 GHz.

Figure 5-13: Photo of the 150-Watt combiner system with two waveguide taper sections at the input/output ports, providing linear transition from an oversized to a standard waveguide environment.
Figure 5-14: Return loss and insertion loss of the waveguide tapered placed back-to-back against each other.

Figure 5-15: Measured power performance for the 150-Watt combiner system based on an 8×4 array at Pin = 40 dBm.
Measurements were made with Pin = 40 dBm and the MMIC amplifiers biased at 8 Volts. A maximum output power of 150 Watts was achieved at 8.1 GHz, with a corresponding gain of about 12 dB, as shown in Figure 5-15. The gain varied from 8.1 to 12.0 dB, with a variation less than ±2.0 dB, due to certain oscillation problems that will be discussed in a later section. PAE fluctuated between 11.3 and 29.3 % as frequency varied from 8 to 11 GHz. In this case, the dissipated DC power and drain current increased further to 450 Watts and 57 Amperes, respectively.

5.4 Graceful Degradation

Power combining circuits pride themselves on the property of graceful degradation, meaning that even when one or several array elements fail, the output power decreases but still maintains at a certain level, in stead of dropping to zero. On the other hand, vacuum-tube-based amplifiers present a characteristic of catastrophic degradation, which is understandably undesired.

![Graph](image)

Figure 5-16: Characteristics of graceful degradation for a 40-Watt system.

The graceful degradation property of a 40-Watt combiner system was investigated, as shown in Figure 5-16. Two MMIC amplifiers, located on two outer trays, were turned off intentionally and sequentially (by floating the gate and drain bias pins) to examine the
corresponding impact on the power performance. Three frequency sweeps were performed for three different cases in which no, one and two MMICs were turned off. No catastrophic failure or resonant dips were observed as a result of the loss of these amplifiers. The output power and gain gradually reduced when the number of operating MMIC amplifiers decreased; however, the combiner lost about 19 % and 37 % of original output power, respectively, for the cases when one and two MMIC amplifiers were turned off. Ideally this would be 12.5 % and 25 % if the devices were perfectly isolated.

Another measurements were performed at 8.1 GHz for a 100-Watt system, with MMICs biased at 7 Volts and Pin = 37 dBm. Total twenty-four MMIC amplifiers were turned off two at a time, from the outer MMICs towards the inner ones. It is obvious to see that the output power drops monotonically as the number of working MMICs decreases. The measured curve didn’t present a linear characteristic, probably due to the variation on output power observed among different MMIC amplifiers.

Figure 5-17: Characteristics of graceful degradation for a 100-Watt system. The measurement was performed at 8.1 GHz, with Vd = 7 Volts and Pin = 37 dBm.
5.5 Oscillation Problems

In-band oscillations were observed during the power measurements for combiner circuits, particularly when the input RF power ($P_{in}$) was low. The oscillations, which caused the deterioration of output power and gain, could be suppressed by applying sufficient input RF power. A typical case is illustrated in Figure 5-18, including four photos taken in sequence from the spectrum analyzer during a power measurement for a 100-Watt combiner system. A low-power input RF signal was applied at the input of the combiner with frequency swept from 8 to 11 GHz.

![Figure 5-18: The photos show the spectrums of the output RF signal from a 100-Watt combiner system as the input RF signal swept from 8 to 11 GHz. The marked frequency component, at 11.56 GHz, was the oscillation frequency.](image)
The oscillation signal, which is highlighted with a marker, was found to exist throughout the photos, and even when no input RF power was applied. Also shown in each photo is in general a uniformly spaced pulse train, with the spacing getting narrower as the sweep frequency increasing and approaching towards the oscillation frequency at 11.56 GHz. Obvious some sort of mixing process has taken place between the input RF signal and the oscillation signal. Since no oscillation has ever been noticed when the MMICs were tested individually (with RF probes) and the return loss of the MMICs is reasonably large, it is logical to postulate that a feedback path has been established via the external circuitry.

It was later found that, when two adjacent trays were put together, certain parts of the tapered slot antenna structure on the bottom tray would make contact with the metal body at the back of the top tray, as shown in Figure 5-19. As a result, a feedback path was established between the input and output ports of the combiner circuit. It also helped to explain why sometimes when excessive thermal grease was applied, oscillations were not observed, since the thermal grease covered up the metal edges of the antenna cards and provided electrical isolation between the input and output ports.

Figure 5-19: The effects on gain and output power due to the presence of oscillations. The measurements were performed on a 100-Watt combiner system

In order to confirm the assumption, regular 3M plastic tapes were used and put on proper locations on the test fixture to provide isolation between the antenna sections and the test fixture. Two separate Pout vs. Pin measurements were performed before and after
the isolation engagement, as shown in Figure 5-20. The solid and dotted curves represent the cases with and without isolation (tapes), respectively. For input RF power greater than 36.5 dBm, no oscillations were observed (since they were suppressed by the strong input RF signal), consequently the gain and output power in both cases were virtually the same. However, as Pin decreased, oscillations occurred in the non-isolation case, resulting in drastic drops in output power and gain.

It is worth noting that as Pin further decreased (below 33 dBm), gain and output power started to drop abruptly in the “with isolation” case because of oscillation. The cause was that some antenna cards still made electrical contact with the test fixture in the horizontal direction, instead of vertically, which could not be avoided unless new circuit trays were made. The oscillation problems should be eliminated by using a slightly different circuit design, as will be described in the next chapter.

Figure 5-20: The effects on gain and output power due to the presence of oscillations. The measurements were performed on a 100-Watt combiner system at 8 GHz with Vd = 8 Volts.
References


Chapter 6

Conclusions and Future Works

This thesis presents a continued effort in the development of spatial power combiners implemented in a standard X-band waveguide environment. The combining circuits adopt modular tray architecture, providing full waveguide-band frequency coverage and an excellent thermal environment for an array of MMIC amplifiers. The shape of the tapered-slot or finline structures was optimized not only to minimize return loss and insertion loss, but also to provide a broadband impedance transformation from the waveguide mode to the MMIC amplifiers as well.

A 4×2 array, with four trays and two commercial GaAs MMIC power amplifiers per tray, yielded a maximum of 41 Watts output power (CW) with a gain variation less than ±1.2 dB from 8 to 11 GHz. The average combining efficiency over the operating band was estimated at 73%. By scaling the antenna design, accommodating more MMICs on each tray and increasing the array size, another combiner system implemented by a 6×4 active antenna array rendered a 126-Watt maximum power output with gain variation less than ±1.9 dB within the entire band of interest.

To demonstrate that higher output power could be achieved simply by stacking more active trays together, an over-moded waveguide structure was used to accommodate more active elements. By extending the 120-Watt system to accommodate eight trays with 32 MMICs, as much as 150 Watts of output power was obtained at X-band, which signifies the fact that high output power can be realized by using spatial power combining techniques.

The combiner circuits also presented a graceful degradation property, which is the desired characteristic that the vacuum-tube technology lacks. Gradual degradation in RF power output was observed while the MMIC amplifiers were turned off intentionally to emulate device failure. The thermal property of the combiner circuits were proven to be
excellent, even with as much as 550 Watts of DC power being dissipated by the MMIC amplifiers during operation. Simulated results agreed well with the measured results, which was performed during power measurements.

The hybrid circuit approach allows circuit designer with flexibility of choosing active devices based on different technologies. Thanks to the modular design of the combiner circuit, enabling easy maintenance, variable output power level and potential medium-scale fabrication. The results so far have been very encouraging, suggesting the efficacy of the combiner design and a strong potential for higher powers by moving towards a greater number of MMICs per tray and a larger number of trays. The performance of the combiner systems suggests promising outlook in competing with the currently dominating traveling-wave tube amplifiers (TWTAs) in high-power applications.

![Diagram of a finline structure with back-side and front-side metallization.](image)

**Figure 6-1**: Circuit layout for antipodal finline structure.

There is still plenty of room for further improvement on the combiner performance. To begin with, full wave analysis can be performed for the 6x4 array to optimize the performance of the passive structures so that return loss and insertion loss of the combiner circuits can be minimized. Finite-difference analysis can be performed to directly predict the characteristic impedance corresponding to a finline structure with a
specific gap size, which will reduce a great deal of measurement effort for verifying the impedance value.

The slotline-to-microstrip transition can be implemented by using antipodal finline structure, as shown in Figure 6-1, which provides a gradual transition from slotline to microstrip without the need for bondwire connections. In addition, the tapered slot antenna and microstrip transformer can be realized on a single substrate, which not only eliminates an extra assembly step for epoxy attachment, but also avoid the possible lamination due to bad attachment. Although double-side photolithography is required, it is an established process in industry.

As discussed in the previous chapter, oscillation occurred due to poor input/output isolation, which can be eliminated by modifying the layout of the tapered slot antennas, as illustrated in Figure 6-2. The signal and ground metallization of the slotline structure can be exchanged, so as to electrically isolate the input signal from the output signal.

![Diagram](image)

Figure 6-2: Modification to the antenna layout to improve input/output isolation.
Figure 6-3: Effect of dielectric loading.

Dielectric loading can be used to mitigate non-uniform illumination problem the combiner input, which is a well-established technique and often seen in literature [1, 2]. After the dielectric loading is introduced into the waveguide, as shown in Figure 6-3, the field profile tends to flatten up near the center region, resulting in more uniform incident power drive among the MMIC amplifiers. As a result, higher combiner efficiency can be expected since all of the amplifiers will more or less saturate at the same time.

In an earlier design of power combining circuits, MMIC amplifiers were epoxy-attached onto aluminum nitride substrates due to their high thermal conductivity. However, in the recent designs, such as the 40-Watt and the 100-Watt systems, the use of aluminum nitride is no longer justified since the MMIC amplifiers were all attached directly to the metallic test fixture. With dielectric constant as high as 8.6, aluminum nitride substrates can be replaced by other ceramic substrates with much lower dielectric constant, such as the Duroid substrates, which is also inexpensive and less fragile.

References
