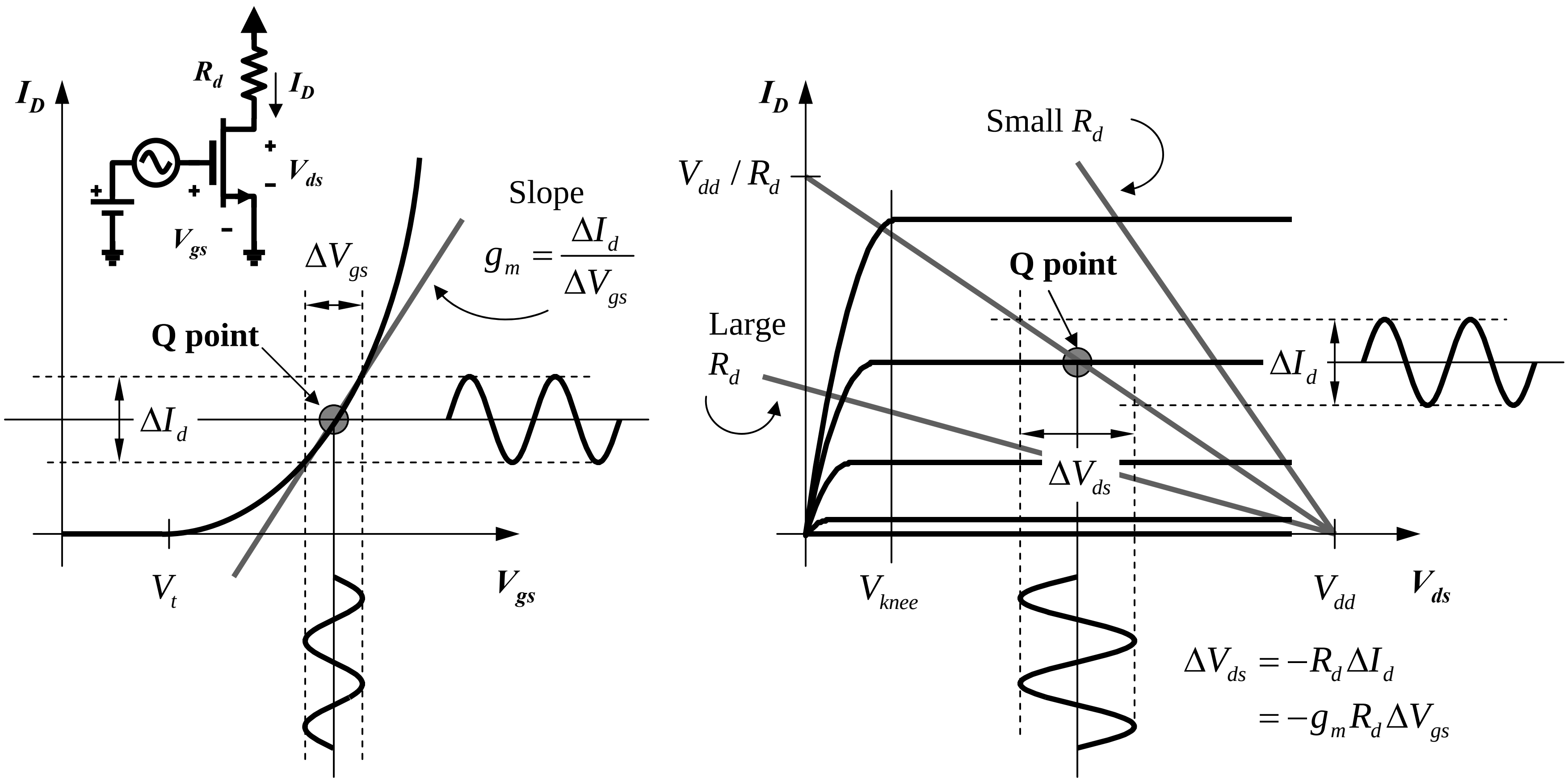
# Small-Signal Linearization at Q-point

- Input-Output transfer function is approximately linear if we restrict attention to small AC signals.
- Linear voltage amplification possible when: $g_m R_d > 1$
- Bias point and load line control gain and maximum allowable signal swings



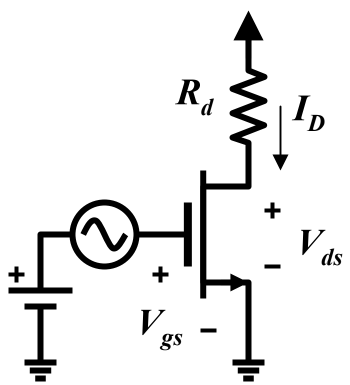


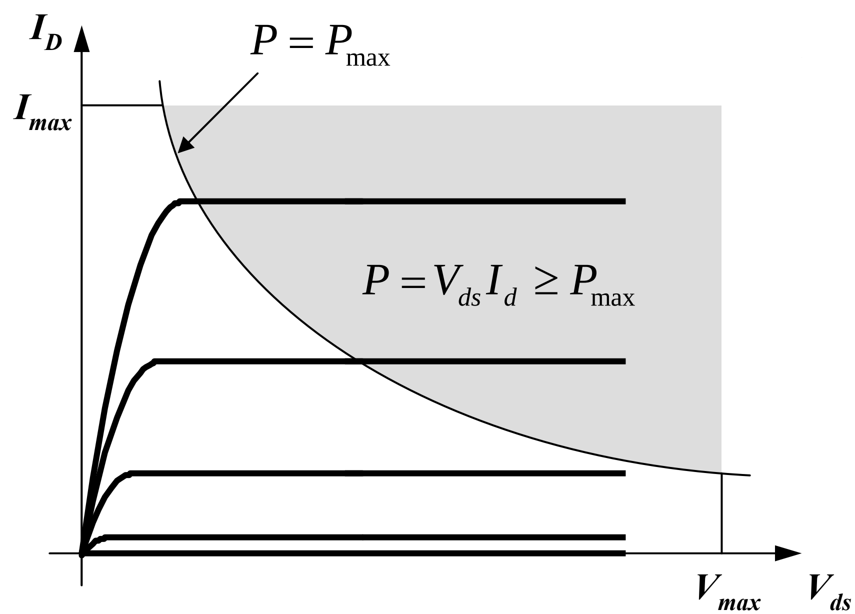

Back to TOC

# Power Dissipation

Choice of DC Bias point (Q-point) is also limited by DC power-dissipation considerations

Data sheet will specify maximum DC power for various packaging options






Back to TOC

# Channel-Length Modulation

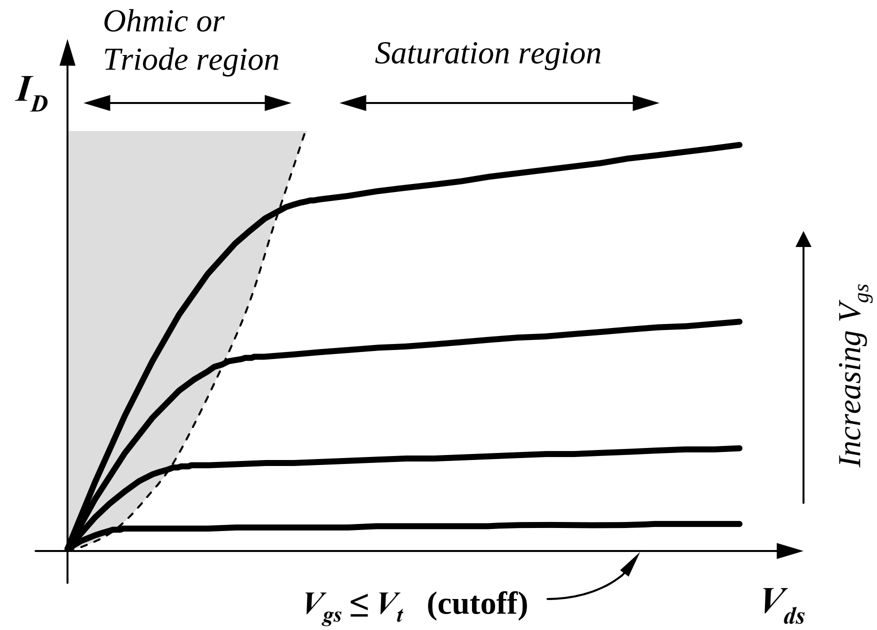
In real devices the output current is not constant, increasing slightly with drain voltage

This can be attributed to the modulation of the channel length by the drain voltage

If this is a small effect then

$$I_d \approx \frac{1}{2}\mu_n c_{ox} \frac{W}{L-\Delta L}\left(V_{gs}-V_t\right)^2$$

$$\approx \frac{1}{2}\mu_n c_{ox} \frac{W}{L}\left(V_{gs}-V_t\right)^2\left(1+\frac{\Delta L}{L}\right)$$




Assume $\Delta L$ is proportional to $V_{ds}$:

$$\frac{\Delta L}{L} = \lambda V_{ds} = \frac{V_{ds}}{V_A}$$

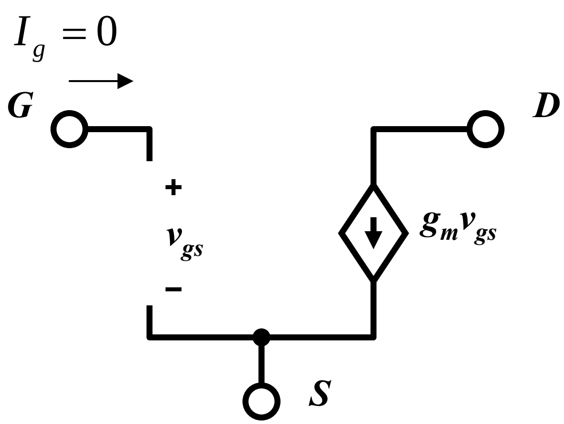
$\lambda$ Is the *channel-length modulation parameter*
$V_A$ is the *Early voltage*

So in saturation we can write: $I_d \approx K_n\left(V_{gs}-V_t\right)^2\left(1+\lambda V_{ds}\right)$

# FET Small-Signal Model (LF)

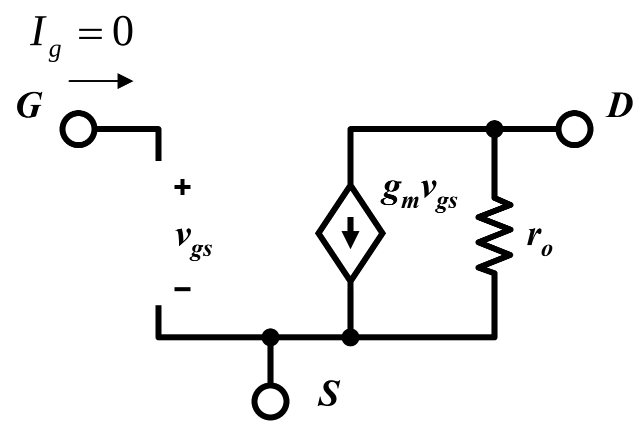
## Low-Frequency Model Linearized around bias-point in saturation

### Ideal Case




$$I_d = K_n \left(V_{gs} - V_t\right)^2$$

### With channel-length modulation

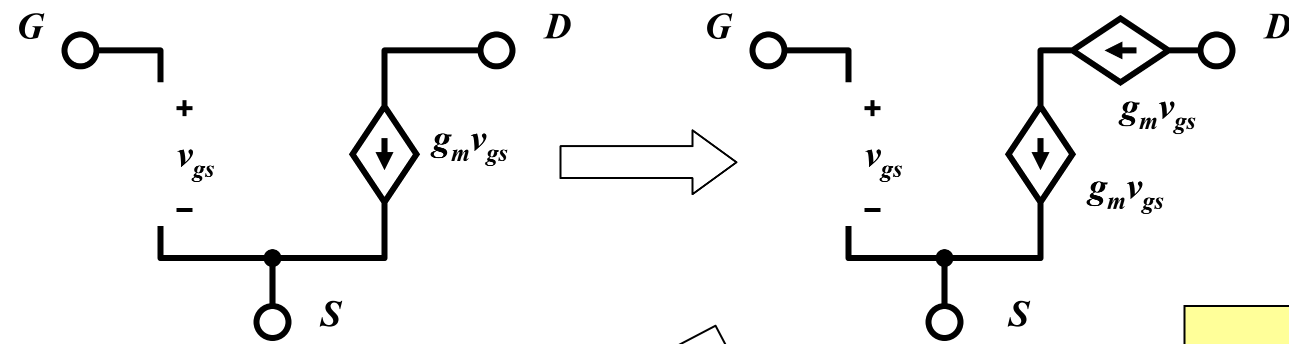



$$I_d = K_n \left(1 + \lambda V_{ds}\right)\left(V_{gs} - V_t\right)^2$$

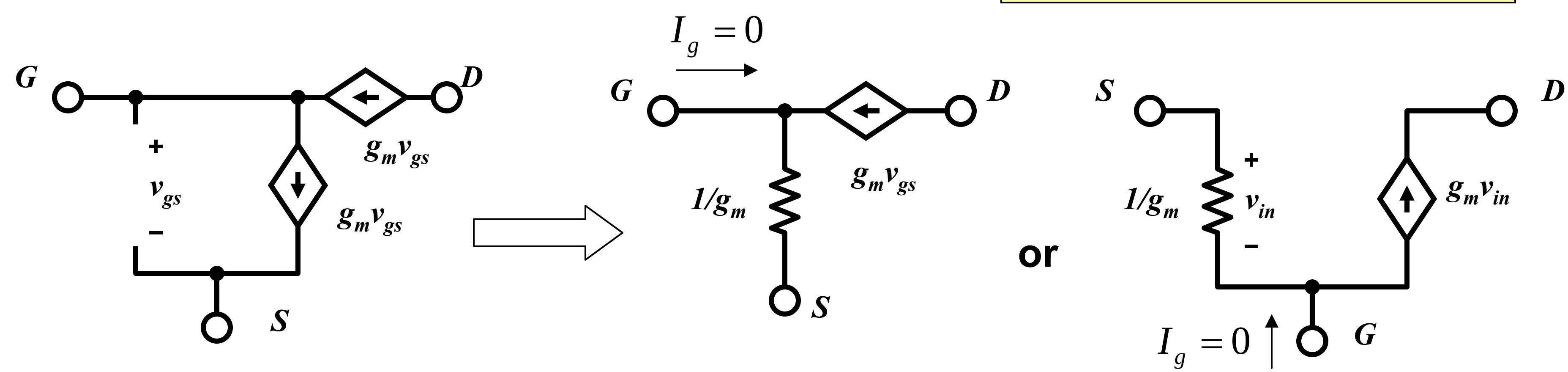
$$g_m = 2K_n (V_{gs} - V_t) = 2\sqrt{K_n I_d} = \frac{2I_d}{(V_{gs} - V_t)}$$

$$r_o = \frac{1}{\lambda I_d} = \frac{|V_A|}{I_d}$$

# FET T-model




**Note: KCL insures that** $I_g = 0$



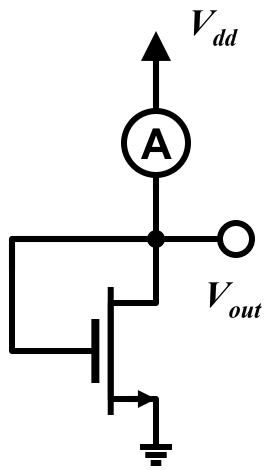



Back to TOC

# Measuring Parameters $g_m$, $V_t$

**This is a simple method for estimating device parameters**

- **Use diode-connected device (forces operation in saturation)**
- **With an ammeter, vary the supply voltage until the desired bias current is achieved, and record the gate voltage $V_{gs}$**
- **Adjust $V_{dd}$ so that $V_{gs}$ changes by a small amount (say 50mV), and record the resulting change in current**




$$g_m \approx \frac{\Delta I_d}{\Delta V_{gs}}$$

- **Continue varying the gate voltage until the current increases by a factor of 4. If the device follows a parabolic law, this means that the ($V_{gs}$-$V_t$) must have changed by a factor of 2**

$$I_{d1} = K_n \left(V_{gs1} - V_t\right)^2$$

$$I_{d2} = 4I_{d1} = K_n \left(V_{gs2} - V_t\right)^2$$

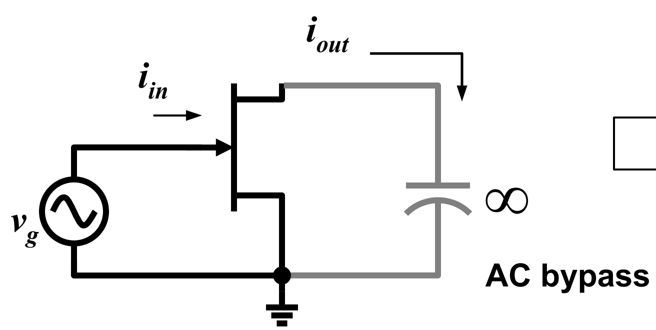
$$r = \sqrt{\frac{I_{d2}}{I_{d1}}}$$

$$V_t = \frac{rV_{gs1} - V_{gs2}}{r-1}$$

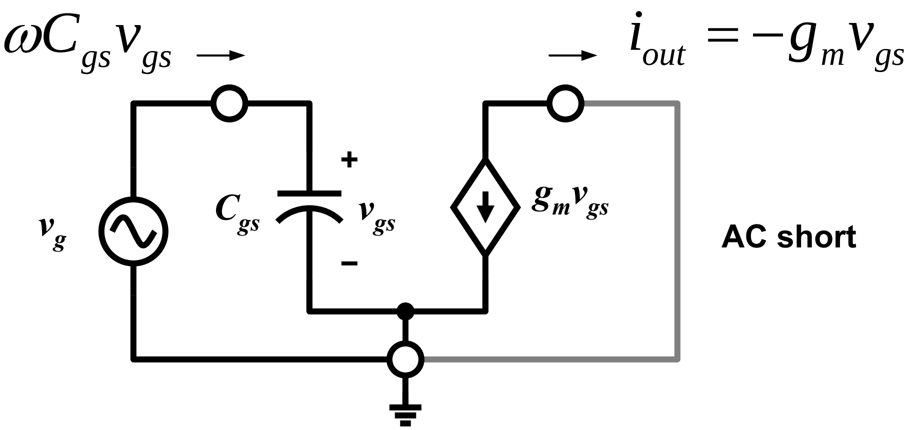
**For $r$ = 2:** $V_t \approx 2V_{gs1} - V_{gs2}$

# Cutoff Frequency, $f_\tau$

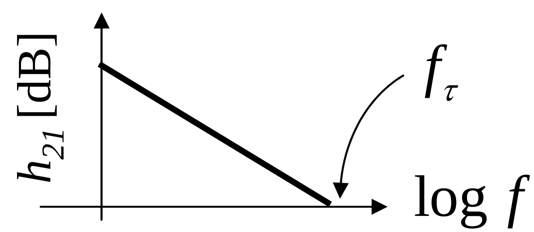
**Device capacitances create high-frequency poles in transistor circuits**




**Simple small-signal equivalent circuit**




**Short-circuit Current Gain** $$h_{21} = \left|\frac{i_{out}}{i_{in}}\right| = \frac{g_m}{2\pi f\, C_{gs}}$$

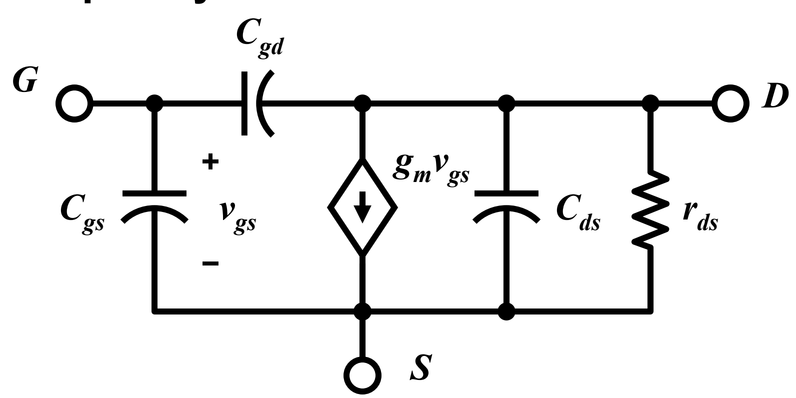



**Unity current gain frequency:** $$f_\tau = \frac{g_m}{2\pi C_{gs}}$$

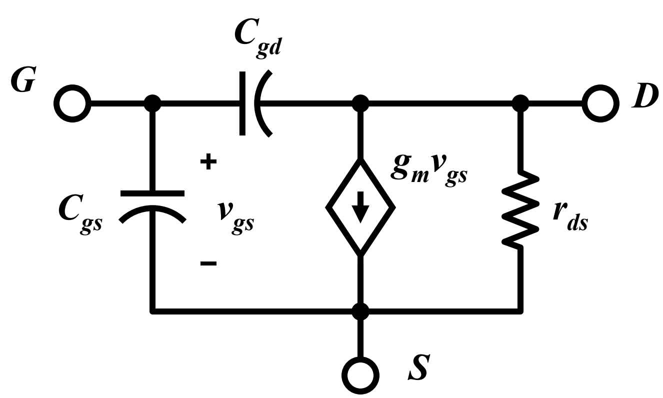
**$f_t$ is a convenient figure-of-merit for comparing devices in terms of high-frequency performance. A specification of $f_t$ also gives us an esimate of $C_{gs}$**

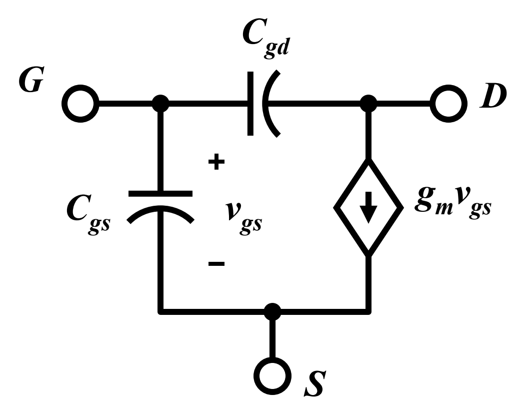
# FET Small-Signal Models (HF)

A more complete high-frequency model for the FET would look like this:




However, $C_{ds}$ is often significantly smaller than the other capacitances. And $r_{ds}$ can also sometimes be ignored. So more commonly we will use one of these:




The Miller Theorem will help us deal with $C_{gd}$