12 W/mm power density AlGaN/GaN HEMTs on sapphire substrate

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Record power performance at 4 GHz has been obtained using field-plated AlGaN/GaN HEMTs on sapphire substrate. High power density (12 W/mm) as well as high efficiency (58%) have been measured. A comparison between devices with and without field plate on the same sample showed a significant reduction in knee-voltage walk-out for the field-plated device, thus enabling high power and efficiency operation.

Introduction: AlGaN/GaN HEMTs represent the most promising devices for microwave and millimetre-wave power applications [1]. However, device performance is known to be often limited by 'DC-to-RF dispersion'. Surface traps, acting as a 'virtual gate' in the gate-drain access region, prevent proper device operation, reducing the available current swing as well as degrading the knee-voltage [2]. The introduction of a field-plated gate structure proved an effective method for reducing dispersion. This method was successfully applied by Asano *et al.* [3] on AlGaAs/GaAs HFETs. Recently, Ando *et al.* [4] also applied this technique to AlGaN/GaN HFETs, showing a significant improvement in device performance. In this Letter we compare performance of devices with and without an overlapping field-plate structure. Field-plated devices yielded power densities as high as 12 W/mm, more than twice (5.2 W/mm) those obtained for devices without the field plate.

Device fabrication: Fig. 1 shows a cross-section of the fabricated HEMT. AlGaN/GaN heterostructures were formed using a 290 Å-thick $Al_{0.22}Ga_{0.78}N$ barrier layer on sapphire substrate. Details on device processing can be found in [5]. The PECVD SiN passivation layer was 700 Å. Gate width and length on all the devices tested were 2 × 75 µm, and 0.7 µm, respectively. Gate-source and gate-drain spacings were 0.7 and 2 µm, respectively. The field plate was formed by evaporating a second gate on top of the passivation layer. Field-plate extensions, with respect to the gate-drain edge, are 0.7 µm toward the drain, and 0.4 µm toward the source, resulting in a 1.1 µm total length, as shown in Fig. 1. Electrical connection between the gate and field plate was formed through the common path of gate-pad and gate-feeder in the extrinsic device region.

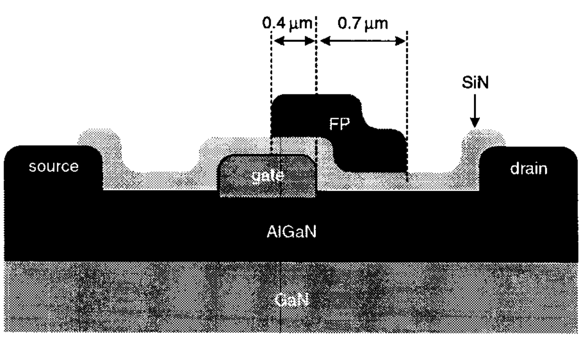

Fig. 1 *Device cross-section*

After SiN PECVD deposition a second gate is evaporated on the dielectric layer, acting as a field plate. The two gates are electrically shorted through the device pad and gate feeders

Measurements: As can be seen in Fig. 2, passivated devices without field plates show a larger knee-voltage than those fabricated with the field-plate structure. The significant reduction in drain current dispersion clearly points out the benefits of the field-plated gate structure. Two possible mechanisms involved in the field-plate operation are (i) reduction of electric field at the gate edge resulting in a lower electron injection in surface states traps and/or (ii) modulation of surface state traps in the gate-drain access region. Gate-drain destructive breakdown voltage increased. Devices without field plate yielded breakdown voltages in the 90 to 100 V range, while those with field plate ranged from 120 to 130 V. The introduction of additional capacitance degraded small-signal characteristics: peak f_t decreased from 21 to 16 GHz, and peak f_{max} went from 45 to 35 GHz, for devices without and with the field plate, respectively.

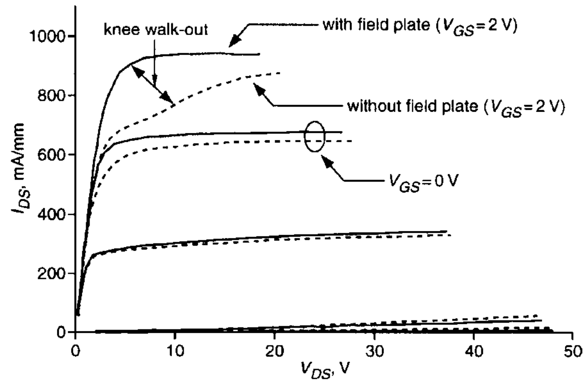

Fig. 2 *Pulsed I–V characteristics measured with 200 ns pulsewidth*

Device without field plate (dashed line) shows large walk-out of knee compared to that with field plate (solid line)
V_{GS}: −8 V → 2 V, 2 V/step

The improvement observed with pulsed *I–V* measurements was also confirmed by large-signal RF power testing carried out at 4 GHz. At V_{DS} = 45 V, field-plated devices yielded saturated output power densities (P_{SAT}) and peak power added efficiencies (PAE) in the 9.5 to 11.5 W/mm and 54 to 58% range, respectively. At V_{DS} = 50 V, the best result achieved was 12 W/mm with a 58% peak PAE, see Fig. 3. Measured power performance for devices without a field plate were significantly poorer. At V_{DS} = 45 V, average P_{SAT} was in the 4 to 5.2 W/mm range with peak PAE in the 40 to 43% range.

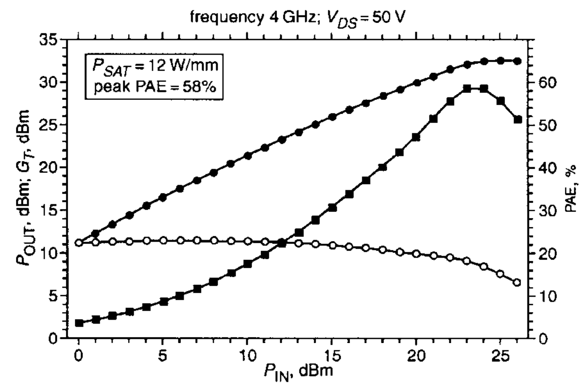

Fig. 3 *Single tone power measurement at 4 GHz*

Device measured was with field plate and on sapphire substrate. Bias point V_{DS} = 50 V and I_{DS} = 50 mA/mm. Saturated output power 12 W/mm, while peak PAE 58%
• P_{OUT}
○ G_T
■ PAE

The reduction in knee walk-out observed by pulsed *I–V* measurements was thus confirmed by large-signal RF characterisation. Moreover, it must be stressed that high efficiency operation was a key factor in obtaining high power densities. At high drain biases, devices experienced severe degradation when using matching and/or bias points with PAEs lower than 40%. The low power added efficiency due to the large knee walk-out was the main limitation of devices without the field plate, which could be biased no higher than 45 V.

Conclusions: Record performance of AlGaN/GaN HEMTs fabricated on sapphire substrate with an overlapping field-plated gate contact has been presented. The adoption of a field plate greatly reduced dispersion phenomena, improving device large signal characteristics. The reduction of knee walk-out allowed the device to operate at high efficiencies (58%) and high power densities (12 W/mm). Although present device operation at a frequency higher than 4 GHz is limited by excess capacitance arising from the field plate, we believe that operation at higher frequencies can be achieved by reducing gate length and/or optimising field-plate geometry and SiN thickness.

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