High-Power Polarization-Engineered GaN/AlGaN/GaN HEMTs Without Surface Passivation

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Abstract—**In this paper, a high-power GaN/AlGaN/GaN high electron mobility transistor (HEMT) has been demonstrated. A thick cap layer has been used to screen surface states and reduce dispersion. A deep gate recess was used to achieve the desired transconductance. A thin SiO_2 layer was deposited on the drain side of the gate recess in order to reduce gate leakage current and improve breakdown voltage. No surface passivation layer was used. A breakdown voltage of 90 V was achieved. A record output power density of 12 W/mm with an associated power-added efficiency (PAE) of 40.5% was measured at 10 GHz. These results demonstrate the potential of the technique as a controllable and repeatable solution to decrease dispersion and produce power from GaN-based HEMTs without surface passivation.**

Index Terms—**GaN, microwave power field effect transistors (FETs), MODFETs, passivation, RF-dispersion.**

I. INTRODUCTION

AS A PROMISING candidate for future microwave power devices, GaN-based high electron mobility transistors (HEMTs) have attracted much research interest [1]. A combination of high breakdown field, high sheet charge density and high electron velocity in AlGaN/GaN HEMTs gives great potential for high power high frequency applications. Output power density of 11.2 W/mm at 10 GHz has been reported recently [2]. However, many GaN-based power HEMTs suffer from current collapse during large signal operation at high frequency, usually referred as "dc-to-radio frequency (RF) dispersion". Slow response of surface traps is believed to be one of the major contributing factors [3]. SiN passivation has been used to suppress this problem [4], but reproducibility of breakdown voltage, gate leakage, and effectiveness of dispersion elimination is undependable. Recently, solutions to the dispersion problem have been addressed at epitaxial level [5]–[7]. The development of the GaN/AlGaN/GaN HEMT is one of these efforts [7]. A thick GaN cap was introduced in the access region to reduce surface potential fluctuations from affecting device performance, thus decreasing dispersion. Very promising power data have been shown recently utilizing these structures [7], namely, 3.4 W/mm with PAE of 32% at drain bias of 15 V at 10 GHz without SiN passivation on sapphire. However, the maximum drain bias that could be applied to these devices during power measurements was limited by high gate leakage and low breakdown voltage. A reduction in gate leakage and an increase in breakdown voltage are needed to obtain higher power. In this paper we propose a general solution to these problems. By depositing a SiO_2 insulating layer against the gate recess sidewall on the drain side, gate leakage current decreased and breakdown voltage increased. Due to the effective dispersion control and increased breakdown voltage, a record output power density was achieved without passivation.

II. DEVICE STRUCTURE

The device structures studied in this paper were grown by metal-organic chemical vapor deposition (MOCVD) on both sapphire and SiC substrates. The epitaxial structure (shown in Fig. 1) consisted of a semi-insulating Fe-doped GaN buffer layer [8], followed by a 0.7-nm AlN interfacial layer, a 40-nm $Al_{0.22}Ga_{0.78}N$ layer, a 10-nm graded $Al_xGa_{1-x}N$ layer ($x = 0.22{-}0$) doped by Si (8×10^{18} cm^{-3}) and a 250–nm unintentionally doped (UID) GaN cap layer. Room temperature sheet charge density and Hall mobility were 8×10^{12} cm^{-2} and 2000 cm^2/V- s, respectively.

Using charge control analysis, the ability of surface potential to modulate the channel charge is inversely proportional to the distance between surface and channel. The 250–nm GaN cap layer is used to increase the surface-channel distance to a value where surface potential fluctuations no longer effectively modulate the channel charge. Dispersion from surface states is therefore reduced or eliminated. The graded AlGaN layer is Si-doped to compensate the negative polarization charge and prevent hole accumulation. The thin AlN layer is utilized to remove alloy disorder scattering and improve mobility [9].

To investigate the contribution of the recessed sidewalls to the gate leakage current, two devices were processed. The first had a full gate metal coverage on the recess sidewalls, while the other had spacing ($\sim 0.3{-}0.4$ μm) between the gate metal and the recess sidewalls. The latter showed one order of magnitude lower gate leakage current. This suggested that most of the gate leakage was not through the bottom of the recessed trench,

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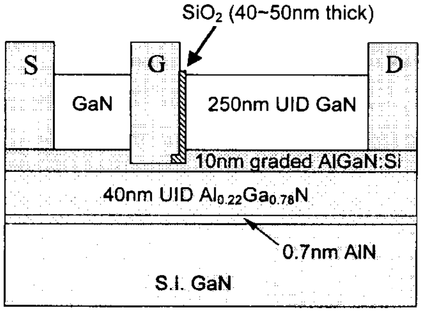

Fig. 1. Schematic of the proposed GaN/AlGaN/GaN HEMT structure. The thin SiO_2 insulating layer helps reducing the gate leakage and improving the breakdown voltage.

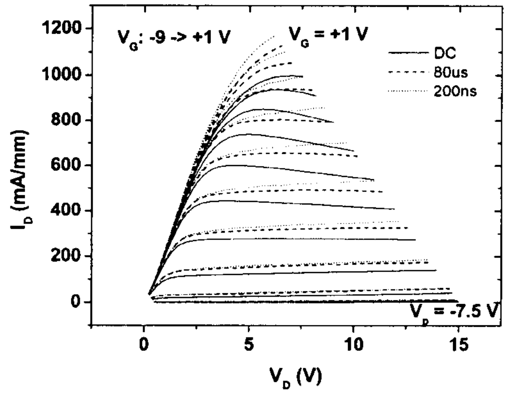

Fig. 2. DC and pulsed *I–V* characteristics of an unpassivated GaN/AlGaN/GaN HEMT on sapphire. Device dimension: 0.7 × 150 μm^2. No dispersion was observed up to 200 ns.

but through the sidewalls. Moreover, because the gate-drain bias voltage is much larger than the gate-source bias voltage, the sidewall of the drain side is the major current path of the gate leakage current.

To decrease this leakage, a thin SiO_2 layer (40–50 nm) was introduced to cover the sidewall of the drain side and eliminate the leakage current path [10]. Fig. 1 shows the schematic cross section of the device. Device fabrication was similar to conventional AlGaN/GaN HEMTs. Self-aligned deep recesses before ohmic and gate metallizations were needed to obtain ohmic contacts, reasonable pinch-off voltage ($-5 \sim -7$ V) and transconductance ($\sim$200 mS/mm). SiO_2 was deposited prior to the gate metallization. During e-beam SiO_2 evaporation, the sample was tilted so that the drain sidewall was covered and the coverage of the gate region remained as small as possible. Gate length was 0.7 μm and gate width was 150 μm (2 × 75 μm). This method can be extended to smaller gate-length devices by using some other SiO_2 deposition techniques (e.g., PECVD SiO_2 deposition with dry-etching of SiO_2 on the etched gate surface).

III. DEVICE PERFORMANCE

The introduction of the SiO_2 layer improved gate leakage current and breakdown voltage while retaining dispersion removal. Fig. 2 shows the dc and pulsed current–voltage (*I–V*) characteristics of an unpassivated device on a sapphire substrate. At pulse width of 200 ns, no dispersion was observed when the SiO_2 coverage under the gate was minimized and a current density of 1.2 A/mm was obtained. Gate leakage was decreased by one to two orders of magnitude, from 10 to 0.3 mA/mm at a gate-drain bias of −20 V, as shown in Fig. 3. The destructive two terminal breakdown voltage was more than 90 V, compared to 35 V for devices without the SiO_2 layer. This allowed the application of higher drain bias. For unpassivated devices on sapphire substrate, a maximum drain bias of 25 V could be applied, compared to a drain bias of 15 V without SiO_2. Uncooled continuous-wave (CW) power measurements were performed. A saturated power density of 4.8 W/mm with peak PAE of 33% was obtained for devices on sapphire substrate at 10 GHz. Similar devices grown on SiC substrate were also processed. A record output power density of 12 W/mm with an associated PAE of 40.5% at a drain bias of 45 V at 10 GHz was achieved without SiN passivation, as shown in Fig. 4. At peak PAE point of 42%, a power density of 11 W/mm was obtained. This is due to the effective dispersion control and the application of high drain bias.

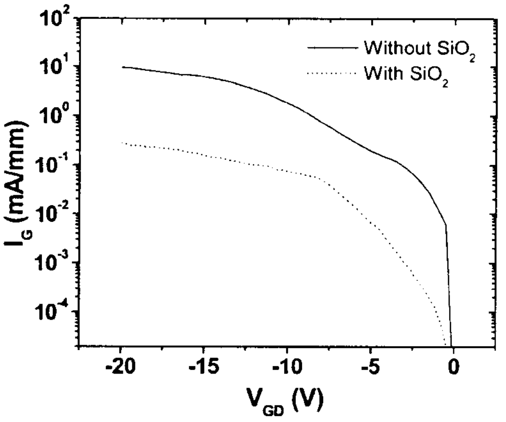

Fig. 3. Gate-drain leakage current densities for devices with and without SiO_2 sidewall coverage. For the SiO_2 covered devices, the insulator thickness on the sidewall was about 50 nm. More than one order of magnitude reduction in gate leakage current was achieved by the introduction of SiO_2.

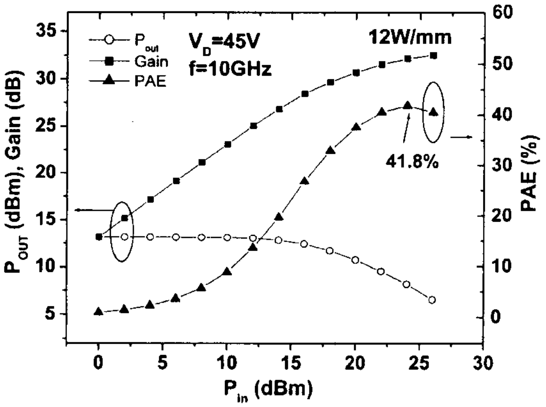

Fig. 4. Power performance of an unpassivated 0.7 μm× 150 μm GaN/AlGaN/GaN HEMT on SiC substrate at 10 GHz. Bias conditions were V_D = 45 V and I_D = 270 mA mm. An output power density of 12 W/mm with an associated PAE of 40.5% was achieved.

Preliminary investigation of the effect of SiO_2 coverage on the bottom of the gate recess was carried out. Different tilt angles were used during SiO_2 deposition to apply varying SiO_2 coverage under the gate. The coverage length was characterized by atomic force microscopy (AFM). Though there was a small increase in dispersion with increasing coverage under the gate (studied to a maximum coverage of 0.3 μm), the effect was small enough such that similar microwave performance was observed from these devices. It showed that the process has acceptable tolerance to the SiO_2 deposition step.

IV. CONCLUSION

In conclusion, an improved GaN/AlGaN/GaN HEMT was demonstrated. A thin SiO_2 layer was introduced to cover the gate recess sidewall of the drain side. The gate leakage current was reduced and breakdown voltage increased compared to devices without SiO_2. An output power density of 12 W/mm with an associated PAE of 40.5% was achieved without SiN passivation at 10 GHz with a drain bias of 45 V. This is the highest output power density ever reported for GaN devices. This promising result demonstrates the great potential of this technique as a controllable and repeatable solution for decreasing dispersion and producing power without surface passivation.

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