Integration of $Ba_xSr_{1-x}TiO_3$ Thin Films With AlGaN/GaN HEMT Circuits

Hongtao Xu, Nadia K. Pervez, Peter J. Hansen, Likun Shen, Stacia Keller, Umesh K. Mishra, and Robert A. York

***Abstract*—$Ba_xSr_{1-x}TiO_3$ (BST) thin films have large dielectric constants that can be varied by as much as a factor of 3 with an applied field, making them attractive for radio frequency (RF) circuits as small-area ac bypass/dc blocking capacitors, or high-power varactors. However, BST must be deposited at relatively high temperatures in an oxidizing environment, presenting significant integration challenges for MMIC applications. This letter describes the successful integration of BST films on AlGaN/GaN high electron-mobility transistor (HEMT) monolithic microwave integrated circuits on sapphire substrates. A sacrificial SiO_2 buffer layer is used to protect the underlying AlGaN during the RF magnetron sputtering of the BST film at an elevated temperature, with a carefully controlled heater ramp rate to avoid degradation of the ohmic contacts on the HEMT.**

***Index Terms*—$BaSrTiO_3$ (BST), ferroelectric varactors, GaN, high electron-mobility transistor (HEMT), monolithic microwave integrated circuit (MMIC).**

I. Introduction

AlGaN/GaN high electron-mobility transistor (HEMTs) have attracted considerable interest as power devices in microwave applications, promising greater than a tenfold increase in power-density as compared with GaAs devices [1]–[3]. Similarly, $Ba_xSr_{1-x}TiO_3$ (BST) thin films have been investigated for microwave circuit application because of their high dielectric constants (200–300), high tunability (3:1), relatively low loss ($\tan\delta < 0.01$), and fast switching speed (sub-nS). Several research groups have exploited the field-dependent dielectric constant of BST in radio frequency (RF) varactor circuits [4]–[6]. BST-based varactors are especially attractive for high-power RF circuits since they can sustain relatively large ac fields at low average dc fields, unlike diode technologies. Additionally, due to its high dielectric constant, BST is a candidate for very compact MMIC dc blocking capacitors, promising a 100-fold reduction in capacitor area as compared with SiN and SiO_2 capacitors. The goal of this work was to develop an integration strategy for exploiting the complementary characteristics of GaN HEMTs and BST capacitors in monolithic circuits.

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H. Xu, N. K. Pervez, L. Shen S. Kellar, U. K. Mishra, and R. A. York are with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA (e-mail: hongtao@engineering.ucsb.edu).

P. J. Hansen is with the Materials Department, College of Engineering, University of California, Santa Barbara, CA 93106 USA.

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Initial efforts to integrate a standard BST capacitor process with a GaN HEMT process highlighted some key technical challenges. First, early measurements indicated that the AlGaN two-dimensional electron gas (2DEG) channel was damaged during the RF magnetron sputtering of BST, most likely due to ion damage from the plasma. Secondly, both HEMT and BST devices require high temperature processes which adversely impact each other. Typical electrode metallurgies for BST capacitors containing Au could not sustain the rapid thermal annealing (RTA) required for the ohmic contacts of the HEMT. Similarly, the ohmic contacts on the GaN HEMT can be adversely affected by the BST deposition process, which typically requires long duration at high substrate temperatures in an oxidizing environment. In this letter, several experiments for HEMT/capacitor integration were described and analyzed. We will show our solutions to these problems, providing a valid method of process integration for future active GaN circuit design and fabrication using BST capacitors.

II. Device Fabrication

The HEMT devices tested were grown by metal–organic chemical vapor deposition (MOCVD) on sapphire substrates. The epitaxial structure consisted of a semiinsulating Fe-doped GaN base layer [7], followed by a 290-Å-thick $Al_{0.35}Ga_{0.65}N$ barrier layer. The room temperature sheet electron concentration and Hall mobility were $\sim 1.5\times10^{13}$ cm^{-2} and ~ 1170 cm^2/Vs, respectively. The HEMT device fabrication started with ohmic contact formation. Ti/Al/Ni/Au (200/1500/375/500 Å, respectively) were evaporated and annealed at 870 °C for 30 ss in N_2. Device mesa isolation was then performed using a Cl_2 reactive ion etch (RIE). TLM measurements showed an average contact resistance of 0.4 $\Omega\cdot$mm, and a sheet resistance $R_{sq} \approx 370\ \Omega/\square$. The gate contact was formed by evaporating Ni/Au/Ni (300/2500/500 Å, respectively). The final processing step was a 170-nm plasma-enhanced chemical vapor deposition (PECVD) Si_3N_4 passivation layer, which has been shown to eliminate dc-to-RF dispersion [8], [9]. The gate width and length on all the devices tested were 2×75 μm, and 0.7 μm, respectively.

A 3000-Å BST thin film was grown on an AlGaN/GaN substrate with 3000 Å of electron-beam evaporated Pt that was prepatterned by liftoff as a bottom electrode for an MIM capacitor. The BST films were deposited using RF magnetron sputtering. The film growth conditions were optimized for tunability and microwave loss performance; typical growth conditions for a $\sim$ 3000 -Å $Ba_{0.5}Sr_{0.5}TiO_3$ film are a substrate temperature of 700 °C, base pressure of 50 mtorr (90 sccm Ar/10 sccm O_2),

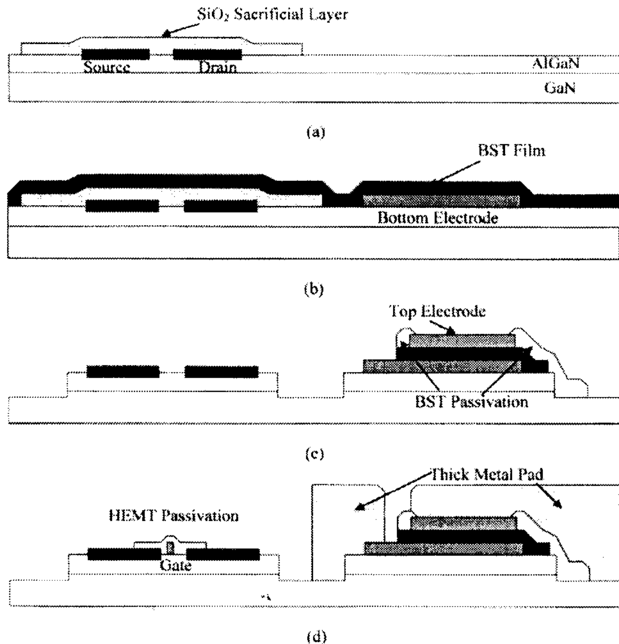

Fig. 1. Process flow. (a) Source/drain ohmic contacts with SiO_2 sacrificial layer. (b) Prepatterned bottom electrodes and BST film deposition. (c) BST pattern etch, top electrodes, mesa isolation, and BST film passivation. (d) Gate metallization, HEMT passivation, and thick metal pad.

and RF power of 150 W on two 3-in targets. Pt/Au top electrodes were evaporated followed by a BST etch in 1:1 buffered HF:DI water. The BST capacitors were passivated by a 3000-Å SiO_2 film to prevent contamination during subsequent processing. This passivation layer also functions as an insulating layer beneath the overpass bridge, which connects the top electrodes to a high-conductivity interconnect metal layer.

In this letter, both BST capacitors and HEMT devices were fabricated on the same samples. A schematic cross-section of the process and a completed parallel plate capacitor and HEMT device is shown in Fig. 1.

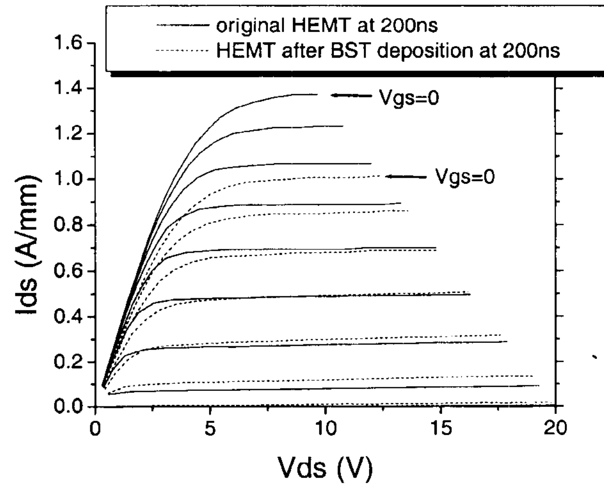

Fig. 2. The 200-ns pulsed I–V for HEMT device with BST deposition compared to control device.

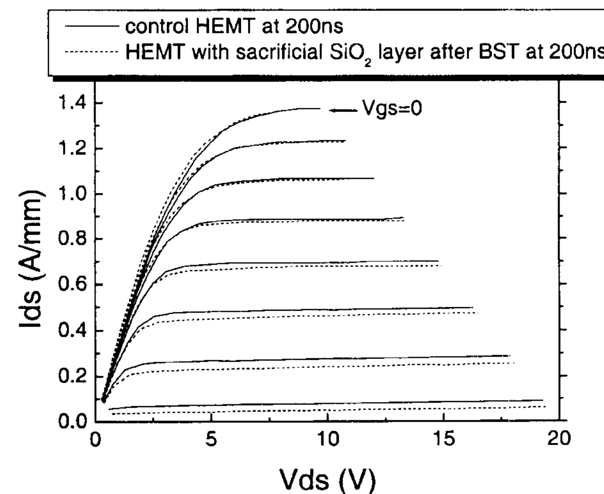

Fig. 3. The 200-ns pulsed I–V for HEMT device protected by sacrificial SiO_2 with BST deposition compared to control device.

III. Results and Discussion

Reference HEMT devices were fabricated without incorporating the BST film process as an experimental control sample. The HEMT devices were subjected to current–voltage (I–V) characterization. Pulsed I–V measurement at 200 ns shows the drain current density reaches 1.37 A/mm for $V_{gs} = 0$ V.

BST capacitors were first fabricated directly on the AlGaN surface before the HEMT process. Following the BST deposition, the BST was selectively removed and HEMT devices were fabricated in the area where the BST film was completely removed. In Fig. 2, pulsed I–V curves measured at 200 ns on both a control HEMT and a HEMT exposed to the plasma during BST growth are compared. Exposure to the plasma decreased the current density by 28% and decreased the magnitude of the pinch-off voltage from -7.5 to -6 V. Further investigation showed that both the sheet electron concentration and Hall mobility are decreased due to plasma damage in the HEMT structure during the BST sputtering [10]. To avoid this damage, a barrier layer is required to protect the 2DEG during BST growth. A thin SiO_2 layer was introduced for this purpose. Because of the stability of group III-nitrides, the SiO_2 layer should not react with the AlGaN. Since it can be wet etched uniformly by the same etchant (buffered HF) as the BST film, the choice of a SiO_2 buffer layer is compatible with both the GaN HEMT and BST capacitor processes.

Based on these initial findings, a 3000-Å SiO_2 layer was evaporated on the HEMT device area after bottom electrodes of the BST capacitors were pre-patterned. Following the BST deposition, both the SiO_2 and BST films were etched away from the HEMT device area using buffered HF during the BST pattern definition. In Fig. 3, pulsed I–V curves at 200 ns on both a control HEMT and a HEMT protected by SiO_2 were compared. The performance of the HEMT was not degraded by exposure to the BST deposition. A 3000-Å sacrificial SiO_2 layer efficiently protects HEMTs 2DEG channel. Additionally, the pinch off voltage did not change and the average ohmic contact resistance was the same as the control devices, indicating that the

SiO_2 did not react with the AlGaN during the approximately 3 h high temperature BST deposition.

While the sacrificial SiO_2 layer solved one problem, another problem in the integration is that the source/drain annealing causes a reduction in the BST capacitors' breakdown voltage. Before the source/drain annealing, the BST capacitors could sustain the application of more than a 20 V bias, but after the annealing the capacitors broke down at 3 V. Even for BST devices with pure Pt top electrodes, the breakdown voltage was still as low as 7 V. Devices with such low breakdown voltage cannot be used in high power microwave GaN HEMT circuits. To avoid this problem, the sequence of process steps was rearranged. Source and drain ohmic contacts were fabricated first, followed by the ebeam evaporation of a 3000-Å SiO_2 film. The BST capacitors were made following the completion of these two steps, with HEMT device mesa isolation and gate metallization following the BST capacitor fabrication. The complete process flow is depicted in Fig. 1.

The effect of the heater ramp rate during the BST deposition was also investigated. When the heater ramp rate was 50 °C/min, the ohmic contact resistance increased from 0.4 $\Omega \cdot$ mm to 0.9 $\Omega \cdot$ mm after BST deposition. In addition, the source and drain contacts appeared cracked, delaminated and discolored. The thermal mismatch between the ohmic contact metals and SiO_2 layer could account for both the metal and SiO_2 layers cracking during the rapid temperature change due to the heater ramping. With a slower heater ramp rate (20 °C/min) during BST deposition, no cracks, delamination, or significant discoloration was observed on the source and drain ohmic contacts. The average ohmic contact resistance was 0.4 $\Omega \cdot$ mm both before and after the BST deposition. A capacitance–voltage (C–V) measurement was performed on BST capacitors manufactured with the integrated GaN/AlGaN HEMT-BST process. The capacitance density at 0 V bias is 14.3 $fF/\mu m^2$ and the tunability is 3.3:1 with a 20 V bias. The capacitance density is about 50 times that of the usaual SiN (2000 Å) MMIC capacitor value, which is typically 0.3 $fF/\mu m^2$. The 1-MHz zero-bias Q factor of this film was 85.

IV. Conclusion

In this letter, a new method has been developed to incorporate BST thin-film capacitors in microwave circuits based on GaN HEMTs. A 3000-Å sacrificial SiO_2 layer protects the AlGaN surface and 2DEG from plasma damage. Reduction of the heater ramp rate to 20 °C/min during BST growth mitigates damage to the source and drain ohmic contacts, such as cracking and delamination. Using BST thin films, varactors and small area dc blocking capacitors can be integrated into GaN HEMT microwave circuits. High voltage (>20 V) operation and compatibility with a monolithic process are other advantages realized in this work. Higher operating valtages can be achieved by increasing the BST film thickness or using BST capacitors in series. Compact GaN MMIC circuits, such as power amplifiers, oscillators and VCOs, can be implemented with the integration of BST film to the GaN/AlGaN process.

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