

# Power and Linearity Characteristics of Field-Plated Recessed-Gate AlGaIn–GaIn HEMTs

A. Chini, D. Buttari, R. Coffie, L. Shen, S. Heikman, A. Chakraborty, S. Keller, and U. K. Mishra

**Abstract**—Record power density and high-efficiency operation with AlGaIn–GaIn high-electron mobility transistor (HEMT) devices have been achieved by adopting a field-plated gate-recessed structure. Devices grown on SiC substrate yielded very high power density (18.8 W/mm with 43% power-added efficiency (PAE) as well as high efficiency (74% with 6 W/mm) under single-tone continuous-wave testing at 4 GHz. Devices also showed excellent linearity characteristics when measured under two-tone continuous-wave signals at 4 GHz. When biased in deep-class AB (33 mA/mm, 3%  $I_{max}$ ) device maintained a carrier to third-order intermodulation ratio of 30 dBc up to a power level of 2.4 W/mm with 53% PAE; increasing bias current to 66 mA/mm (6%  $I_{max}$ ) allowed high linear operation (45 dBc) up to a power level of 1.4 W/mm with 38% PAE.

**Index Terms**—GaIn, high-electron mobility transistors (HEMTs), microwave power field-effect transistors (FETs).

## I. INTRODUCTION

AlGaIn–GaIn high-electron mobility transistors (HEMTs) represent the most promising devices for microwave and millimeter-wave power applications [1]. However, device performance is known to be often limited by the “dc-to-RF dispersion” phenomena. Surface traps, acting as a “virtual gate” in the gate–drain access region, prevent proper device operation, reducing the available current swing as well as degrading the knee voltage [2]. A method proved effective in reducing the dispersion phenomena is the introduction of a field-plated gate structure. This method was successfully applied by Asano *et al.* [3] on AlGaAs–GaAs HFETs, resulting in power densities as high as 1.7 W/mm at 1.5 GHz. Recently, Ando *et al.* [4] also applied this technique to AlGaIn–GaIn HFETs showing a significant improvement in device performance. Device linearity is also another important factor in order to meet the requirements of new generation communication systems. Previous work on GaAs-based HEMTs proposed increasing device transconductance as a viable solution to improve device linearity [5]. The advantages of increasing device transconductance have also been demonstrated for AlGaIn–GaIn HEMTs in [6]. In this letter, we report record single-tone and two-tone continuous-wave performance at 4 GHz of AlGaIn–GaIn HEMTs on SiC substrate, fabricated by adopting both a field-plate structure and gate recess. Uncooled devices yielded power densities up to 18.8 W/mm

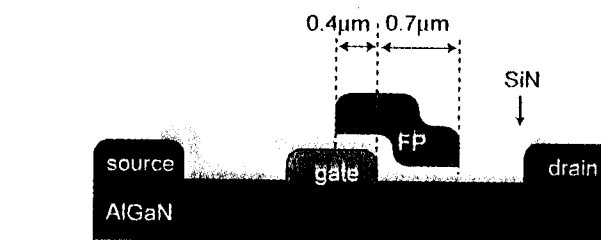


Fig. 1. Device cross section. After SiN plasma-enhanced chemical vapor deposition, a second gate is evaporated on the dielectric layer, acting as a field plate. The two gates are electrically shorted through the device pad and gate feeders.

with 43% peak power-added efficiency (PAE), and efficiencies up of 74% at 6 W/mm power density. When operated in deep class AB (3%  $I_{max}$ ), the device was capable of maintaining a carrier to third-order intermodulation ratio (C/I3) of 30 dBc up to a power level of 2.4 W/mm with 53% PAE. Increasing bias current to 6%  $I_{max}$  allowed highly linear operation (45 dBc), up to a power level of 1.4 W/mm with 38% PAE.

## II. DEVICE STRUCTURE

Device cross section is shown in Fig. 1. The devices tested were grown by metal–oxide chemical vapor deposition on an SiC substrate. The epitaxial growth began with a 200-Å GaIn nucleation layer, followed by a 3- $\mu$ m-thick insulating GaIn layer as a device buffer, followed by a 290-Å-thick Al<sub>0.22</sub>Ga<sub>0.78</sub>N barrier layer. Room-temperature sheet electron concentration and electron mobility were  $n_s \approx 0.84 \times 10^{13} \text{ cm}^{-2}$  and  $\mu \approx 1490 \text{ cm}^2/\text{Vs}$ , respectively. Device fabrication started with ohmic contact formation. Ti–Al–Ni–Au (200/1500/375/500 Å) were evaporated and annealed at 870 °C for 30 s in forming gas. Device mesa isolation was then formed by Cl<sub>2</sub> reactive ion etching. Transmission-line matrix measurements showed an average contact resistance of  $\approx 0.25 \Omega/\text{mm}$ , and a sheet resistance  $R_{sq} \approx 450 \Omega/\square$ . Gate recess was formed following the technique presented in [7]. Gate contact was then formed by evaporating Ni–Au–Ni (300/2500/500 Å) self-aligned with the gate recess. Etch depth was  $\sim 80 \text{ Å}$ . The next processing step was a 200-nm Si<sub>3</sub>N<sub>4</sub> passivation layer. The field plate was then formed by evaporating a second gate on top of the passivation layer. Field-plate metallization was Ni–Au–Ni (300/2500/500 Å). Field-plate extensions, with respect to the gate–drain edge, are 0.7  $\mu$ m toward the drain, and 0.4  $\mu$ m toward the source, resulting in a 1.1- $\mu$ m total length, as shown in Fig. 1. Electrical connection between the gate and field plate was formed through

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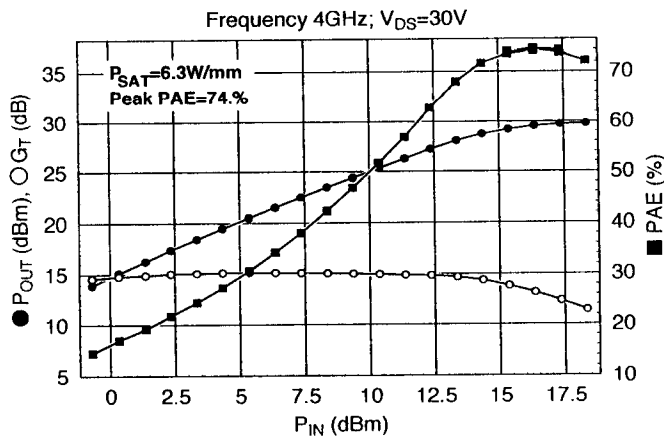


Fig. 2. Single-tone power measurement at 4 GHz. Bias point was  $V_{DS} = 30$  and  $I_{DS} = 33$  mA/mm. Saturated output power is 6.3 W/mm, while peak PAE is 74%. Output power density at peak PAE is 6 W/mm.

the common path of gate pad and gate feeder in the extrinsic device region. Gate width and length of the devices tested were  $2 \times 75 \mu\text{m}$ , and  $0.7 \mu\text{m}$ , respectively. Gate-source and gate-drain spacings were 0.7 and  $2 \mu\text{m}$ , respectively.

### III. DEVICES MEASUREMENTS

Devices were first tested using dc measurements. When measured under a constant dc-bias devices showed a maximum drain current level of approximately 1.1 A/mm, peak transconductance was  $\sim 260$  mS/mm, threshold voltage was  $\sim -2.9$  V, while catastrophic gate-drain breakdown occurred at approximately 150 V. At a drain bias of 25 V, small-signal measurements yielded peak  $f_t$  and  $f_{max}$  values of  $\sim 20$  and  $\sim 50$  GHz, respectively.

On-wafer RF power performance of uncooled devices were then tested using single-tone continuous-wave signal at 4 GHz. At a drain voltage of 30 V a maximum PAE of 74% with 6-W/mm power density was obtained (see Fig. 2). Saturated output power was 6.3 W/mm. The device was biased in class AB using a quiescent drain current of 33 mA/mm (3%  $I_{max}$ ), while device matching was optimized for maximum PAE. Load match was  $\Gamma_L = 0.855 + j0.1$  corresponding to the maximum  $|\Gamma_L|$  available with our tuning range ( $\max |\Gamma_L| \simeq 0.86$ ). Source matching point was  $\Gamma_S = 0.65 + j0.49$  still within the available tuning range of the system ( $\max |\Gamma_S| \simeq 0.86$ ). When matched for best power performances (not shown), device yielded approximately 8 W/mm with a PAE of  $\sim 50\%$ . Device were then measured at a drain bias of 90 V using a quiescent drain current of 33 mA/mm. Due to the limited tuning range, best power/PAE performances were obtained at  $\Gamma_L = 0.855 + j0.1$ . Source match-point was  $\Gamma_S = 0.79 + j0.23$ , and had little influence on device performance ( $P_{SAT}$ , PAE), except for device power gain, that was maintained at a 13 dB value. Total saturated output power was 18.8 W/mm, while peak PAE was 43%.

The reduced PAE obtained is believed to be a consequence of the limited tuning range rather than device knee walk out. Details on knee walk-out will be addressed elsewhere, since they go beyond the purpose of this letter. Moreover, we believe that operation at 90 V was achieved under a reduced voltage swing due

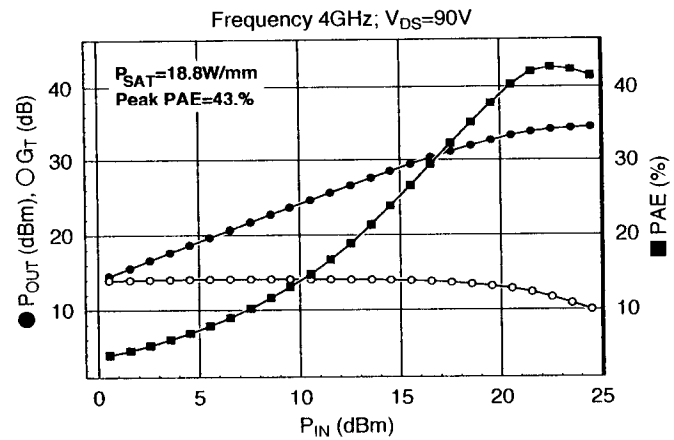


Fig. 3. Single-tone power measurement at 4 GHz. Bias point was  $V_{DS} = 90$  and  $I_{DS} = 33$  mA/mm. Saturated output power is 18.8 W/mm, while peak PAE is 43%.

to an imperfect load match. At this point some speculations are needed in order to clarify device operation. Although a correct calculation of the voltage-current swing during RF measurements is difficult, some approximation can be made in order to estimate the actual voltage swing. First, the load impedance has to be calculated; in this case,  $\Gamma_L = 0.855 + j0.1$  corresponds to a load impedance of

$$Z_L = Z_O \frac{1 + \Gamma_L}{1 - \Gamma_L} \simeq (417 + j322)\Omega. \quad (1)$$

The equivalent parallel representation of this impedance is

$$Z_{LP} = R_{LP} || jX_{LP} \simeq (666 || j862)\Omega. \quad (2)$$

Assuming that 1) the reactive component of the load compensate the capacitive component at the device output and 2) all the harmonics are presented with a short circuit [8], it can be easily demonstrated that the RF signal will clip because of the maximum device current ( $I_{max}$ ). For the device tested,  $I_{max}$  was 165 mA (1.1 A/mm). At the onset of compression, the voltage swing on  $R_{LP}$  is  $\Delta V = I_{max} \times R_{LP} \simeq 110$  V. Thus, the maximum drain voltage reached during RF operation will be  $90 \text{ V} + \Delta V/2 = 145$  V. In the present case the harmonics were not terminated. Assuming a simple resonant inductance-capacitance network on the output a value of  $\sim 142$  V was obtained by simulations. Both values are within the operating voltage of the device.

Uncooled device linearity at 4 GHz was then tested on wafer using two-tone continuous-wave signal, with a tone spacing of 100 kHz. Tone amplitude was calibrated to be within a 0.1-dB difference. The carrier-to-third-order intermodulation ratio (C/I3) was calculated using the larger intermodulation product between the IM3-low and IM3-high products (i.e., worst case). However, the difference between IM3-low and IM3-high was typically below 1 dBc across the swept range. When biased at 30 V under deep-class AB condition (33 mA/mm), the device was capable of maintaining a C/I3 level of 30 dBc up to power level of 2.4 W/mm with 53% PAE [see Fig. 4(a)]. Increasing the bias current to 66 mA/mm resulted in better linearity characteristics, while maintaining a C/I3 level of 45 dBc device yielded power level of 1.4 W/mm with 38% PAE [see Fig. 4(b)]. While load matching was equivalent

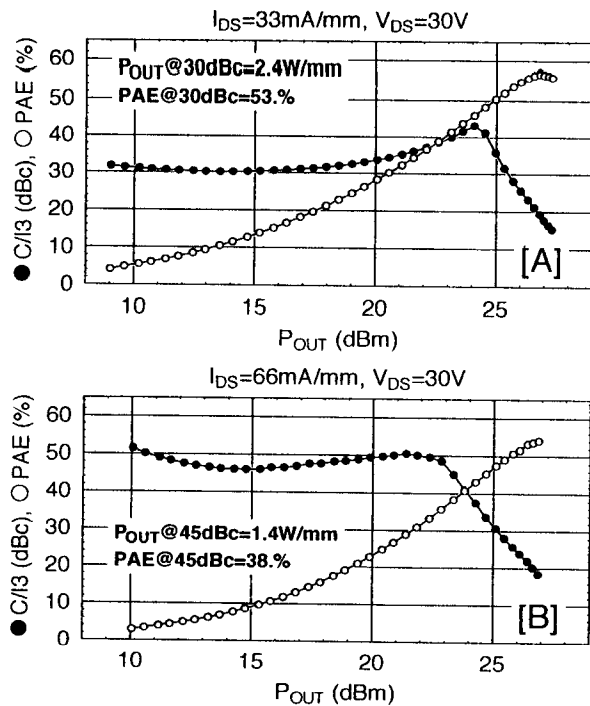


Fig. 4. Two-tone linearity measurements carried out at 4 GHz, with 100 kHz tone spacing. (a) Bias point was  $V_{DS} = 30$  V,  $I_{DS} = 33$  mA/mm. Device maintains a  $C/I3$  level of 30 dBc while yielding 2.4 W/mm power density with 53% PAE. (b) Bias point was  $V_{DS} = 30$  V,  $I_{DS} = 66$  mA/mm. Device maintains a  $C/I3$  level of 45 dBc while yielding 1.4-W/mm power density with 38% PAE.

to the single-tone measurements previously presented, source matching was optimized in order to achieve best  $C/I3$  versus PAE performances ( $\Gamma_S = 0.79 + j0.23$ ). Power gain was in the 10–11 dB range.

#### IV. CONCLUSION

In conclusion, power and linearity performance of AlGaIn-GaN HEMTs fabricated with a field-plated and

gate-recessed structure have been presented. Uncooled devices on SiC substrates yielded PAEs up to 74% (6 W/mm) with power densities up to 18.8 W/mm (43% PAE) under continuous-wave single-tone testing at 4 GHz. Device linearity also proved to be very promising: at  $C/I3$  level of 30 dBc device yielded 2.4 W/mm with 53% PAE when operated in deep class AB (33 mA/mm). Increasing the quiescent drain current level to 66 mA/mm allowed linear operation at 45 dBc up to 1.4 W/mm with an associated 38% PAE. These linearity results are believed to be the best power/PAE combinations for linear operation (30–45 dBc) at 4 GHz achieved to date.

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