

Distributed Analog Phase Shifters with Low Insertion Loss

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Abstract—This paper describes the design and fabrication of distributed analog phase-shifter circuits. The phase shifters consist of coplanar-waveguide (CPW) lines that are periodically loaded with varactor diodes. The circuits are fabricated on GaAs using standard monolithic processing techniques. The phase velocity on these varactor diode-loaded CPW lines is a function of applied reverse bias, thus resulting in analog phase-shifting circuits. Optimally designed circuits exhibit 0° – 360° phase shift at 20 GHz with a maximum insertion loss (IL) of 4.2 dB. To the best of our knowledge, this is the lowest reported IL for a solid-state analog phase shifter operating at 20 GHz.

Index Terms—Distributed circuit, phase shifter.

I. INTRODUCTION

DIODE-LOADED transmission lines have been used for a variety of applications, both nonlinear [1]–[4] and linear [5]–[7]. In the linear (small-signal) regime, the diode-loaded line behaves like a synthetic transmission line with voltage variable phase velocity and can, therefore, be used as a time-delay/phase-shift element. In recent demonstrations [5], [6], diode-loaded lines have been used as true time-delay elements in prototype phased arrays. The useful frequency range of these time-delay elements was relatively low (<5 GHz) due to limitations imposed by the hybrid implementation adopted there. In this paper, we present a monolithic version of a distributed phase-shifter circuit that has been optimized for low-loss operation at 20 GHz. The circuit is comprised of a high-impedance coplanar-waveguide (CPW) line periodically loaded with varactor diodes. The distributed phase-shifter circuit described here is capable of producing a continuously variable 0° – 360° phase shift at 20 GHz with a maximum insertion loss (IL) of 4.2 dB and return loss better than -12 dB over all phase states.

In addition to low IL, this circuit has several desirable features—the phase shift can be controlled with any desired resolution, as opposed to digital phase shifters where the number of bits fixes the resolution. This results in more accurate beam control when used in phased arrays. Since the phase velocity on the diode-loaded line is a function of the bias voltage across the varactor diodes (all the diodes share the same bias since they are in parallel), only one control line is needed. This is an advantage over a switched line or switched network phase shifters where the number of control lines is equal to the number of bits. The circuit

dissipates very low DC power as the varactor diodes are reverse biased in all phase states and draw extremely low currents. The Schottky diodes employed in the phase shifter have fast response times, enabling rapid phase control and beam scanning. The circuit is suitable for low-cost monolithic production and is desirable from an integration standpoint since the fabrication process is compatible with standard GaAs monolithic-microwave integrated-circuit (MMIC) technology. Also, the distributed nature of the circuit makes it less sensitive to small variations in the varactor diode properties, making the design robust.

The layout of this paper is as follows. We first present the basic principle of operation of the distributed phase-shifter circuits and the relevant design equations. The effects of the various design parameters on the total circuit loss are then discussed, along with strategies to minimize the IL. Details of the monolithic fabrication process are followed by RF measurements on the fabricated circuits. The experimental data is compared with expected performance based on the design equations. The simple synthetic transmission-line model is refined to obtain better agreement with measured performance.

II. BASIC PRINCIPLE AND DESIGN EQUATIONS

The distributed phase-shifter circuit, shown in Fig. 1(a), is comprised of a high-impedance (Z_i) transmission line periodically loaded with voltage variable capacitors (C_{var}) with spacing L_{sect} . We can define a unit cell for this periodic structure, which consists of a section of transmission line of length L_{sect} and a shunt variable capacitor to ground. The transmission-line section can be approximated as a lumped inductance (L_t) and capacitance (C_t), as shown in the equivalent circuit in Fig. 1(b). This periodic structure has a Bragg frequency [1], [2] given by (1) as follows:

$$f_{\text{bragg}} = \frac{1}{\pi \sqrt{L_t(C_t + C_{\text{var}})}} \quad (1)$$

$$L_t = \frac{L_{\text{sect}}}{v_i} Z_i$$

$$C_t = \frac{L_{\text{sect}}}{Z_i v_i} \quad (2)$$

where L_t and C_t are the inductance and capacitance per unit cell and Z_i and v_i are the impedance and phase velocity on the high-impedance line, respectively. For frequencies well below the Bragg frequency, the periodically loaded line may be treated as a synthetic transmission line [see Fig. 1(c)] whose capacitance per unit length has been increased due to the periodic loading. The inductance per unit length for this

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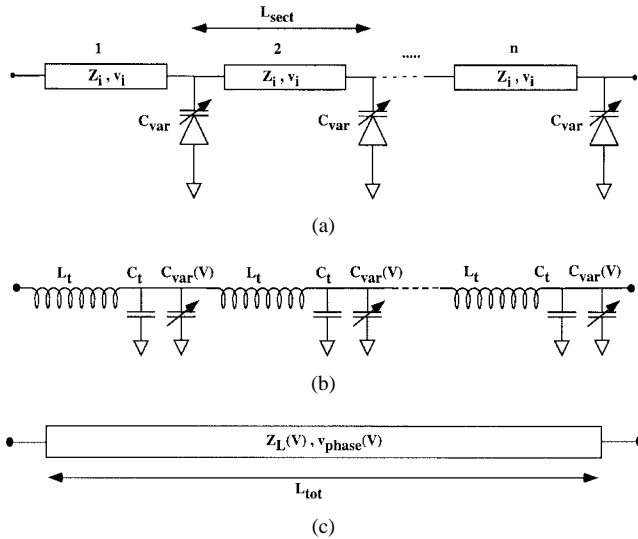


Fig. 1. (a) Schematic of a distributed phase-shifter circuit showing a high-impedance line (Z_i) periodically loaded with varactor diodes (C_{var}) with diode spacing L_{sect} . (b) Equivalent circuit for the varactor diode loaded line. (c) Synthetic transmission line with voltage-dependent characteristic impedance ($Z_L(V)$) and phase velocity ($v_{phase}(V)$).

synthetic line is unchanged from that of the original unloaded line. Since the loading capacitors are voltage dependent, the properties of this synthetic transmission line, such as its characteristic impedance and phase velocity, are voltage dependent (3)–(5). Thus, it is possible to change the phase shift for a given length of line by changing the bias voltage. This is the essential principle behind the distributed phase-shifter circuit

$$Z_L = \sqrt{\frac{L_l}{(C_l + C_{var}(V)/L_{sect})}} \quad (3)$$

$$v_{phase} = \frac{1}{\sqrt{L_l(C_l + C_{var}(V)/L_{sect})}} \quad (4)$$

$$L_l = \frac{Z_i}{v_i} \quad (5)$$

$$C_l = \frac{1}{Z_i v_i}$$

Note that, in (3)–(5), the line inductance (L_l) and line capacitance (C_l) are normalized per unit length. In assuming a synthetic transmission line, we are essentially distributing the discrete variable capacitance over the length of the cell. This is why all terms involving C_{var} are divided by the spacing between capacitors L_{sect} . As will be shown, this approach breaks down in the vicinity of the Bragg frequency and a more exact analysis must recognize the discrete nature of the loading.

We now present equations used to design distributed phase-shifter circuits. These equations are based on the synthetic transmission-line approach, which is valid at frequencies well below the Bragg frequency. Two important parameters used here are the loading factor “ x ” and the capacitance ratio “ y ,”

” which are defined as follows:

$$x = \frac{C_{var}^{max}/L_{sect}}{C_l} \quad (6)$$

$$y = C_{var}^{min}/C_{var}^{max}. \quad (7)$$

The parameter y is just the ratio of the minimum-to-maximum varactor capacitance. The loading factor (x) is the ratio of maximum varactor capacitance per unit length to the transmission line (C_l) capacitance per unit length.

The first key design relationship is obtained by imposing the constraint that when the varactor is in its maximum capacitance state, the loaded-line characteristic impedance (Z_L) be 50Ω . Using this condition with (3), (5), and (6) gives a relation between the unloaded line impedance (Z_i) and the loading factor

$$Z_i = 50\sqrt{1+x}. \quad (8)$$

Equation (8) indicates that, for higher loading factors, the unloaded line impedance must be higher in order to keep the impedance of the loaded line 50Ω .

Combining (1), (2) and (6), we obtain a relationship linking the diode spacing L_{sect} to the minimum Bragg frequency and loading factor. From (1), it is easily seen that the Bragg frequency depends on the bias and is minimum when the varactor capacitance is maximum

$$L_{sect} = \frac{v_i}{\pi f_{bragg}^{min} \sqrt{1+x}}. \quad (9)$$

Equation (9) indicates that once we have decided what minimum Bragg frequency to use, the diode spacing becomes a function of the loading factor alone. Care must be taken to ensure that the minimum Bragg frequency is higher than the frequency of interest.

Another important design variable is the maximum varactor capacitance, calculated from the definition of the loading factor. Using (5) and (6), it can easily be shown that

$$C_{var}^{max} = x L_{sect} C_l = x \frac{L_{sect}}{Z_i v_i}. \quad (10)$$

Since L_{sect} and Z_i have already been expressed in terms of known quantities and the loading factor x , it possible to express the maximum varactor capacitance as a function of x alone (10).

At any given frequency f , the maximum possible differential phase shift obtainable from a single section is given by

$$\delta\phi = 2\pi f \frac{L_{sect}}{v_i} \left(\sqrt{1+x} - \sqrt{1+xy} \right) \quad (11)$$

Equation (11) tells us that increasing loading (x) and/or the capacitance ratio (y) results in more differential phase shift. This makes intuitive sense because both these conditions lead to higher variation in phase velocity. The number of sections (n_{sect}) required for a 360° phase shifter at frequency f is given by

$$n_{sect} = \frac{2\pi}{\delta\phi}. \quad (12)$$

The quantities Z_i , L_{sect} , C_{var} , and n_{sect} completely specify the distributed phase-shifter circuit design. Thus, we have succeeded in specifying the entire design in terms of the loading factor (x).

We are mainly interested in studying the circuit loss as a function of loading factor (x). The total circuit loss has two components: diode loss and transmission-line loss (dependent on the type of transmission line). Thus, to further the analysis, it becomes necessary to assume a specific transmission-line geometry. We analyze here in detail the case of a CPW line loaded with varactor diodes. For this particular case, the total IL is given by [1]

$$\text{IL} = n_{\text{sect}} \pi \frac{f^2}{f_s} C_{\text{var}}^{\text{max}} Z_L + n_{\text{sect}} L_{\text{sect}} \alpha(Z_i) \frac{Z_i}{Z_L} \quad (13)$$

$$f_s = \frac{1}{2\pi r_i C_{\text{var}}^{\text{max}}} \quad (14)$$

where f_s is the diode cutoff frequency. The first term in (13) describes the diode loss, and increases as the square of the frequency. The second term in (13) is due to skin losses in the CPW conductors. The attenuation per unit length $\alpha(Z_i)$ on the CPW line is given by [8, eq. (13.16)] and depends on the unloaded line impedance (Z_i), substrate dielectric constant, metal thickness (t), and CPW linewidth. Note that the CPW loss term is multiplied by the factor (Z_i/Z_L) to account for the effect of the loading. The loss analysis (13)–(14), presented above, is specific to the case of varactor diodes loading a CPW line, but (1)–(12) are applicable to distributed phase-shifter circuits using any transmission-line geometry and device technology.

Fig. 2 shows curves of loss versus loading factor for varactor-loaded CPW lines. The parameters used for these curves are appropriate for circuits fabricated on GaAs: substrate dielectric constant (ϵ_s) of 13, CPW conductor thickness (t) of 1.8 μm , diode cutoff frequency (f_s) of 700 GHz, and capacitance ratio $y = 0.45$. The loss per section shown in Fig. 2(a) is calculated at 20 GHz. The number of sections is determined from (12) for a circuit capable of producing 360° of phase shift at the same frequency. As the loading factor is increased, the phase shift per section is increased as discussed in (11), thus, fewer sections are required to get the desired 360° phase shift. At the same time, the loss per section due to CPW skin losses increase rapidly since the required interconnect impedance is increasing (higher CPW impedances require narrower center conductors, which result in higher losses). The diode loss per section also increases, but not as rapidly as the CPW loss. Since the loading and unloaded line impedance are linked by (8), the plot in (2a) uses Z_i as an alternate x -axis.

Fig. 2(b) indicates that the total diode loss decreases slowly with increasing loading factor. The total CPW loss curve, on the other hand, is U-shaped with an optimum loading factor of 1.2 for minimum loss. For loading below the optimum, the number of required sections increases rapidly, whereas for loading factors greater than 1.2, the loss per section increases strongly. The total circuit loss, which is the sum of the total diode loss and total CPW loss, also shows a minimum loss at a loading factor of 1.2. Similar trends have been reported by

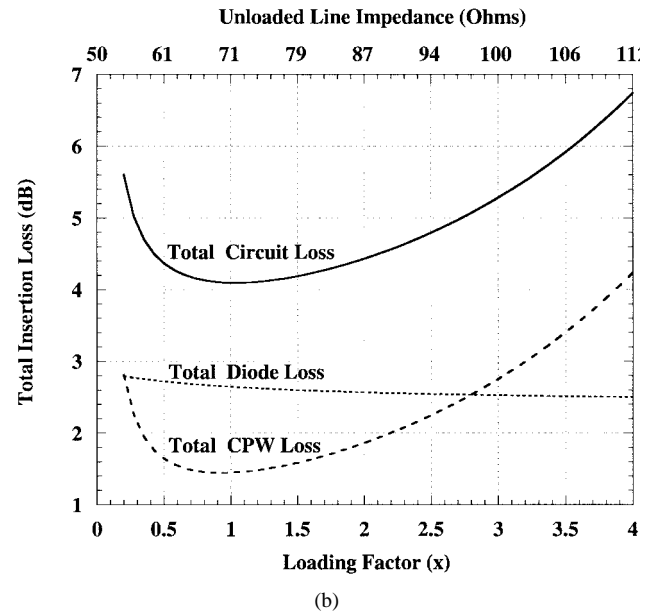
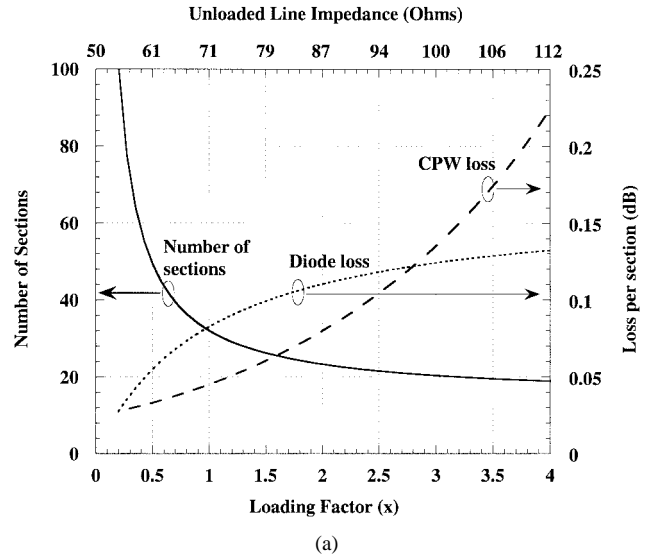


Fig. 2. Low-loss design curves for a distributed phase shifter on GaAs. (a) Number of sections required for 360° of phase shift at 20 GHz. Also depicted are the diode and CPW losses per section as function of the loading factor (x). (b) Total circuit loss at 20 GHz for a 360° phase shifter as a function of loading factor (x).

Rodwell *et al.* [1] in their nonlinear transmission lines. It is important to emphasize that this optimum value is specific to varactor-loaded CPW lines on GaAs whose parameters were used here. However, it is relatively straightforward to repeat the calculations for other parameters/transmission-line types.

III. CIRCUIT FABRICATION

Distributed phase-shifter circuits with different values of the loading factor (x) were fabricated on the same wafer. The GaAs epitaxial layers for the Schottky varactor diodes were grown by molecular beam epitaxy (MBE) on a semiinsulating GaAs substrate of thickness 600 μm . In order to reduce the series resistance, a heavily doped (n^+) layer of thickness 9000 \AA and doping $8 \times 10^{17}/\text{cm}^3$ was included below the active layer (n^-) of doping $5 \times 10^{16}/\text{cm}^3$ and thickness 5000 \AA ,

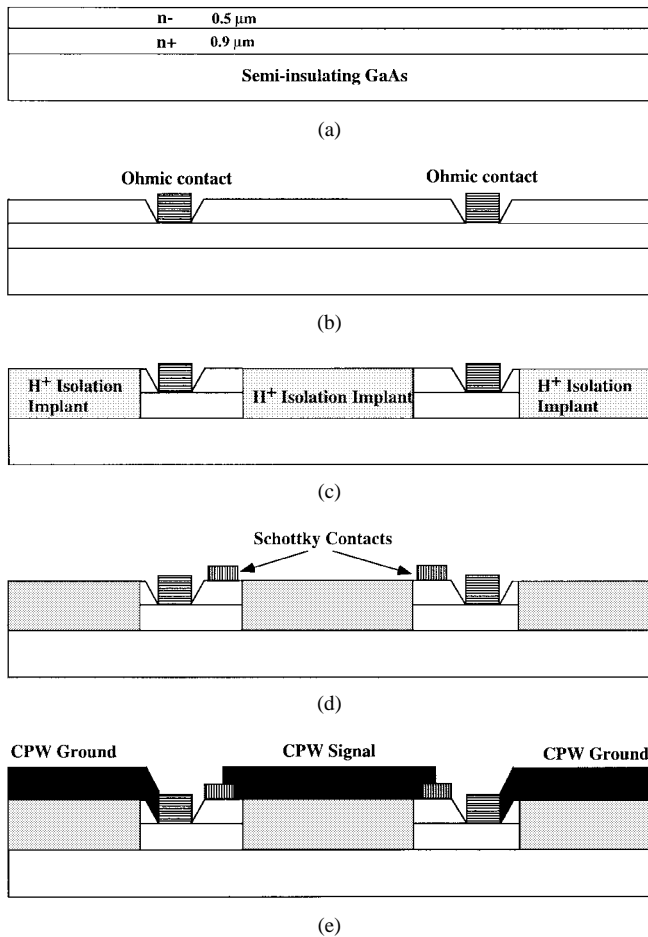


Fig. 3. (a) Epitaxial layer structure used in the Schottky varactor diodes. (b)–(e) Process flow diagram for the monolithic fabrication of the distributed phase-shifter circuits.

as shown in Fig. 3(a). Standard GaAs processing techniques similar to those used in [9] were employed here. The process flow diagram is depicted in Fig. 3(b)–(e). Ohmic contacts were made after etching down to the heavily doped layer n^+ layer and then evaporating AuGe/Ni/Au. The contacts were alloyed in a rapid thermal annealer at 400 °C for 1 min. Next, the diodes were isolated using proton (H^+) implants. Two implants of energies 120 and 170 KeV were used to ensure adequate isolation over the entire epitaxial layer thickness. Schottky contacts were made by depositing Ti/Pt/Au metal directly on the lightly doped (n^-) active layer. The interconnect and CPW lines were deposited by evaporating 1.8-μm-thick Ti/Au and were patterned using the liftoff technique. The final step was the etch of the n^- layer in order to reduce the fringing capacitance. The etch was performed using Cl_2 reactive ion etching (RIE) and the Schottky metal was utilized as the mask. Details of this step can be found in [10].

Fig. 4(a) shows the layout of a fabricated circuit. In order to preserve the symmetry of the structure, the loading capacitors were implemented as two varactor diodes connected from the CPW center conductor to either ground plane. Each varactor has half the designed zero bias capacitance and in parallel they give the correct loading capacitance value. For ease of

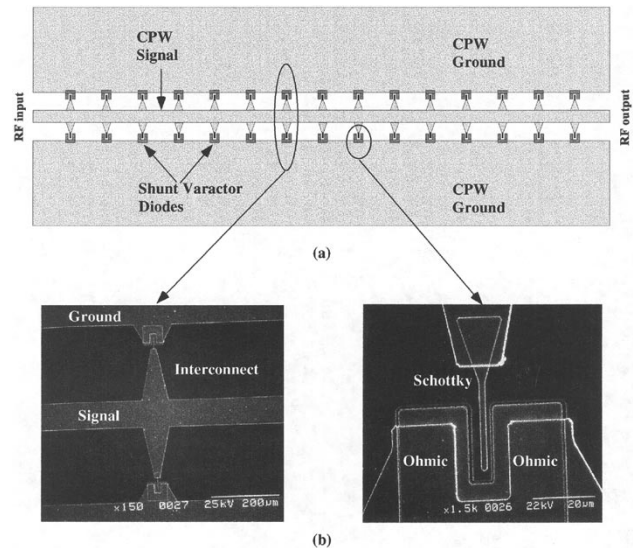


Fig. 4. (a) Layout of the fabricated distributed phase-shifter circuit showing the symmetric arrangement of the shunt varactor diodes. (b) SEM images of the fabricated circuit showing the connection details and layout of the Schottky varactor diodes.

fabrication, the Schottky contact width was limited to 2 μm and alignment tolerances of 3 μm were used throughout the process. Details of the fabricated Schottky diode can be seen in the SEM image in Fig. 4(b).

IV. DC AND RF CHARACTERIZATION

The processed wafer included several test structures to study the DC performance and the low-frequency (1 MHz) capacitance versus voltage characteristics of the Schottky diodes. DC I - V characterization of the Schottky diodes was done on an HP 4145 Semiconductor Parameter Analyzer. The Schottky diodes had an ideality factor of 1.05, series resistance (r_s) of 3.4 Ω, and reverse-breakdown voltage of -15 V. The zero bias capacitance ($C_{var}(0)$) at 1 MHz was measured to be 65 fF and the capacitance ratio (y) was 0.45 at a reverse bias of -10 V.

RF measurements were made on an HP 8510B network analyzer that was calibrated using on-wafer standards. One-port S_{11} measurements were made on test varactor diodes mounted at the end of CPW lines. The measured S_{11} data for the varactor diodes was fitted to a series RC model and good agreement was obtained with the DC values listed above. Based on the extracted parameters, the small-signal cutoff frequency (f_s) for the varactor diodes is estimated to be ~700 GHz using (14).

The processed wafer had phase-shifter circuits with loading factors of 0.4, 1.2, and 3.2, in order to test out the theory that there exists an optimum loading factor for a given substrate dielectric constant (ϵ_{sub}), varactor diode cutoff frequency (f_s), and capacitance ratio (y). For the parameters used here ($\epsilon_s = 13$, $f_s = 700$ GHz, $y = 0.45$, and $f_{bragg} = 30$ GHz), the design equations used in Section II had predicted an optimum loading factor (x) of 1.2. Fig. 5 shows that the measured values of IL compare quite well with the theoretically predicted values. This data gives us confidence in

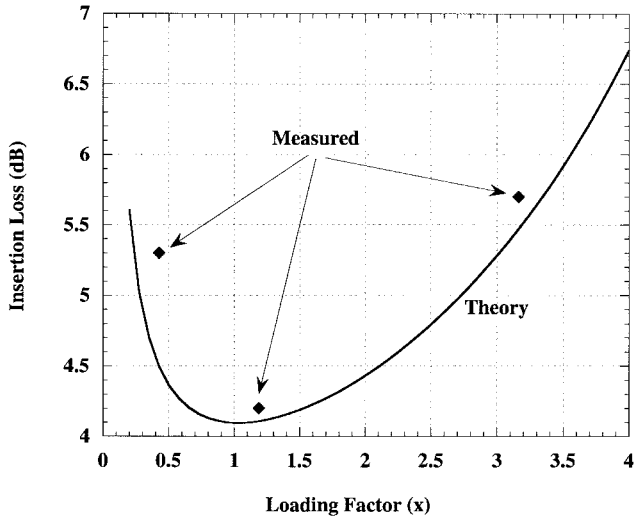


Fig. 5. Comparison of theoretically calculated and measured IL versus loading factor (x). The losses are specified at 20 GHz for distributed 360° phase shifters on GaAs.

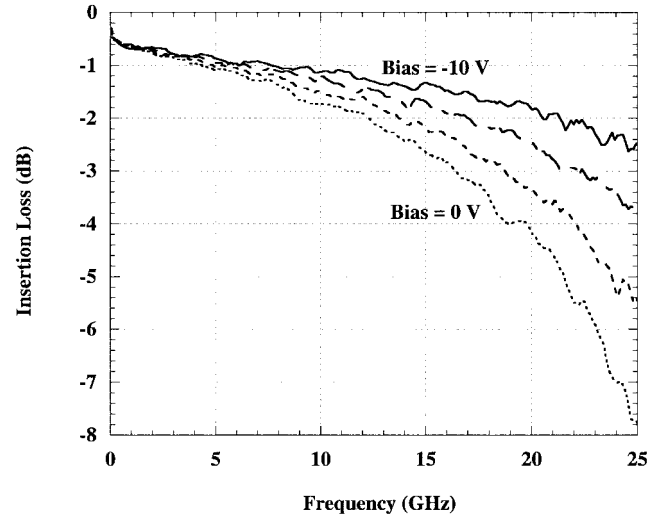


Fig. 7. Measured IL curves for different applied bias values for an optimally loaded 360° phase shifter.

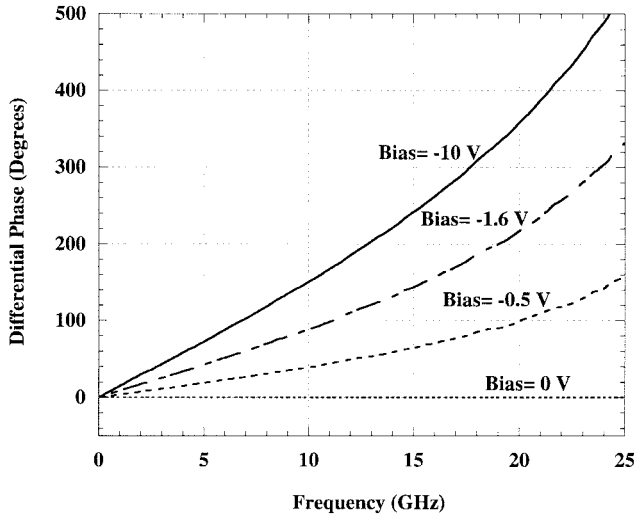


Fig. 6. Differential phase shift versus frequency curves for different applied bias values. Measurements were made on an optimally loaded circuit ($x = 1.2$).

the design equations and provides strong evidence that there is an optimum loading condition.

The detailed performance characteristics of only the optimally loaded ($x = 1.2$) distributed phase-shifter circuit are presented here. Fig. 6 shows the differential phase shift as a function of frequency for several reverse-bias values. It can be seen from this graph that, at 20 GHz, the differential phase shift is continuously variable from 0° to 360° by adjusting the reverse bias on the CPW center conductor. For frequencies up to 15 GHz, the distributed phase-shifter circuit behaves like a variable velocity transmission line and the phase shift varies linearly with frequency. As the frequency approaches the Bragg frequency (30 GHz), the phase shift becomes nonlinear, and a better model is presented in the following section that is capable of predicting this behavior. The maximum IL at 20 GHz occurs at zero bias and is only 4.2 dB (for the optimally loaded circuit), as can be verified from Fig. 7. Also,

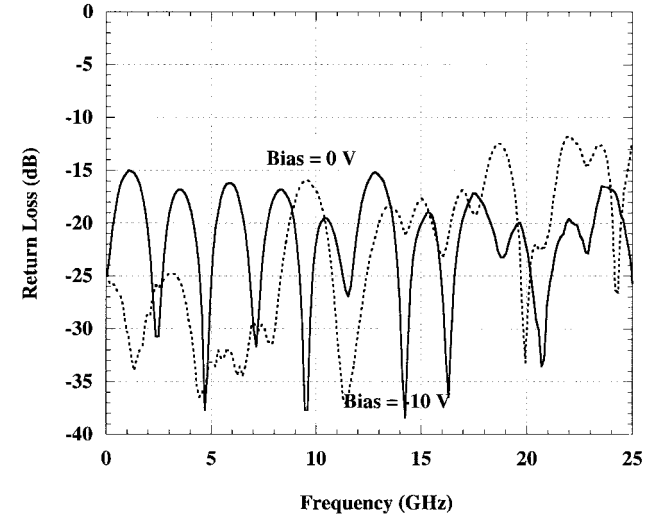


Fig. 8. Measured return loss versus frequency curves for the two extreme bias values. Curves for intermediate bias values have been suppressed for clarity of presentation.

the return loss is less than -12 dB over all phase states, as shown in Fig. 8. This indicates that the impedance of the loaded line is close to 50Ω and does not vary strongly with bias since the voltage-dependent varactor capacitance does not dominate over the CPW line capacitance.

V. ANALYSIS AND MODELING OF RESULTS

As has been mentioned earlier, the synthetic transmission-line model is only valid for frequencies well below the Bragg frequency. A more accurate model is based on the lumped-element equivalent circuit depicted in Fig. 1(b). The $ABCD$ propagation matrix for a unit cell is expressed in terms of the equivalent lumped elements L_t , C_t , and C_{var} . In order to model the diode-based losses, the series resistance (r_s) is converted to an equivalent conductance G_{var} in parallel with the capacitor (15)

$$G_{\text{var}} \approx (2\pi f C_{\text{var}}^{\text{max}})^2 r_s. \quad (15)$$

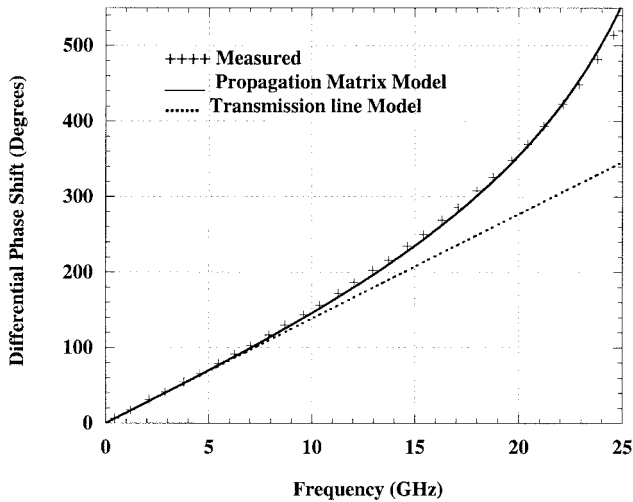


Fig. 9. Comparison of measured and modeled curves for maximum differential phase shift versus frequency (for an optimally loaded distributed phase-shifter circuit).

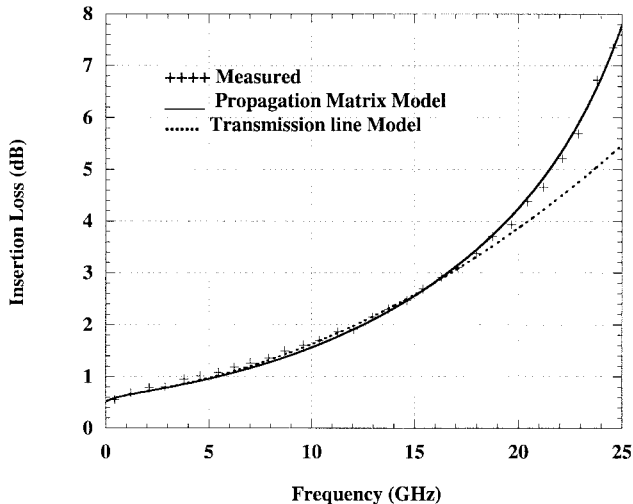


Fig. 10. Comparison of measured and modeled zero-bias IL as a function of frequency (for an optimally loaded differential phase-shifter circuit).

On solving for the complex propagation constant ($\Gamma = \alpha + j\beta$) for the unit cell, the following equations are obtained (see [9]):

$$\cosh(\alpha) \cos(\beta) = 1 - (2\pi f)^2 \frac{L_t(C_t + C_{\text{var}})}{2} \quad (16)$$

$$\sinh(\alpha) \sin(\beta) = (2\pi f) \frac{L_t G_{\text{var}}}{2}. \quad (17)$$

For small attenuation α per unit cell, the above equations can be written in the following simpler form:

$$\cos(\beta) = 1 - (2\pi f)^2 \frac{L_t(C_t + C_{\text{var}})}{2} \quad (18)$$

$$\alpha = (2\pi f) \frac{L_t G_{\text{var}}}{2\sqrt{1 - \cos(\beta)}}. \quad (19)$$

Note that the attenuation calculated above is due to diode losses only, and the second term in (13) that determines the CPW skin loss must be added to obtain the total circuit loss. Figs. 9 and 10 show comparisons of the measured phase

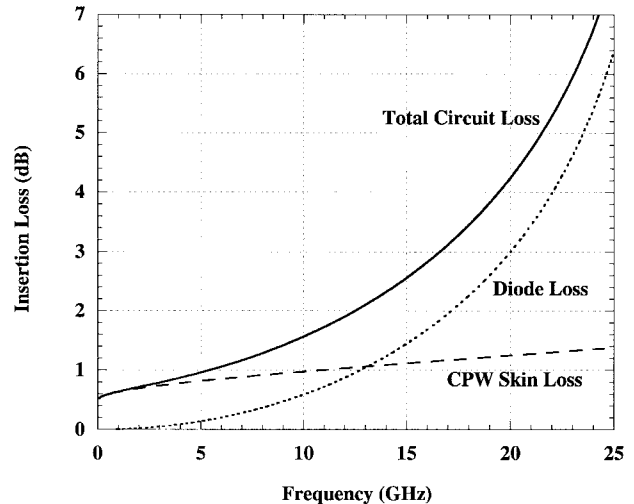


Fig. 11. Relative contributions of the diode loss and CPW skin loss to the zero-bias IL.

shift and IL with theoretically predicted results. The optimally loaded phase-shifter circuits are modeled using measured parameters from Section III. At low frequencies, both the theoretical models predict identical behavior and match the measured data well. For frequencies above 15 GHz, the synthetic transmission-line model fails to predict the rapid increase in loss and phase shift with frequency, while the propagation matrix method continues to show good agreement with experimental data.

Using the theoretical loss model, it is possible to study the relative contributions of the CPW loss term and the diode loss term as a function of frequency. Fig. 11 shows one such set of curves for the optimally loaded phase shifter. From these curves, it is apparent that at 20 GHz the diode losses are the dominant mechanism and, therefore, future attempts to further reduce circuit losses must be aimed at reducing diode series resistance. This is easily achievable using more aggressive layout design rules—by reducing the Schottky contact width to 1 μm and doubling the diode perimeter, it should be possible to decrease the series resistance by half for the same capacitor value.

Another interesting feature of the distributed phase-shifter circuit is that the design can be easily scaled to different frequencies. The scaling here is just simply the addition or removal of sections, i.e., length scaling. Fig. 12 shows the predicted loss for 360° phase shifters designed for operation at different frequencies. It is apparent that by picking the appropriate number of sections, it is possible to design this circuit with less than 4.2-dB IL at any frequency in the 7–20-GHz range. Note that a single circuit does not cover this frequency range.

VI. CONCLUSIONS

We have presented design equations for distributed phase-shifter circuits. The specific case of Schottky varactor-diode-loaded CPW lines on GaAs was analyzed in detail. Optimum loading conditions for minimum circuit loss were determined from the design equations. Measured losses on 360° phase

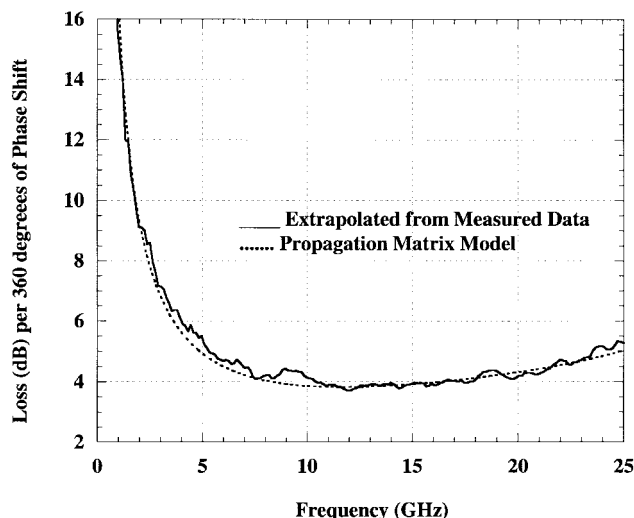


Fig. 12. Curve predicting losses for the distributed phase shifter if the design was scaled to obtain 360° phase shift at different frequencies.

shifters fabricated on GaAs showed good agreement with the theoretical predictions and demonstrated a minimum loss for a loading factor of 1.2. The optimally loaded phase shifter demonstrated continuous phase shift from 0° to 360° at 20 GHz with a maximum IL of 4.2 dB. To the best of our knowledge, this is the lowest reported IL for an analog solid-state phase shifter at 20 GHz. We also presented a model capable of analyzing the distributed phase-shifter circuits up to the Bragg frequency. Using this model, we showed that at 20 GHz, the majority of the circuit losses are due to the varactor diodes and that by more aggressive diode design, it is possible to reduce the total circuit loss below 3 dB.

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