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99 (1996).

ortens, K. A. Muller, Europhys. Lett. **17**,

Watanabe, H. Ono, M. Yoshida, Integr.

n, T. Venkatesan, D. W. Reagor, Appl.

ls, C. H. Mueller, R. E. Treece, T. V.

Tech. **11**, 1323 (1998).

A. R. Bishop, N. Gronbech-Jensen, Q.
86, 1558 (1999).

, G. Kaduchak, K. O. Rasmussen, A. R.

o, J. Appl. Phys. **84**, 993 (1998).

ew York, 1929).

5 (1983).

966).

FIRST DEMONSTRATION OF A PERIODICALLY LOADED LINE PHASE SHIFTER USING BST CAPACITORS

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ABSTRACT

Periodically loaded line phase shifter circuits using voltage tunable $BaSrTiO_3$ (BST) parallel plate capacitors have been demonstrated at X-band. The first such phase shifter circuit was capable of 100° of phase shift with an insertion loss of 7.6 dB at 10 GHz. Subsequently, the monolithic fabrication procedure was refined resulting in an improved phase shifter circuit with 200° of phase shift and an insertion loss of 6.2 dB at 10 GHz. In addition to promising loss performance (32°/dB) at 10 GHz, the circuits reported here have several desirable features such as moderate control voltages (20 V), room temperature operation, and compatibility with monolithic fabrication techniques.

INTRODUCTION

The cost of phase shifters is a major component of the cost of modern phased array antennas. Thus it is of paramount importance to reduce the cost of phase shifters to ensure widespread acceptance of phased arrays in military/civilian applications. Ferroelectric thin film based phase shifters promise to be low cost because of two factors- 1) the ferroelectric material can be deposited relatively inexpensively using RF sputtering/MOCVD 2) the films can be processed using low cost, high volume monolithic fabrication techniques. Apart from cost, the use of ferroelectric thin films in phase shifter circuits also has potential performance advantages such as low insertion loss, high power handling capability and low DC power requirements.

Several groups [1-4] are investigating the possibility of implementing phase shifter circuits using barium strontium titanate (BST) which has an electric field tunable dielectric constant. In these circuits the ferroelectric material (BST) either forms the entire microwave substrate [1,2] on which the conductors are deposited (thick films/bulk crystals) or a fraction of the substrate with thin BST films sandwiched between the substrate and the conductors [3,4]. These circuits rely on the principle that the phase velocity of the waves propagating on these structures can be altered by changing the permittivity of the ferroelectric layer. This approach has several limitations including high conductor losses, inefficient use of the BST tunability and high control voltages. The approach used by us was to periodically load a coplanar wave guide transmission line with voltage tunable ferroelectric (BST) capacitors. The phase velocity of the periodically loaded line depends on the values of the BST capacitors and thus could be changed by applying bias to the BST capacitors. Parallel plate capacitors were employed here since they utilize the tunability of the BST film effectively and require much lower control voltages than interdigitated capacitors. Also, the use of discrete BST capacitors made it easy to control the amount of capacitive loading due to the ferroelectric film and thus allowed the structure to be optimized for good loss performance [5].

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THEORY

The schematic of the proposed phase shifter circuit is shown in figure 1. The phase shifter basically consists of a high impedance transmission line that is periodically loaded with thin film BST capacitors with spacing L_{sect}. For frequencies much below the Bragg frequency, this structure behaves like a synthetic transmission line [5] with modified propagation velocity and characteristic impedance. Since the capacitance value of the loading BST capacitors can be varied by applying bias, it is possible to change the phase velocity and impedance of the line. For phase shifter applications, the value of the loading capacitors is chosen such that the impedance variation is small but by cascading the correct number of sections the phase shift can be made as large as desired.

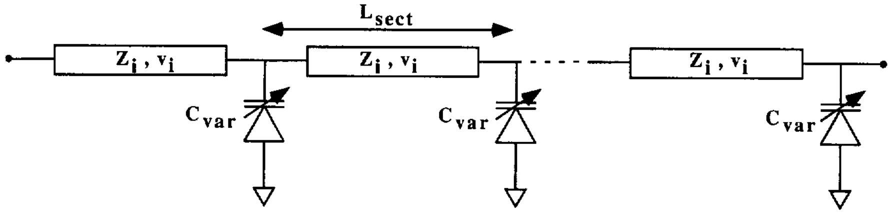
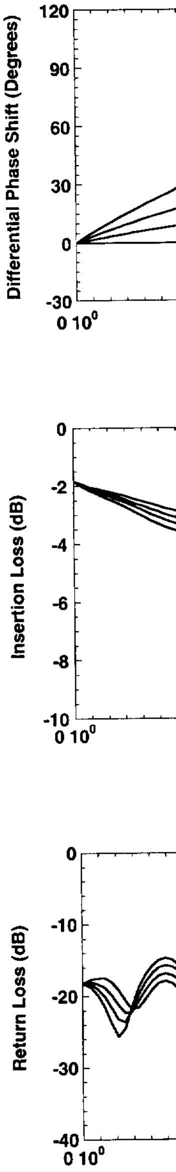


Figure 1: Circuit schematic for a periodically loaded line phase shifter

The phase shifter circuits presented here were designed using the same techniques as [5] and consisted of a CPW transmission line of characteristic impedance 73 Ω on a high resistivity silicon substrate (40 KΩ-cm). A thin insulating layer of silicon nitride was deposited between the CPW metal and the silicon substrate to prevent DC leakage. The CPW line was periodically loaded with BST capacitors whose zero bias capacitance was 270 fF. The BST (150 nm thick) for the tunable capacitors was deposited by RF magnetron sputtering. Platinum was used as the top and bottom electrode for the BST capacitors. The spacing between BST capacitors was chosen to be 580 μm resulting in a Bragg frequency of 25 GHz. A total of 16 periods was used in the phase shifter circuit resulting in an overall length of 9.3 mm. Standard monolithic circuit fabrication techniques were used for the fabrication of the periodically loaded line phase shifters.

RESULTS

RF measurements were made on a HP 8722D network analyzer that was calibrated using on-wafer standards. The two-port s-parameters of the phase shifter circuit were recorded up to 12 GHz. Figure 2a shows the differential phase shift (with respect to the zero bias insertion phase) as a function of frequency for several bias values. As expected for a variable velocity transmission line, the circuit produced a phase shift that varied linearly with frequency (for frequencies well below the Bragg frequency). The circuit was capable of continuous 0-100° phase shift at 10 GHz with any desired resolution. The maximum insertion loss at 10 GHz occurred at zero bias and was 7.6 dB (see figure 2b). The return loss was better than 12 dB over all phase states as shown in figure 2c.



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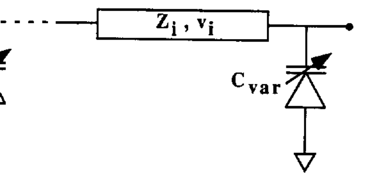

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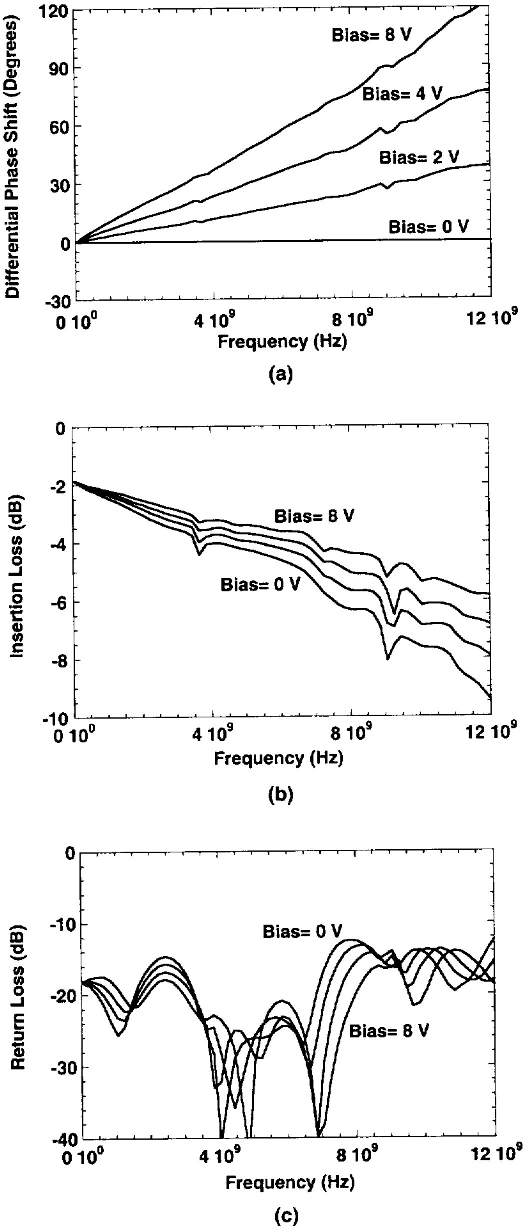
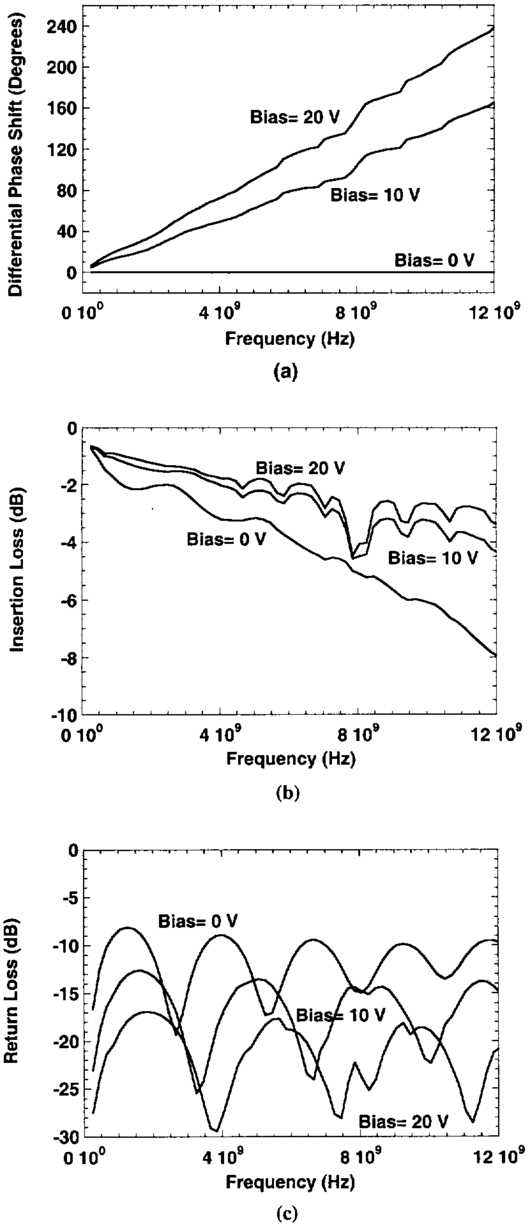


Figure 2: Measured performance of first ever periodically loaded line phase shifter with BST capacitors- a) Differential phase shift b) Insertion loss c) Return loss



(a)

(b)

(c)

Figure 3: Measured performance of improved periodically loaded line phase shifter with BST capacitors- a) Differential phase shift b) Insertion loss c) Return loss

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factor is only about 10 at the X-band.
due to advances in BST film processi
better insertion loss performance.

CONCLUSIONS

Periodically loaded line phase
parallel plate capacitors have been de
200° of phase shift with an insertion l
is expected with further improvements

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REFERENCES

1. Vijay K. Varadan, K.A. Jose, Vas
Novel Microwave Planar Phase Sh
2. Franco De Flaviis, N. G. Alexo
Integrated Phase Shifter Desig
Transactions on Microwave The
1997.
3. F. W. Van Keuls, R. R. Romanov
H. Mueller, R. E. Treece, T. V. Ri
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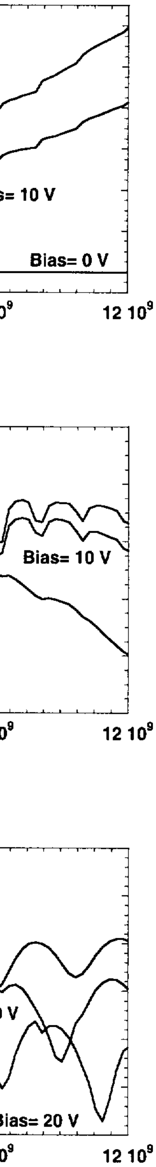

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sertion loss c) Return loss

The measured performance of the first periodically loaded line phase shifter circuit did not meet the design expectations and it was determined that fabrication process related issues were responsible. Due to lift-off problems during top metal deposition, the BST capacitor yield on the first phase shifter process was only about 50% (capacitors failed open). As a result of the low device yield, the capacitive loading of the transmission line was much lower than designed resulting in reduced phase shift. The higher than expected losses were attributed to CPW losses in the high resistivity silicon substrate due the formation of a parasitic MIS (metal-insulator-semiconductor) capacitor.

These problems were addressed in subsequent fabrication runs. The thickness of the capacitor top electrode metal was reduced to 0.3 μm resulting in a substantially easier lift-off process and the BST capacitor yield improved to 100%. In order to reduce the additional CPW losses arising due to the formation of a MIS capacitor, the silicon nitride was etched away from the gap regions of the CPW lines as suggested in [6]. The phase shifters fabricated with the modified process showed improved performance as indicated in figure 3. The improved phase shifter circuit was capable of 200° of phase shift with 6.2 dB of insertion loss and return loss better than 10 dB at 10 GHz. Detailed microwave characterization of the BST capacitors was also performed and it showed that BST capacitor loss is the dominant loss mechanism in the phase shifters since the BST capacitor quality factor is only about 10 at the X-band. Further improvements in BST capacitor quality factors due to advances in BST film processing and growth should lead to phase shifters with even better insertion loss performance.

CONCLUSIONS

Periodically loaded line phase shifter circuits using voltage tunable $BaSrTiO_3$ (BST) parallel plate capacitors have been demonstrated at X-band. The best circuits demonstrated 200° of phase shift with an insertion loss of 6.2 dB at 10 GHz. Even better loss performance is expected with further improvements in BST capacitor quality factors.

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REFERENCES

1. Vijay K. Varadan, K.A. Jose, Vasundara V. Varadan, R. Hughes, and James F. Kelly, "A Novel Microwave Planar Phase Shifter," *Microwave Journal*, pp. 244-54, April 1995.
2. Franco De Flaviis, N. G. Alexopoulos and Oscar M. Stafsudd, "Planar Microwave Integrated Phase Shifter Design with High Purity Ferroelectric Material," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, No. 6, pp. 963-9, June 1997.
3. F. W. Van Keuls, R. R. Romanovsky, D.Y. Bohman, M. D. Winters, F. A. Miranda, C. H. Mueller, R. E. Treece, T. V. Rivkin, and D. Galt, "($YBa_2Cu_3O_{7-\delta}$, Au)/$SrTiO_3$/$LaAlO_3$ Thin Film Conductor/Ferroelectric Coupled Microstripline Phase Shifters for Phased

Array Applications," *Applied Physics Letters*, vol. 71 (21), pp. 3075-7, 24 November 1997.

4. F. W. Van Keuls, R. R. Romanovsky, N. D. Varaljay, F. A. Miranda, C. L. Canedy, S. Aggarwal, T. Venkatesan, and R. Ramesh, "A Ku-Band Gold/$Ba_xSr_{1-x}TiO_3$/$LaAlO_3$ Conductor/Thin-Film Ferroelectric Microstrip Line Phase Shifter for Room Temperature Communications Applications," *Microwave and Optical Technology Letters*, vol. 20, No. 1, pp. 53-6, Wiley, Jan. 1999.
5. Amit S. Nagra and Robert A. York, "Distributed Analog Phase Shifters with Low Insertion Loss," *IEEE Transactions on Microwave Theory and Techniques,* vol. 47, No. 9, pp.1705-1711, Sept. 1999.
6. Y. Wu, H. S. Gamble, B. M. Armstrong, V. F. Fusco, and J. A. Carson Stewart," SiO_2 interface layer effects on microwave loss of high-resistivity cpw line," *IEEE Microwave and Guided Wave Letters,* vol. 9, No. 1, pp.10-12, Jan. 1999.

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