

# A C-Band High-Dynamic Range GaN HEMT Low-Noise Amplifier

Hongtao Xu, Christopher Sanabria, Alessandro Chini, Stacia Keller, Umesh K. Mishra, and Robert A. York

**Abstract**—A C-band low-noise amplifier (LNA) is designed and fabricated using GaN HEMT power devices. The one-stage amplifier has a measured noise figure of 1.6 dB at 6 GHz, with an associated gain of 10.9 dB and IIP3 of 13 dBm. It also exhibits broadband operation from 4–8 GHz with noise figure less than 1.9 dB. The circuit can endure up to 31 dBm power from the input port. Compared to circuits based on other material and technology, the circuit shows comparable noise figure with improved dynamic range and survivability.

**Index Terms**—GaN, high electron-mobility transistor (HEMT), high linearity, low-noise amplifier (LNA).

## I. INTRODUCTION

AlGaIn–GaN HEMTs have been developed as power devices in microwave applications, as they have shown one-order higher power density over conventional GaAs-based HEMTs and comparable cutoff frequencies for similar gate-lengths. These devices have not only been identified as the technology of choice for next generation high-power, high-frequency applications but have also shown excellent noise characteristics for LNA circuits [1]–[4]. Typical receiver configurations include additional circuitry to protect the system from damaging signals, increasing complexity and introducing additional noise to the receiver system. Low-noise, high-breakdown GaN HEMTs in amplifier front-ends reduce the need for diode limiters as protection against RF overstress. The high-power capability directly translates into the ability to handle a high-input power or energy spike without failure in a receiver front-end. This can reduce the overall LNA noise figure by 1 dB. In this paper, we will demonstrate our noise figure and linearity of a robust LNA using GaN HEMT technology. A LNA with a noise figure of 1.6 dB at 6 GHz, high-linearity and high-survivability is presented.

## II. CIRCUIT DESIGN AND SIMULATION

The circuit was designed using Agilent Advanced Design System (ADS) as shown in Fig. 1(a). To achieve desirable accuracy of the modeling, the small signal and noise properties of the transistors were characterized for circuit design. A single stage low-noise amplifier was designed with the input and output-matching network using only on-wafer spiral inductors. The amplifier input circuitry transformed the  $50\ \Omega$  input line into a com-

plex impedance, varying with frequency, that was as close as possible to the measured optimum noise matching of the transistors. The output-matching circuit was optimized for maximum gain, gain flatness, and output matching using a small signal model extracted from s-parameter measurements. Special attention was paid to develop adequate models of the passive components. The average  $Q$  factor of these on-wafer spiral inductors is 20 at 6 GHz. The LNA design avoids the use of metal-insulator-metal capacitors and thin-film resistors. The elimination of these components improves yield, reduces die area and lowers the cost of the chip fabrication.

## III. CIRCUIT FABRICATION AND RESULTS

The AlGaIn/GaN HEMT devices were grown by metal organic chemical vapor deposition (MOCVD) on sapphire substrates. The epitaxial structure consisted of a semi-insulating Fe-doped GaN base layer [5], followed by a 290 Å thick  $\text{Al}_{0.27}\text{Ga}_{0.73}\text{N}$  barrier layer. The room temperature sheet electron concentration and Hall mobility were  $\sim 1.15 \times 10^{13}\ \text{cm}^{-2}$  and  $\sim 1211\ \text{cm}^2/\text{Vs}$ , respectively. The GaN HEMT device has gate length and width of  $L_g = 0.7\ \mu\text{m}$  and  $W_g = 2 \times 100\ \mu\text{m}$ , current density  $I_{\text{dss}} = 1\ \text{A/mm}$  at  $1\ \text{V}\ V_{\text{gs}}$ , and a breakdown voltage larger than 35 V. The measured unit current gain cutoff frequency ( $f_t$ ) of the device is 20 GHz.

The GaN HEMT LNA fabrication started with a standard HEMT process [6], followed by device isolation, then a spiral inductor process with air bridges. The chip size is  $3.1\ \text{mm} \times 1.25\ \text{mm}$ . As shown in Fig. 1(b), all input and output networks are on wafer. Circuit characterization was done on a Maury ATS system from 4–8 GHz with a bias condition of  $V_{\text{gs}} = -3.5\ \text{V}$  ( $\sim 15\% I_{\text{dss}}$ ) and  $V_{\text{ds}} = 4\ \text{V}$ . Bias feeds for gate and drain were provided through off-wafer bias tees for convenience in testing.

The noise and gain performance of the LNA is shown in Fig. 2. The LNA has a noise figure of 1.6 dB and a gain of 10.9 dB at 6 GHz. Moreover, it exhibits broadband operation: from 4–8 GHz with a noise figure less than 1.9 dB. The return losses at the input and the output ports are less than  $-2.3\ \text{dB}$  and  $-21.1\ \text{dB}$ , respectively at 6 GHz (Fig. 3). The dc power consumption of the amplifier is 120 mW.

We have investigated the nonlinear behavior of the amplifier through 1 dB compression point and third order intermodulation distortion. In Fig. 4, the single tone power measurement at 6 GHz shows  $P_{1\ \text{dB}} = 12.8\ \text{dBm}$ . The IM3 characterization was performed using a two-tone signal at 6 GHz with an offset frequency of 100 kHz. In Fig. 5, the IIP3 of the LNA is 13 dBm in the linear region. The LNA shows very high-dynamic range with decent gain and noise figure.

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The authors are with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA (e-mail: hongtao@engineering.ucsb.edu).

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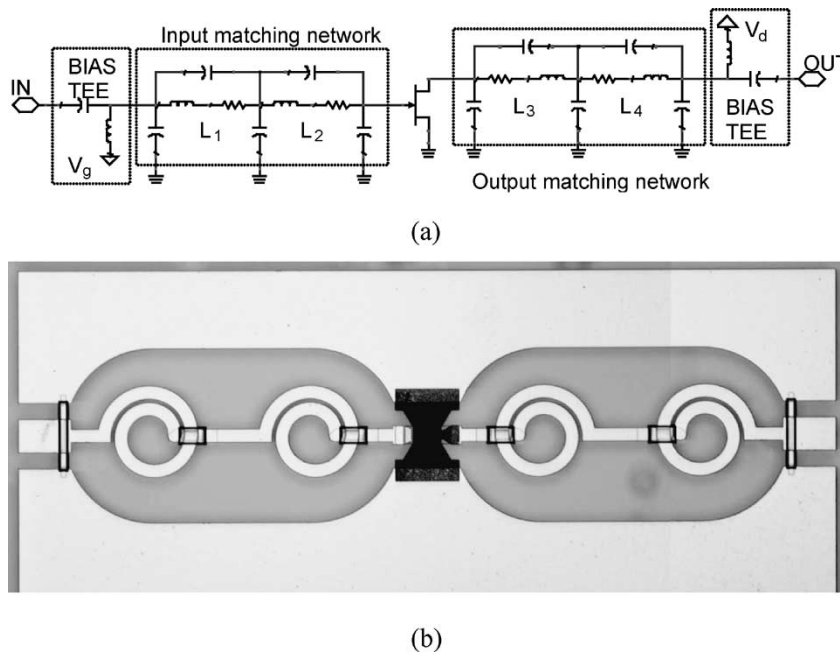


Fig. 1. (a) Circuit schematic of the LNA and (b) chip photomicrograph of the developed LNA (3.1 mm × 1.25 mm).

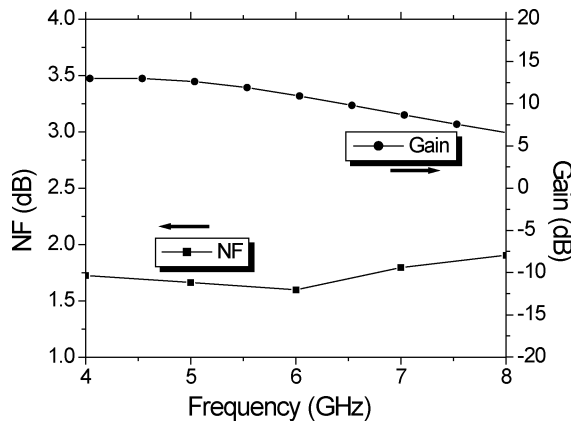


Fig. 2. Noise figure and gain versus frequency of LNA.

Survivability characterization was performed on the LNA for sustaining high-input power without failure. We drove the LNA with increasing CW input power until failure. In Fig. 6, the LNA shows an input survivability of 31 dBm. For input power levels larger than 20 dBm, the device gate diode is partially forward biased during each RF cycle.

With the increasing of the drive level, the forward gate current increases, resulting in device burn-out when it reaches a  $\sim 400$  mA/mm level (i.e., at a 31 dBm input power level). 20 dBm input power was the safe power level for CW input, since we observed a slight performance degradation for larger input power levels. However, the circuit was capable to handling up to 31 dBm input power before experiencing a catastrophic failure.

#### IV. CONCLUSION

We have presented the performance of a LNA based on GaN HEMT technology and demonstrated that the GaN HEMT is

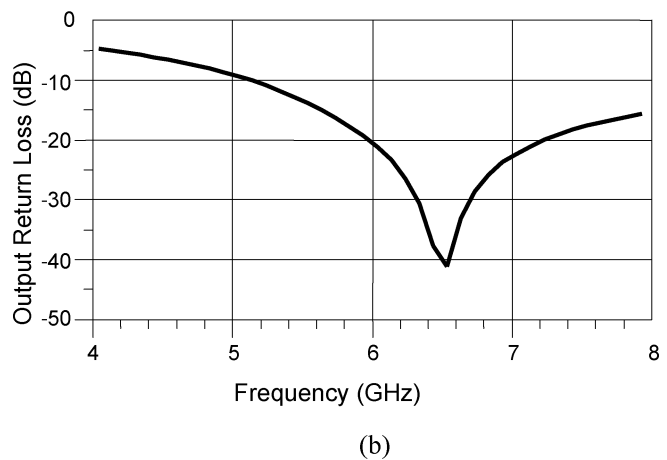
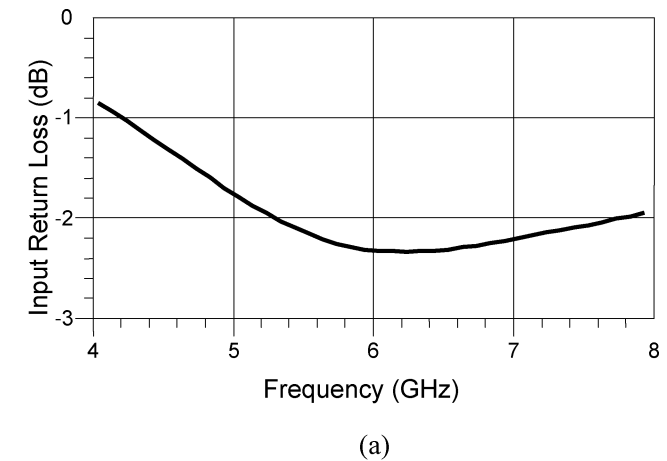


Fig. 3. (a) Input and (b) output return loss of LNA.

an attractive candidate for low-noise application. The integrated C-band LNA offers 1.6 dB noise figure and 10.9 dB gain at 6 GHz. With respect to other technologies, it has comparable

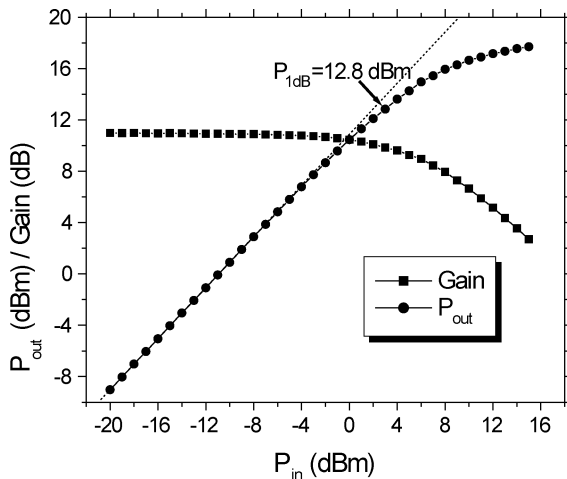


Fig. 4. Single tone output power and gain of LNA at 6 GHz.

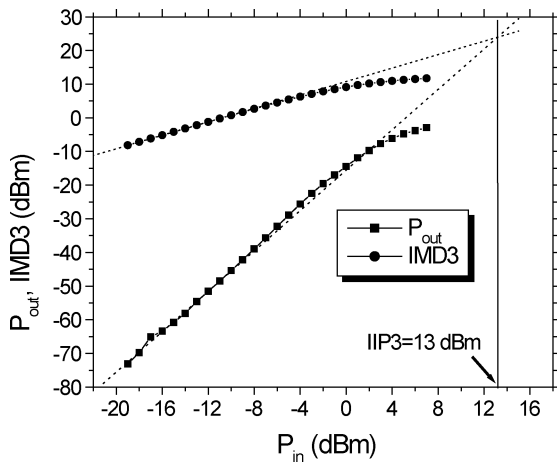


Fig. 5. Linearity measurement at 6 GHz.

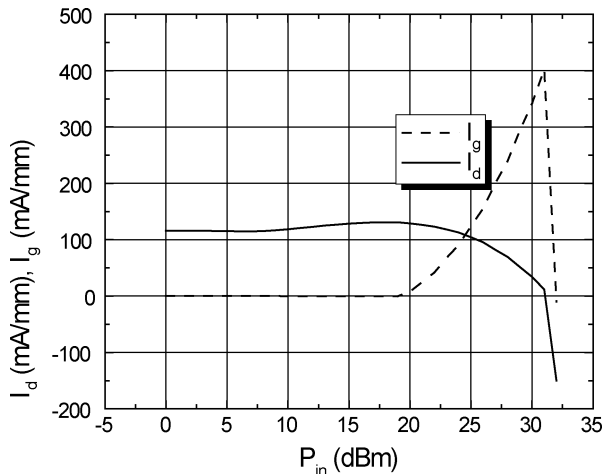


Fig. 6. Survivability test of LNA at 6 GHz.

reduction or elimination of front-end protection, and the fabrication of both low-noise and high-power circuits on the same wafer.

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noise specifications with higher dynamic range and survivability. Moreover, using GaN HEMT technology allows the