This new node has also been used to model resistive loads in a parallel plate test structure, where it effectively models the desired resistive load at zero frequency.

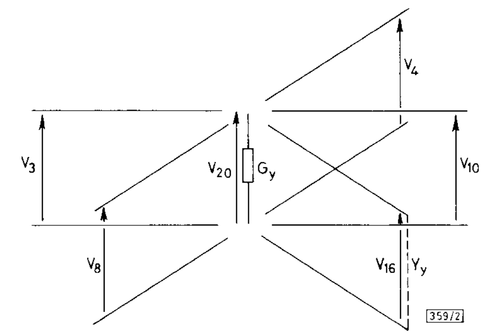

Fig. 2 *2-D slice through a 3-D node showing addition of conductance term*

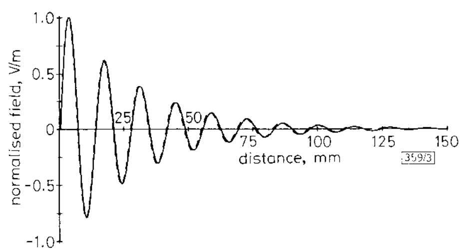

Fig. 3 *Comparison between an analytic solution and TLM*

$\varepsilon_r = 78 - j12$; $\mu_r = 1$

——— analytic

- - - - TLM

Conclusions: A new 3-D lossy symmetrical condensed node for the TLM method has been presented. Comparison with an analytical result shows excellent agreement.

Acknowledgments: R. A. Desai, who performed the penetration comparisions, is financially supported by the Ministry of Agriculture, Fisheries & Food. The results of the research are the property of the Ministry of Agriculture, Fisheries & Food, and are Crown Copyright.

P. NAYLOR *4th December 1989*

Department of Electrical & Electronic Engineering
University of Nottingham
University Park
Nottingham, NG7 2RD, United Kingdom

R. A. DESAI

Department of Applied Biochemistry and Food Science
University of Nottingham School of Agriculture
Sutton Bonington
Loughborough LE12 5RD, United Kingdom

References

1 JOHNS, P. B.: 'The art of modelling', *Electron. & Power*, 1979, **25**, pp. 565–569
2 JOHNS, P. B.: 'A symmetrical condensed node for the TLM method', *IEEE Trans.*, 1987, **MTT-35**, pp. 370–377
3 ALLEN, R., MALLIK, A., and JOHNS, P.: 'Numerical results for the symmetrical condensed TLM node', *IEEE Trans.*, 1987, **MTT-35**, pp. 378–382
4 COLLIN, R. E.: 'Foundations for microwave engineering' (McGraw-Hill, 1966)
5 JOHNS, P. B.: 'Ideal transformers and gauge transformations in lumped network models of electromagnetic fields', *IEE Proc. A*, 1982, **129**, pp. 381–386

ACTIVE PATCH ANTENNA ELEMENT FOR ARRAY APPLICATIONS

Indexing terms: Antennas, Microstrip, Field-effect transistors

A packaged microwave FET has been integrated directly onto a rectangular patch antenna, forming an active radiating element for array applications. The FET is mounted across a narrow slot in the patch, and operates in a single bias, common-source configuration. A total radiated power of approximately 6 mW was measured at 8·2 GHz.

Introduction: Recent research into quasioptical power combining has centred on using large active arrays, in which an active component (Gunn diode, IMPATT, or FET) is integrated directly into each radiating element. Several novel architectures have appeared in the literature[1–4] which creatively incorporate the active element with a planar antenna. For power combining and active-array applications, considerable success has been achieved using an FET as the active device. The FET has inherently better noise properties and DC-to-RF efficiency than two-terminal devices. The technology for making microwave FETs and HEMTs is also well established. This letter describes a new method of integrating an FET into a rectangular patch antenna.

Description: An illustration of the active patch element is shown in Fig. 1. The patch is split into two sections by a narrow slot. The FET is mounted across this slot, with the drain and gate leads soldered on opposite sides. The source leads are soldered to the earth plane through the substrate; they do not make contact with the gate side of the patch. The drain bias line is isolated from the RF using a shunt bypass capacitor, located a quarter wavelength from the patch. A DC path from the gate to earth is established using a short-circuited quarter-wavelength stub.

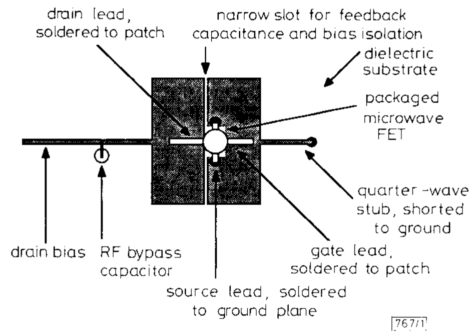

Fig. 1 *Illustration of the hybrid patch element with an integrated FET*

The prototype patch element was fabricated on 31 mm epoxy-resin PC board, with a measured dielectric constant of 4·1 and loss tangent of 0·015. A Fujitsu FSX03 GaAs FET was used, which has a 0·5 μm gate and an f_{max} of approximately 30 GHz. Patch dimensions and slot width were empirically determined for single-mode operation at about 8 GHz. The transistor bias was adjusted for maximum power output when measured at the broadside angle. This corresponded to a bias voltage of about 6 V at 40 mA. A tuning range of 250 MHz was observed with changing bias voltage.

Pattern measurements: The far-field patterns of the active patch element were measured in a small anechoic chamber lined with 13 cm pyramidal absorber material. A 20 dB receiving horn was placed 1 metre from the antenna positioner. The output spectrum observed on an HP 8569 spectrum analyser was stable to better than 2 MHz over the complete 180° rotation of the antenna, indicating that the DC bias lines and other experimental apparatus were indeed isolated from the RF. Measurements were performed at a frequency of 8·2 GHz.

The measured E- and H-plane patterns are shown in Fig. 2. These patterns agree well with theoretical predictions for a

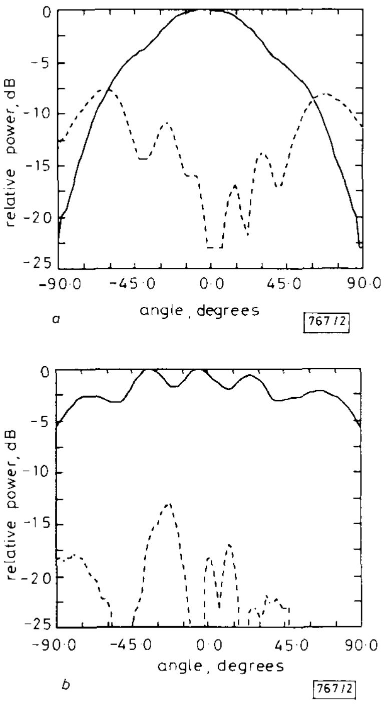

Fig. 2 *Far-field patterns for transistor/patch element of Fig. 1*

a H-plane; *b* E-plane; – – – – crosspolarisation measurement

rectangular patch, except for the bumpy structure in the E-plane measurement. Additional measurements performed with metal tape covering the slot suggest that the variation in the E-plane measurement may be caused by some radiation from the slot. The dashed lines in the figure represent the crosspolarisation measurements, which are at least 8 dB down from the peak copolarisation measurement. Using these measured patterns, an estimate of the total radiated power was calculated to be 6 mW, giving an effective isotropic radiated power (EIRP) of 40 mW and a DC-to-RF efficiency of 5%. This output power is comparable to the 10 mW generated by these FETs in a microstrip oscillator circuit.

Conclusions: A new integrated active-array element has been developed. This design features a single bias line and occupies relatively little substrate space because the transistor is embedded in the patch. Further work is underway to investigate variations in FET placement on the patch, scaling the design to higher frequencies and incorporating the active patch into quasioptical power combiners and transmit-receive arrays.

Acknowledgments: This work was supported by the US Army Research Office, General Electric and Fujitsu, who donated the FETs.

R. A. YORK
R. D. MARTINEZ
R. C. COMPTON

School of Electrical Engineering
Cornell University
Ithaca, NY 14853, USA

6th February 1990

References

1 THOMAS, H. J., FUDGE, D. L., and MORRIS, G.: 'Gunn source integrated with microstrip patch', *Microwaves & RF*, 1985, pp. 87–89

2 PERKINS, T. O.: 'Active microstrip circular patch antenna', *Microw. J.*, 1987, pp. 110–117

3 CHANG, K., HUMMER, K. A., and GOPALAKRISHNAN, G. K.: 'Active radiating element using FET source integrated with microstrip patch antenna', *Electron. Lett.*, 1988, **24**, pp. 1347–1348

4 CAMILLERI, N., and BAYRAKTAROGLU, B.: 'Monolithic mm-wave IMPATT oscillator and active antenna', *IEEE Trans.*, 1988, **MTT-36**, p. 1670

PERFORMANCE OF MULTISTAGE INTERCONNECTION NETWORKS FOR INTEGRATED SERVICES

Indexing terms: Telecommunications, Switching

The performance of multistage interconnection networks used to switch prioritised packets is examined. The relationship between the normalised throughput for each class of packet and that when packets are not categorised into priority classes is determined. Our results are useful for networks providing integrated services where packets of different types of information have different priorities.

Introduction: Multistage interconnection networks (MINs) have been widely considered for use in constructing the switching fabrics in communication networks. An $N \times N$ MIN with $N = \alpha^n$ is constructed by n stages of crossbar switching elements (SEs) of size $\alpha \times \alpha$. Each stage consists of N/α such SEs and the interconnection pattern between stages is an α shuffle.[1] Self-routing, potential VLSI implementation, and ease of fault diagnosis are the main benefits that make MINs attractive. The normalised throughputs of MINs under the uniform traffic assumption can be computed by the use of a simple recursive formula.[1] It was found that MINs are more cost effective than single-stage crossbar networks for large systems. Fig. 1 illustrates an example of a 3-stage MIN with $\alpha = 2$.

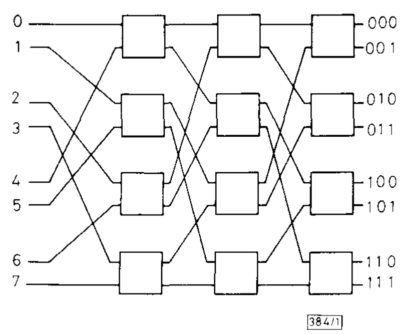

Fig. 1 *3-stage MIN*

$\alpha = 2$

To date, most of the results regarding the performance of MINs considered all packets to be equally important. A SE will randomly select a packet and route the selected packet to its destination output link whenever there is a conflict. No priority scheme is imposed in such an operation. In a network providing integrated services, packets of different types of information are likely to have different priorities. In this letter, we explore the performance of unbuffered MINs when they are used to switch prioritised packets.

System model: The MINs considered operate in a synchronous format. Time is divided into slots called network cycles. A network cycle is further divided into two portions τ_1 and τ_2. In τ_1, control signals are passed across the network to determine which inlets are granted to transmit their packets. In τ_2, packets are transmitted in accordance with the control signals.