GaN HEMTs based Flip-chip Integrated Broadband Power Amplifier

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Outline

**GaN power HEMTs design**
- Small device evaluation (100µm)
- Large device design
- Thermal management (Flip-chip mounting)

**GaN broadband power amplifier design**
- Limit of conventional TWA
- GaN modified TWA
- GaN LCR-matched PA
- GaN 2×2 matrix modified TWA

**Conclusions**
Why AlGaN/GaN HEMTs?

- Wide $E_g$
- High $v_s$
- High $n_s$
- High $\mu$
- Low $R_{on}$ (low $V_{knee}$)
- High $V_{br}$
- High $I_{max}$

GaN

AlGaN/GaN HEMTs

High Power Level
High Frequency ($f_t$)
High Efficiency (PAE)
High Operating Temp

Promising Microwave Power Device
Power Device Realization Flow
(5-6 masks & dicing)

- MOCVD growth of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HEMTs
- Device Process
  - Ohmic Contact (Source and Drain)
  - Pad Isolation & Schottky Contact (Gate)
  - Mesa Isolation
- DC & RF measurement on small device
  - Power Density, Gain, PAE
    - $P_{\text{out}} > 3\text{W/mm}$?
- Large Area Device Process
  - Bonding Bumps
  - Air-bridges
- Dicing Wafer Into Discrete Devices
- Ready for Bonding to Circuit

Start

\[ \begin{align*}
\text{No} & \quad \Rightarrow \quad \text{Yes} \\
\text{Yes} & \quad \Rightarrow \quad \text{Ready}
\end{align*} \]
Power Device Design Flow

- Evaluation of small FET
  - Total gate width
  - Unit gate finger width
  - Gate-gate pitch
  - Number of fingers/pad
  - Pattern layout

- DC & RF, Power Density, Gain
- Power, Impedance
- Gain (loss, phase delay)
- Thermal Issue, Bonding pad
- Uniform operation, Parasitic
- Parasitic, Thermal Resistance
Evaluation of small devices (100μm)

1) DC characterization

2) Dispersion

3) RF characterization

4) Immature GaN material
DC Characterization

Expected Power Density for GaN on Sapphire

\[ P_{out} = \frac{I_{max}}{8} \times (V_{br} - V_{knee}) \]

\[ P_{out} = 5.6 \text{ W/mm} \]

- \( V_{knee} \): \( \sim 5 \text{ V} \)
- \( I_{max} \): \( \sim 1000 \text{ mA/mm} \)
- \( V_{pinch} \): \( \sim -5 \text{ V} \)
- \( V_{br} \): \( \sim 50 \text{ V} \)
- \( G_{m-ext} \): \( \sim 200 \text{ mS/mm} \)
Effect of Traps in GaN Materials

Reasons:
- Traps in AlGaN & GaN, Surface States, etc.

RF I-V: $I_{\text{max}}$ $\downarrow$ $V_{\text{knee}}$ $\uparrow$

$P_{\text{out}}$ $\downarrow$ PAE $\downarrow$
Maximum Power Density and PAE (100 μm device)

- $P_{out} = 4.6 \text{ W/mm}$, $\text{PAE} = 40\%$
  - biased @ $V_d = 25 \text{ V}$, $I_d = 200 \text{ mA/mm}$

- $P_{out} = 3.6 \text{ W/mm}$, $\text{PAE} = 52\%$
  - biased @ $V_d = 18 \text{ V}$, $I_d = 200 \text{ mA/mm}$
Immaturity of GaN materials

Material NonUniformity across Wafer
Typical map of power density

*Power density:*
1- 4 W/mm

- 2 – 3 W/mm
- 3 – 4 W/mm
- 1 – 2 W/mm
- 2 – 3 W/mm

*Issues:*
- Non-uniformity of the Wafer
  20 – 30 %
- Dispersion Variation
  10 – 20 % to 50-60%
- Breakdown Voltage Limit
  40 – 50 V
- High Dislocation Density
  ~ 10^8 cm^-2
- Poor Reliability
  Overdriven failure
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$L_g = 0.7 \mu m$, biased @ $V_{ds} = 15 V$, $I_{ds} = 400mA/mm$

\[ f_t = \frac{g_m}{(2\pi C_{gs})} = \frac{V_s}{L_g} \]

\[ f_{\text{max}} = 0.5f_t \left( \frac{R_{ds}}{R_{in}} \right)^{1/2} \]

- Reduce $L_g$
- Reduce $R_{in}^*$
- Increase $R_{ds}$

\[ R_{in} = R_g + R_{gs} + R_s \]

- $f_t (20GHz)$
- $f_{\text{max}} (38GHz)$
Large-periphery Device Design

1) **Pattern layout**
2) **Thermal management**
3) **Results and problems**
4) **Optimum Load**
How to choose $L_{gg}$, $W_{gu}$, n?

- **Number of Gate Pads**: $(n-1)L_{gg}$
- **Air-bridges**
- **Bonding Pads**
- **$L_{gg}$**
- **$W_{gu}$**
Unit Gate Finger Width

\[ \gamma = \alpha + j \beta = \sqrt{Z \times Y} = \sqrt{\frac{r_g + jw l_g}{r_{gs} + 1/jw c_{gs}}} \]

\[ V(x) = \frac{V_0}{2} (e^{-\gamma x} + e^{-\gamma (2W_{gu} - x)}) \]

\[ P_{out} = \int_0^{W_{gu}} P_{out}(x) \, dx = P_{out_{ideal}} \times \frac{1}{4W_{gu}} \int_0^{W_{gu}} |V(x)|^2 \, dx \]

Gain Degradation < 2 dB:
C-band:<200µm  X-band:<100 µm  Ku-band:<75 µm
Large \((n-1)L_{gg}\) \rightarrow \text{Lower Gain}

- Phase rotation
- Non-uniform operation
  \((\text{materials and process variation})\)
- Non-uniform channel temperature
- Additional parasitics & losses

Large \(L_{gg}\) \rightarrow \text{Lower } R_{th}

\((n-1)L_{gg} < \lambda / 16\)

\((760 \ \mu m \text{ for GaN})\)

\(N = 10\)

\(L_{gg} = \sim 50 \ \mu m\)
Large-periphery Device Design

1) Pattern layout

2) Thermal management

3) Results and problems

4) Optimum load
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Thermal Management of Power Devices

More power dissipation $\rightarrow$ Temperature $\rightarrow$ Electron mobility $\downarrow$

$\rightarrow$ Gain $\downarrow$ $I_{\text{max}}$ $\downarrow$ $\rightarrow$ Output power $\downarrow$

Problems for Via-holes of GaN:

- **GaN HEMTS on Sapphire**
  - very difficult to etch
- **GaN HEMTS on SiC**
  - need develop complex process
- **Introduce parasitic $L_S$**

Back-side Heat-sink Via-holes
Advantages:

- *Minimum parasitics*
- *Better thermal management*
  
  Sapphire: $\sigma = 30 \text{ W/mK}$
  
  AlN: $\sigma = 180 \text{ W/mK}$

- *Cost effective*
Flip-Chip Mounting

- E-beam evaporation of Au bonding bumps
- Align FET chip with circuit board using flip-chip bonder
- Bond with pressure and temp
Thermal Management using Flip-chip bonding

For 4 W/mm
T>200°C w/o flip-chip bonding
T < 60°C with flip-chip bonding

(Finite Element Simulation)
Experimental comparison of a device before/after flip-chip bonding

50 µm x 0.25 µm Gate MODFETs before bonding
1.1 A/mm, 200 mS/mm

50 µm x 0.25 µm Gate MODFETs after bonding
1.6 A/mm, 280 mS/mm

Dramatic improvement in both $I_{d,max}$ and $g_m$ due to heat sinking
Large-periphery Device Design

1) Pattern layout

2) Thermal management

3) Results and problems

4) Optimum load
Flip-chip Bonded 1-mm GaN HEMT($L_g=0.75\mu m$)

- $P_{out} = 4.4\,\text{W}$
- $\text{PAE} = 35\%$
- $V_{ds} = 27\,\text{V}$
- $f = 8\,\text{GHz}$
- $I_{\text{max}} = 800\,\text{mA}$
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**Flip-chip Bonded 2-mm GaN HEMT**

\[ P_{out} = 6.3 \text{ Watt}, \quad \text{PAE} = 32 \%, \quad \text{Gain} = 13 \text{ dB} \]

**Biased @** \( V_{ds} = 25 \text{ V}, \quad f = 4 \text{ GHz}, \text{class AB} \)
### Performance
**GaN vs. GaAs**

Jane’s GaN HEMT  
(W<sub>g</sub> = 1mm, L<sub>g</sub> = 0.7 µm)

Triquint’s GaAs HFET  
(W<sub>g</sub> = 1.2mm, L<sub>g</sub> = 0.5 µm)

<table>
<thead>
<tr>
<th></th>
<th>V&lt;sub&gt;br&lt;/sub&gt; (V)</th>
<th>I&lt;sub&gt;max&lt;/sub&gt; (A/mm)</th>
<th>V&lt;sub&gt;knee&lt;/sub&gt; (V)</th>
<th>P&lt;sub&gt;out&lt;/sub&gt; (dBm/W)</th>
<th>PAE (%)</th>
<th>Gain (@8GHz)</th>
<th>R&lt;sub&gt;opt&lt;/sub&gt; (Ω-mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs</td>
<td>22</td>
<td>0.3</td>
<td>1</td>
<td>28.5/0.7</td>
<td>55</td>
<td>10</td>
<td>50</td>
</tr>
<tr>
<td>GaN</td>
<td>40-50</td>
<td>1</td>
<td>5</td>
<td>36.5/4.4</td>
<td>35</td>
<td>10</td>
<td>32</td>
</tr>
</tbody>
</table>
Mm-wide GaN HEMTs Power Performances

<table>
<thead>
<tr>
<th>Device size</th>
<th>$I_{\text{max/DC}}$ (mA)</th>
<th>Gain (dB)</th>
<th>Power (Watt)</th>
<th>PAE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1mm*</td>
<td>800 ~ 900</td>
<td>10</td>
<td>4.4</td>
<td>35</td>
</tr>
<tr>
<td>2mm**</td>
<td>1500 ~ 1800</td>
<td>13</td>
<td>6.4</td>
<td>32</td>
</tr>
<tr>
<td>4mm</td>
<td>2800 ~ 3200</td>
<td>?</td>
<td>?</td>
<td>?</td>
</tr>
</tbody>
</table>

*: RF measurement was performed at 8 GHz.

**: RF measurement was performed at 4 GHz.

Practical Issues:
- *Flip-chip bonding limit*
- *ATN loadpull measurement power & biasing limit*
- *Low yield*
Non-scalable Property of Large Devices

1mm to 2mm:

- \( DC \ I_{max} \): 10 – 20% drop
- Gain: 3dB drop
- Power: 2dB drop
- PAE: 5% drop

- Connection parasitics & losses
- Non-uniform channel temperature
- Non-uniform operation
- Self-heating
- Phase rotation

Conclusion: Use multiple small-area discrete devices
Large-periphery device design

1) Pattern layout

2) Thermal management

3) Results and problems

4) Optimum load
Optimum Load

\[ R_{\text{opt}} = \frac{V_{br} - V_{knee}}{I_{\text{dss}}} \]

\[ P_{RF,\text{max}} = \frac{1}{8} I_{\text{max}} \times (V_{br} - V_{knee}) \]

For \( R > R_{\text{opt}} \):  
\[ P_{RF} = \frac{1}{2} \frac{(V_{br} - V_{knee})^2}{R_L} = P_{RF,\text{max}} \times \frac{R_{\text{opt}}}{R_L} < P_{RF,\text{max}} \]

For \( R < R_{\text{opt}} \):  
\[ P_{RF} = \frac{1}{8} I_{\text{max}}^2 R_L = P_{RF,\text{max}} \times \frac{R_L}{R_{\text{opt}}} < P_{RF,\text{max}} \]
Effect of $C_{ds}$:
Reducing maximum $P_{out}$ especially near $f \sim 1/2\pi R_{opt}C_{ds}$ (15 GHz)

$C_{ds}$ must be compensated for optimum design
From Loadpull Measurement:

\[ R_{\text{opt}} = 32 \, \Omega \cdot \text{mm}, \quad C_{\text{ds}} = 0.3 \, \text{pF/mm} \]
Broadband power amplifier design

1) Limitation of conventional TWA
2) Modified TWA
3) LCR-matched PA
4) 2×2 matrix modified TWA
Conventional TWA Efficiency Limitation

- Maximum efficiency < 25%
- Devices
- Drain line dummy load
- Gate line dummy load
- $P_{out} - P_{in} = DE \times (1 - \frac{1}{G})$
- $G < 10 \text{ dB}$
- PAE < 20%
Conventional TWA Power Limitation

Largest Voltage across last FET < $V_{br}$

Maximum $P_{out}$ fixed by device technology ($Z_0 = 50\Omega$):

$$P_{RF\ max} = \frac{(V_{dr} - V_{knee})^2}{8Z_0}$$

For GaAs FET:
$V_{dgB} = 20\ V$, $V_{pinch} = -2.5\ V$, $V_{knee} = 1\ V$, then $P_{RF\ max} = 0.7\ W$

For GaN HEMT:
$V_{dgB} = 50\ V$, $V_{pinch} = -5\ V$, $V_{knee} = 5\ V$, then $P_{RF\ max} = 4\ W$
P_{out} cannot be increased

- **device technology limit**

Efficiency can be improved by:

- **forcing more current to the real load**
- **using less devices**
Broadband power amplifier design

1) Limitation of conventional TWA
2) Modified TWA
3) LCR-matched PA
4) 2×2 matrix modified TWA
Goal:
- **Bandwidth**: 8:1 (1 – 8 GHz)
- **Gain**: ~ 10 dB
- **PAE**: > 20%
- **$P_{out}$**: 6 Watt (2W/mm)

**Approach:**
- **Input distributed match**: Bandwidth & gain flatness
- **Capacitive division**: Broadband
- **Corporate power combiner**: Broadband & power
- **GaAs prototype circuits**: Topology verification
Schematic of GaN Modified TWA

Modified TWA:
1) Eliminate backward wave
2) Broad band
3) High efficient corporate combiner
4) Avoid high impedance lines
Equivalent of Tapered Drain-lines

GaN HEMT

In

Zg,E

Corporate Power Combiner

Z1 Z2 Z3 Z4 Z5

Out

50 ohm

Device Device Device Device

Z1 2

Z1 3

Z1 4

Z1 4

Out

Z1

In

Zg, τ

Zo

Cin
• For power FETs, large $C_{gs}$ is limiting the bandwidth

$$Z_{gate} = \sqrt{\frac{L_{gate}}{C_{gate}}} = 50\Omega$$

$$f_{brag} = \frac{1}{\pi \sqrt{L_{gate} C_{gate}}}$$

$$C_{gate} = \frac{C_{in} C_{gs}}{C_{in} + C_{gs}}$$

• Compensate the gate line loss by increasing the capacitance ($C_{in4} > C_{in3} > C_{in2} > C_{in1}$)

$$V_x = \frac{C_{inx}}{C_{inx} + C_{gs}} V_{in} \quad x = 1, 2, 3 \ldots N$$
Define: Bandwidth > 3:1

\( \frac{f_{\text{High}}}{f_{\text{Low}}} \)

**High Impedance Transformation Ratio**

(4mm device):

Input: 50 : 1

\((50 \ \Omega / 1 \ \Omega)\)

Distributed match

LCR lossy match

Output: 6:1

\((50 \ \Omega / 8 \ \Omega)\)

Corporate power divider

Multi-section LC match
Single-section Wilkinson Power Combiner

Bandwidth: 2:1

![Diagram of Wilkinson Power Combiner with equations and bandwidth plot.](image-url)
Bandwidth of $\lambda/4$ Transformer

To have bandwidth 3 to 1
$\lambda/4$ transformer ratio < 1.5:1
N-way & Corporate Combiner
(to extend bandwidth)

Multi-section λ/4 Transformers

N-way Combiner

Corporate Combiner
**BW & Efficiency of Corporate Power Combiner**

- **Efficiency:** > 80% (1 dB loss)
- **Bandwidth:** ~ 10:1 (1 – 10 GHz)
- **Disadvantage:** Not Area-efficient (But AlN carrier cheap)

![Graph showing gain and efficiency vs frequency](image)
1.2mm-wide 0.5µm-long GaAs PHEMT, $P_{out} = 27$ dBm, PAE = 50% @ 8GHz
Capacitor-division Modified TWA with Corporate Power Combiner

$S_{21}$

$S_{11}$

$S_{22}$

$S_{12}$

$V_{ds} = 18 \, \text{V}$

$I_{ds} = 400 \, \text{mA}$

PAE (%) vs. Freq (GHz)

Pout (dBm) vs. Freq (GHz)
Power Sweep at 4 GHz

\[ P_{\text{out}} = 4.5 \text{ W}, \text{ PAE} = 14\% \]
@ \( V_{\text{ds}} = 22 \text{ V}, I_{\text{ds}} = 400\text{mA}, f = 4\text{GHz} \)
Unequal Drive Problem

\[ \alpha_g = \frac{1}{2} \omega_c^2 R_{in} C_{gs}^2 Z_0 \]

Unequal drive:
- Reduce combing efficiency
- Reduce device reliability

Gate attenuation is frequency dependent
- Compensated at one frequency
Broadband power amplifier design

1) Limitation of conventional TWA

2) Modified TWA

3) LCR-matched PA

4) 2×2 matrix modified TWA
LCR-matched PA Design

Goal:
- **Bandwidth:** 3:1 (3 – 10 GHz)
- **Gain** ~ 10 dB
- **PAE** > 20 %
- **P_{out}** 8 Watt (2W/mm)

Approach & Improvement:

- **Input LCR lossy match**
- **Low Q LC match**
- **Corporate power combiner**
- **C_{ds} compensation**
- **Gain flatness**
- **Broadband**
- **Broadband & power**
- **Higher power**
Schematic of LCR-matched Broadband GaN Power Amplifier

Corporate Power Divider

1mm GaN HEMTs

L-C-R match

S_{11}^*

R_{opt}

Input LC Match

Output LC Match

Input LC Match

Output LC Match

Input LC Match

Output LC Match

Input LC Match

Output LC Match

Corporate Power Combiner

Z1 Z2 Z3 Z4

Z5 Z6

In

Out
Bandwidth > 3:1

\( f_{\text{High}} / f_{\text{Low}} \)

High Impedance Transformation Ratio
(4mm device size):

**Input:** 50 : 1
(50 Ω / 1 Ω)

**Distributed match**
**LCR lossy match**

**Output:** 7:1
(50 Ω / 8 Ω)

**Corporate power divider**
**Multi-section LC match**
The network eliminates gain peaks at low band
R also can be stabilizing resistor
Bandwidth $> 3:1$

$$\frac{f_{\text{High}}}{f_{\text{Low}}}$$

High Impedance Transformation Ratio
(4mm device size):

Input: $50 : 1$
$(50 \, \Omega / 1 \, \Omega)$
- Distributed match
- LCR lossy match

Output: $7:1$
$(50 \, \Omega / 8 \, \Omega)$
- Corporate power divider
- Multi-section LC match
Single-section Lowpass LC Networks

- \( R_L > R_S \)
- \( R_S > R_L \)

\( R_L > R_S \)
Define Q of LC Networks

\[ X_P^* = \frac{X_P^2 R_L}{X_P^2 + R_L^2} \quad X_S = X_P^* \]

\[ R_L^* = \frac{X_P^2 R_L}{X_P^2 + R_L^2} \quad R_S = R_L^* \]

For \( R_L > R_S \)
\[ Q = \sqrt{\frac{R_L}{R_S}} - 1 \]
\[ X_S = \frac{\omega L}{R_S}, \quad X_P = \frac{1}{\omega C} = \frac{R_L}{Q} \]

For \( R_S > R_L \)
\[ Q = \sqrt{\frac{R_S}{R_L}} - 1 \]
\[ X_P = \frac{1}{\omega C} = \frac{R_S}{Q}, \quad X_S = \frac{\omega L}{R_L} = R_L \times Q. \]
Multi-section (Low-Q) LC Matching Networks

For Complex impedance, Reactance can be absorbed into LC networks
LCR Matched 4mm GaN-based Power Amplifier

Gain: ~ 7dB, BW: 3 - 10 GHz

\[ P_{out} = 8.5 \text{ W}, \ PAE = 20\% \text{ @ 8 GHz} \]
Power Sweep at 8 GHz

\[ P_{\text{out}} = 8.5 \, \text{W} , \, \text{PAE} \approx 20\% @ 8 \, \text{GHz} \]

\[ (V_d = 16 \, \text{V}, \, I_d = 500 \, \text{mA, class AB}) \]
Broadband power amplifier design
1) Limitation of conventional TWA
2) Modified TWA
3) LCR-matched PA
4) 2×2 matrix modified TWA
Goal:
- **Bandwidth:** 6:1 (1-6 GHz)
- **Gain** > 10 dB
- **PAE** > 15%
- **$P_{out}$** 8 Watt (2W/mm)

Approach & Improvement:
- **$2 \times 2$ Modified TWA**
  - Bandwidth & equal drive
- **Lower frequency:** 1 – 6 GHz
  - Higher gain
- **Real air-bridges**
  - Better bonding
- **Thicker CPW lines ( > 3 $\mu$m)**
  - Reduce conductive loss
Schematic of $2 \times 2$ Modified TWPA

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1mm GaN HEMTs

$Z_{d} = R_{opt}$

Corporate Power Combiner
Better Equal Drive

\[ \alpha_g = \frac{1}{2} \omega_c^2 R_{in} C_{gs}^2 Z_0 \]

2×2 matrix TWA has better equal drive than 1×4 TWA
Assumption:
- $V_1 = V_{gs}$
- $A_2 = A_3 = 0$
- $Gm$: constant
- $R_{ds}$: infinity

Conclusion:
- First order simulation
- Compatible with small-signal model
Simulation Results

**Gain:** ~ 11 dB  
**BW:** 1 - 7 GHz  
**P\text{out}:** 6 – 8 W  
**PAE:** ~ 20 %
Photos of the Circuit

Circuit components:
GaN HEMTs (4 X 1mm)
MIM Capacitors,
NiCr Resistors
Air-Bridges

Delay Lines
Corporate Combiner

RF IN

RF OUT

10 mm
8 mm

Circuit with flipped GaN HEMTs
**Small-signal and Large-signal Performance**

**Gain:** 9 - 12 dB, **BW:** 1.8 – 6.8 GHz

*Biased @ $V_{ds} = 10$ V, $I_{ds} = 400$ mA*

**Pout:** 5 - 7.5 Watt, **PAE:** 18 - 24%

*Biased @ $V_{ds} = 18$ V, $I_{ds} = 400$ mA*
<table>
<thead>
<tr>
<th></th>
<th>$P_{\text{out}}$ (W)</th>
<th>3dB BW (GHz)</th>
<th>Gain (dB)</th>
<th>PAE (%)</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs modified TWPA</td>
<td>0.6 - 1.3</td>
<td>1 - 8</td>
<td>5 - 8</td>
<td>15 - 25</td>
<td>BW, flat gain, good match</td>
</tr>
<tr>
<td>GaN modified TWPA</td>
<td>2.5 - 4.5</td>
<td>1 - 8</td>
<td>5 - 8</td>
<td>5 - 15</td>
<td>BW, flat gain, good match</td>
</tr>
<tr>
<td>GaN LCR-matched PA</td>
<td>4.5 - 8.5</td>
<td>3 - 10</td>
<td>5 - 8</td>
<td>10 - 20</td>
<td>power compact</td>
</tr>
<tr>
<td>GaN 2×2 matrix modified TWPA</td>
<td>5 - 7.5</td>
<td>1 - 6</td>
<td>9 - 12</td>
<td>18 - 24</td>
<td>BW, power PAE</td>
</tr>
</tbody>
</table>
High Power small GaN HEMTs (un-passivated):

\[ P_{out} = 4.6 \text{ W/mm, PAE} = 40\% \]

- High Power large-periphery GaN HEMTS:
  \[ P_{out} = 4.4 \text{ W, PAE} = 35\% @8\text{GHz} \]

- GaN Modified GaN TWPA:
  \textit{First GaN amplifier!}

- GaN LCR - matched PA:
  \[ P_{out} \text{ up to 8.5 W (>2W/mm)} \]

- GaN 2 × 2 matrix modified TWPA:

\textit{Best overall performance}
Conclusions

Achievements:

Demonstration of power-bandwidth advantage of GaN
(0.7µm HEMTs-on-sapphire technology)

Future work:

Optimization of GaN material and device technology
Incorporate GaN amplifiers into spatially combined modules