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Innovative Microwave Power Amplifier Consortium Center

Ph.D. Defense

GaN HEMTs based Flip-chip Integrated Broadband Power Amplifier

Jane Xu

University of California at Santa Barbara

Committee:
Prof. Stephen Long
Prof. Umesh Mishra
Dr. Yi-feng Wu
Prof. Bob York(Chairperson)

Outline

GaN power HEMTs design

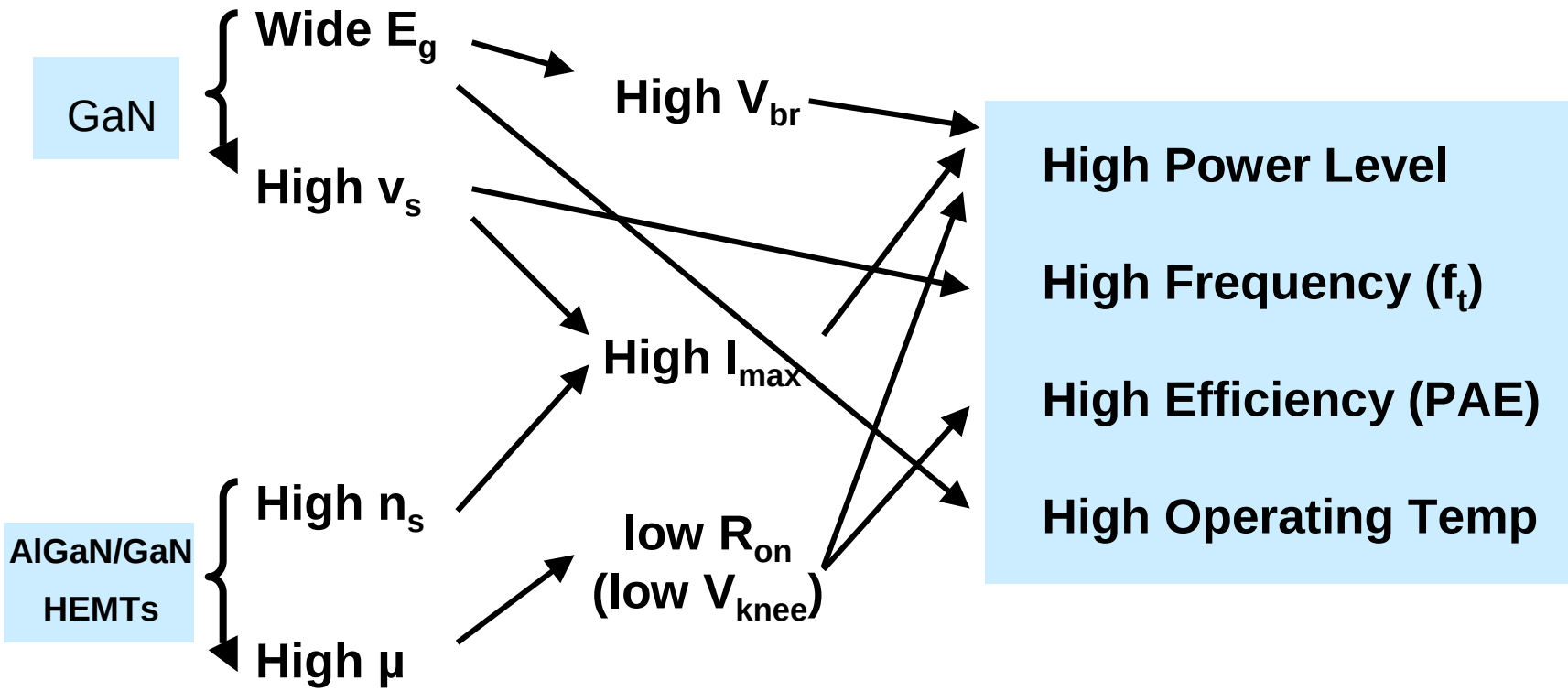
- *Small device evaluation (100μm)*
- *Large device design*
- *Thermal management (Flip-chip mounting)*

GaN broadband power amplifier design

- *Limit of conventional TWA*
- *GaN modified TWA*
- *GaN LCR-matched PA*
- *GaN 2$\times$2 matrix modified TWA*

Conclusions

Why AlGaN/GaN HEMTs?



Promising Microwave Power Device

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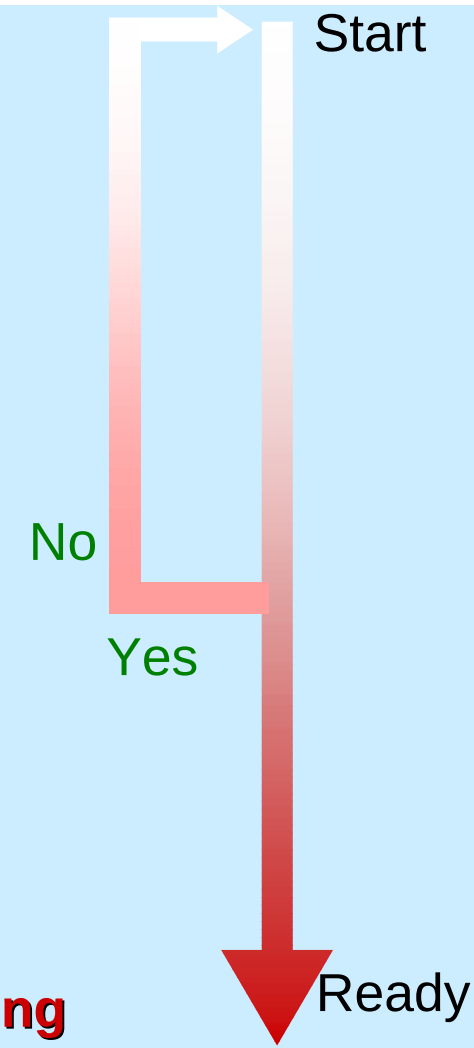
Power Device Realization Flow
(5-6 masks & dicing)

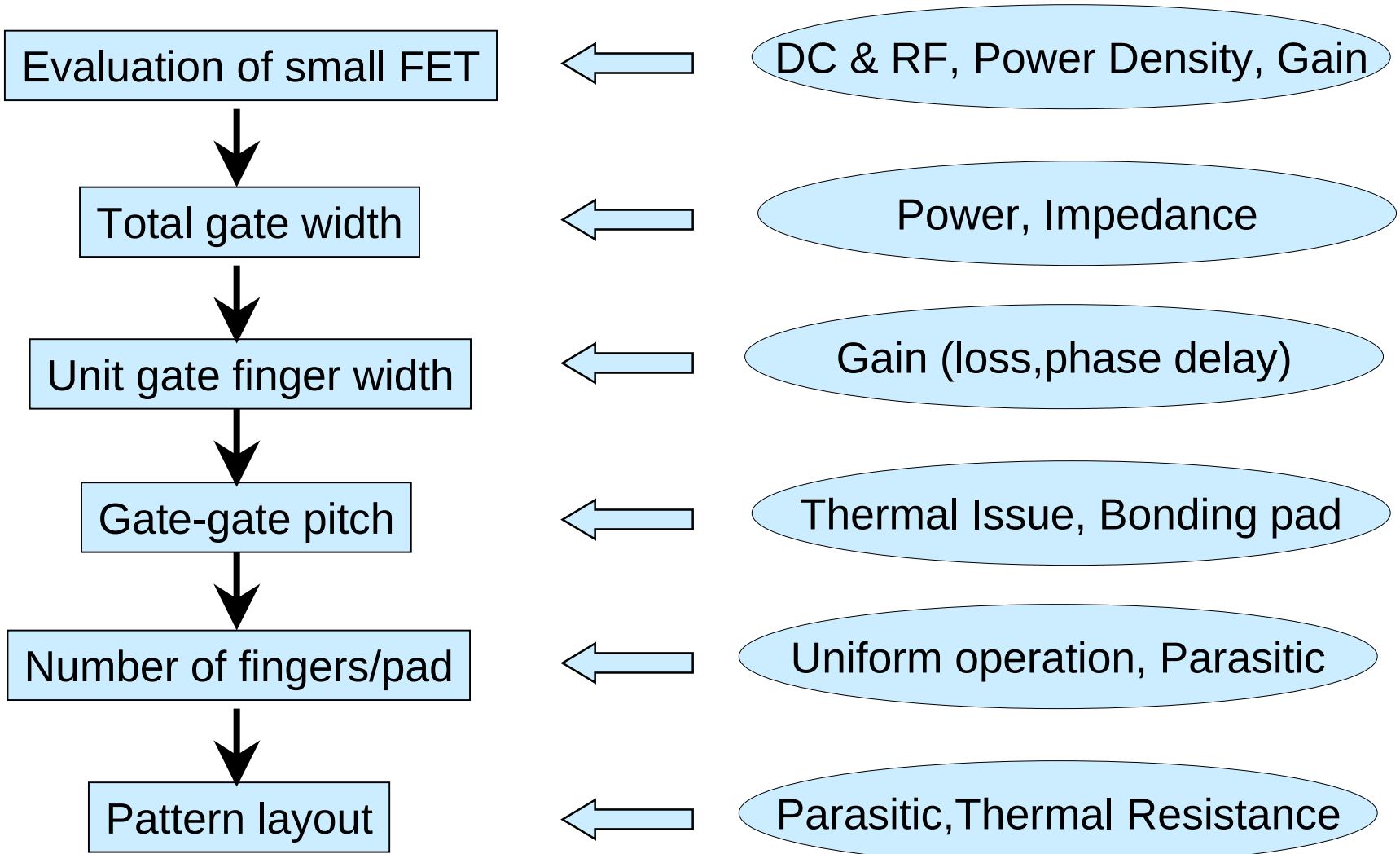
- MOCVD growth of $Al_xGa_{1-x}N$/GaN HEMTs
- Device Process
  - Ohmic Contact (Source and Drain)
  - Pad Isolation & Schottky Contact(Gate)
  - Mesa Isolation
- DC & RF measurement on small device
  - Power Density, Gain, PAE

$P_{out} > 3W/mm$?

- Large Area Device Process
  - Bonding Bumps
  - Air-bridges
- Dicing Wafer Into Discrete Devices — Dicing
- Ready for Bonding to Circuit — Flip-chip Bonding



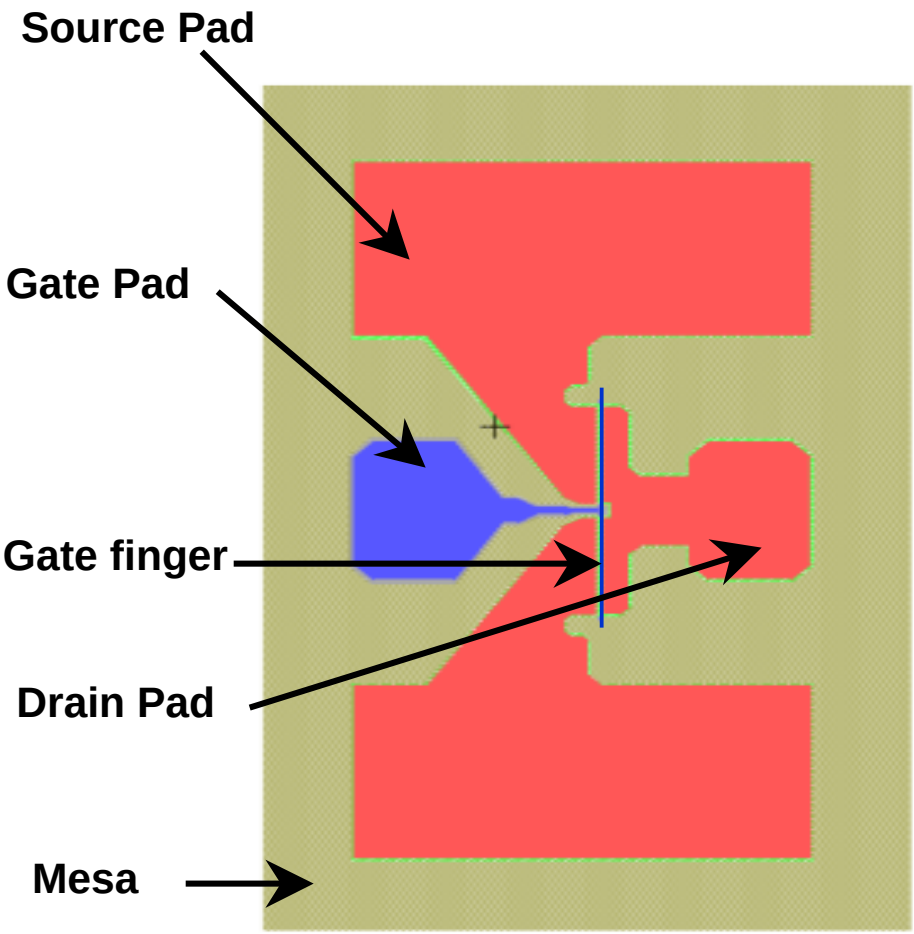
Power Device Design Flow



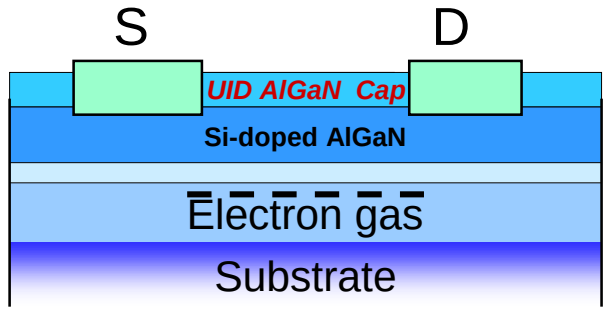
Evaluation of small devices (100μm)

1) *DC characterization*
2) *Dispersion*
3) *RF characterization*
4) *Immature GaN material*

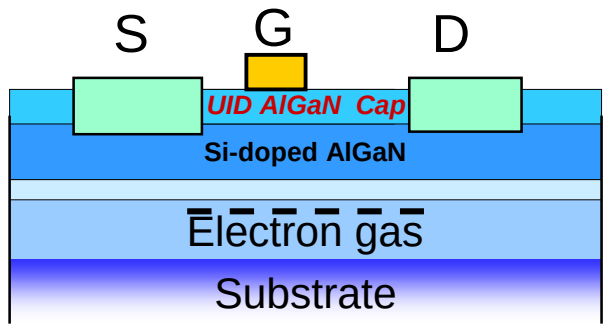
100 μm Unit FET



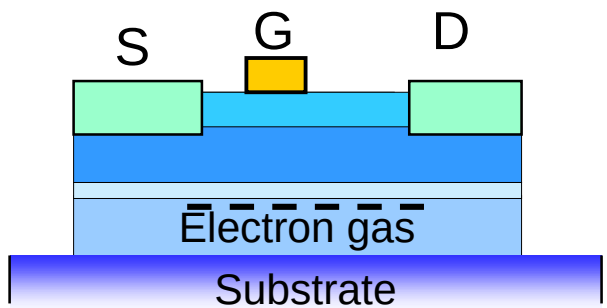
Ohmic Contact



Gate Pad Isolation & Schottky Contact



Mesa Isolation

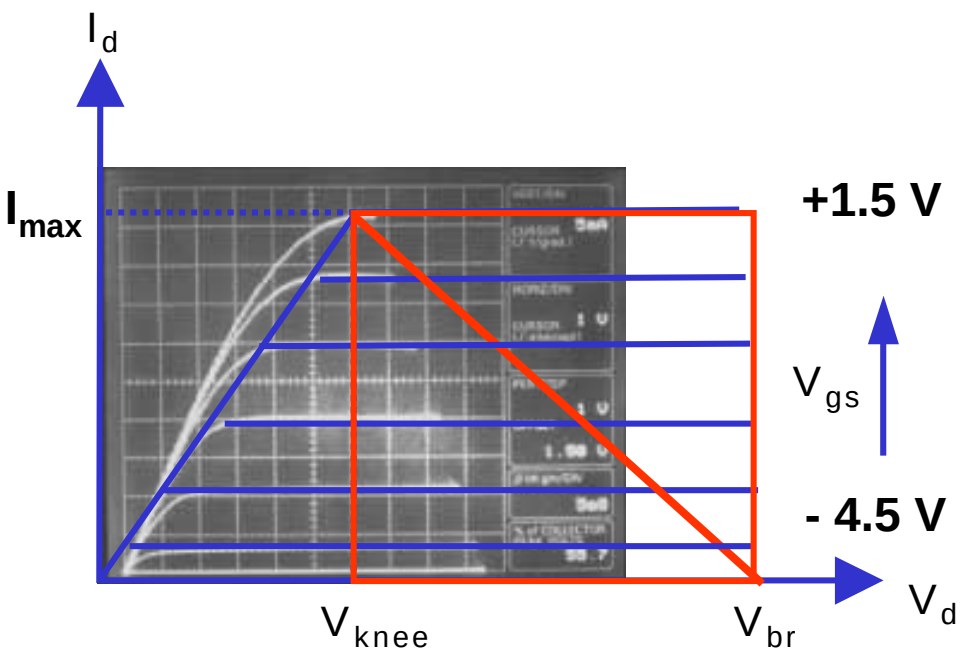


DC Characterization

$$P_{out} = \frac{1}{8} I_{\max} \times (V_{br} - V_{knee})$$

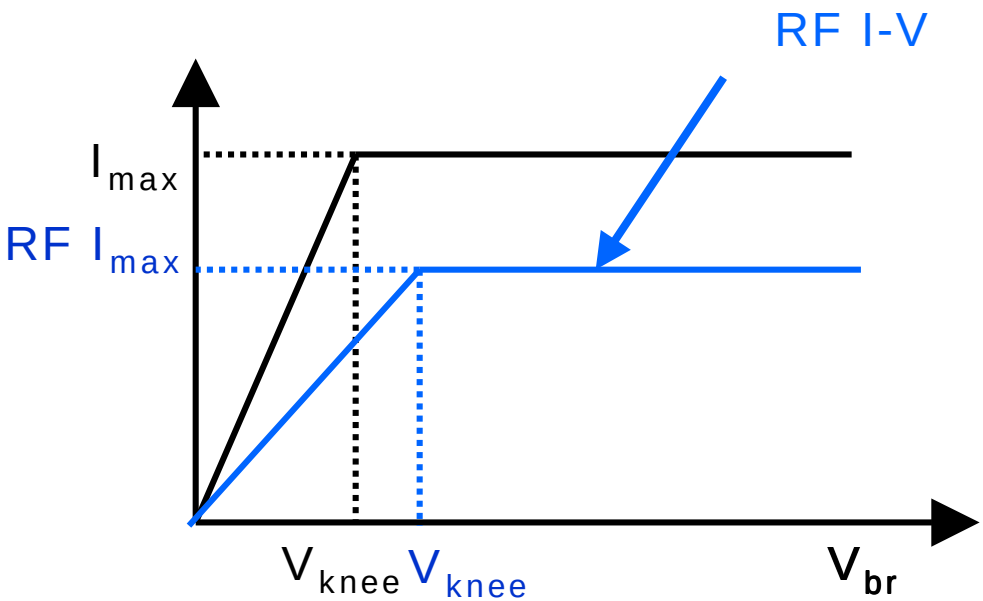
Expected Power Density for GaN on Sapphire

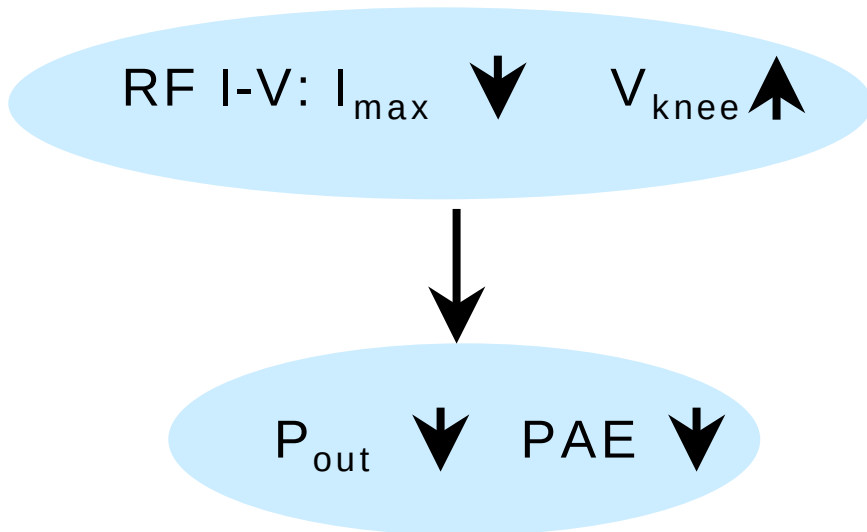
P_{out} = 5.6 W/mm



V_{knee}: ~ 5 V
I_{max}: ~ 1000mA/mm
V_{pinch}: ~ - 5 V
V_{br} : ~ 50 V
$G_{m\text{-}ext}$: ~ 200 mS/mm

Effect of Traps in GaN Materials





Reasons:

Traps in AlGaN & GaN, Surface States,etc

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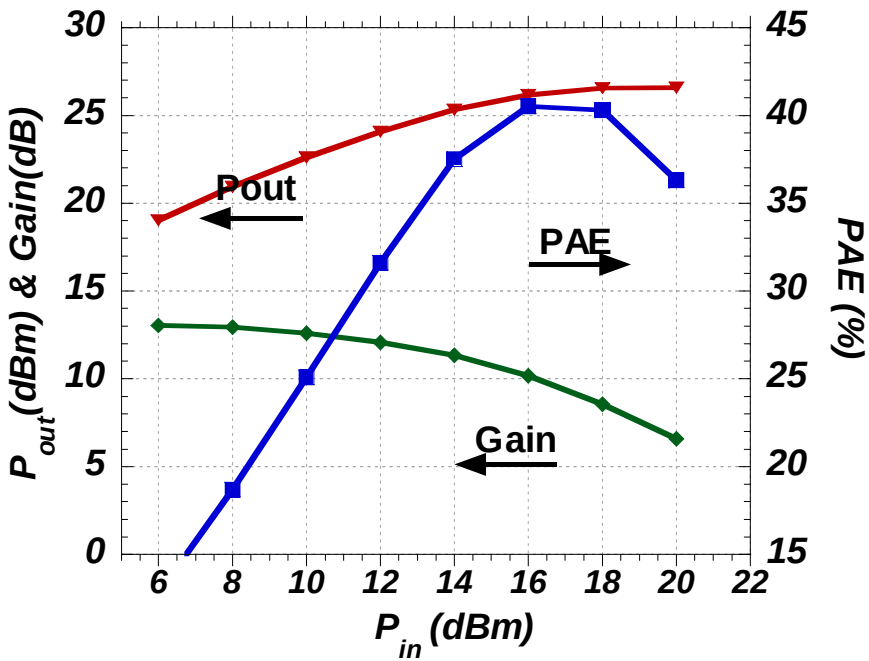
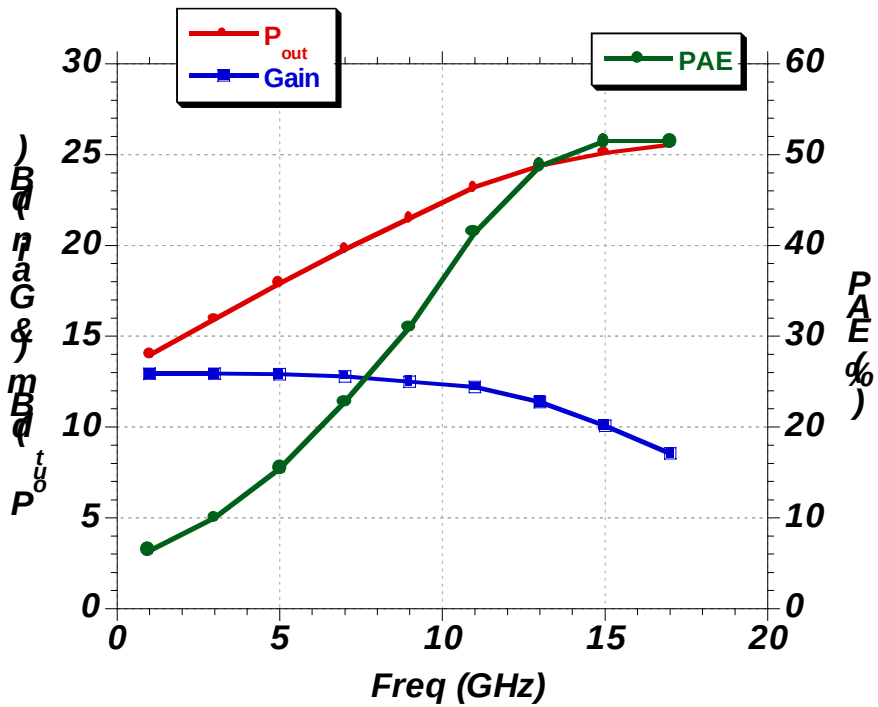
Maximum Power Density and PAE (100 μm device)

P_{out} = 4.6 W/mm, PAE = 40%
biased @ V_d = 25 V, I_d = 200 mA/mm

P_{out} = 3.6 W/mm, PAE = 52%
biased @ V_d =18 V, I_d = 200 mA/mm



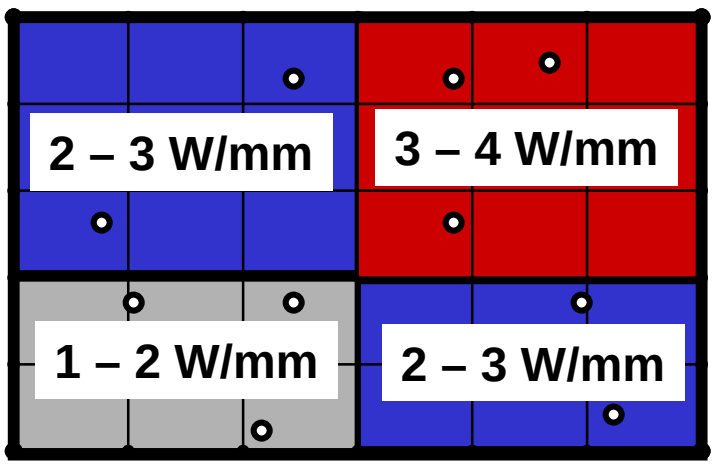


Immaturity of GaN materials

Material NonUniformity across Wafer

Typical map of power density

Power density:
1- 4 W/mm



Issues:

- **Non-uniformity of the Wafer**

20 – 30 %

- **Dispersion Variation**

10 –20 % to 50-60%

- **Breakdown Voltage Limit**

40 –50 V

- ***High Dislocation Density***

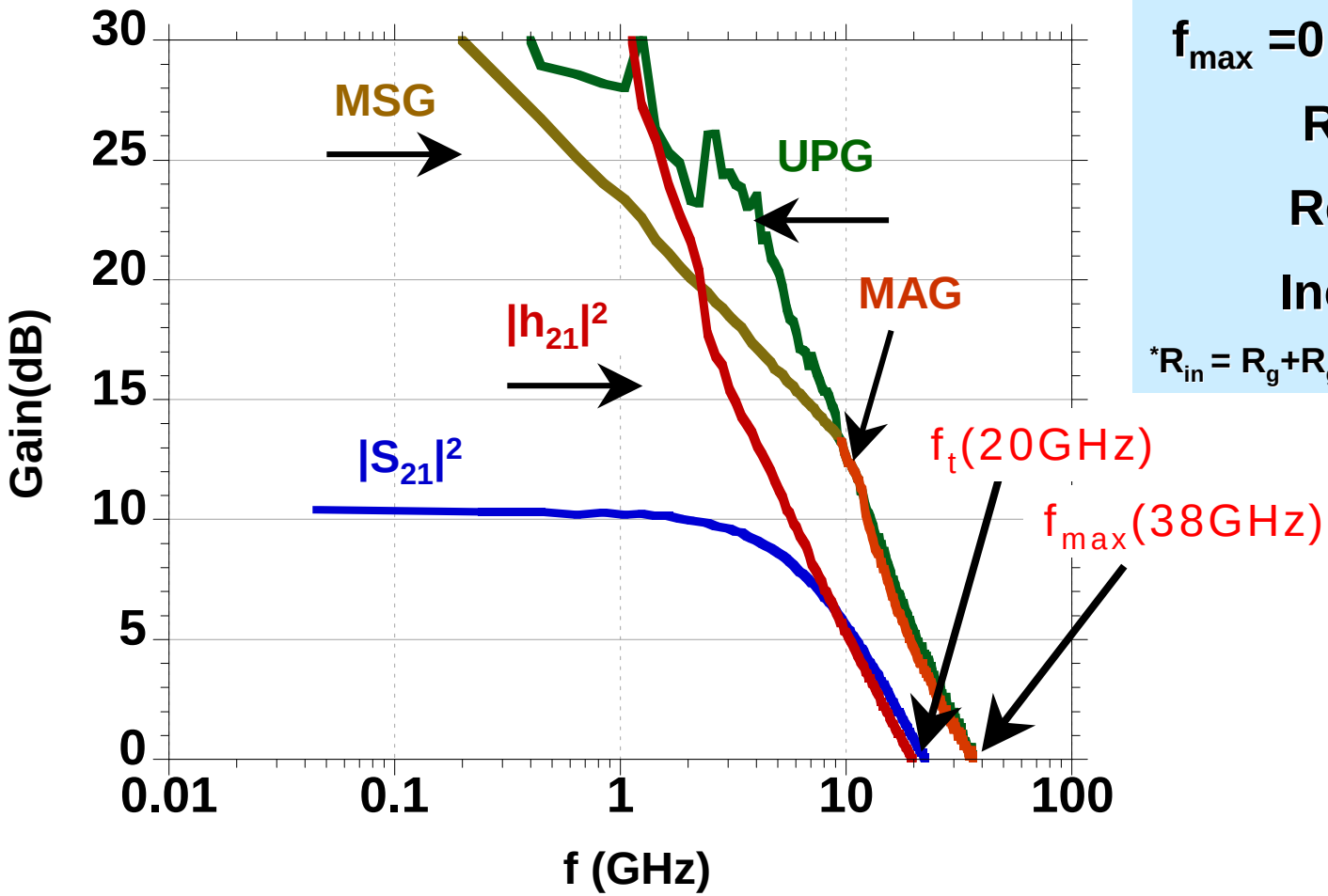
~ 10^{8} cm^{-2}

- **Poor Reliability**

Overdriven failure

f_t and f_{max}

L_g= 0.7 μm, biased @V_{ds} = 15 V, I_{ds} = 400mA/mm



$f_t = g_m/(2\pi C_{gs}) = v_s/L_g$

$f_{max} = 0.5 * f_t * (R_{ds}/R_{in})^{1/2}$

Reduce L_g

Reduce R_{in}*

Increase R_{ds}

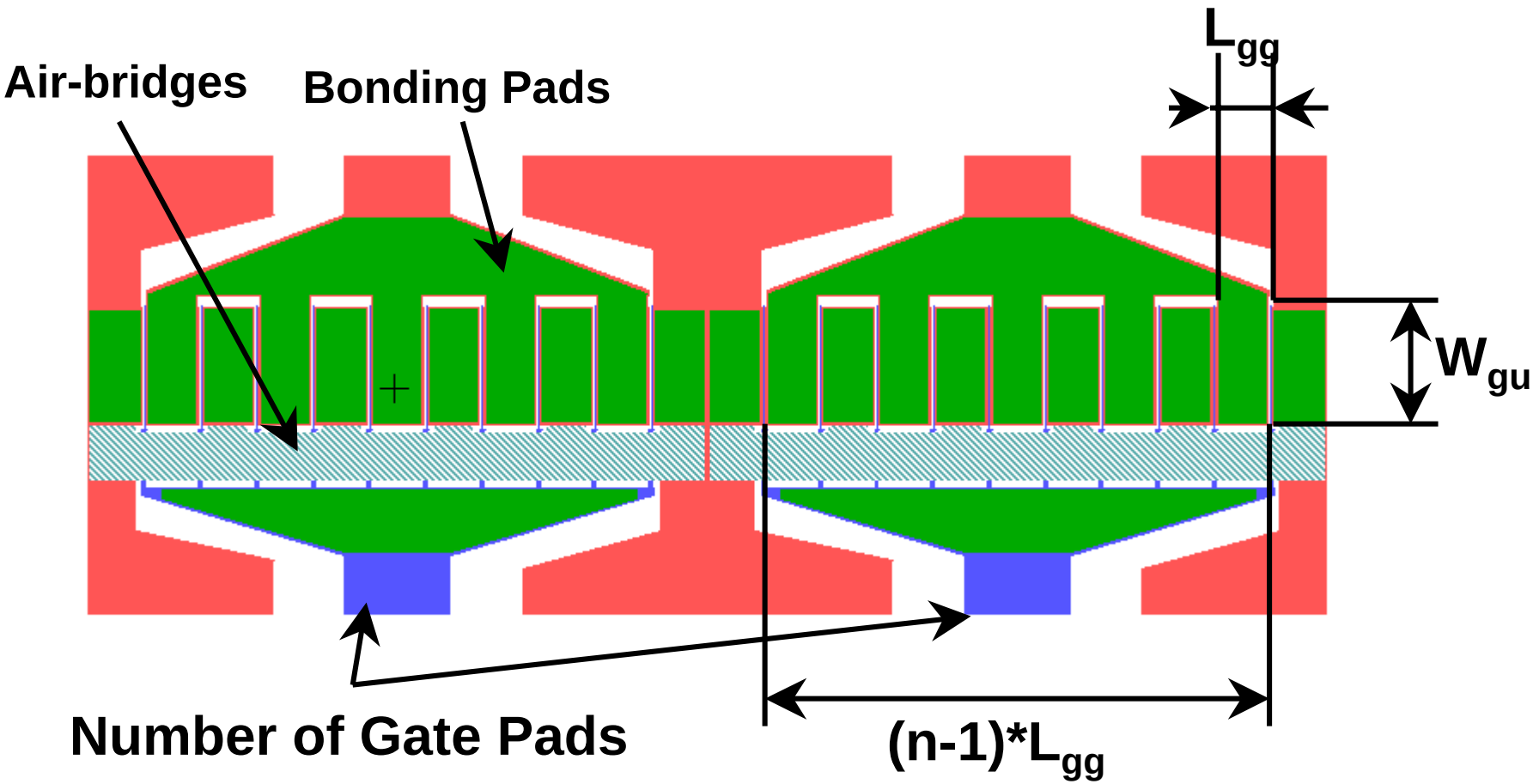
*$R_{in} = R_g + R_{gs} + R_s$

Large-periphery Device Design

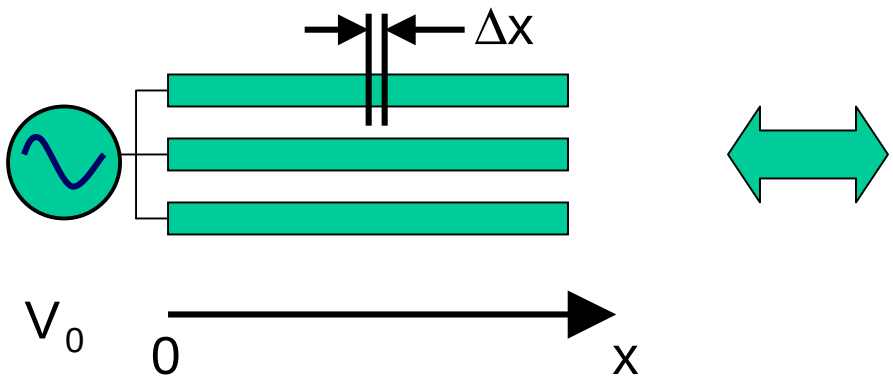
1) *Pattern layout*
2) *Thermal management*
3) *Results and problems*
4) *Optimum Load*

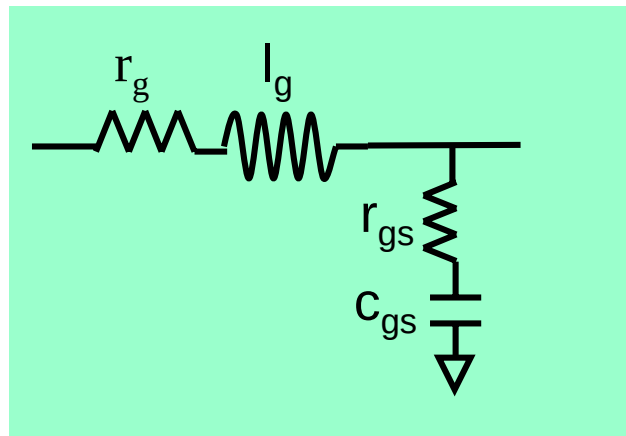
Multi-finger FET Design

How to choose L_{gg} , W_{gu} , n?



Unit Gate Finger Width





$$\gamma = \alpha + j\beta = \sqrt{Z \times Y} = \sqrt{\frac{r_g + jwl_g}{r_{gs} + 1/\ jwc_{gs}}},$$

For gate length L_g= 0.7μm:
r_g = 65 Ω/mm r_{gs} =1.2 Ω /mm
l_g =36 pH/mm c_{gs}=2.5 pF/mm

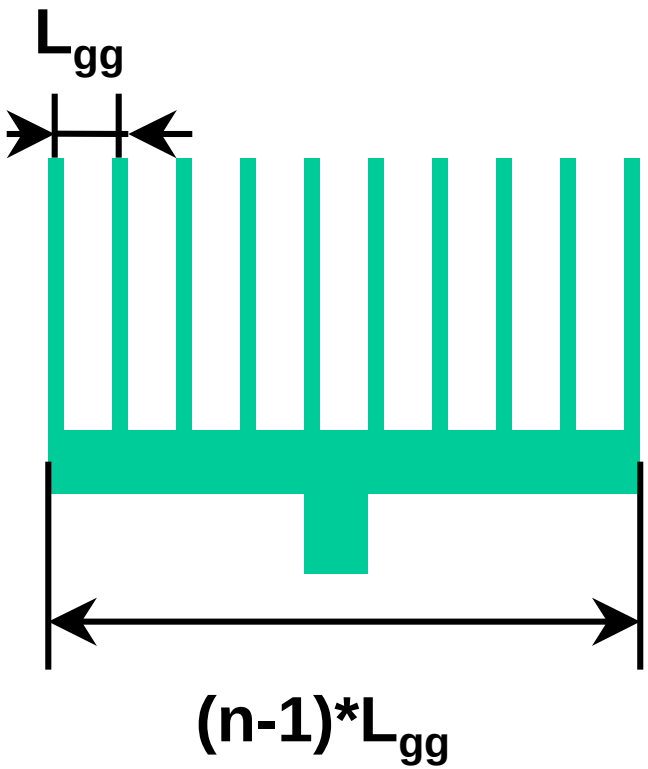
$$V(x) = \frac{V_0}{2}(e^{-\gamma x} + e^{-\gamma(2W_{gu} - x)})$$

$$P_{out} = \int_0^{W_{gu}} P_{out}(x)dx = P_{out\_ideal} \times \frac{1}{4W_{gu}} \int_0^{W_{gu}} |V(x)|^2 \, dx$$

Gain Degradation < 2 dB:

C-band:<200μm X-band:<100 μm Ku-band:<75 μm

Trade-off In Gate Spacing



Large $(n-1)L_{gg}$ ➡ Lower Gain

- ***Phase rotation***
- ***Non-uniform operation***
  (materials and process variation)
- ***Non-uniform channel temperature***
- ***Additional parasitics & losses***

Large L_{gg} ➡ Lower R_{th}

$(n-1)*L_{gg} < \lambda / 16$

(760 μm for GaN)

N = 10

L_{gg} = ~ 50 μm

Large-periphery Device Design

1) *Pattern layout*

2) *Thermal management*

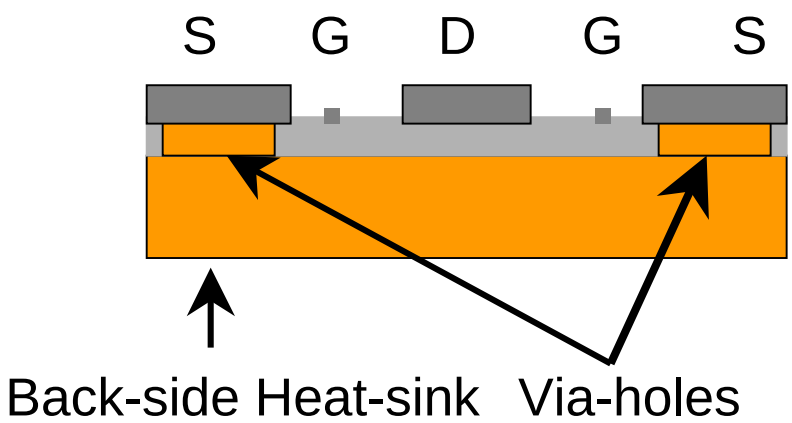
3) *Results and problems*

4) *Optimum load*

Thermal Management of Power Devices

More power dissipation → Temperature ↑ → Electron mobility ↓

→ Gain ↓ I_{max} ↓ → Output power ↓



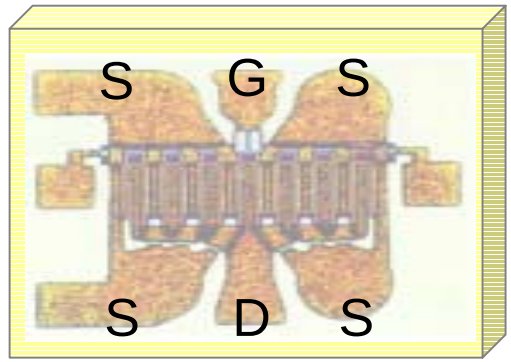
Problems for Via-holes of GaN:

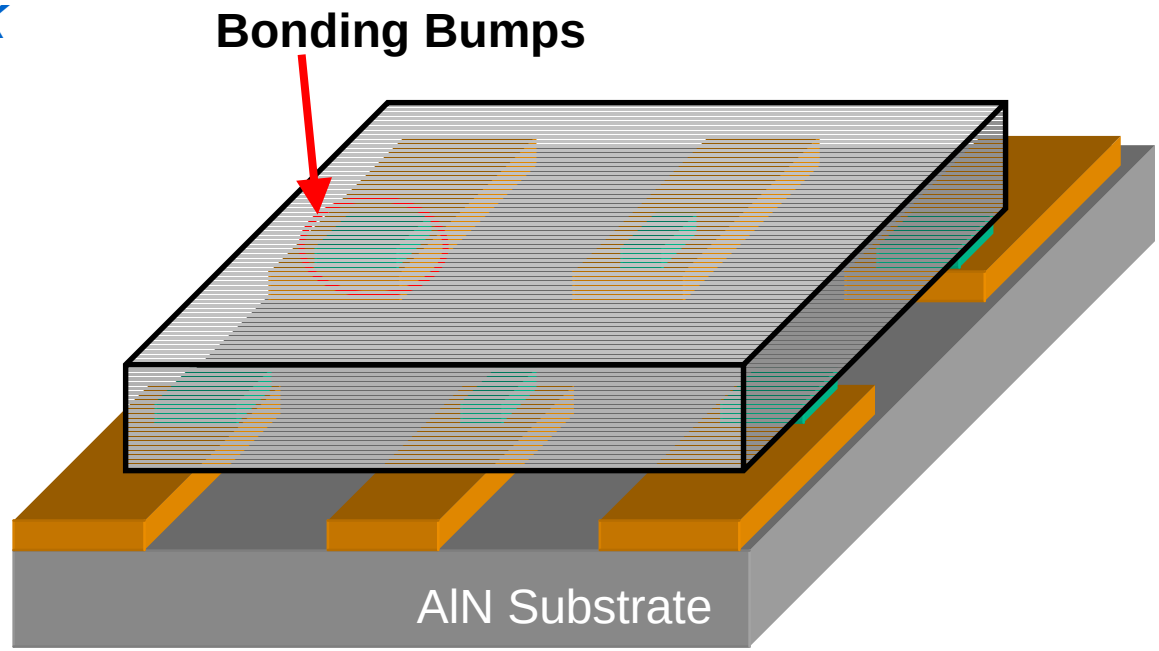
- ***GaN HEMTS on Sapphire***
  very difficult to etch
- ***GaN HEMTS on SiC***
  need develop complex process
- ***Introduce parasitic L_S***

Flip-chip Technology

Advantages:

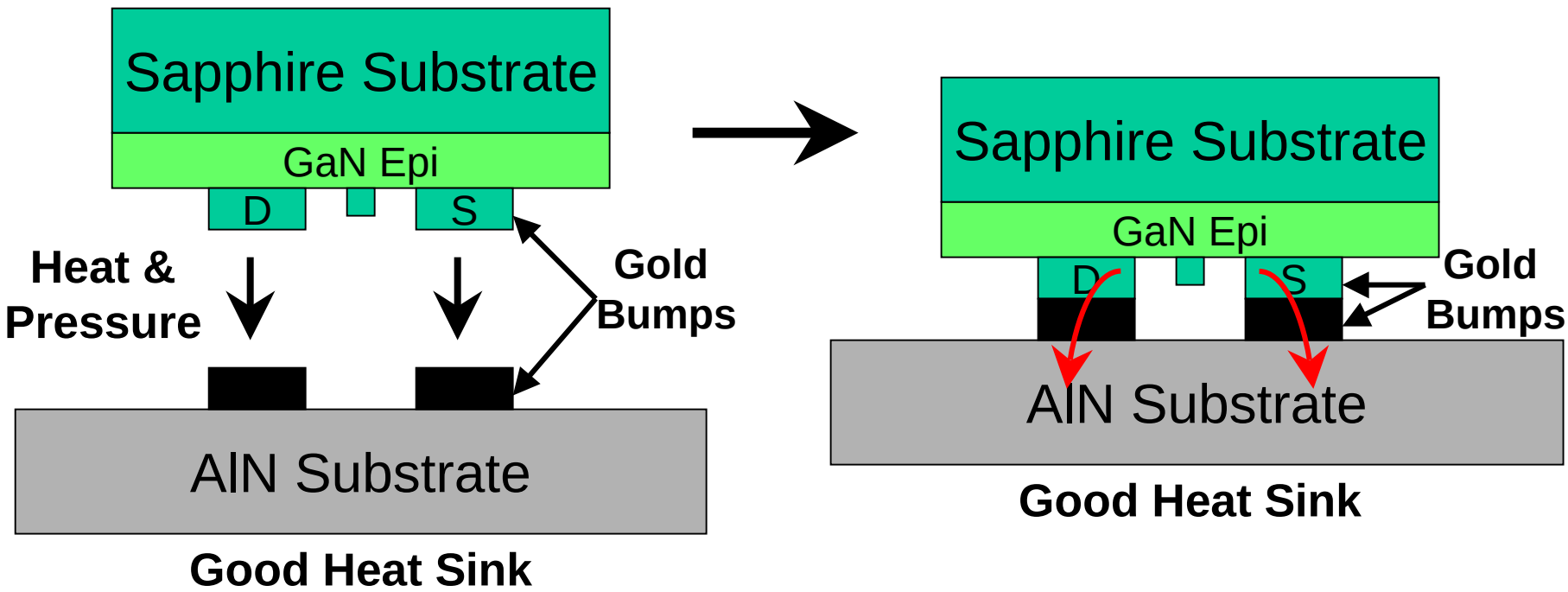
- *Minimum parasitics*
- *Better thermal management*
  - *Sapphire: σ = 30 W/mK*
  - *AlN: σ = 180 W/mK*
- *Cost effective*





Flip-Chip Mounting

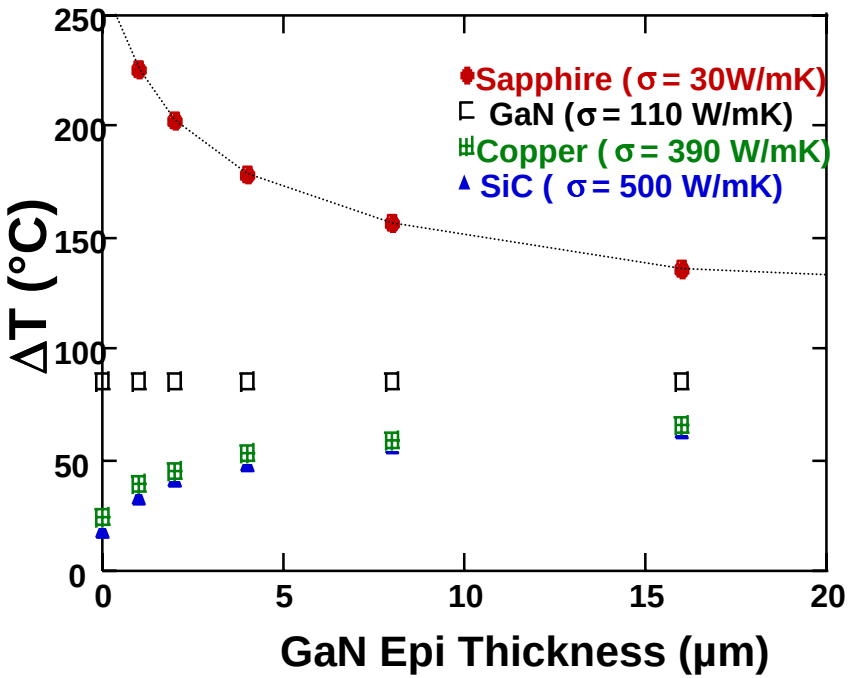
- E-beam evaporation of Au bonding bumps
- Align FET chip with circuit board using flip-chip bonder
- Bond with pressure and temp

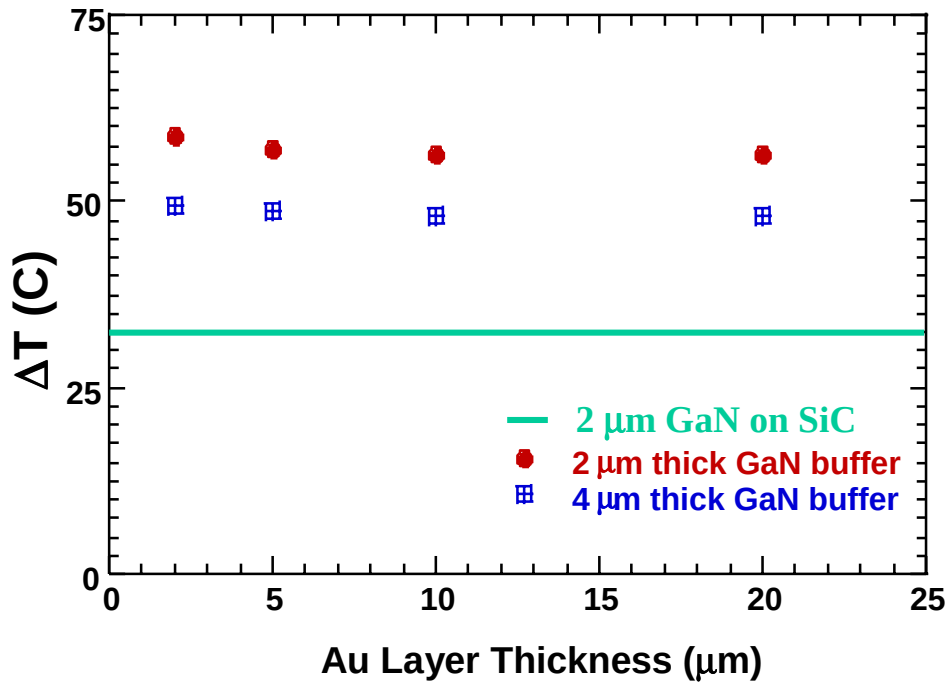


Thermal Management using Flip-chip bonding

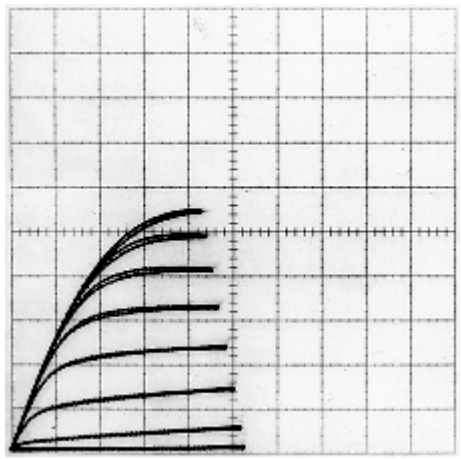
For 4 W/mm
T>200C w/o flip-chip bonding
T < 60 C with flip-chip bonding

(Finite Element Simulation)





Experimental comparison of a device before/after flip-chip bonding



Cur/Div.
200 mA/mm

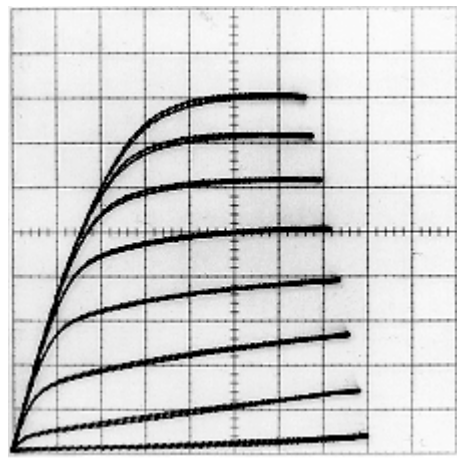
Volt/Div.
2 V

Per Step
1.0V

Offset
1.0 V

gm/div.
10 mS

50 µm x 0.25 µm Gate MODFETs
before bonding
1.1 A/mm, 200 mS/mm



Cur/Div.
200 mA/mm

Volt/Div.
2 V

Per Step
1.0V

Offset
1.0 V

gm/div.
10 mS

50 µm x 0.25 µm Gate MODFETs
after bonding
1.6 A/mm, 280 mS/mm

Dramatic improvement in both $I_{d,max}$ and g_m due to heat sinking

Large-periphery Device Design

1) *Pattern layout*

2) *Thermal management*

3) *Results and problems*

4) *Optimum load*

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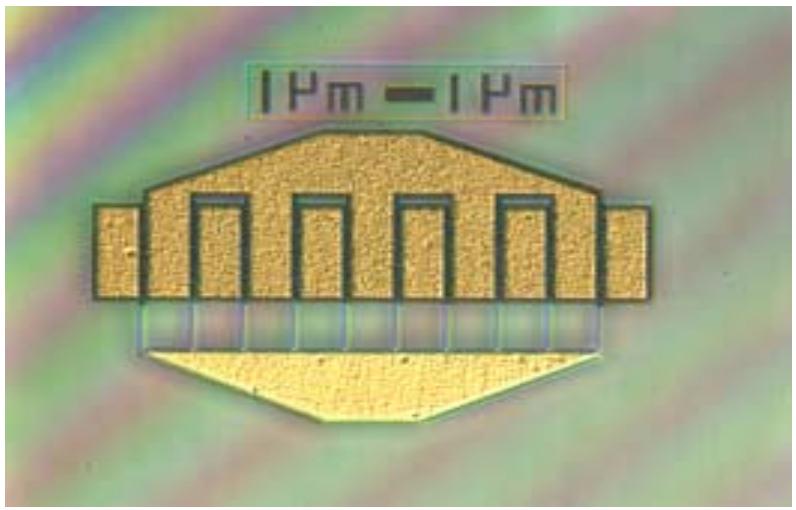
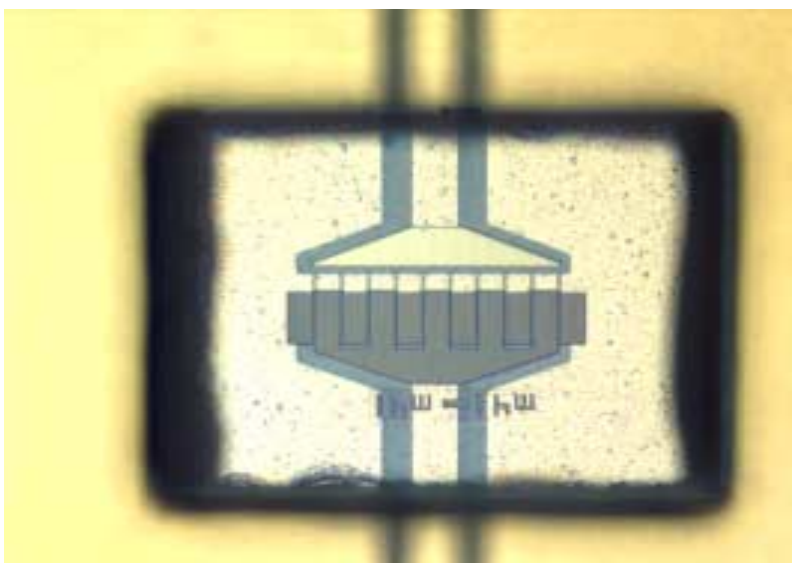
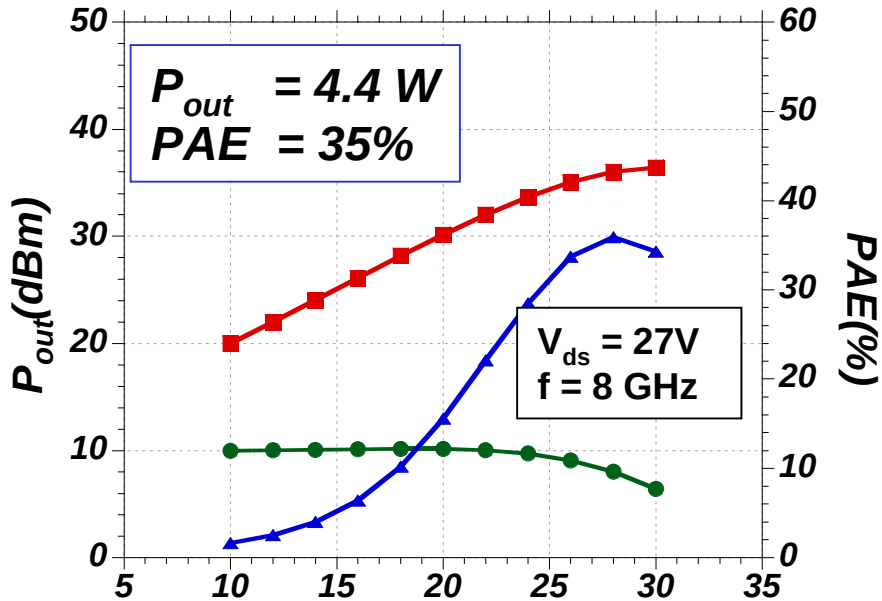
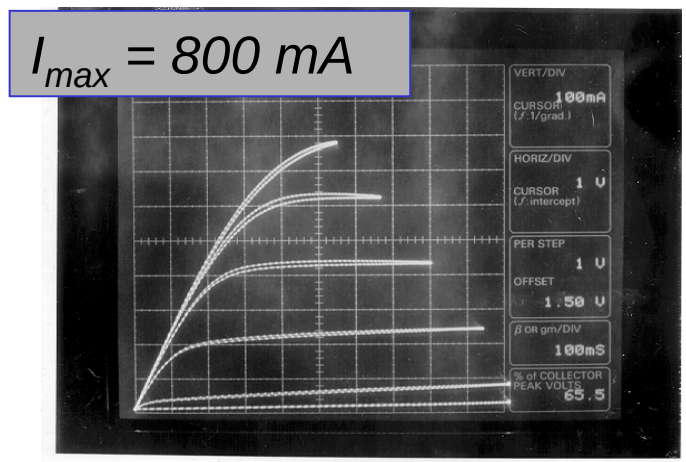
Flip-chip Bonded 1-mm GaN HEMT(L_g=0.75um)









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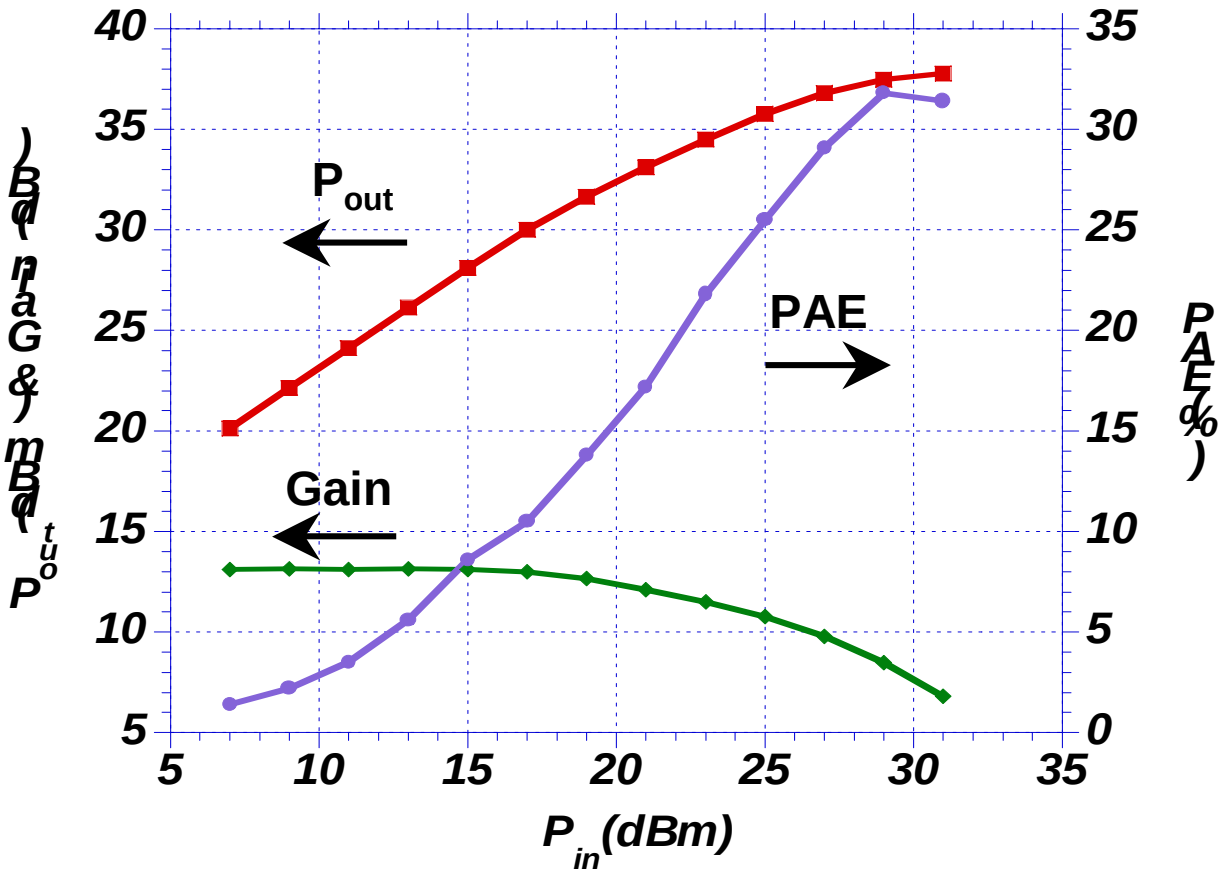
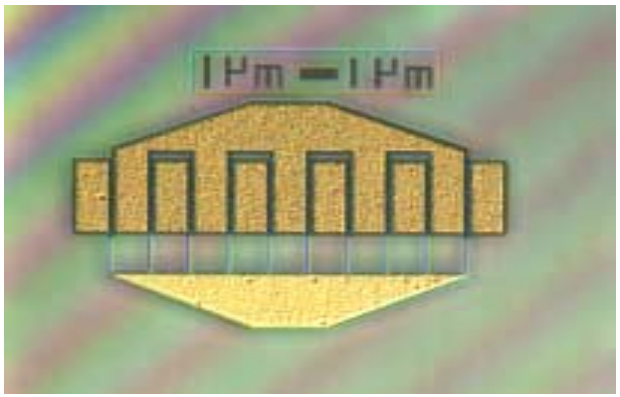
Flip-chip Bonded 2-mm GaN HEMT

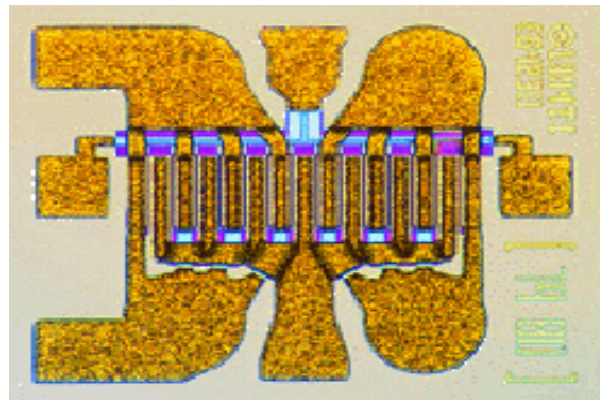
P_{out} = 6.3 Watt, PAE = 32 %, Gain = 13 dB
Biased @ V_{ds} = 25 V, f = 4 GHz, class AB



Performance
GaN vs. GaAs



Jane's GaN HEMT
(W_g = 1mm, L_g = 0.7 μm)



Triquint's GaAs HFET
(W_g = 1.2mm, L_g = 0.5 μm)

	V_{br} (V)	I_{max} (A/mm)	V_{knee} (V)	P_{out} (dBm/W)	PAE (%)	Gain (@8GHz)	R_{opt} (Ω·mm)
GaAs	22	0.3	1	28.5/0.7	55	10	50
GaN	40-50	1	5	36.5/4.4	35	10	32

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Mm-wide GaN HEMTs Power Performances

Device size	I_{max}/DC (mA)	Gain(dB)	Power (Watt)	PAE (%)
1mm*	*800 ~ 900*	*10*	*4.4*	*35*
2mm**	*1500 ~ 1800*	*13*	*6.4*	*32*
4mm	*2800 ~ 3200*	*?*	*?*	*?*

*: RF measurement was performed at 8 GHz.

**: RF measurement was performed at 4 GHz.

Practical Issues:

- *Flip-chip bonding limit*
- *ATN loadpull measurement power & biasing limit*
- *Low yield*

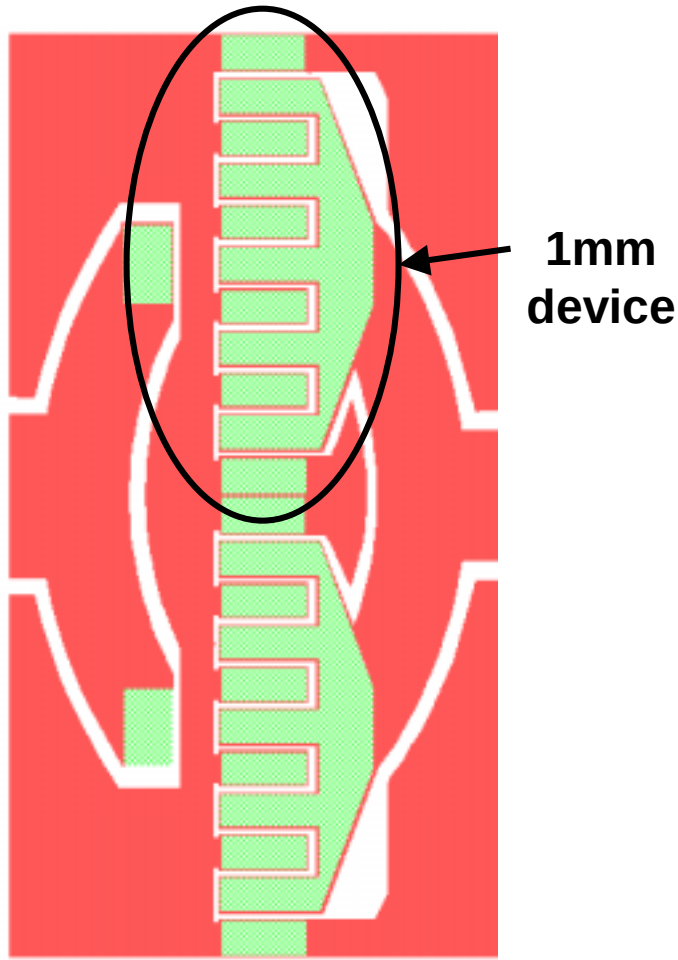
Non-scalable Property of Large Devices

1mm to 2mm:

DC I_{max}:	***10 – 20% drop***
Gain:	***3dB drop***
Power:	***2dB drop***
PAE:	***5% drop***

- ***Connection parasitics & losses***
- ***Non-uniform channel temperature***
- ***Non-uniform operation***
- ***Self-heating***
- ***Phase rotation***

Conclusion: ***Use multiple small-area discrete devices***



Large-periphery device design

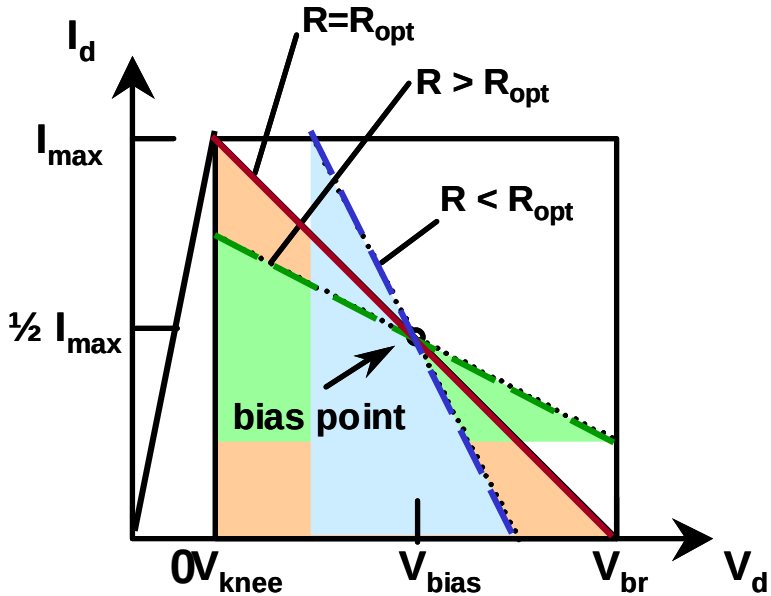
1) Pattern layout

2) Thermal management

3) Results and problems

4) Optimum load

Optimum Load



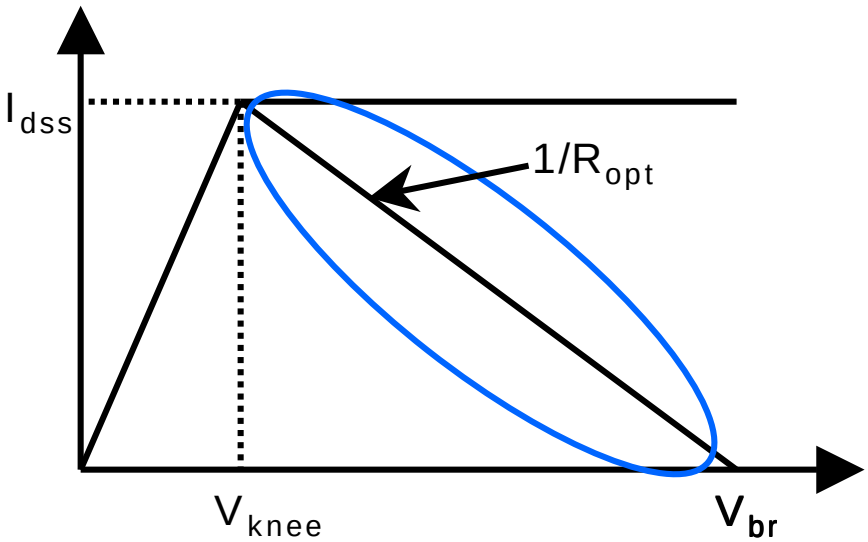
$$R_{opt} = \frac{V_{br} - V_{knee}}{I_{dss}}$$

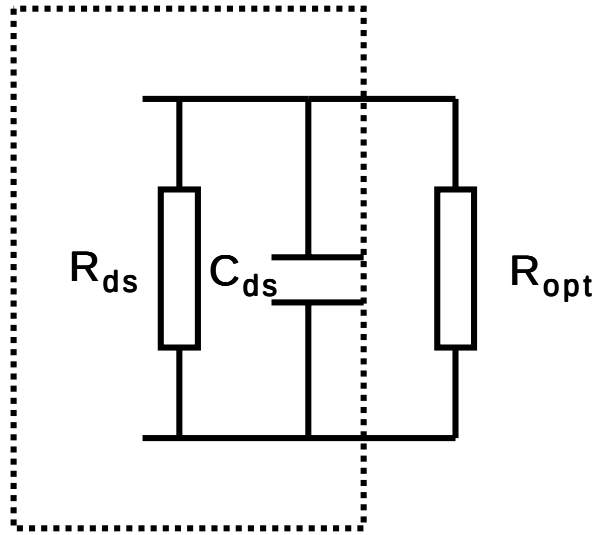
$$P_{RF,\max} = \frac{1}{8} I_{\max} \times (V_{br} - V_{knee})$$

For R >R_{opt}: $$P_{RF} = \frac{1}{2}\frac{(V_{br} - V_{knee})^2}{R_L} = P_{RF,\max} \times \frac{R_{opt}}{R_L} < P_{RF,\max}$$

For R < R_{opt}: $$P_{RF} = \frac{1}{8} I_{\max}^2 R_L = P_{RF,\max} \times \frac{R_L}{R_{opt}} < P_{RF,\max}$$

Effect of C_{ds}





GaN HEMT

Effect of C_{ds}:

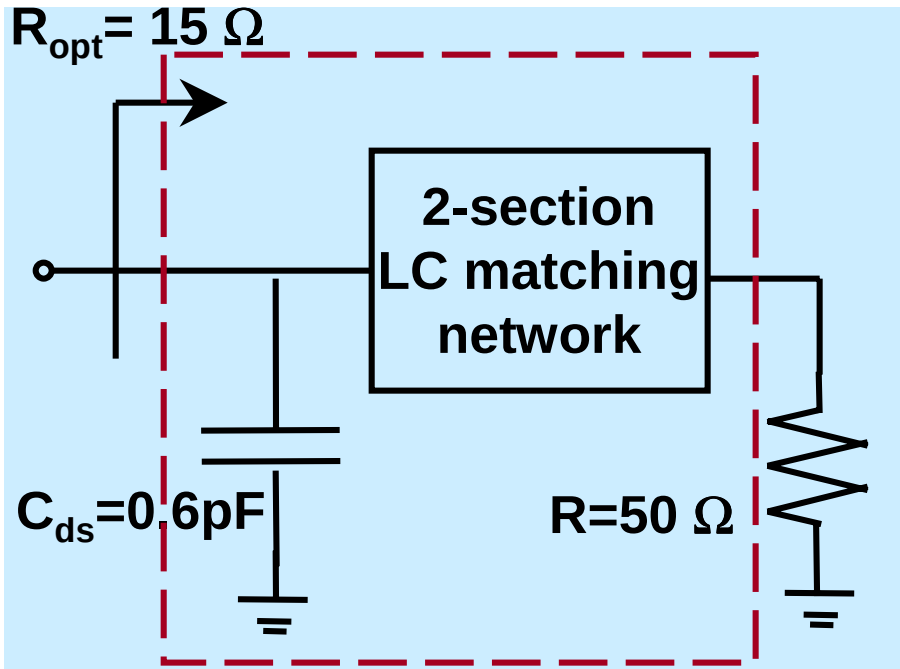
Reducing maximum P_{out}

especially near f ~ $1/2\pi R_{opt}C_{ds}$ (15 GHz)

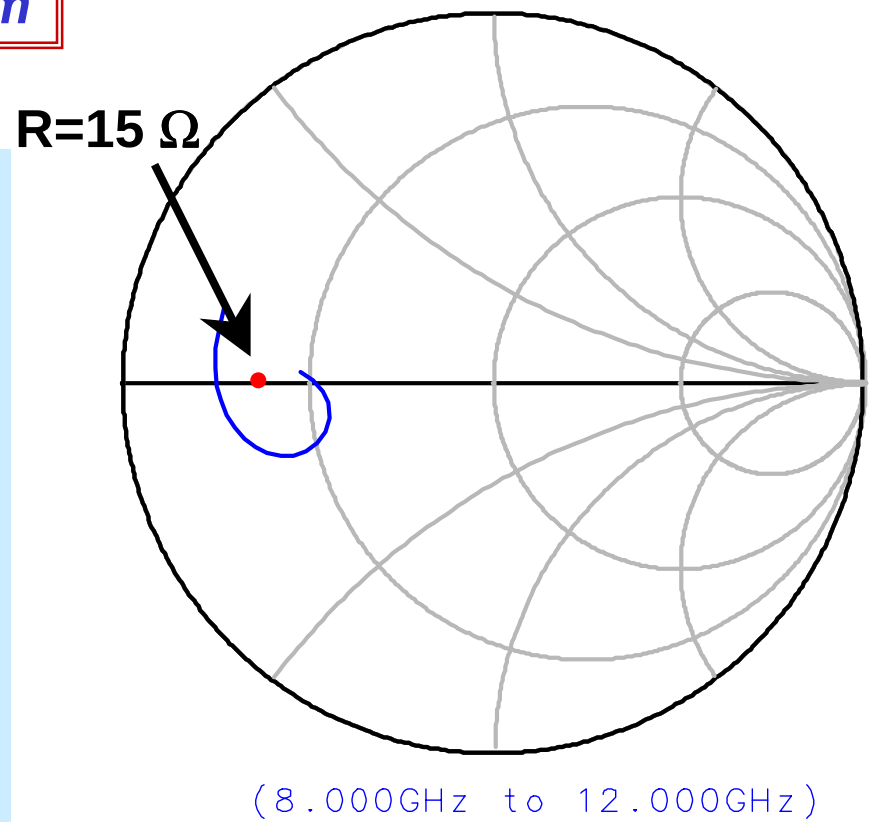
C_{ds} must be compensated for optimum design

C_{ds} Compensation

From Loadpull Measurement:
R_{opt} =32 ∠φ·mm, C_{ds} = 0.3 pF/mm



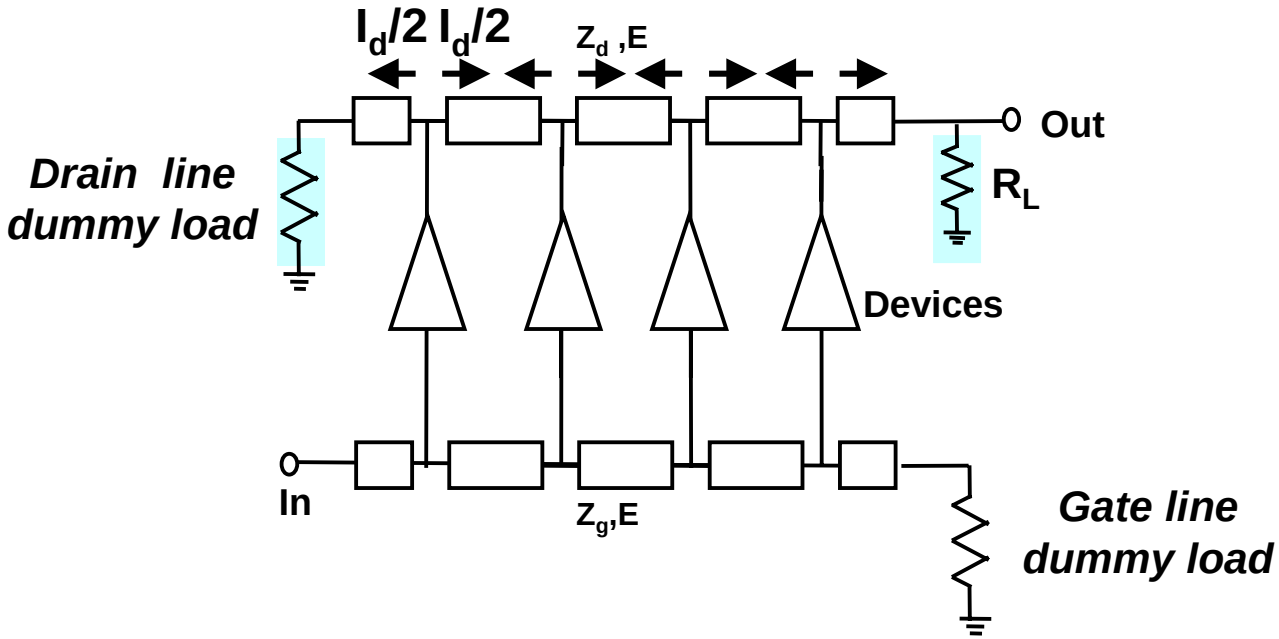
2mm-GaN C_{ds} Compensation



Broadband power amplifier design

1) **Limitation of conventional TWA**
2) **Modified TWA**
3) **LCR-matched PA**
4) **2×2 matrix modified TWA**

Conventional TWA Efficiency Limitation



Output efficiency 50%
Class-A efficiency 50%

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = DE \times (1 - \frac{1}{G})$$

Maximum efficiency < 25%

G < 10 dB

PAE < 20%

Conventional TWA Power Limitation

Largest Voltage across last FET < V_{br}

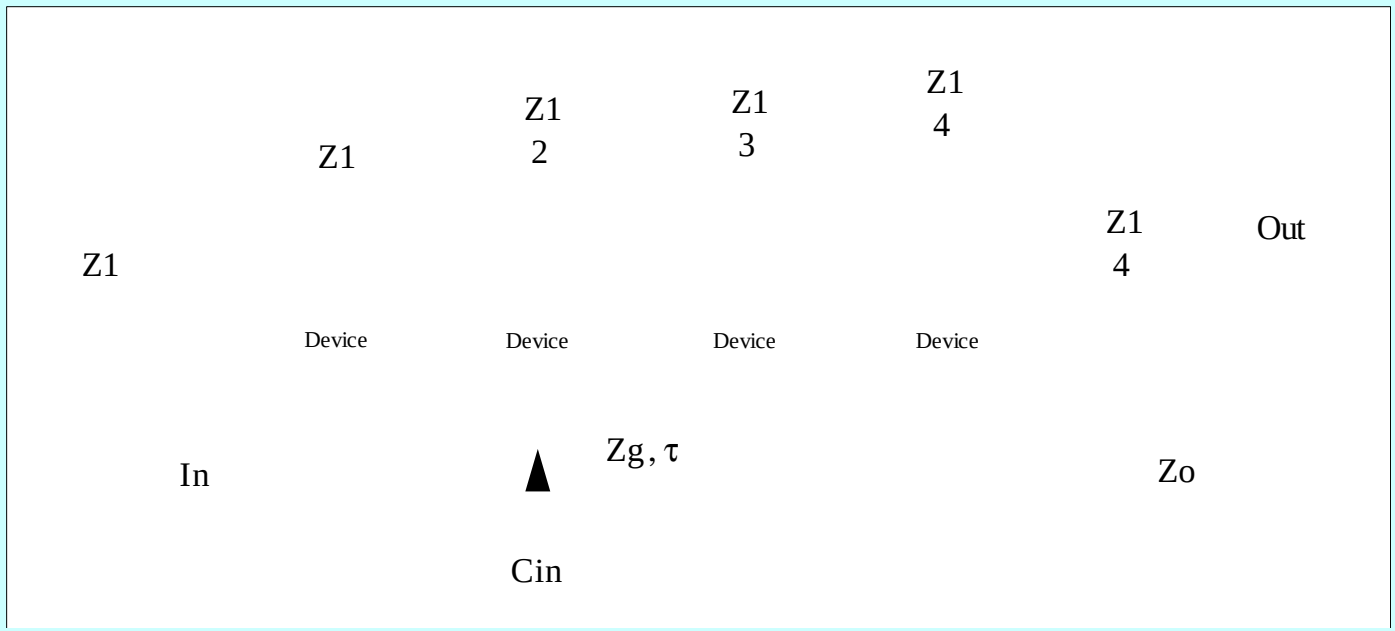
Maximum P_{out} fixed by device technology (Z_0 = 50Ω):

$$P_{RF\max} = \frac{(V_{dr} - V_{knee})^2}{8Z_0}$$

For GaAs FET:
V_{dgB} = 20 V, V_{pinch} = -2.5V, V_{knee} = 1 V, then P_{RFmax} = 0.7 W

For GaN HEMT:
V_{dgB} = 50 V, V_{pinch} = -5V, V_{knee} = 5 V, then P_{RFmax} = 4 W

Tapered Drain-line TWA



P_{out} cannot be increased

•device technology limit

Efficiency can be improved by:

•forcing more current to the real load

•using less devices

Broadband power amplifier design

1) **Limitation of conventional TWA**
2) **Modified TWA**
3) **LCR-matched PA**
4) **2×2 matrix modified TWA**

Modified GaN TWA Design

Goal:

- ***Bandwidth:*** ***8:1 (1 –8 GHz)***
- ***Gain*** ***~ 10 dB***
- ***PAE*** ***> 20 %***
- ***P_{out}*** ***6 Watt (2W/mm)***

Approach :

• *Input distributed match*	*Bandwidth & gain flatness*
• *Capacitive division*	*Broadband*
• *Corporate power combiner*	*Broadband & power*
• *GaAs prototype circuits*	*Topology verification*

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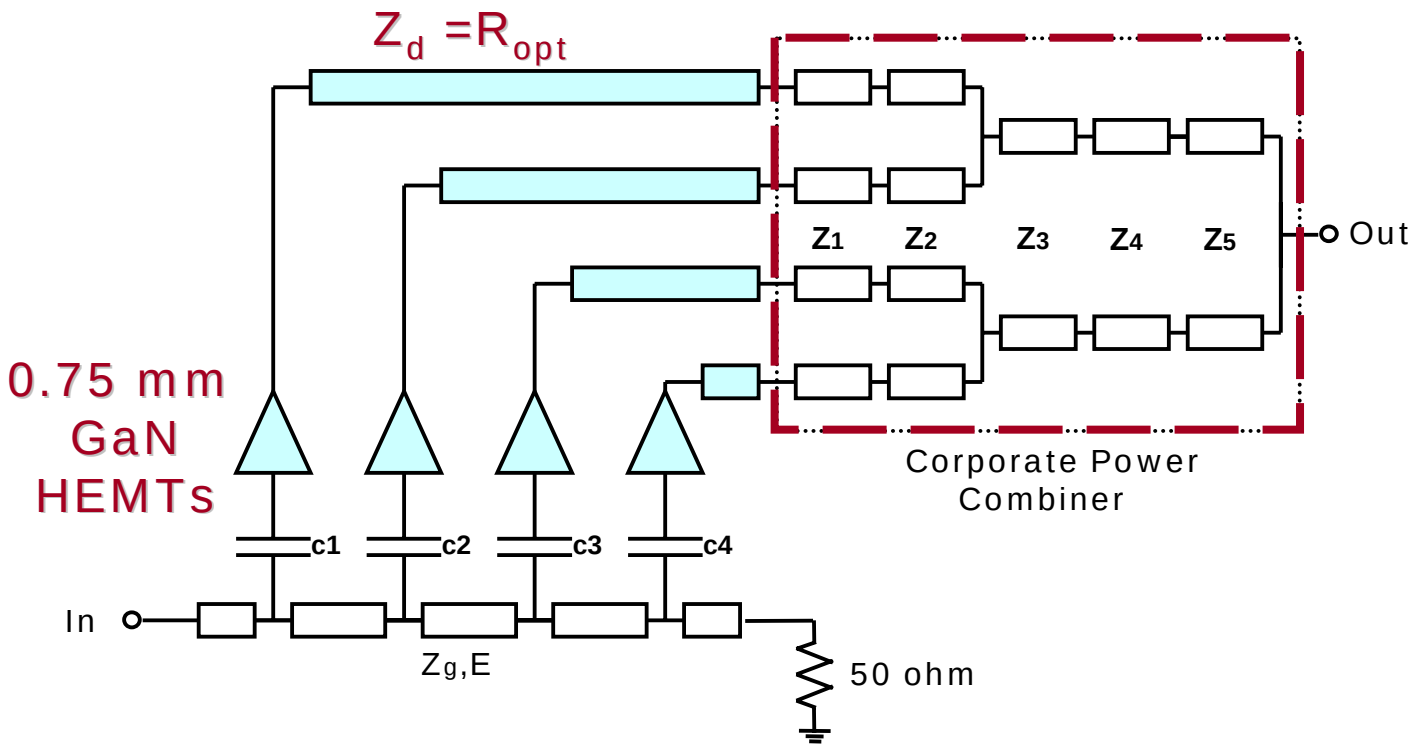
Schematic of GaN Modified TWA



Modified TWA:

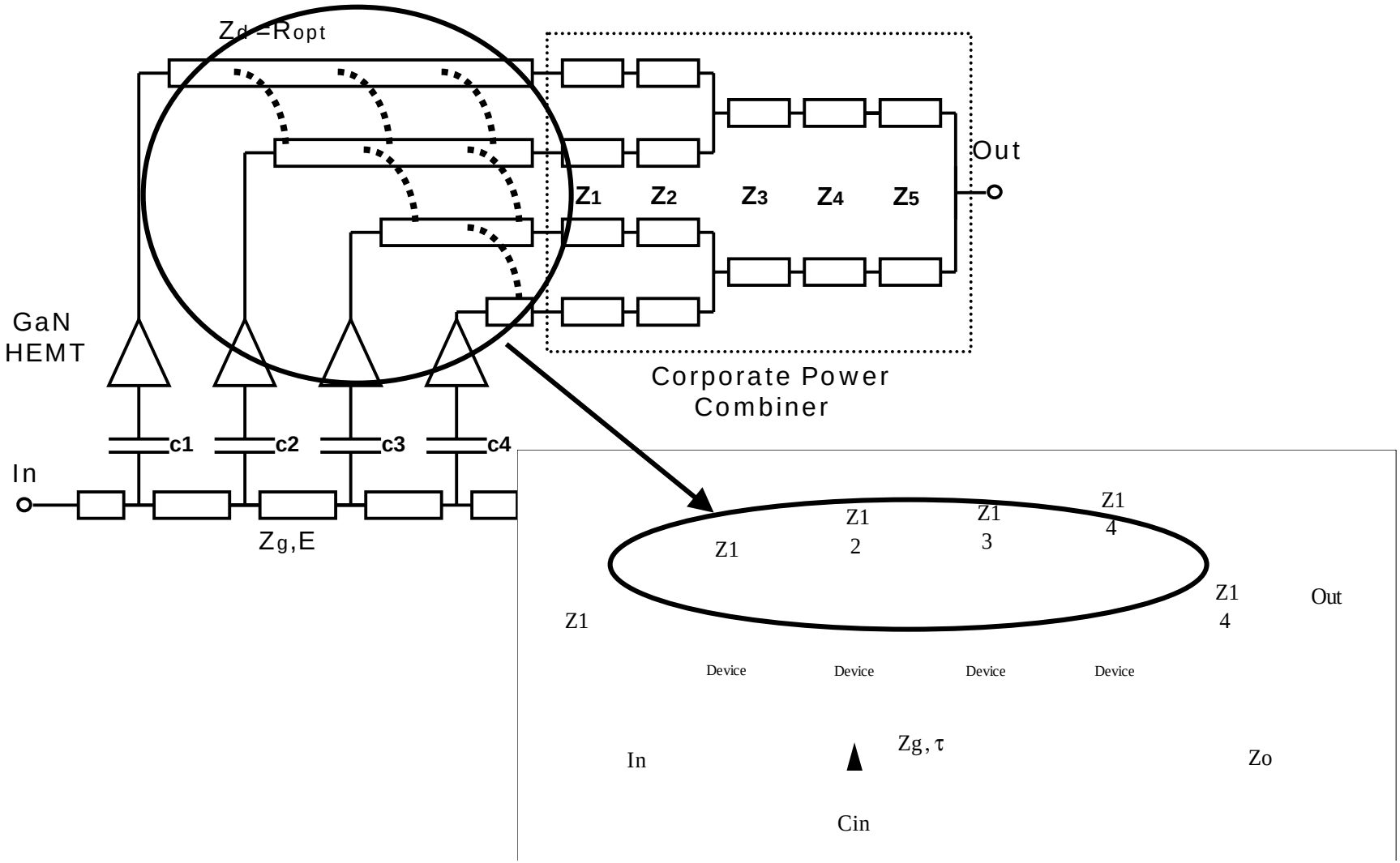
1)Eliminate backward wave

2)Broad band

3)High efficient corporate combiner

4)Avoid high impedance lines

Equivalent of Tapered Drain-lines



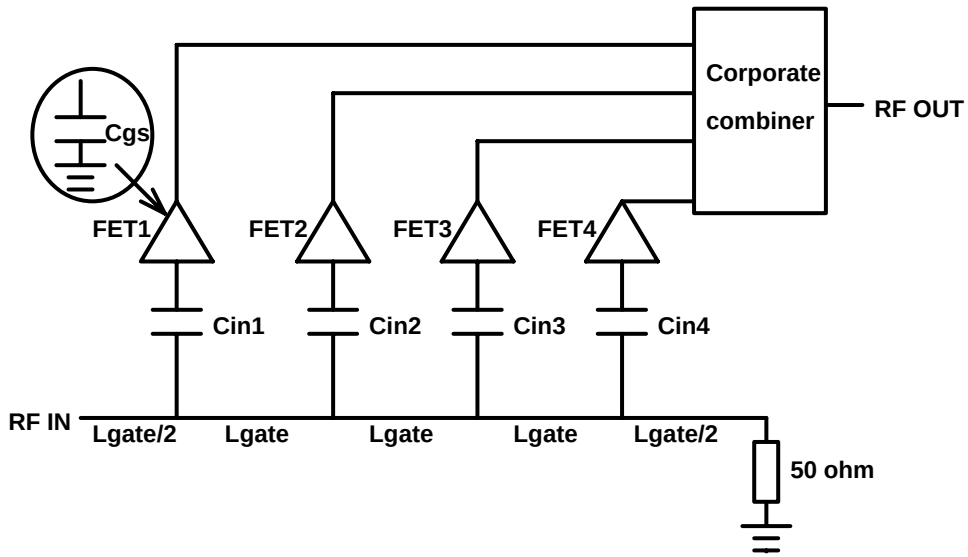
Concept of the Capacitor-division TWA

- *For power FETs, large C_{gs} is limiting the bandwidth*

$$Z_{gate} = \sqrt{\frac{L_{gate}}{C_{gate}}} = 50\Omega$$

$$f_{brag} = \frac{1}{\pi\sqrt{L_{gate}C_{gate}}}$$

$$C_{gate} = \frac{C_{in}C_{gs}}{C_{in} + C_{gs}}$$



- *Compensate the gate line loss by increasing the capacitance ($C_{in4} > C_{in3} > C_{in2} > C_{in1}$)*

$$V_x = \frac{C_{inx}}{C_{inx} + C_{gs}} V_{in} \qquad x = 1, 2, 3 \ldots N$$

Broadband Matching

Define: Bandwidth > 3:1

(f_{High}/f_{Low})

High Impedance Transformation Ratio

(4mm device):

Input: 50 : 1
(50 Ω / 1 Ω)

→ ***Distributed match***
LCR lossy match

↘

Output: 6:1
(50 Ω / 8 Ω)

→ ***Corporate power divider***
Multi-section LC match

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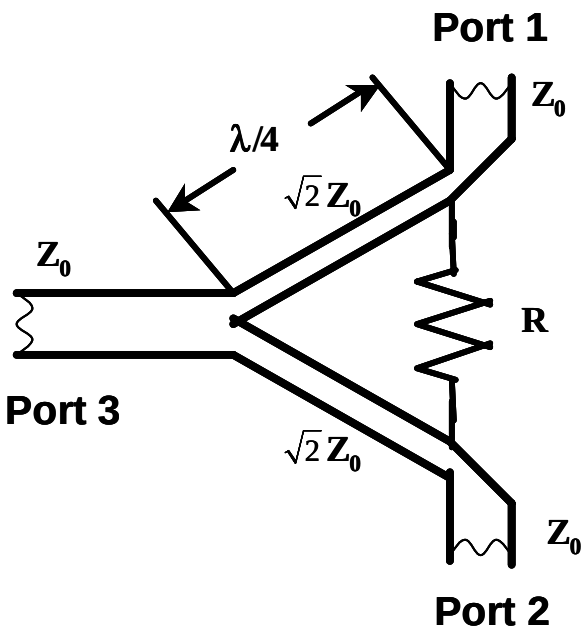
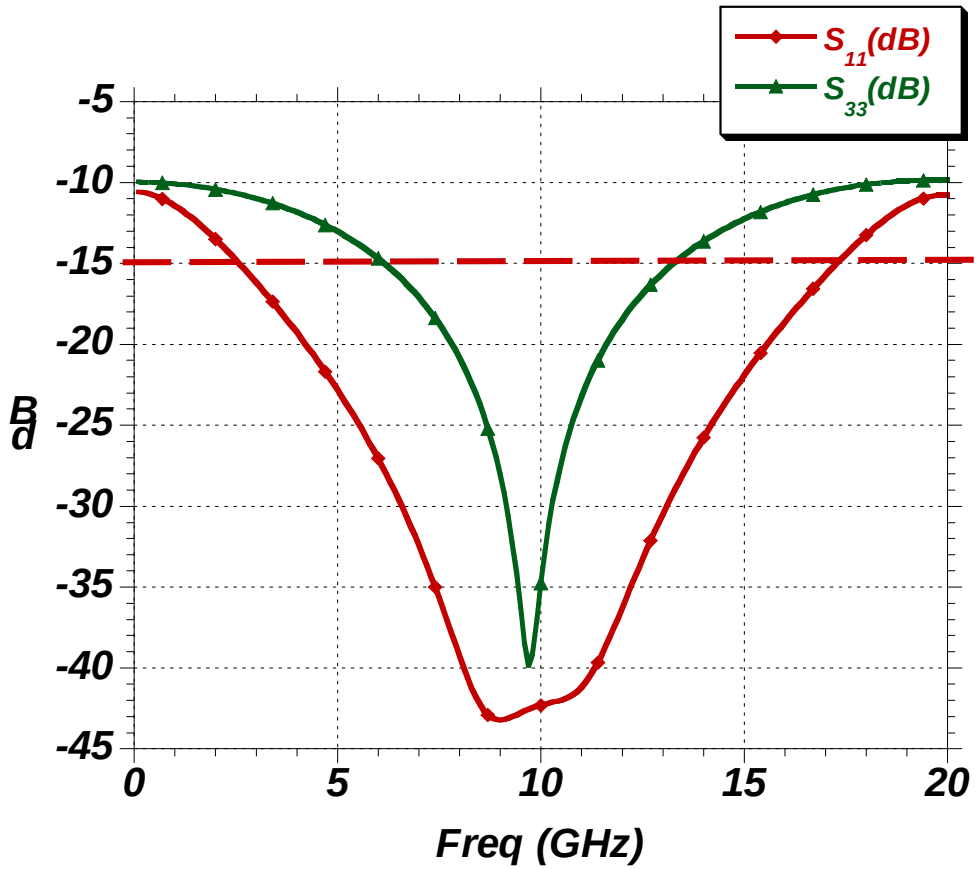
Single-section Wilkinson Power Combiner

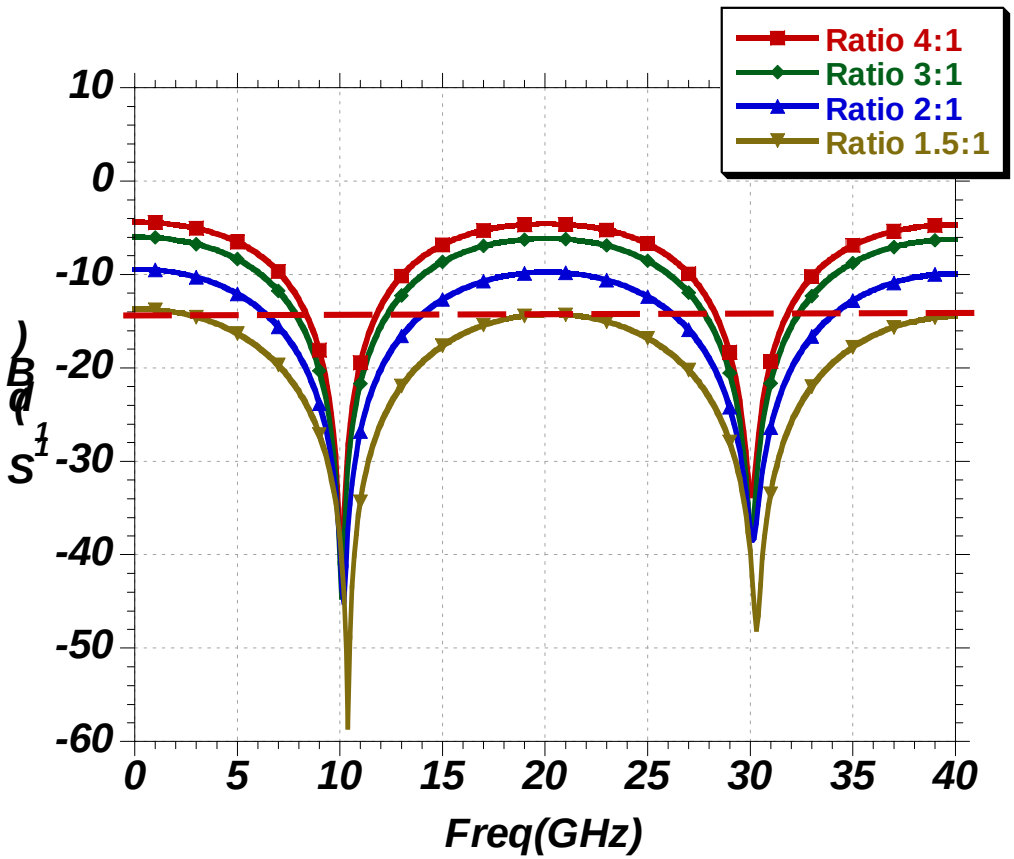
Bandwidth: 2:1



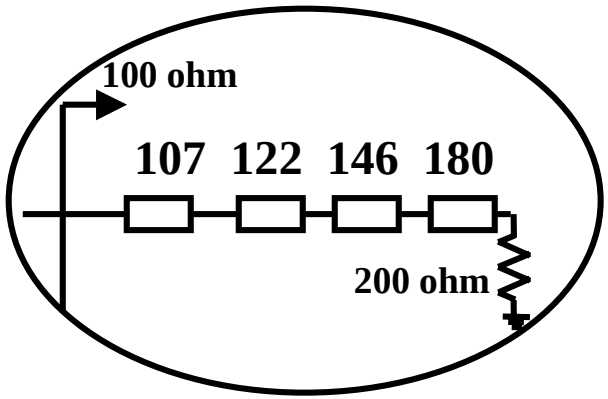


Bandwidth of λ/4 Transformer

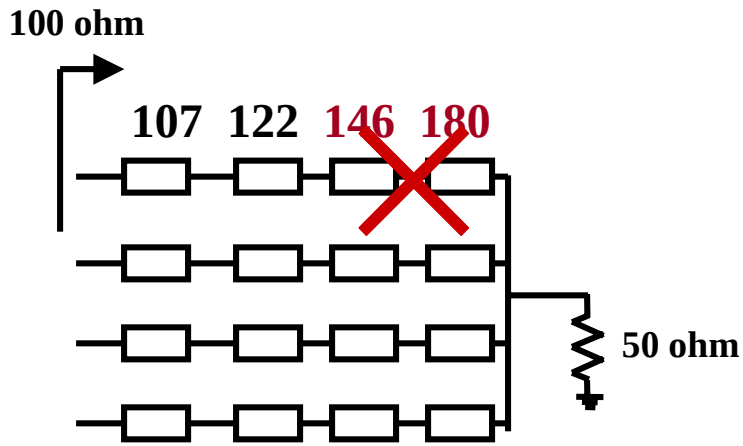
To have bandwidth 3 to 1
λ/4 transformer ratio < 1.5:1



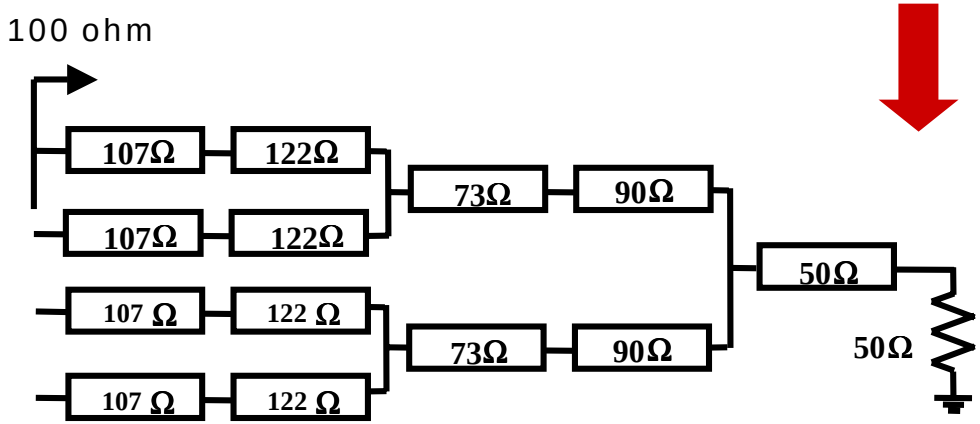
N-way & Corporate Combiner (to extend bandwidth)



Multi-section
λ/4 Transformers



N-way Combiner



Corporate Combiner

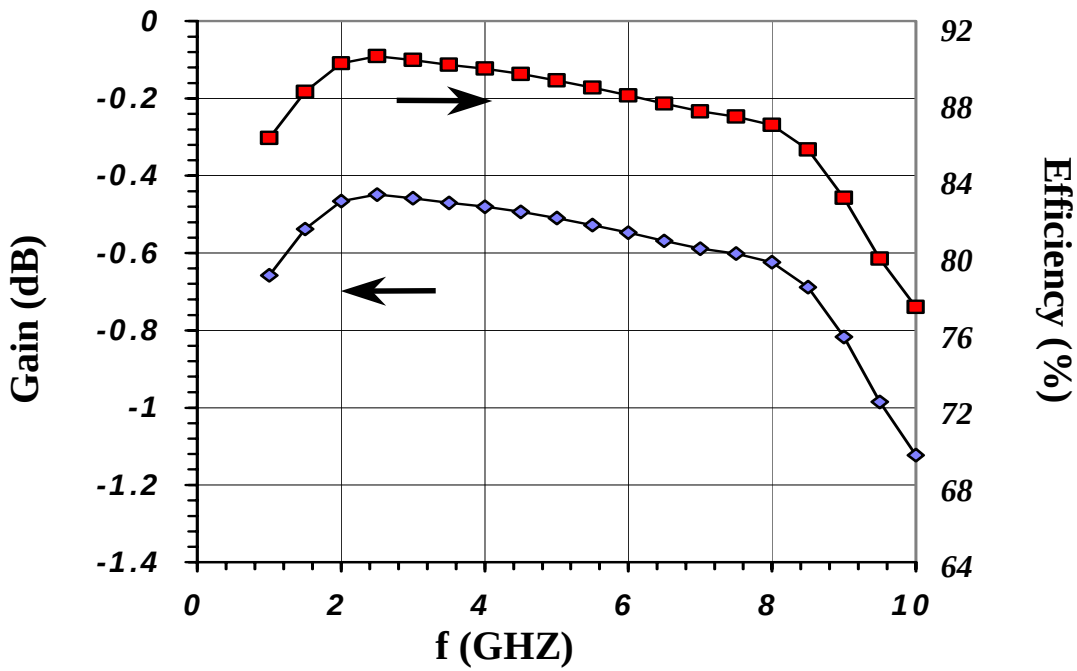
BW & Efficiency of Corporate Power Combiner

Efficiency: ***> 80% (1 dB loss)***

Bandwidth: ***~ 10:1 (1 – 10 GHz)***

Disadvantage:

Not Area-efficient (But AlN carrier cheap)



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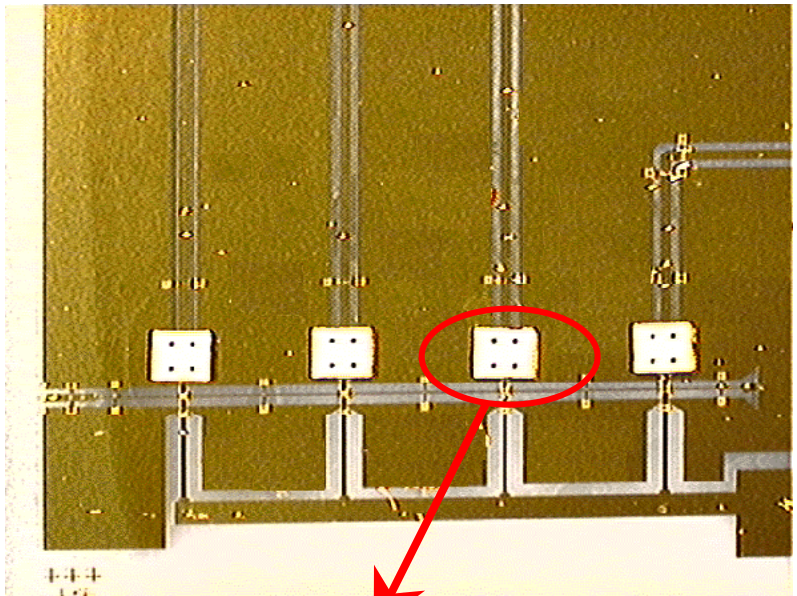
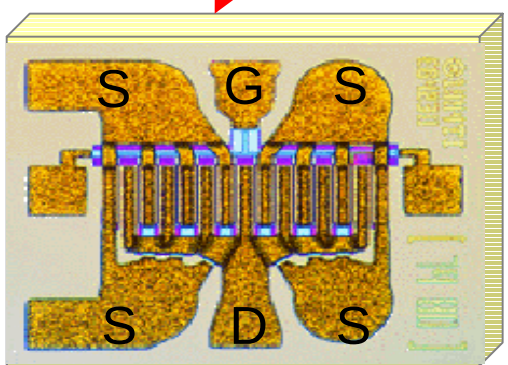
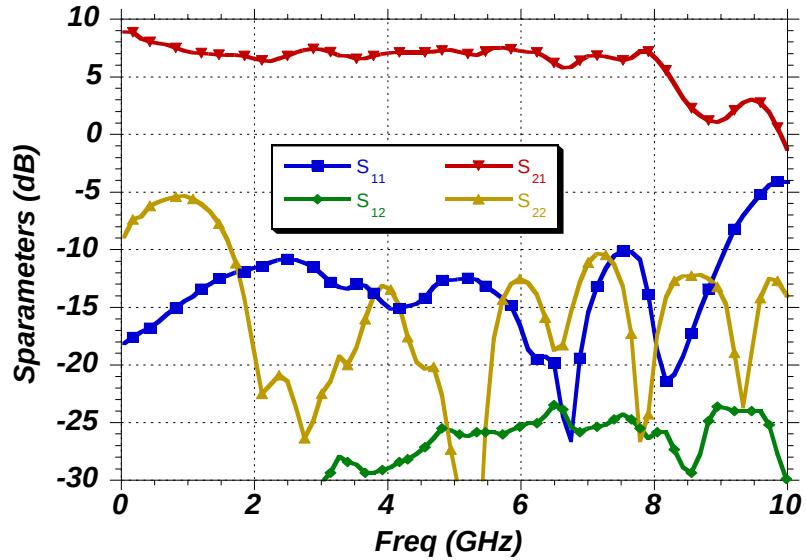
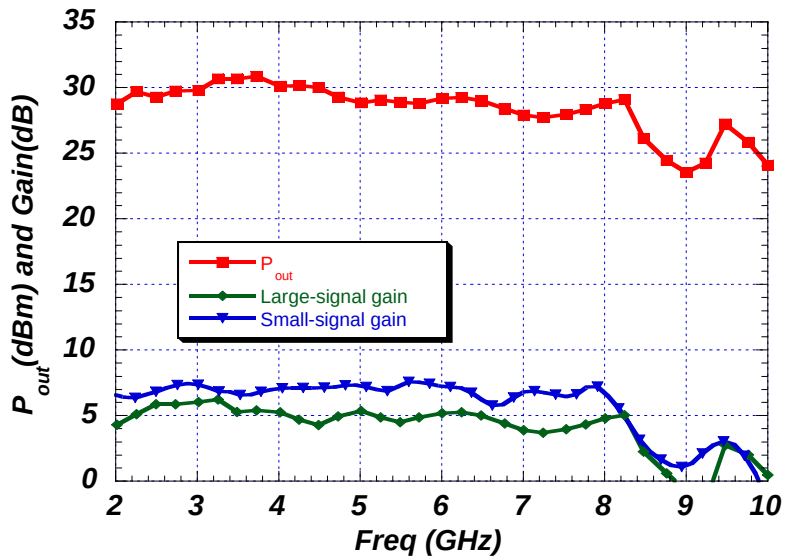
1-8 GHz 1-watt GaAs Modified TWA





1.2mm-wide 0.5μm-long GaAs PHEMT,
P_{out} = 27 dBm, PAE = 50% @ 8GHz





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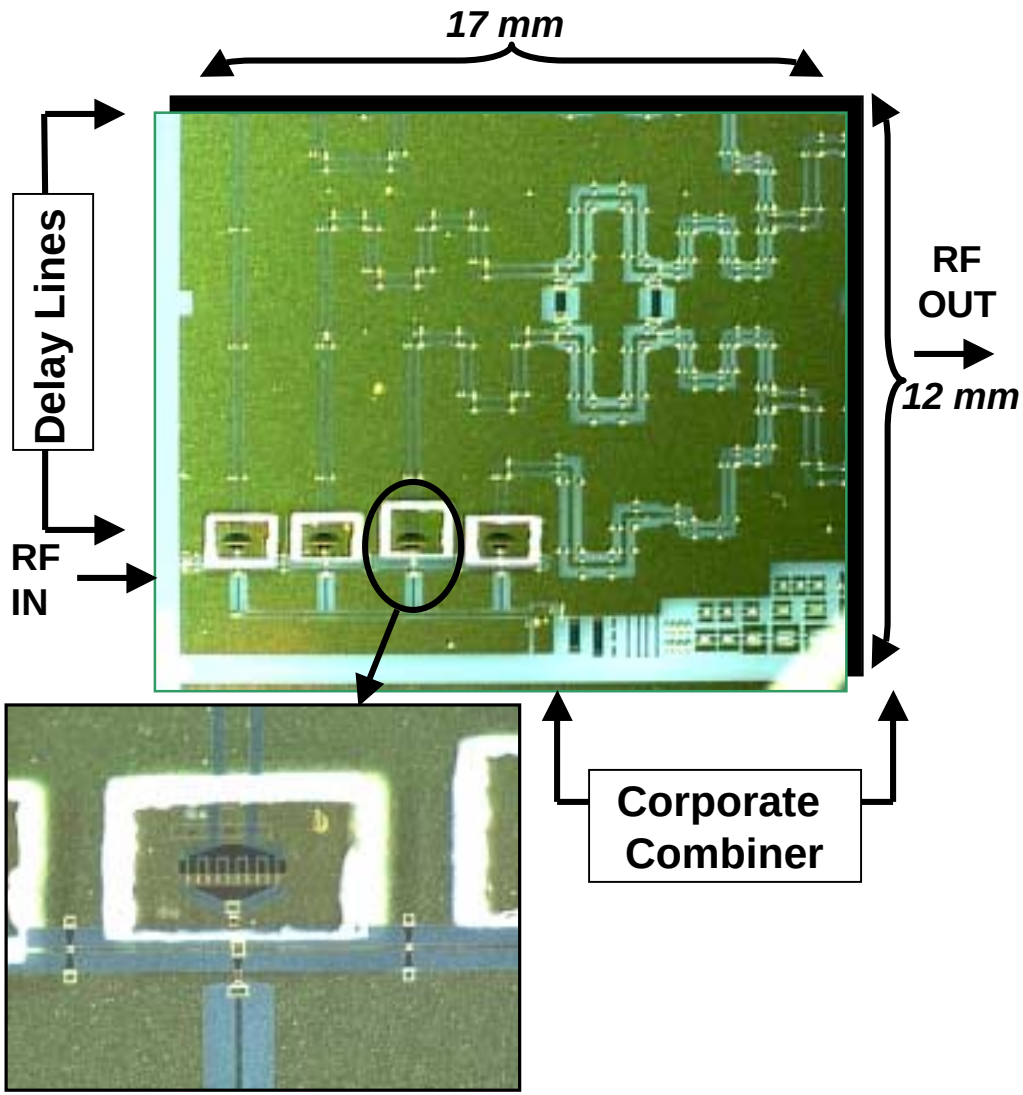
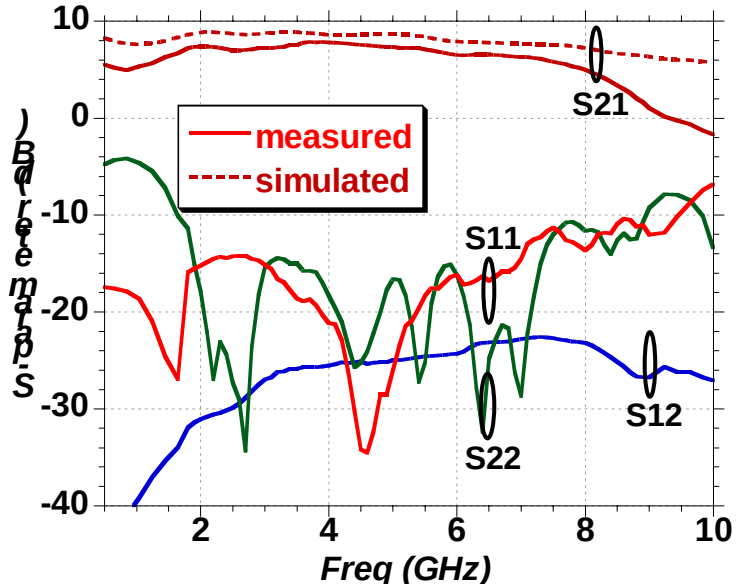
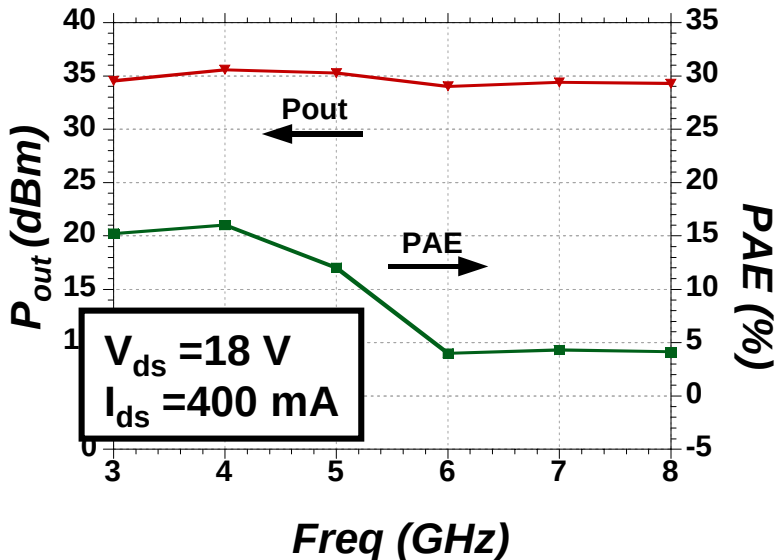
Capacitor-division Modified TWA with Corporate Power Combiner

Fig. 1

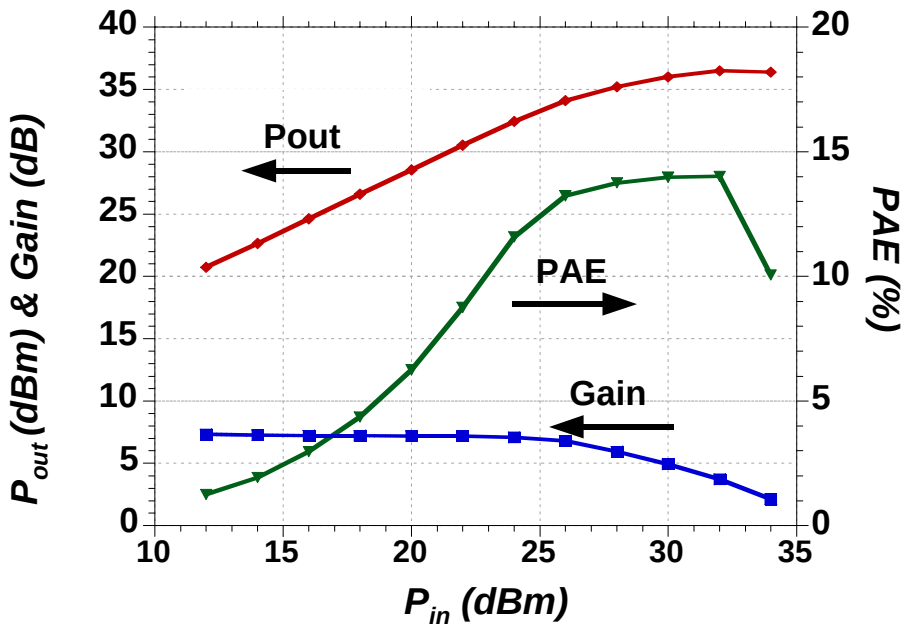






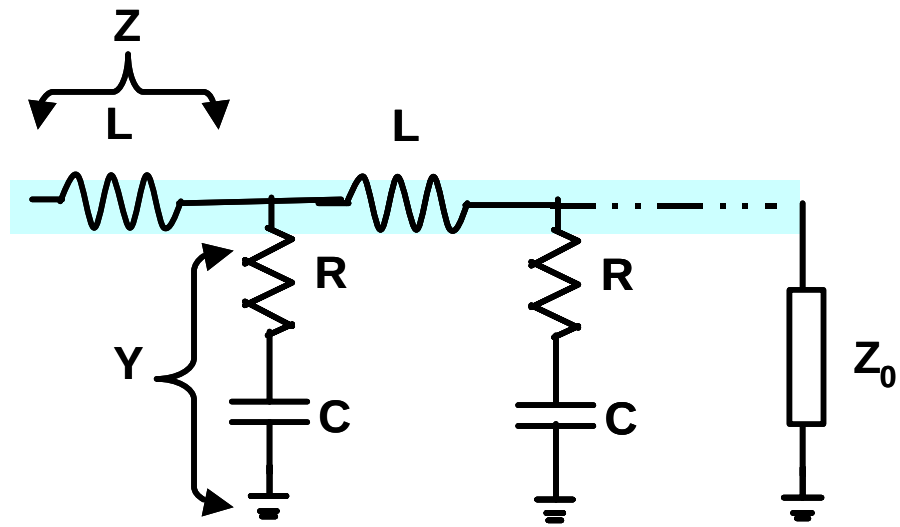
Power Sweep at 4 GHz

P_{out} = 4.5 W, PAE = 14 %
@ V_{ds} = 22 V I_{ds} = 400mA ,f = 4GHz



Unequal Drive Problem

$$\alpha_g = \frac{1}{2}\omega_c^2 R_{in} C_{gs}^2 Z_0$$



Unequal drive:
Reduce combing efficiency
Reduce device reliability

Gate attenuation is frequency dependent
Compensated at one frequency

Broadband power amplifier design

1) **Limitation of conventional TWA**
2) **Modified TWA**
3) **LCR-matched PA**
4) **2×2 matrix modified TWA**

LCR-matched PA Design

Goal:

- ***Bandwidth:*** ***3:1 (3 –10 GHz)***
- ***Gain*** ***~ 10 dB***
- ***PAE*** ***> 20 %***
- ***P_{out}*** ***8 Watt (2W/mm)***

Approach & Improvement:

• Input LCR lossy match	***Gain flatness***
• Low Q LC match	***Broadband***
• Corporate power combiner	***Broadband & power***
• C_{ds} compensation	***Higher power***

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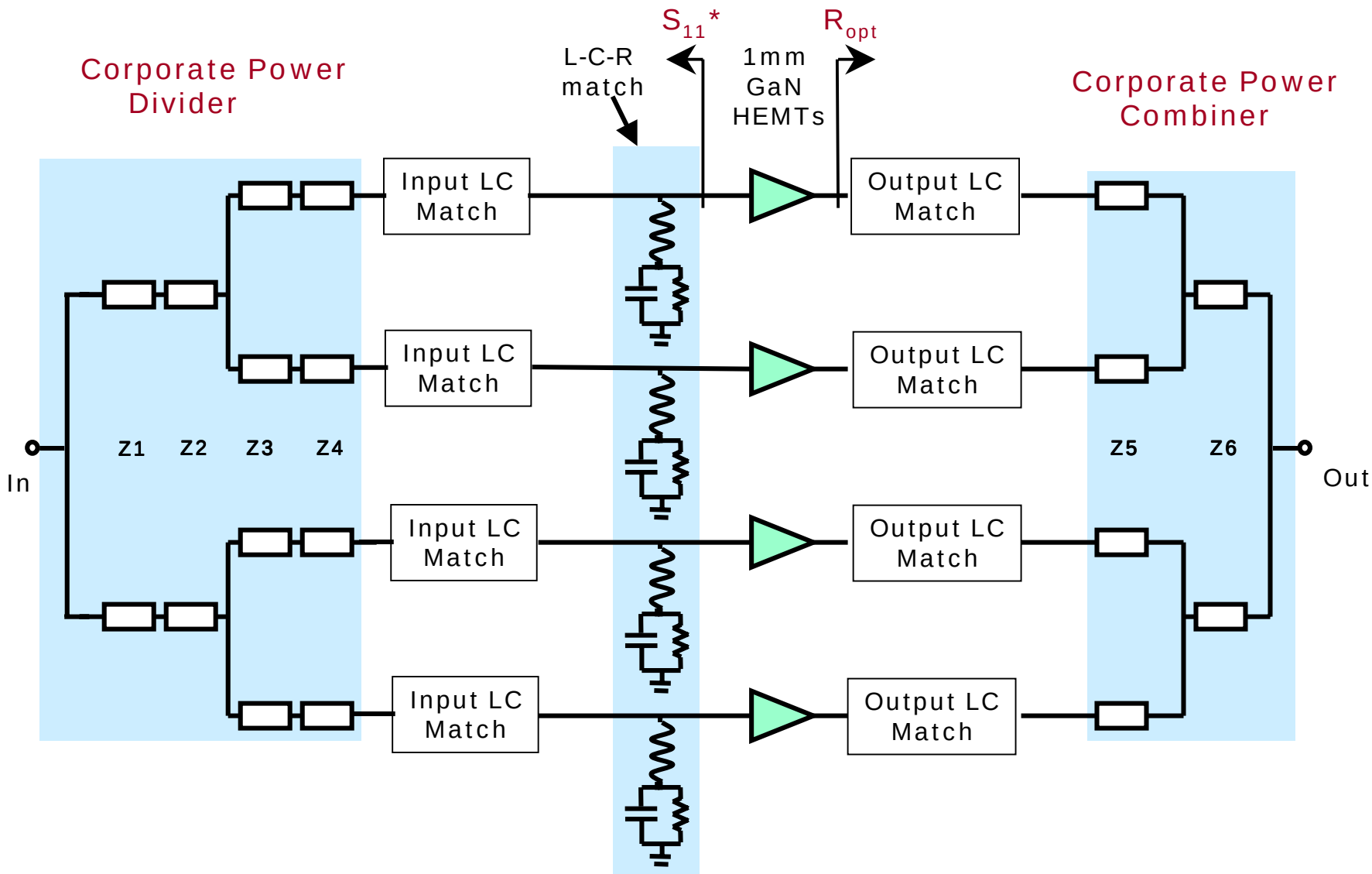
Schematic of LCR-matched Broadband GaN Power Amplifier



Broadband Matching I

Bandwidth > 3:1

(f_{High}/f_{Low})

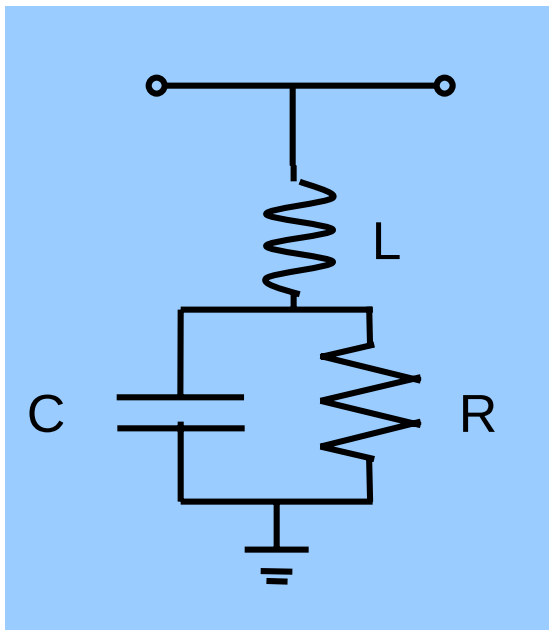
High Impedance Transformation Ratio (4mm device size):

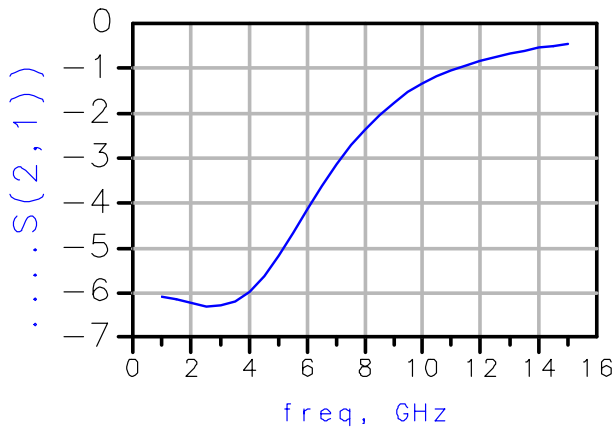
Input: 50 : 1 (50 Ω / 1 Ω) → ***Distributed match*** / ***LCR lossy match***

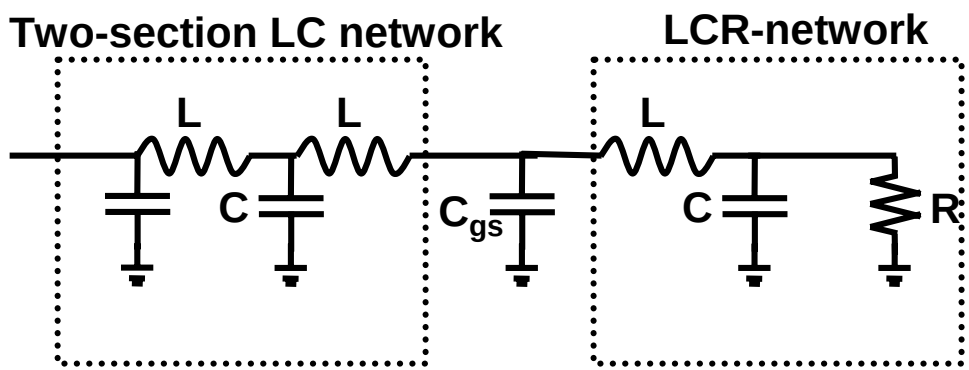
Output: 7:1 (50 Ω / 8 Ω) → ***Corporate power divider*** / ***Multi-section LC match***

LCR
Gain Compensation Network

The network eliminates gain peaks at low band
R also can be stabilizing resistor







Equivalent of transmission line

Broadband Matching II

Bandwidth > 3:1

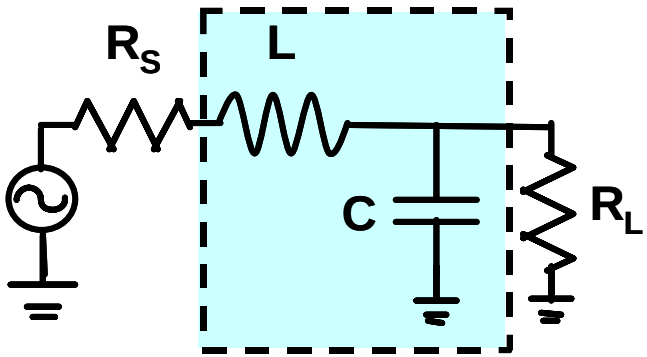
(f_{High}/f_{Low})

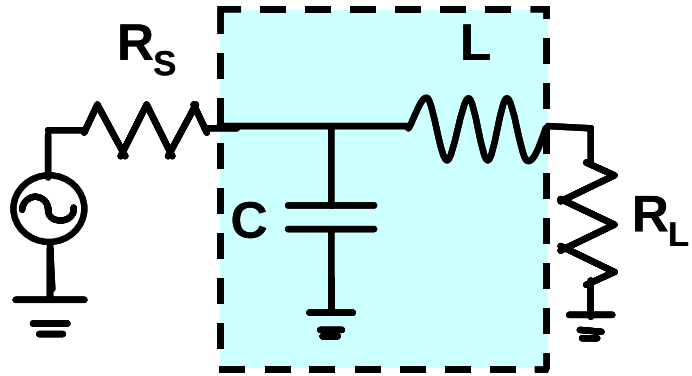
High Impedance Transformation Ratio (4mm device size):

Input: 50 : 1 (50 Ω / 1 Ω) → ***Distributed match*** / ***LCR lossy match***

Output: 7:1 (50 Ω / 8 Ω) → ***Corporate power divider*** / ***Multi-section LC match***

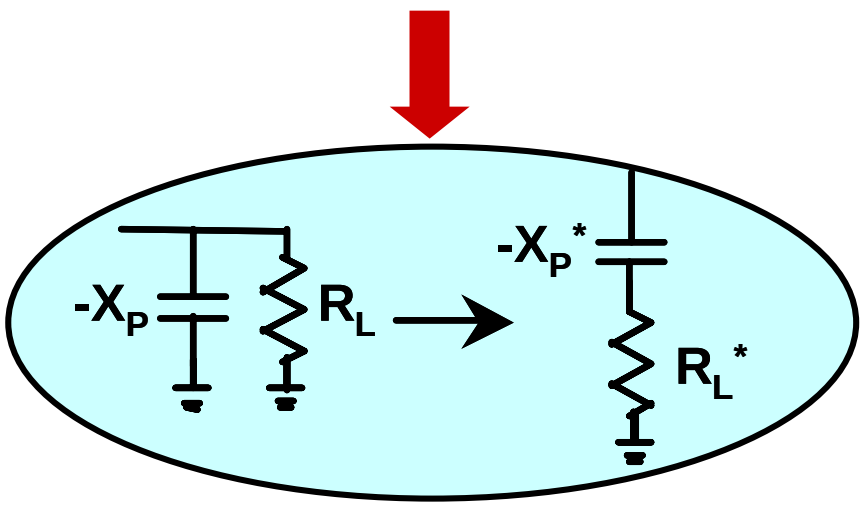
Single-section Lowpass LC Networks

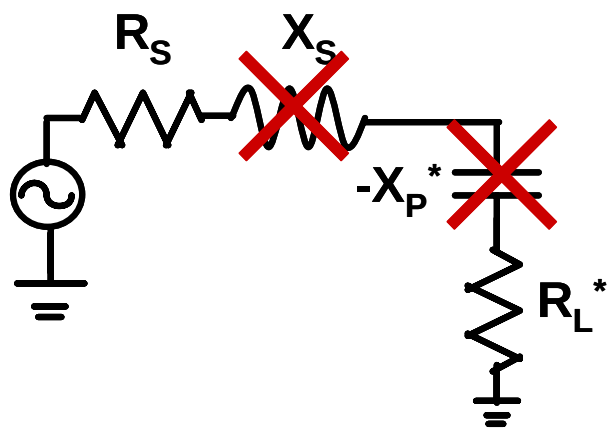




$R_L > R_S$

$R_S > R_L$





Define Q of LC Networks

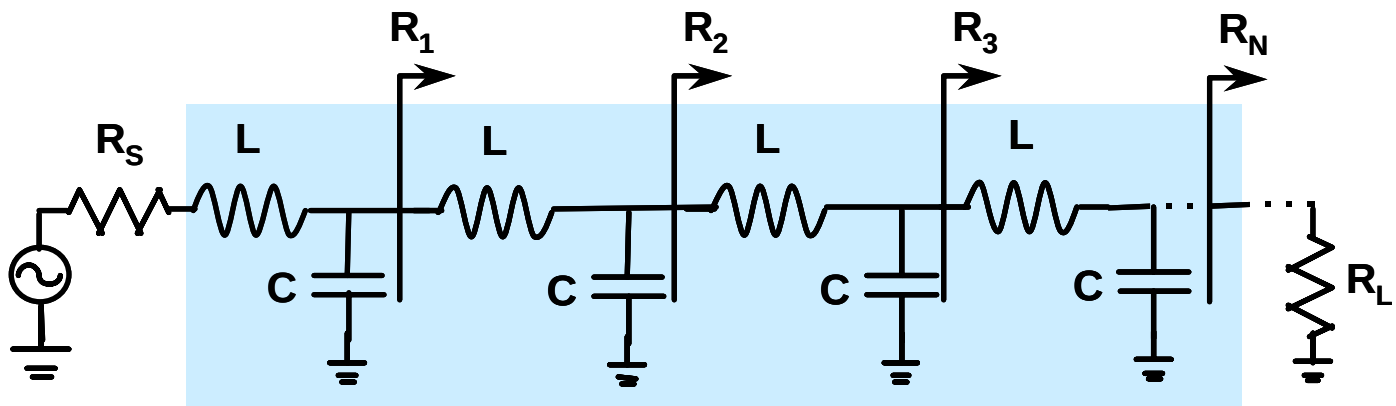
$$X_P^* = \frac{X_P R_L^2}{X_P^2 + R_L^2} \qquad X_S = X_P^*$$

$$R_L^* = \frac{X_P^2 R_L}{X_P^2 + R_L^2} \qquad R_S = R_L^*$$

For $R_L > R_S$ $\quad Q = \sqrt{\frac{R_L}{R_S} - 1}$ $\quad X_S = \omega L = R_S \times Q,\ X_P = 1/\omega C = R_L/Q$

For $R_S > R_L$ $\quad Q = \sqrt{\frac{R_S}{R_L} - 1}$ $\quad X_P = 1/\omega C = R_S/Q,\ X_S = \omega L = R_L \times Q.$

Multi-section(Low-Q) LC Matching Networks



$$R_s < R_1 < R_2 < \ldots < R_L$$
$$R_1/R_s = R_2/R_1 = \ldots = R_L/R_N$$

$$Q = \sqrt{\frac{R_L}{R_S} - 1} \quad \Rightarrow \quad Q = \sqrt{\left(\frac{R_L}{R_S}\right)^{\frac{1}{N}} - 1}$$

For Complex impedance,Reactance can be absorbed into LC networks

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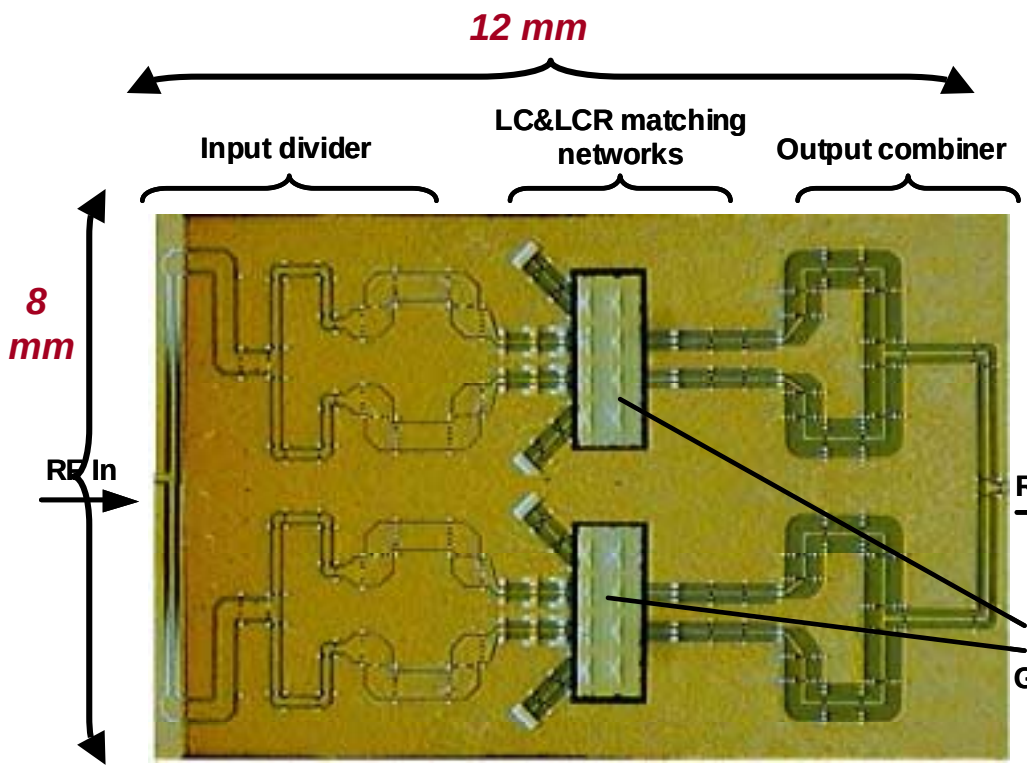
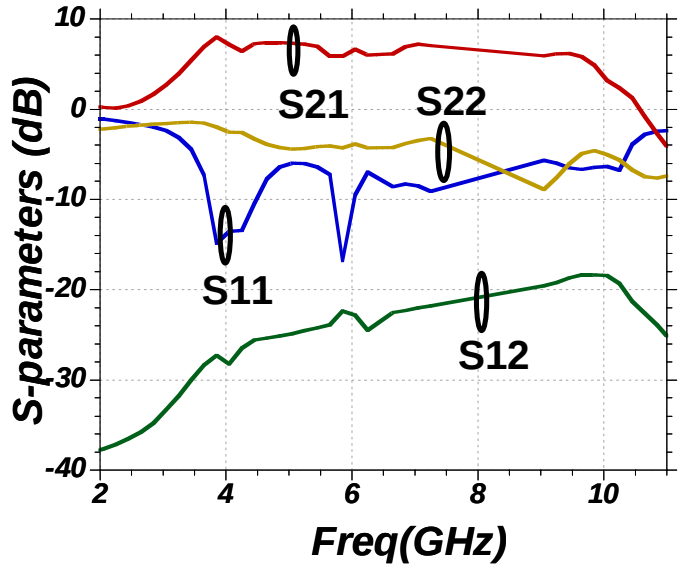
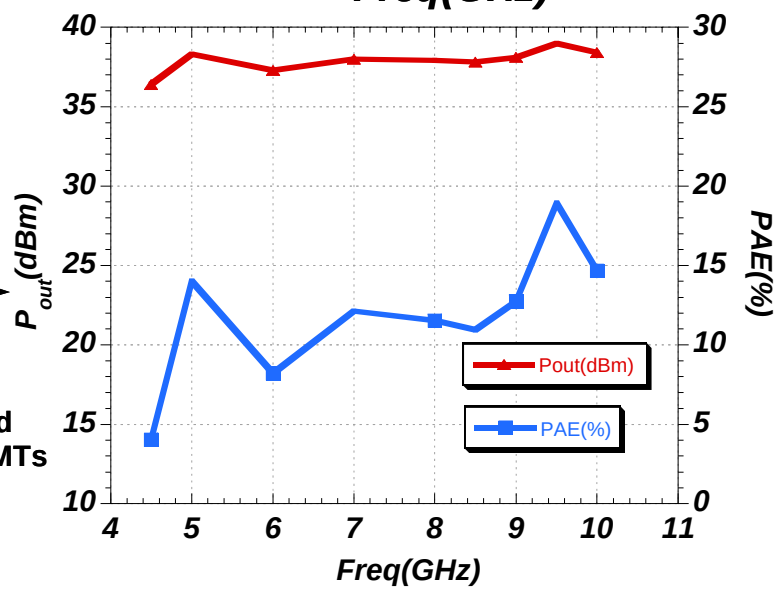
LCR Matched 4mm GaN-based Power Amplifier

Gain : ~ 7dB, BW: 3 - 10 GHz

P_{out} = 8. 5 W , PAE = 20% @ 8 GHz

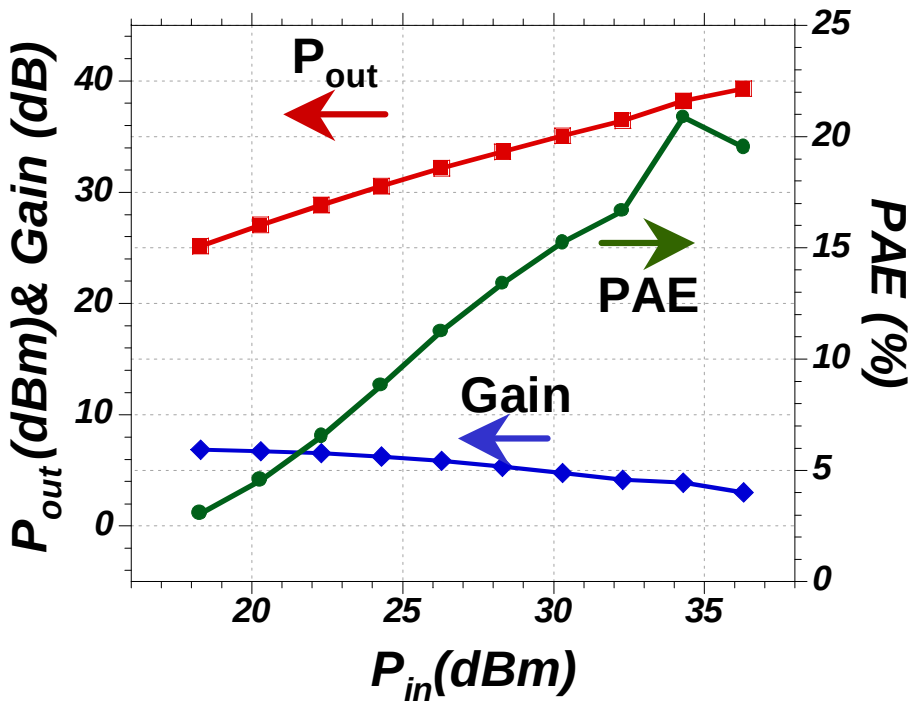






Power Sweep at 8 GHz

P_{out} = 8.5 W , PAE ≈ 20% @ 8 GHz
(V_d = 16 V, Id = 500 mA, class AB)



Broadband power amplifier design

1) **Limitation of conventional TWA**
2) **Modified TWA**
3) **LCR-matched PA**
4) **2×2 matrix modified TWA**

2 × 2 matrix Modified TWA Design

Goal:

- ***Bandwidth:*** ***6:1 (1-6 GHz)***
- ***Gain*** ***> 10 dB***
- ***PAE*** ***> 15 %***
- ***P_{out}*** ***8 Watt (2W/mm)***

Approach & Improvement:

- ***2 ×2 Modified TWA*** → ***Bandwidth & equal drive***
- ***Lower frequency: 1 – 6 GHz*** → ***Higher gain***
- ***Real air-bridges*** → ***Better bonding***
- ***Thicker CPW lines (> 3 μm)*** → ***Reduce conductive loss***

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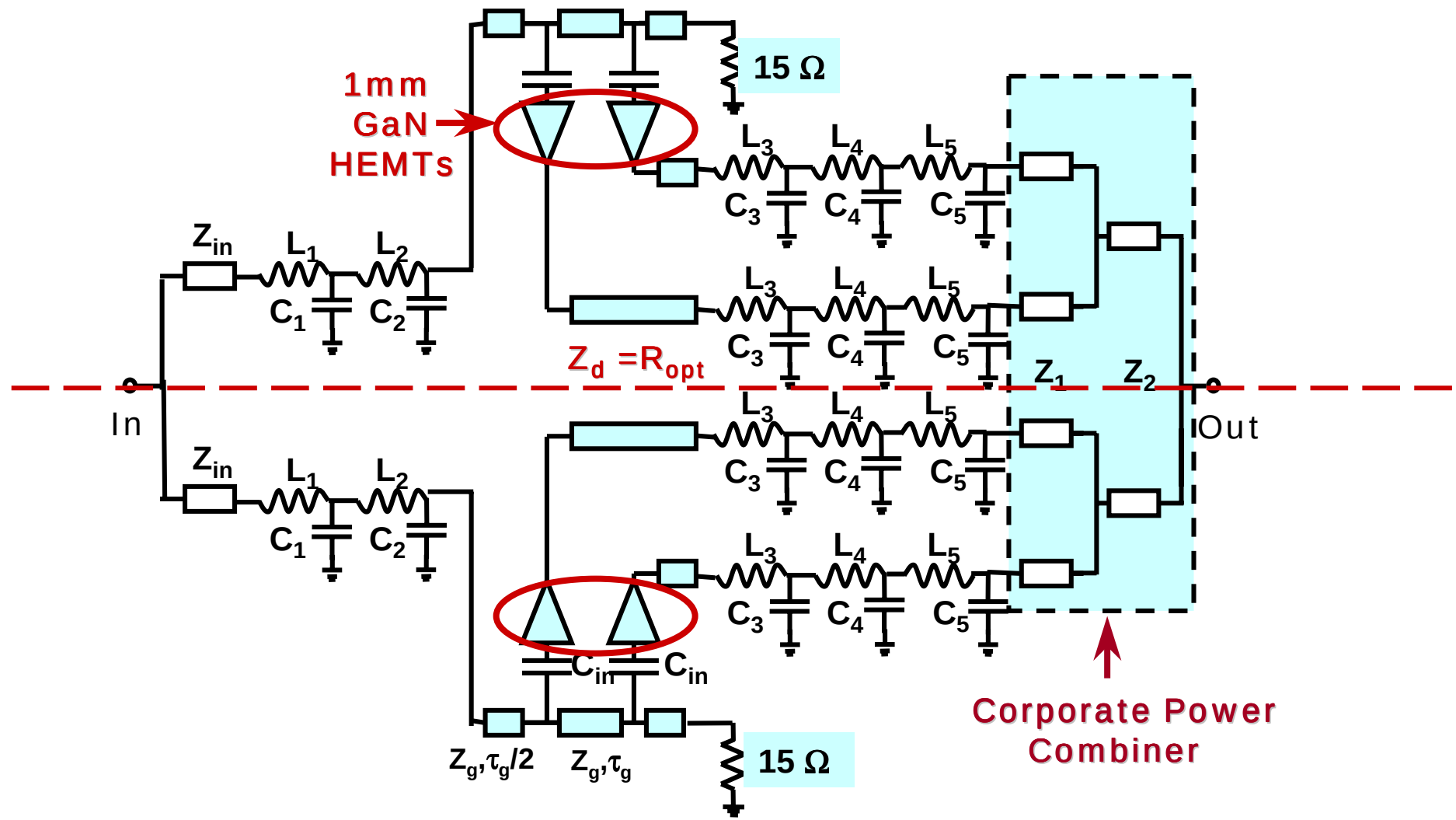
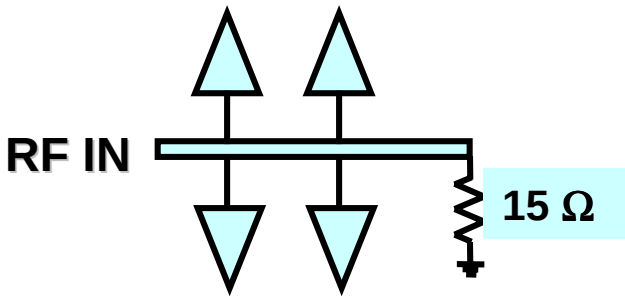
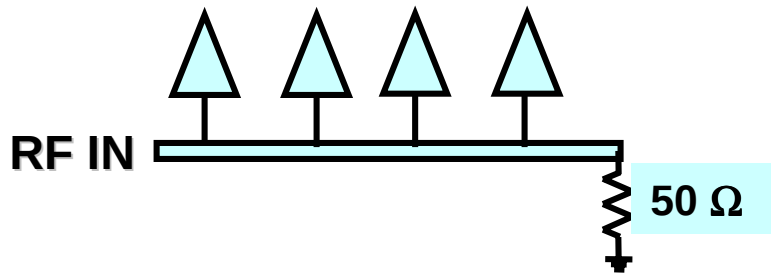
Schematic of 2 × 2 Modified TWPA



Better Equal Drive



2×2 gate feeding



1×4 gate feeding

$$\alpha_g = \frac{1}{2}\omega_c^2 R_{in} C_{gs}^2 Z_0$$

2×2 matrix TWA has better equal drive than 1×4 TWA

Curtice-3 Large-signal Model

$$I_d = (A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3)\tanh \gamma V_{ds}$$

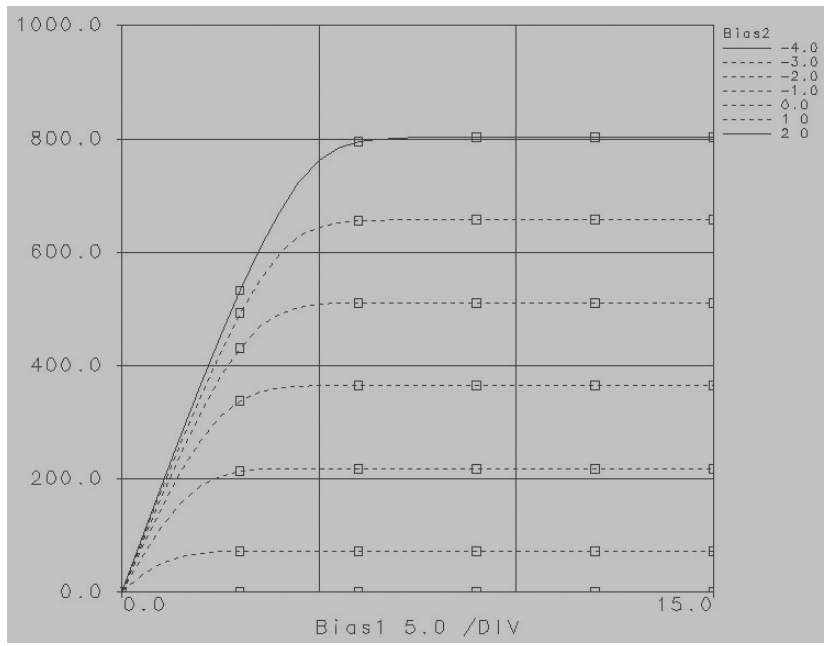
$$V_1 = V_{gs} \times \left[1 + \beta (V_{OUTO} - |V_{ds}|)\right]$$

Assumption:

- ***$V_1 = V_{gs}$***
- ***$A_2 = A_3 = 0$***
- ***Gm: constant***
- ***R_{ds}: infinity***

Conclusion:

- ***First order simulation***
- ***Compatible with small-signal model***



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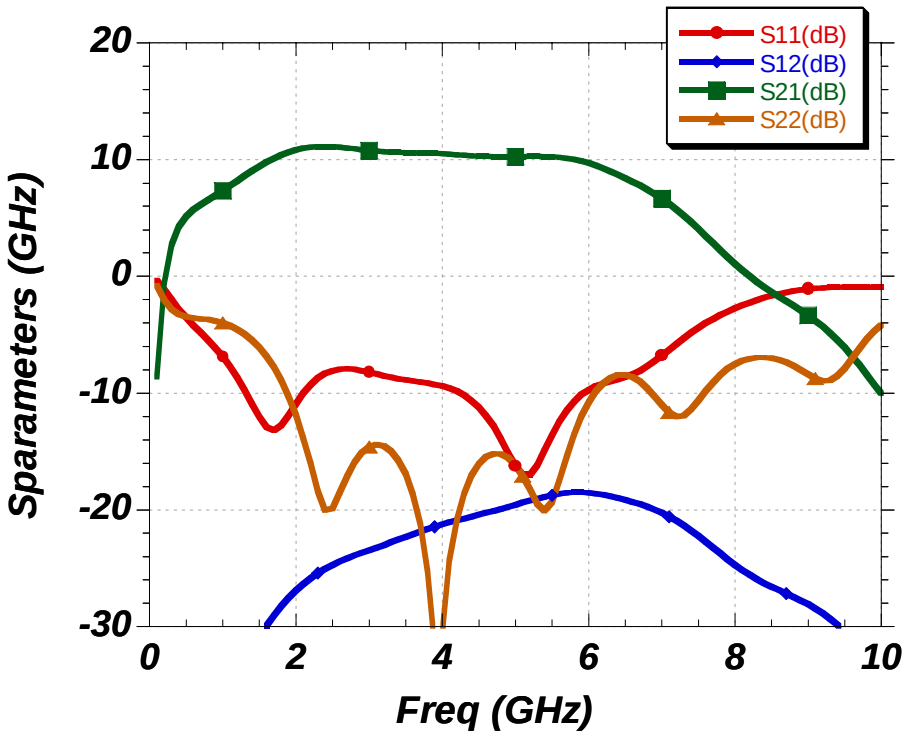
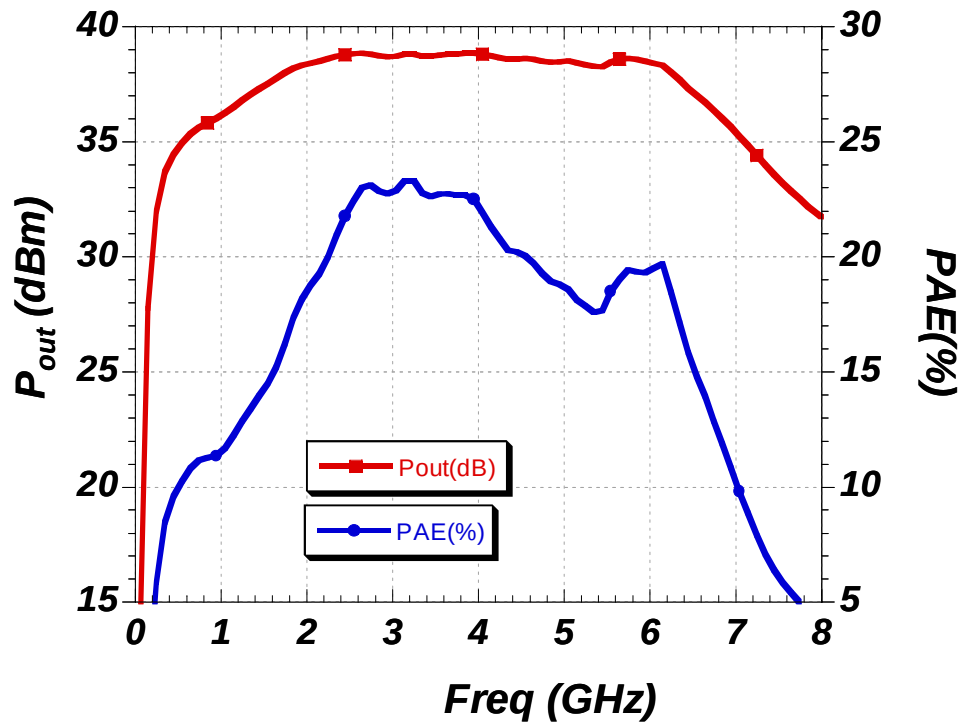
Simulation Results

Gain: ~ 11 dB BW: 1 - 7 GHz
P_{out}: 6 – 8 W PAE: ~ 20 %





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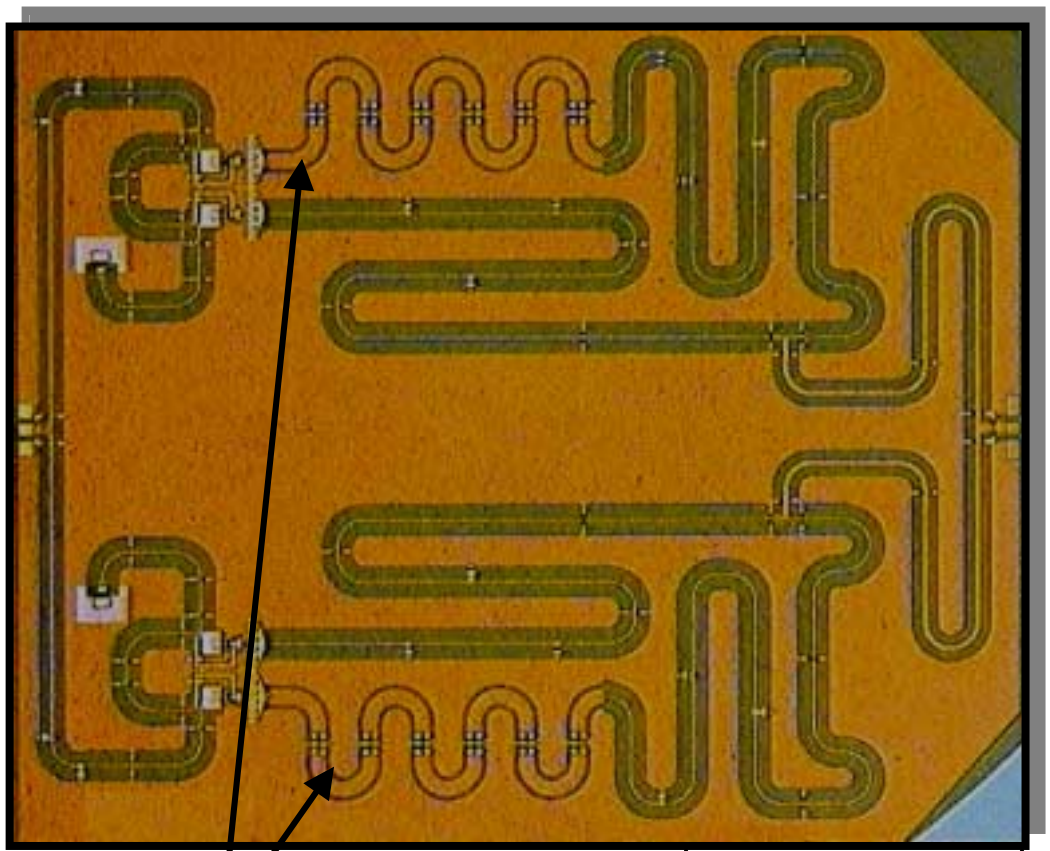
Photos of the Circuit



Circuit components:

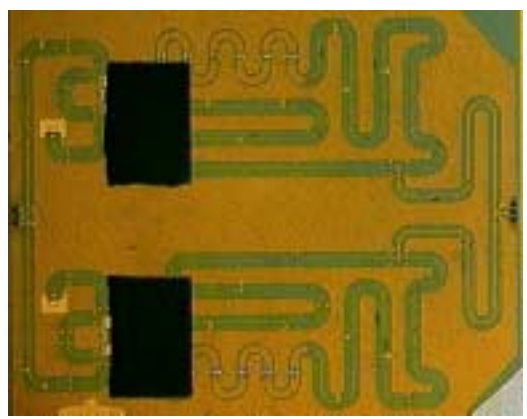
GaN HEMTs (4 X 1mm)

MIM Capacitors,

NiCr Resistors

Air-Bridges

Circuit with flipped GaN HEMTs



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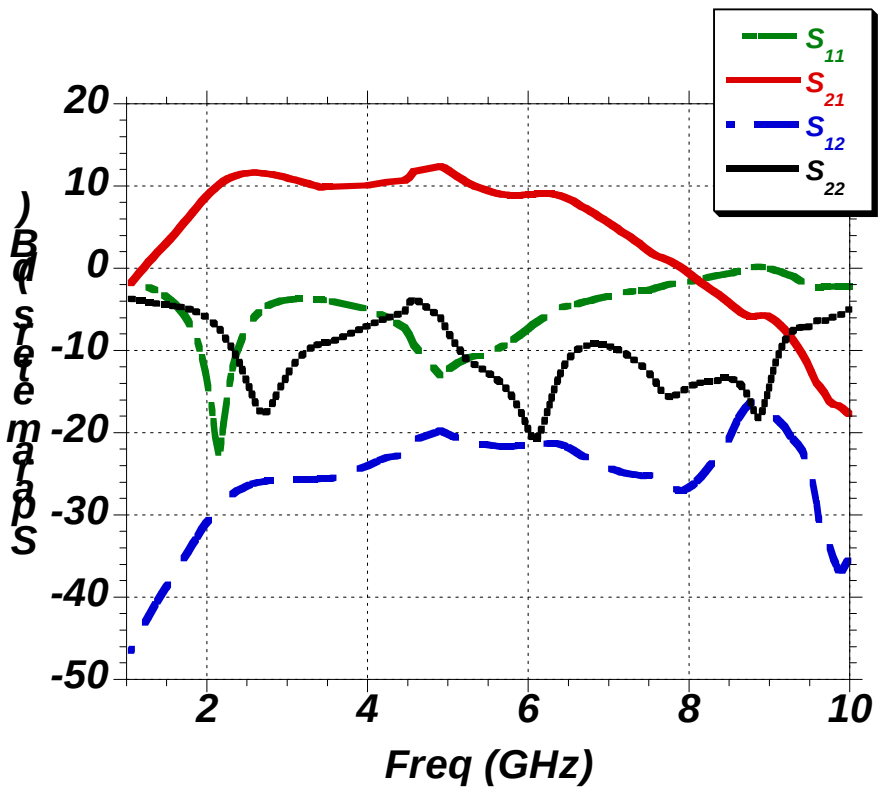
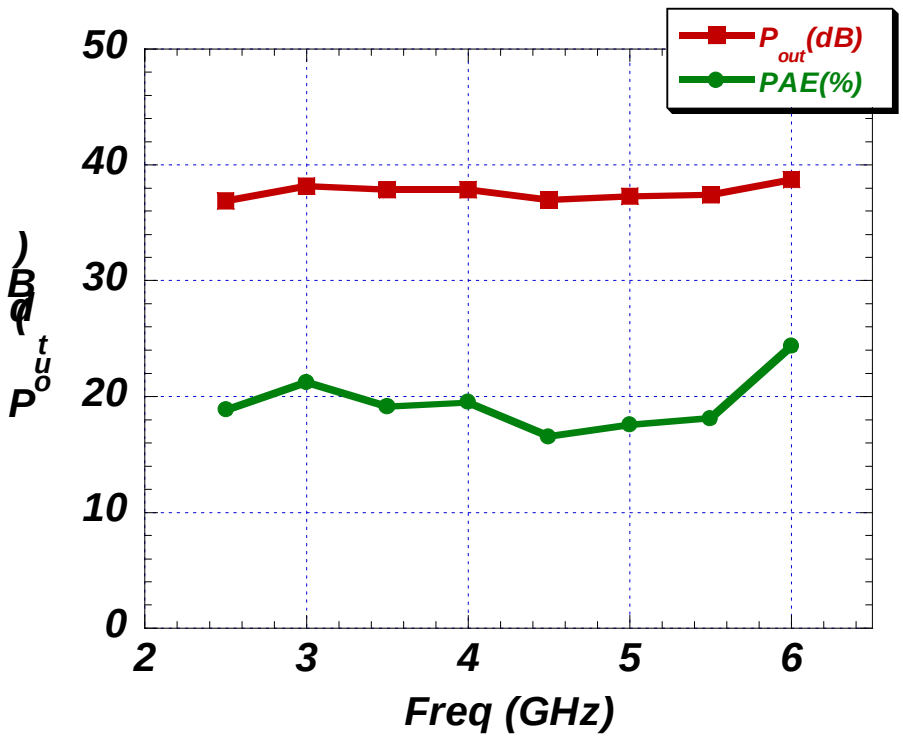
Small-signal and Large-signal Performance

Gain: 9 - 12 dB, BW: 1.8 – 6.8 GHz
Biased @ V_{ds} =10 V, I_{ds} = 400 mA

Pout: 5 - 7.5 Watt, PAE: 18 - 24 %
Biased @ V_{ds} = 18V, I_{ds} = 400 mA





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Circuits Performance Comparison

	P_{out} (W)	3dB BW (GHz)	Gain (dB)	PAE (%)	Features
GaAs modified TWPA	0.6 - 1.3	1 - 8	5 - 8	15 - 25	BW,flat gain good match
GaN modified TWPA	2.5 - 4.5	1 - 8	5 – 8	5 - 15	BW,flat gain good match
GaN LCR-matched PA	4.5 - 8.5	3 - 10	5 – 8	10 - 20	power compact
GaN 2×2 matrix modified TWPA	5 - 7.5	1 - 6	9 - 12	18 - 24	BW,power PAE

Achievements

High Power small GaN HEMTs (un-passivated):

P_{out} = 4.6 W/mm, PAE = 40%

- **High Power large-periphery GaN HEMTS :**

P_{out} = 4.4 W, PAE = 35% @8GHz

- **GaN Modified GaN TWPA:**

First GaN amplifier !

- **GaN LCR - matched PA:**

P_{out} up to 8.5 W (>2W/mm)

- ***GaN* 2 × 2 matrix modified TWPA:**

Best overall performance

Conclusions

Achievements:

Demonstration of power-bandwidth advantage of GaN (0.7μm HEMTs-on-sapphire technology)

Future work:

Optimization of GaN material and device technology
Incorporate GaN amplifiers into spatially combined modules