Oxide Aperture Heterojunction Bipolar Transistors

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Overview

Introduction

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- Growth as related to bipolar transistors
- Growth of $GaAs_{0.49}Sb_{0.51}$, $AlAs_{0.56}Sb_{0.44}$, and $Al_xGa_{1-x}As_ySb_{1-y}$
- n-type doping of arsenide-antimonides

Oxide Aperture Diodes

- Current density: area versus perimeter
- Aperture placement
- Diode Selection Rules

Oxide Aperture HBTs

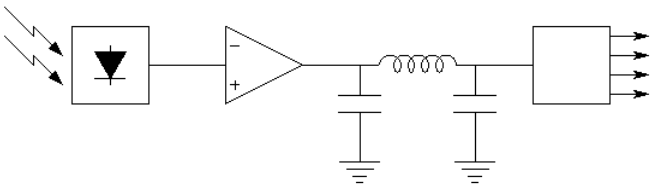
- Generation Ø
- Generation I
- Generation II
- RF results

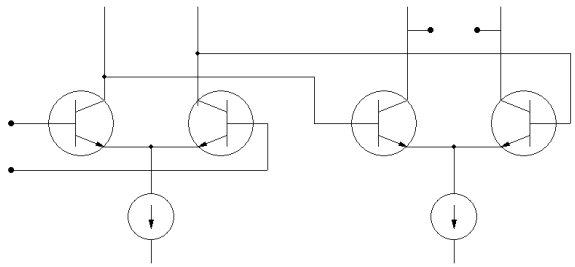
Conclusions and Future Work

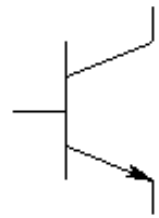
Introduction

The ever-growing demand in communication and radar technology for increased bit-rates and frequency resolution requires systems capable of providing **increased bandwidth** and clock rates

Given that these **systems** are built from **circuits**, which in turn are built from basic **devices** and passive elements…



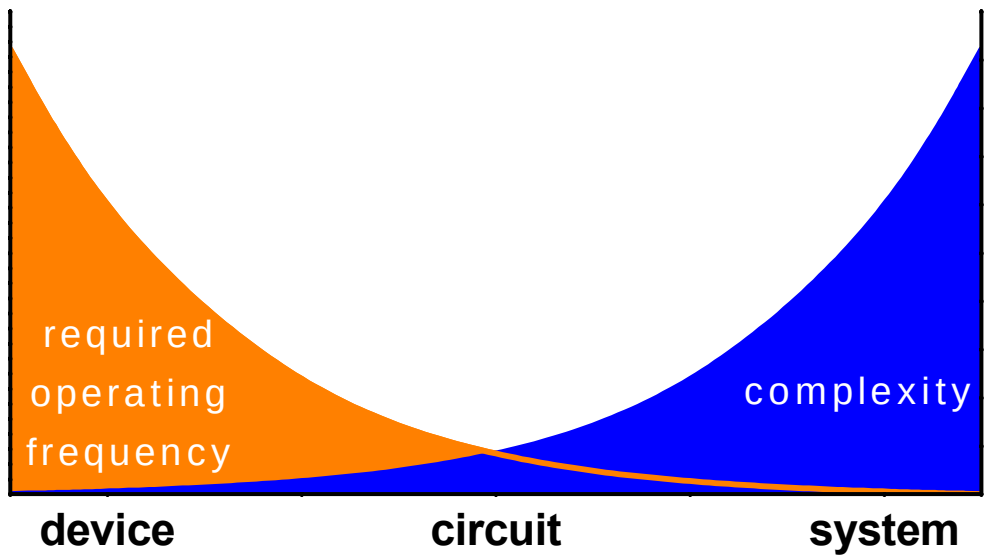




Requires **increased bandwidth** from the **devices**, which are the building block of the system

As complexity increases, the max operating frequency decreases

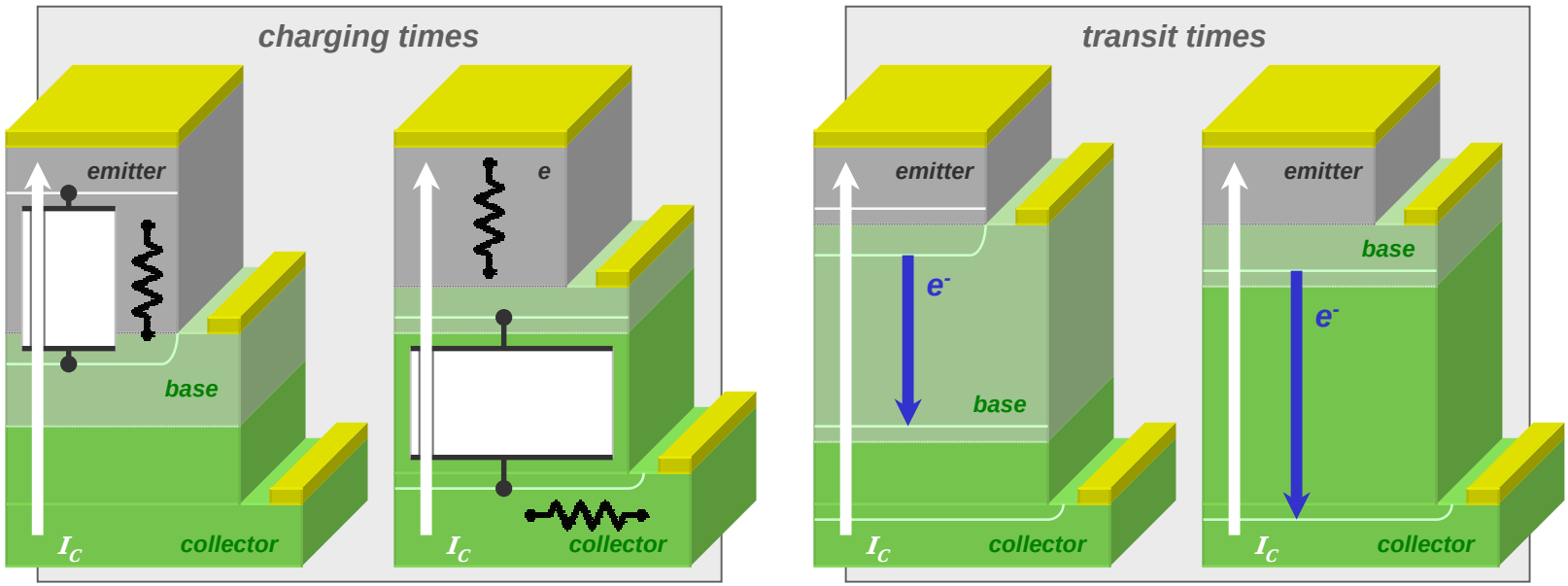
A given system frequency, a **higher device operating frequency** is required



f_τ The current-gain cutoff frequency

Defined as the frequency at which the short-circuit current (h_{21}) gain goes to unity

$$f_\tau = \frac{1}{2\pi}\left[\frac{\eta kT}{qI_C}\left(C_{BE}+C_{BC}\right)+\tau_B+\tau_C+\left(R_E+R_C\right)C_{BC}\right]$$



f_{max} The maximum frequency of oscillation

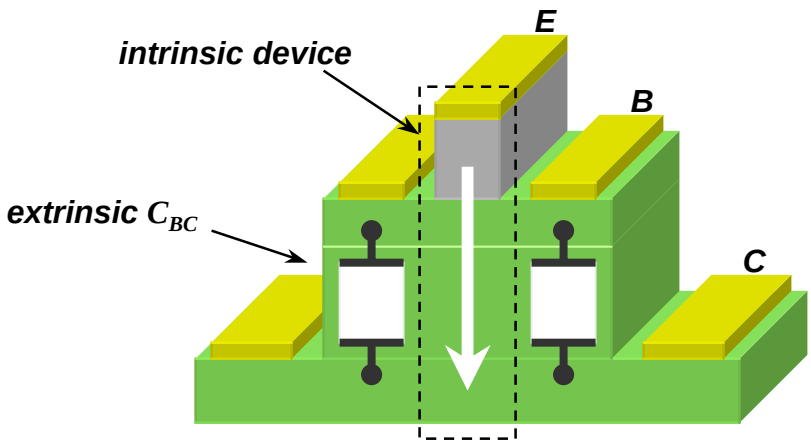
Defined as the frequency at which the unilateral power gain (U) goes to unity

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi R_B C_{BC}}}$$

The Oxide Aperture HBT

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi R_B C_{BC}}}$$

In order to increase f_{max}, R_B and/or C_{BC} must be reduced

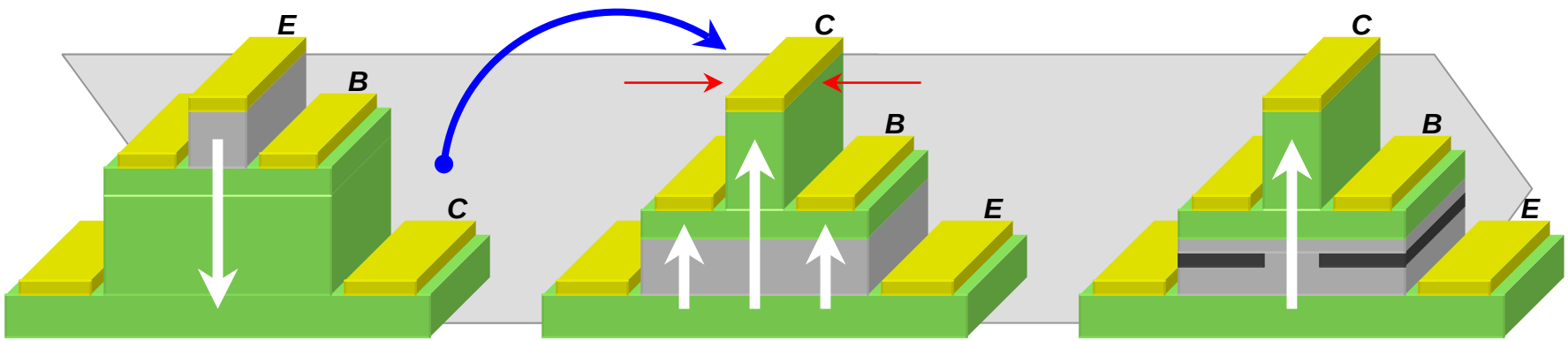


Techniques such as **increased base doping** and **lateral scaling** can reduce R_B; but an **extrinsic portion** of C_{BC} still remains, limiting the device's frequency performance

Various techniques have addressed the reduction of C_{BC}

selective regrowth techniques, sidewall contacted bases, undercut collectors, implanted emitters, and the transferred substrate technology

Oxide Aperture HBT



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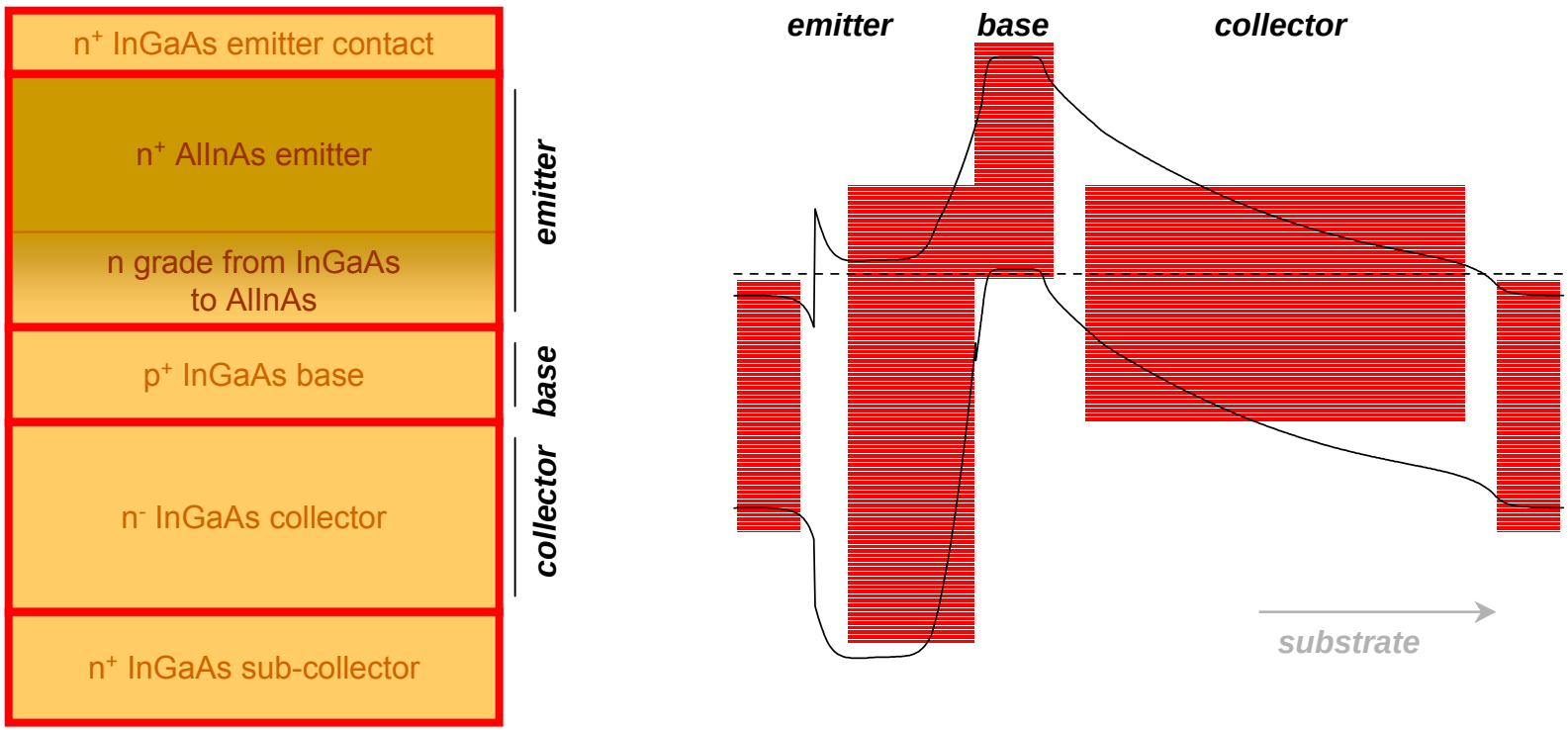
Transistor Design: Materials

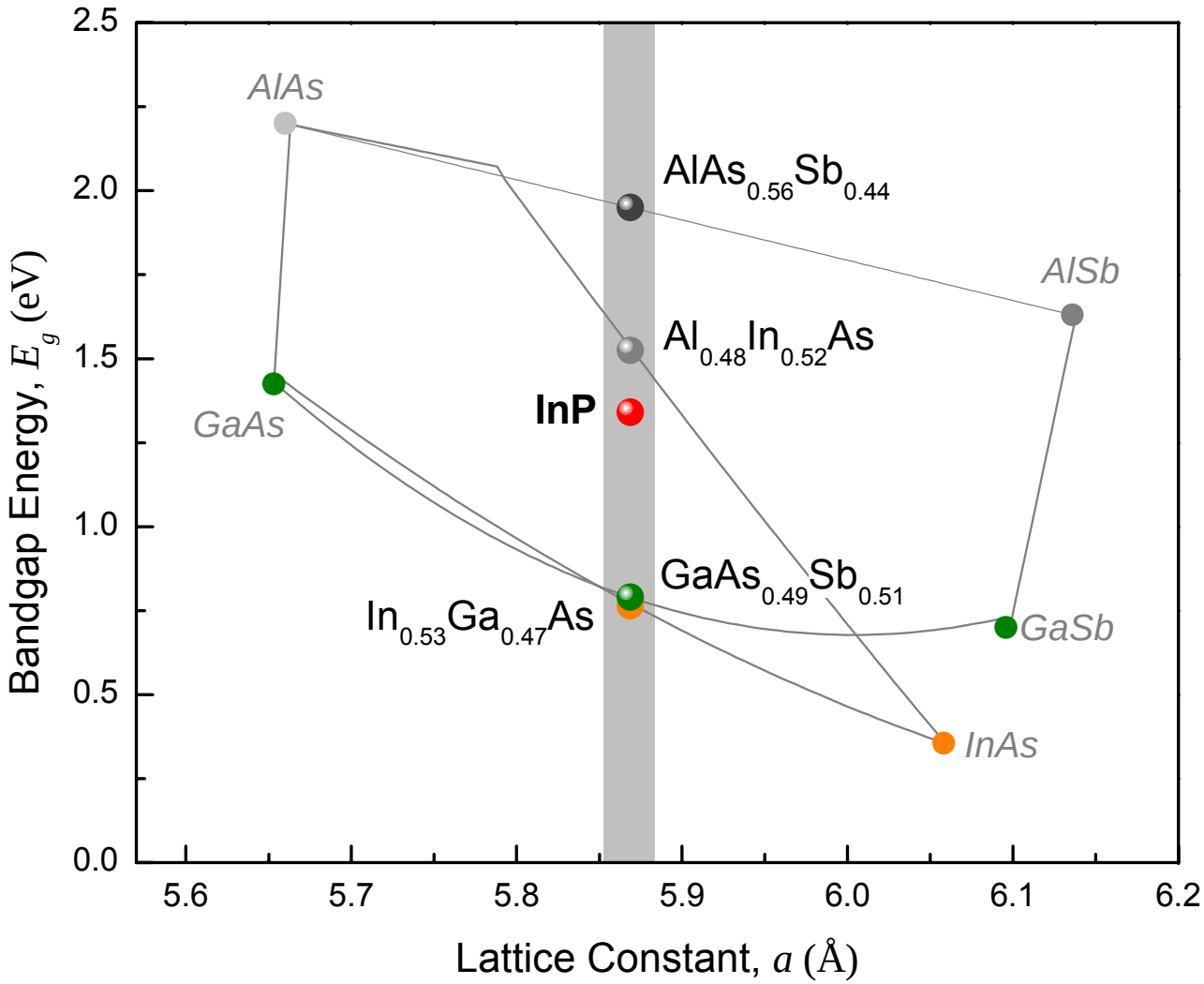
The majority of high-speed HBTs produced today have been InP emitter-up transistors



AlInAs does not readily oxidize and cannot be easily used to form an oxide aperture

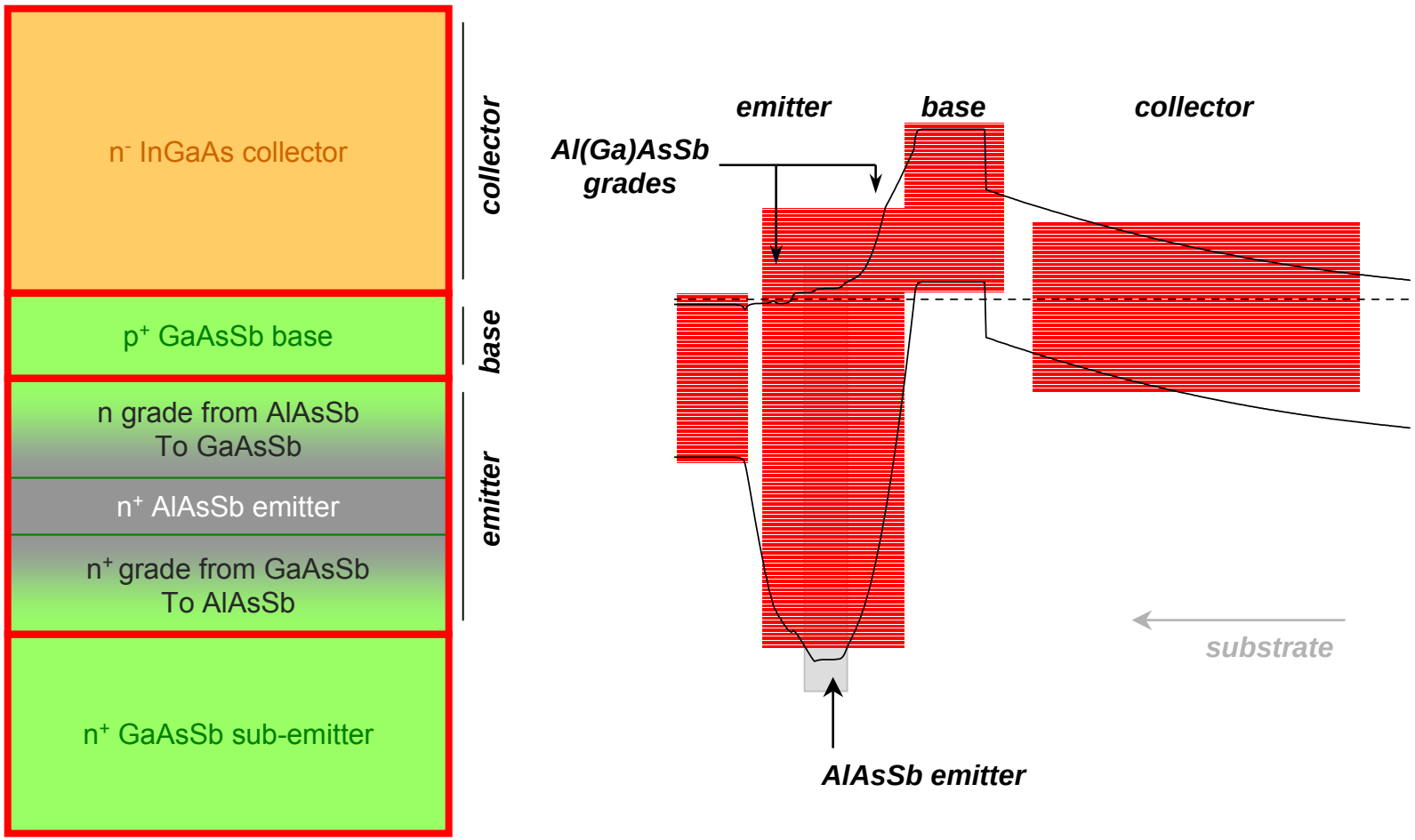
$R_{ox,AlInAs}$ = 2.4 µm/hr @ 520 °C

Transistor Design: Materials



Transistor Design: Materials

Oxide Aperture HBT

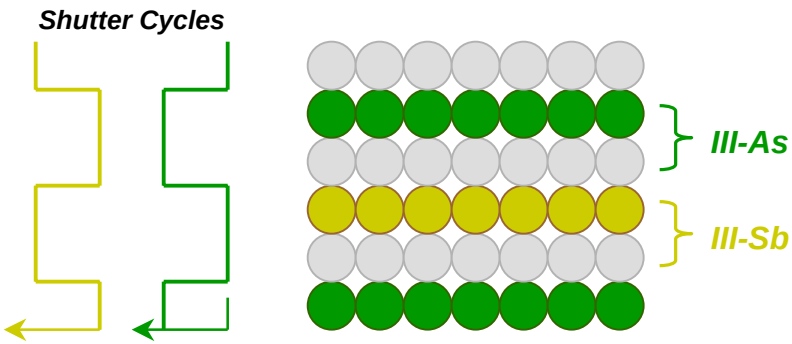


$R_{ox,AlAsSb}$ = 5 µm/hr @ 350 °C

Growth of GaAsSb/AlAsSb

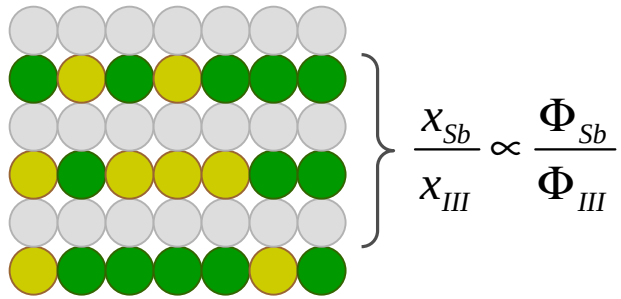
Two methods to grow GaAsSb/AlAsSb

Digital Alloy of III-As/III-Sb



Pros: Highly reproducible
Cons: Heavy wear & tear

Analog Alloy



Pros: Greatly reduced wear & tear
Cons: Requires growth calibrations, maintenance

Growth of $Al_xGa_{1-x}As_ySb_{1-y}$

~~A fully digital growth (III-As/III-Sb) is undesirable due to the wear & tear~~

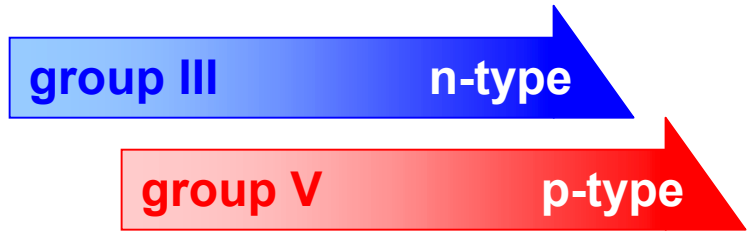
~~A fully analog growth is practically impossible, requiring cals for **each** composition~~

Therefore, a digital alloy of the analog alloys GaAsSb/AlAsSb is used to form the grades between GaAsSb and AlAsSb

n-type Doping of Antimonides

Silicon is the most widely used n-type dopant in III-V semiconductors

As a result of being a **group IV** element, it is also **amphoteric** by nature

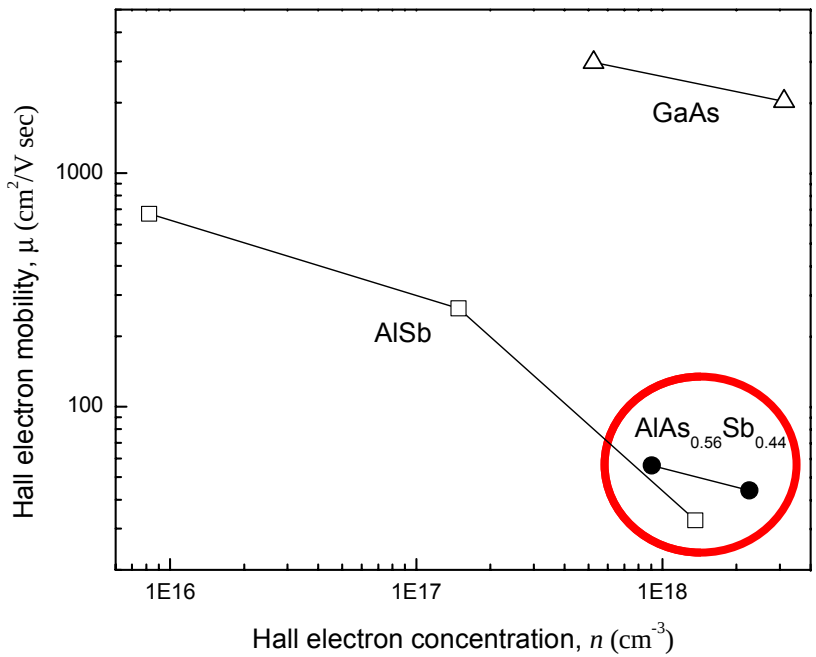


For **most III-V semiconductors**, Si resides on the group III site as a **donor**

Conversely, in **Sb-based semiconductors** Si incorporates as an **acceptor**

Therefore, a **group VI** element, **tellurium**, is used as an **n-type dopant** for Sb-based compounds

One drawback encountered with doping of the Sb-based semiconductors is the **poor mobility of electrons**, especially at higher doping levels



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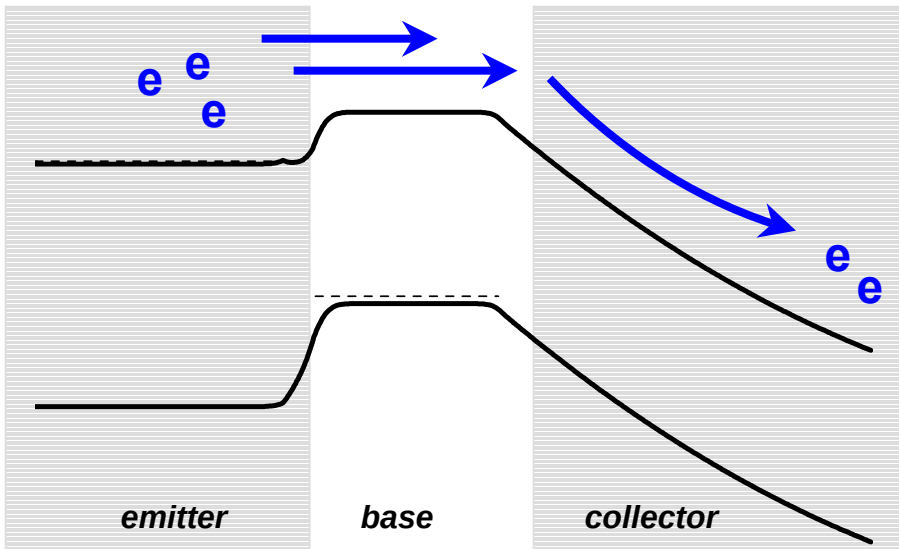
Oxide Aperture Diodes

For every transistor, there are two diodes…

All bipolar transistors are constructed from **2 *pn* diodes**

Under forward-active operation, the **base-emitter** junction acts as a **source** of carriers and the **base-collector** junction acts as a **sink**



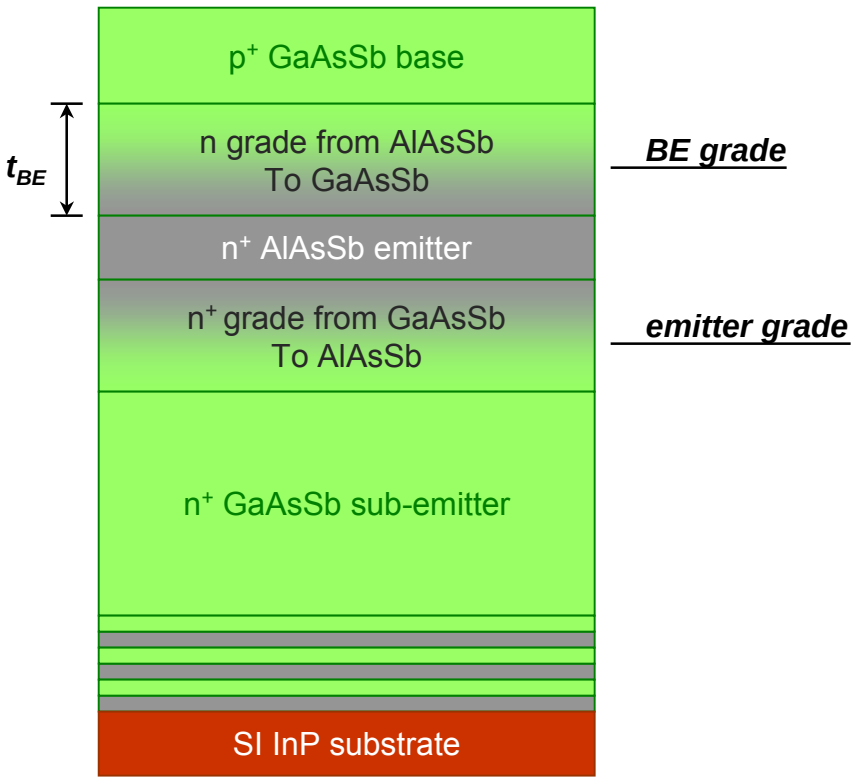
Therefore, much of the transistor's current and current-related characteristics can be related back to the **base-emitter junction**

Oxides formed from the wet oxidation of Al-based semiconductors have been shown to have fairly **high interface recombination velocities**

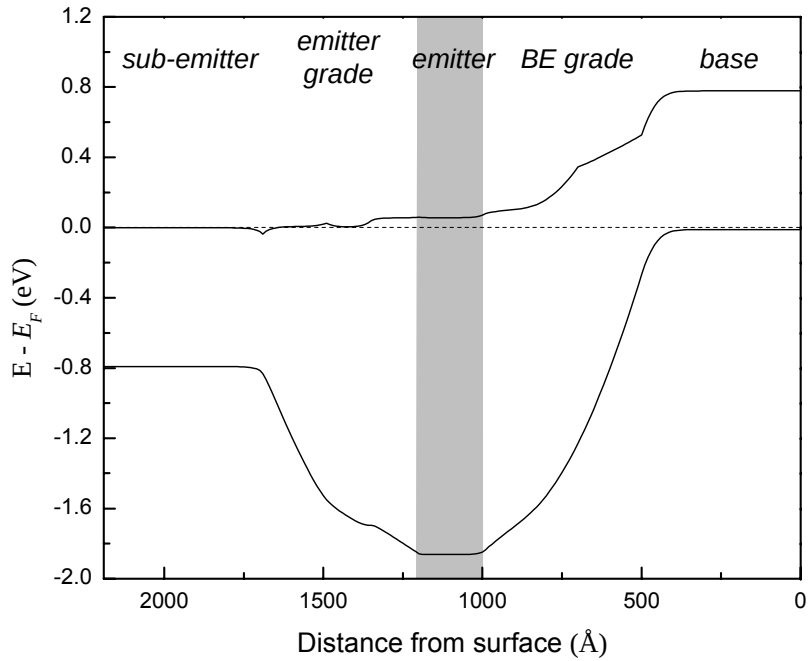
Oxide Aperture Diodes

Oxide aperture diodes were fabricated to understand the **potential effect of the oxide aperture** on the current-voltage characteristics of the BE junction of the HBT

Layer Structure



Band Diagram



Three thickness of BE grade were examined: **100 Å**, **500 Å**, **1000 Å**

Current Density: A versus P

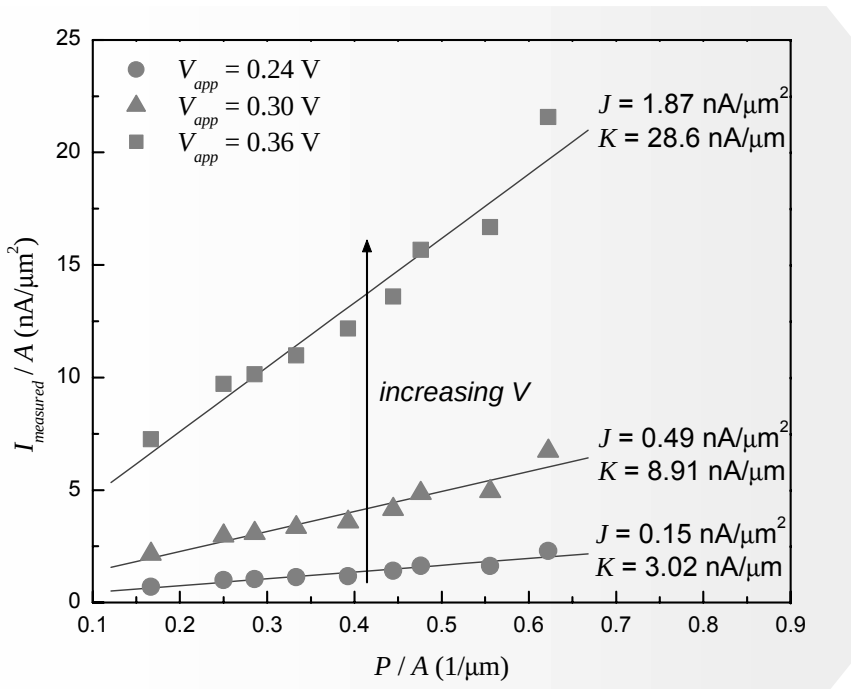
In addition to the ideality factor (η), the **geometric dependence** of the current provides information on the nature of current conduction within a *pn* junction

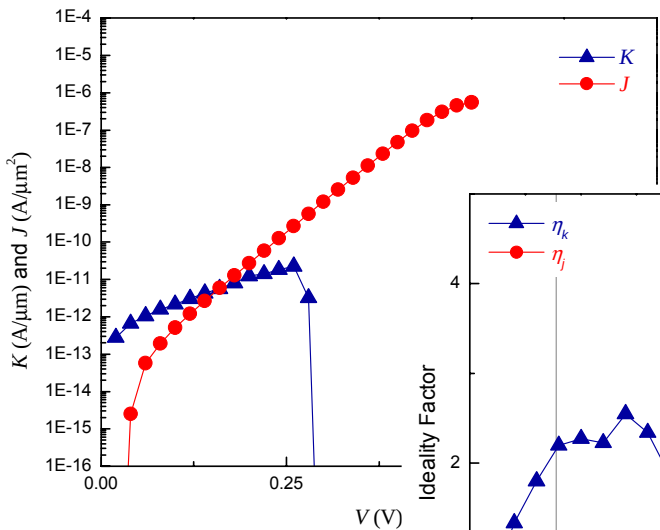
In actual diodes, the **total current** can be written as a sum of an **area dependent** and **perimeter dependent** current

$$I_{measured} = J \cdot A_j + K \cdot P_j$$

$$J_{measured} = \frac{I_{measured}}{A_j} = J + K \cdot \frac{P_j}{A_j}$$

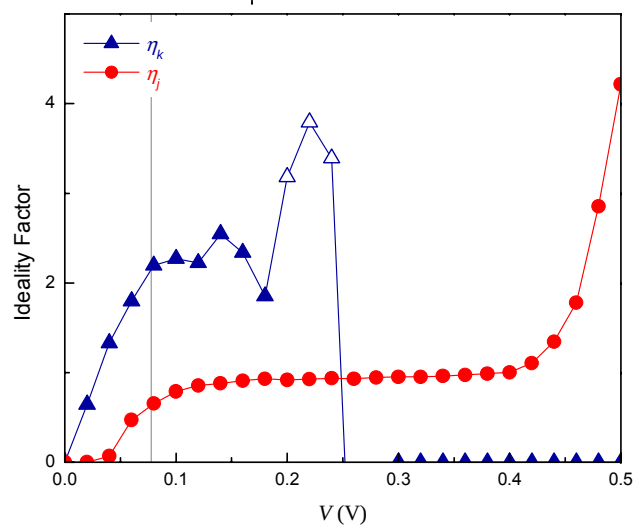
For a given bias with P_j / A_j as the independent variable, J corresponds to the **y-intercept** and K to the **slope** of the equation



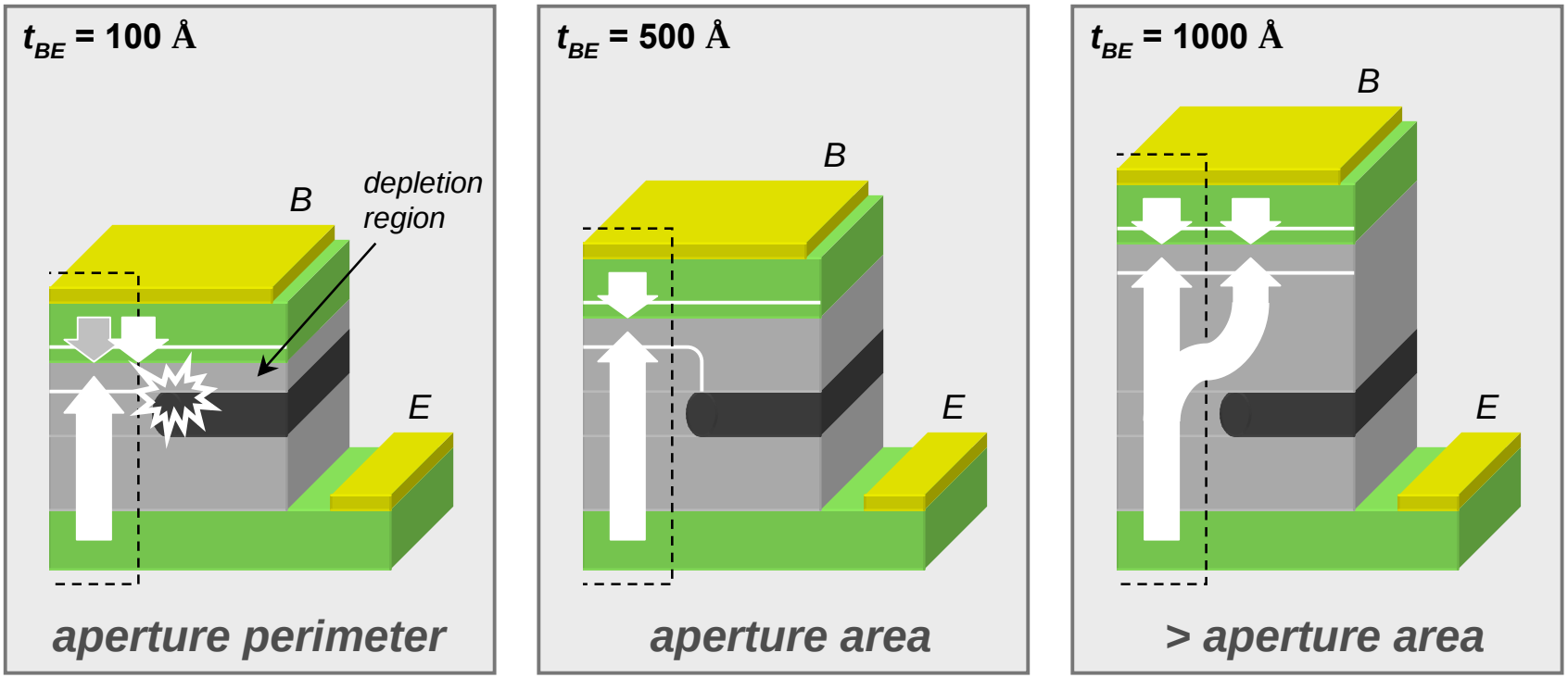


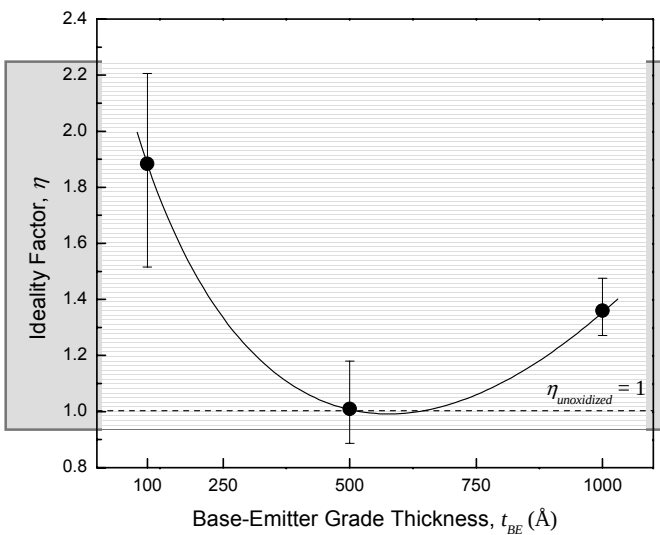
$$J = J_S \left(e^{V/\eta_j V_T} - 1 \right)$$

$$K = K_S \left(e^{V/\eta_k V_T} - 1 \right)$$



Oxide Aperture Diodes: Results



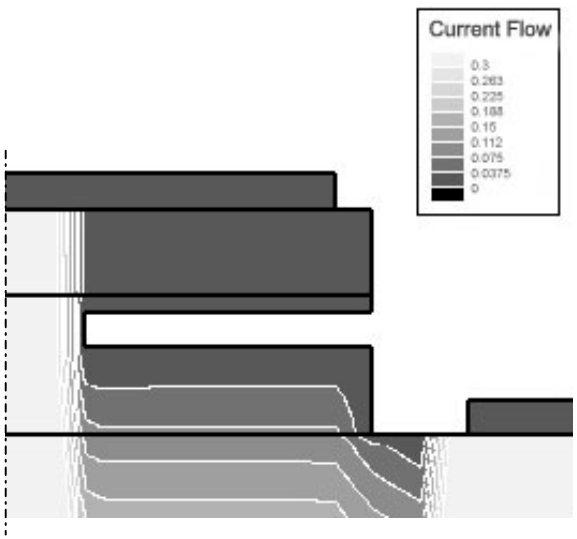


t_{BE}	Dominant geometry	η
unoxidized	Mesa area	~1
100 Å	Aperture perimeter	1.88
500 Å	Aperture area	1.01
1000 Å	Between mesa & aperture area	1.36

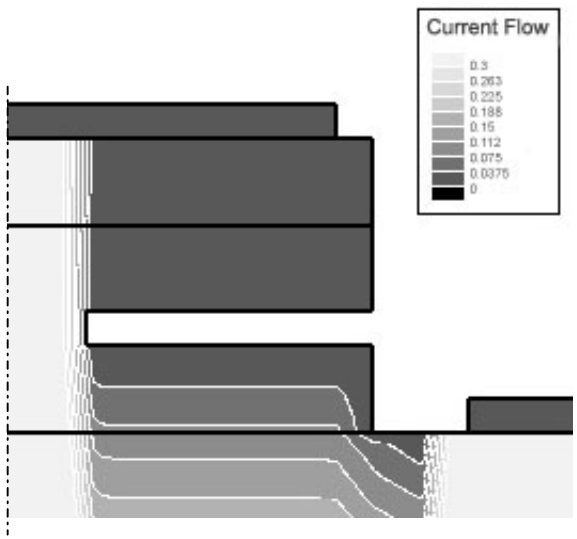
Oxide Aperture Diodes: Sims

Simulations performed using **ATLAS simulation software** generally agree with the experimental results

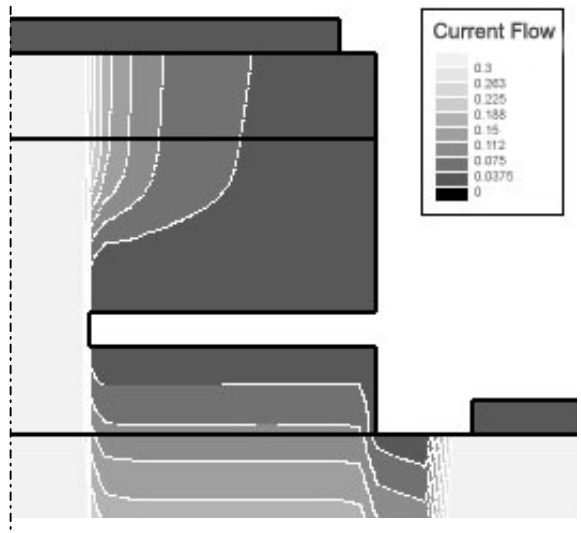
t_{BE} = 100 Å



t_{BE} = 500 Å



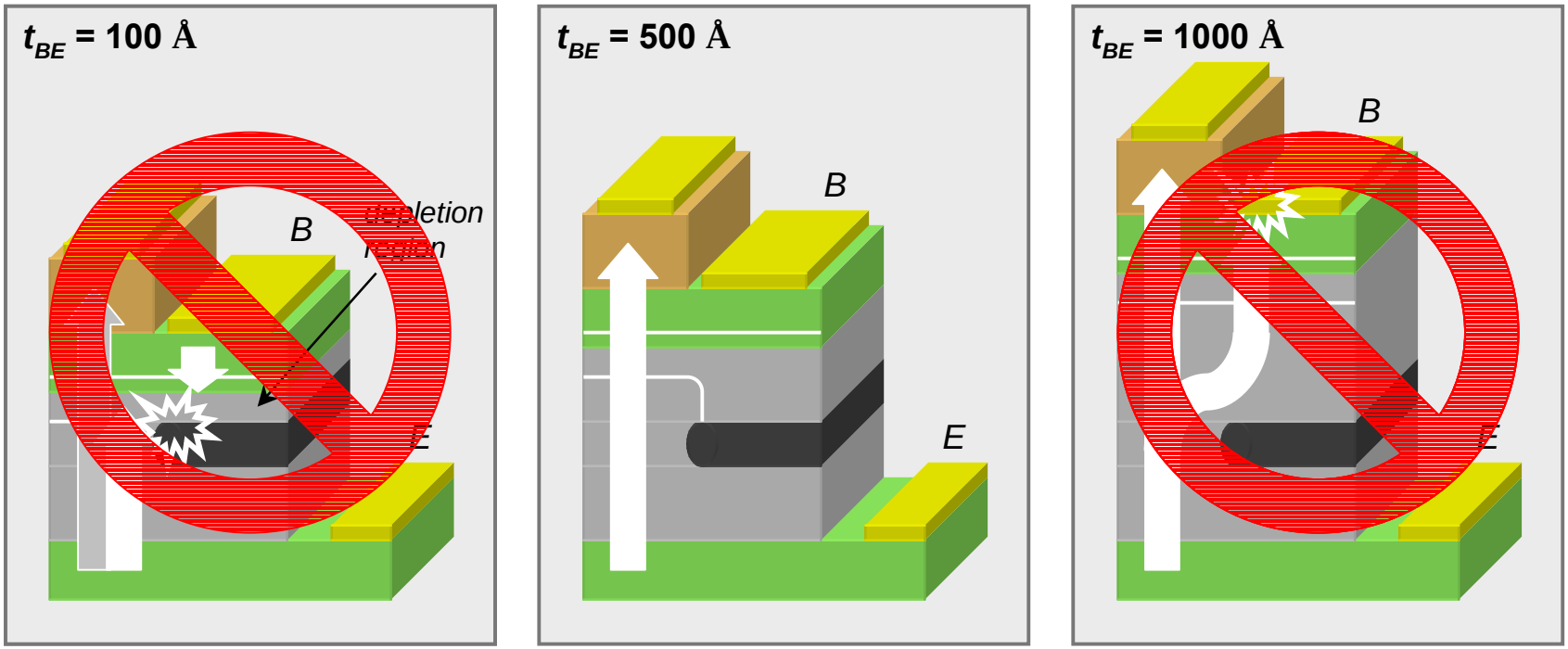
t_{BE} = 1000 Å



Simulations performed **without** interface recombination

Oxide Diodes: Selection Rules

"The Three Bears"



(*1*) The oxide aperture must effectively channel carriers injected from the emitter into the base

(*2*) The current-voltage characteristic should scale with aperture area

(*3*) The ideality factor (η) should be as close to ideal ($\eta \rightarrow 1$) as possible

"The Three Bears": one's too short, one's too long, and one's just right

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Oxide Aperture HBTs

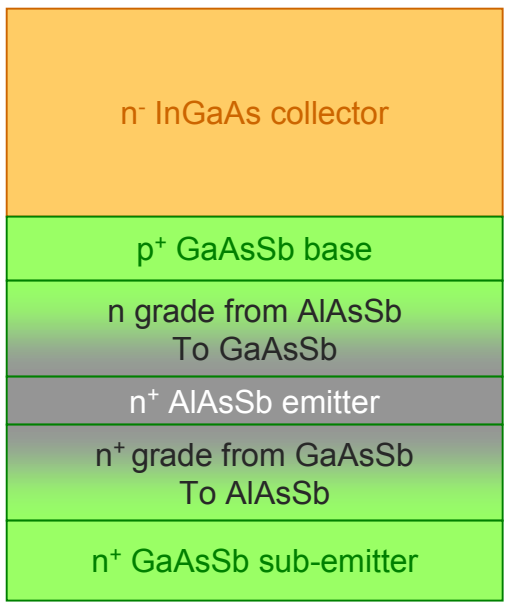
Three generations of oxide aperture HBTs were fabricated:

Generation Ø: The first generation of oxide aperture HBTs, fabricated **before** the oxide aperture diode study

Generation I: The first generation of HBTs to show true transistor action, fabricated **after** the oxide aperture diode study

Generation II: The first generation of oxide aperture HBTs to produce **high-frequency results**

Layer Structure



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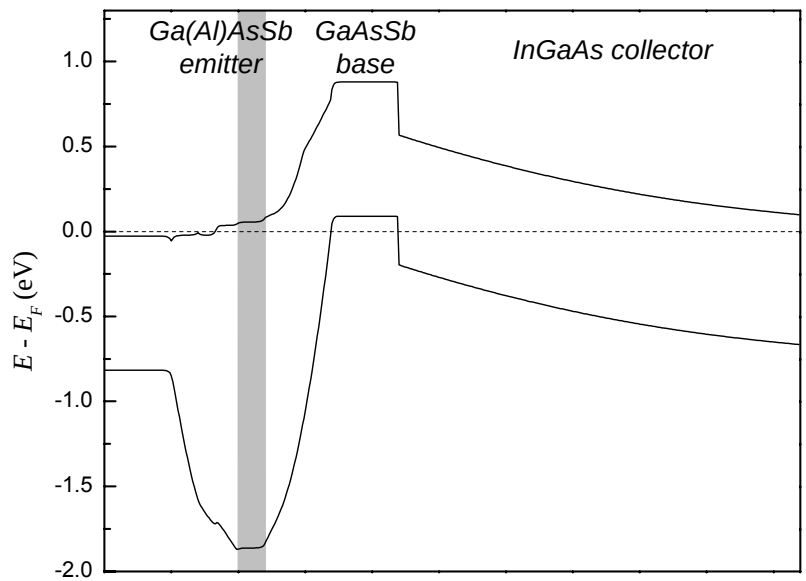
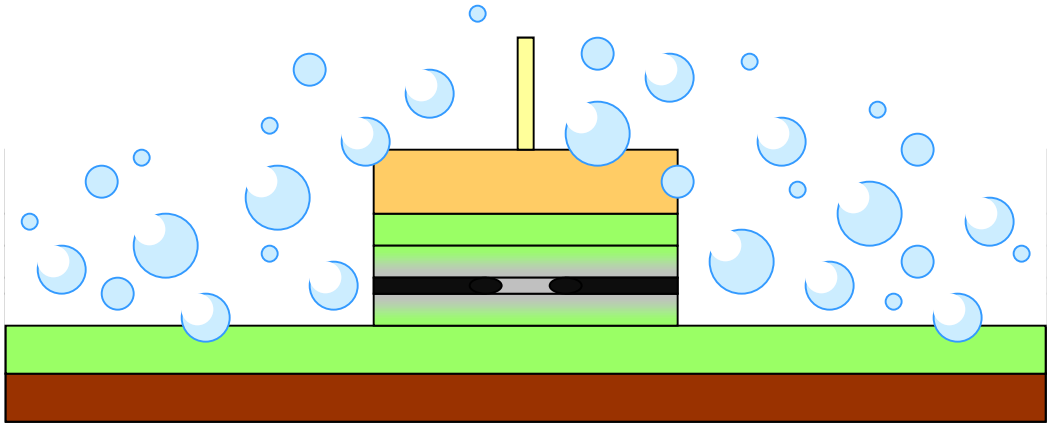


Oxide Aperture HBT: Fabrication



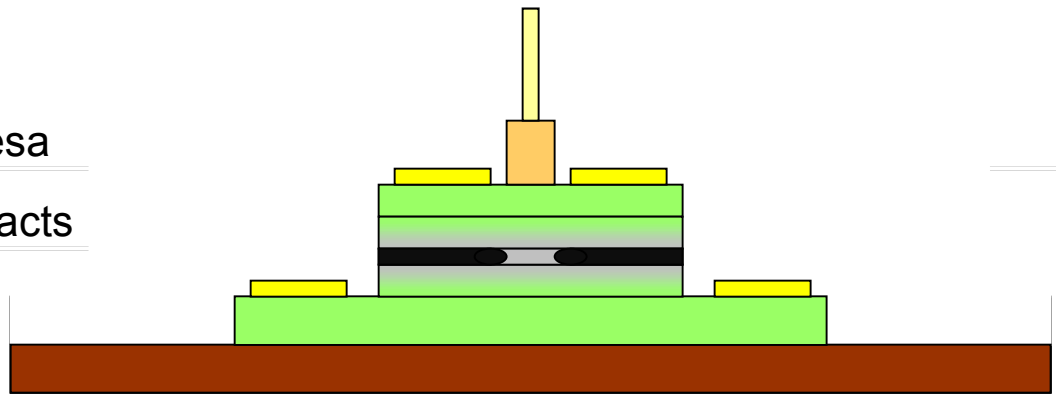
1 Deposit dummy collector

2 Etch base mesa

3 Oxidize emitter aperture

4 Etch collector mesa

5 Deposit B/E contacts

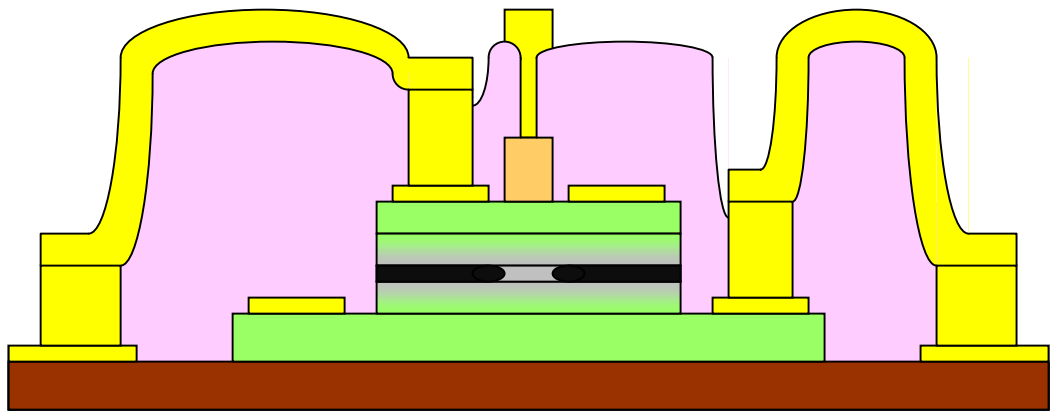


6 Etch emitter mesa

7 Deposit AC lines

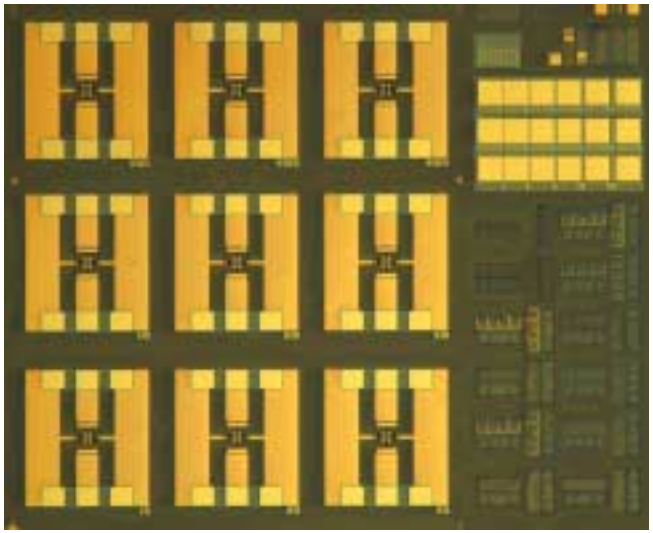
8 Planarize and deposit posts

9 Deposit interconnects



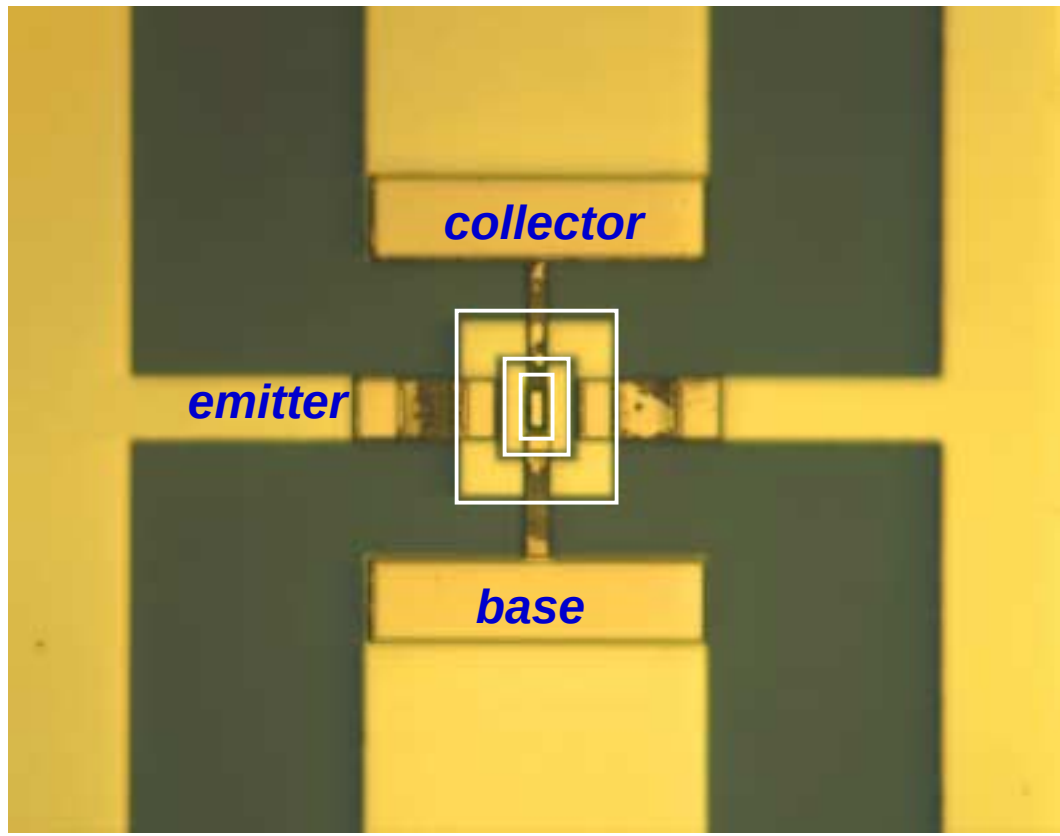
Oxide Aperture HBT: Fabrication

cell



HBT

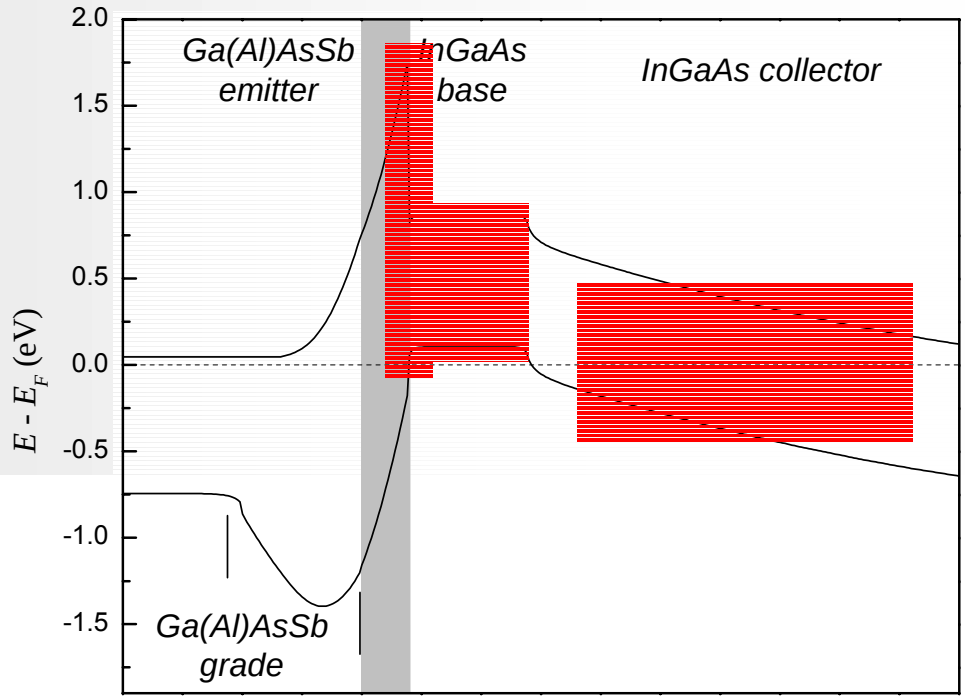
close-up of HBT

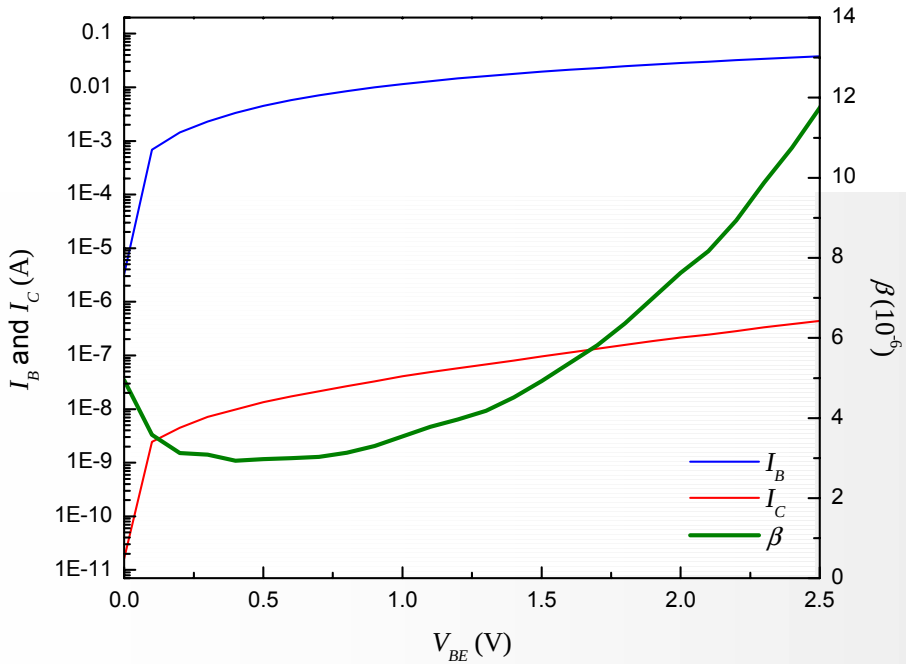


Oxide HBTs: Generation Ø

Key Differences of Gen Ø HBT

- InGaAs base
- Abrupt BE junction
- 2000 Å collector





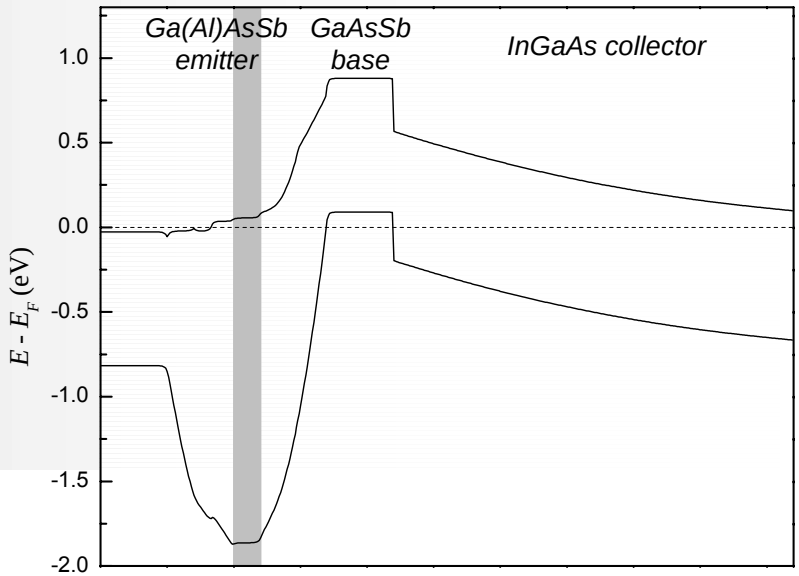
- β on the order of $10^{-6} \sim 10^{-5}$
- $\eta \approx 1.7$
- **Non-existent I_C, low β**, and **high η** all suggest that the characteristic is **recombination** dominated
- Results prompted the oxide diode study

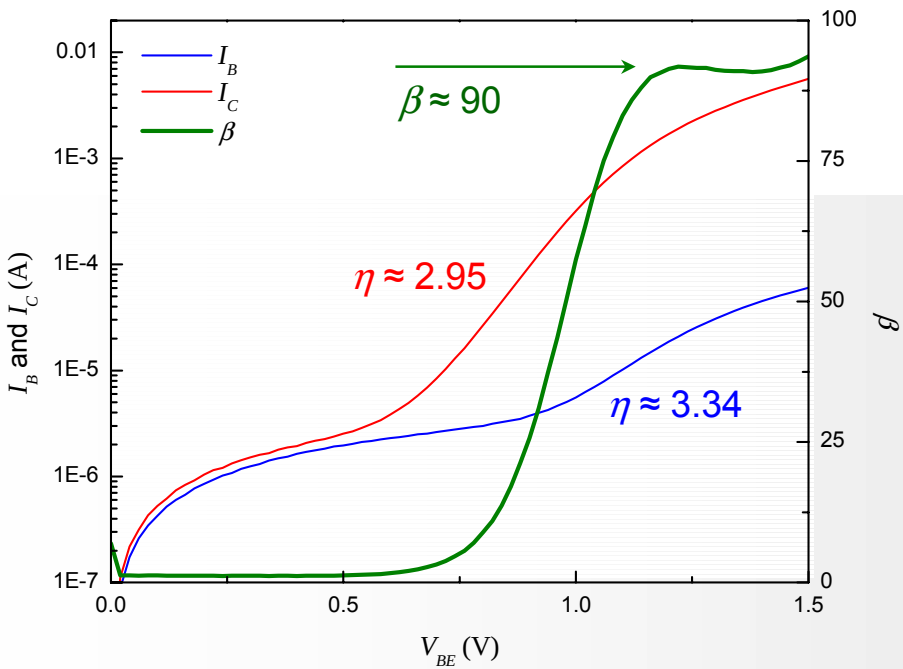
Oxide HBTs: Generation I

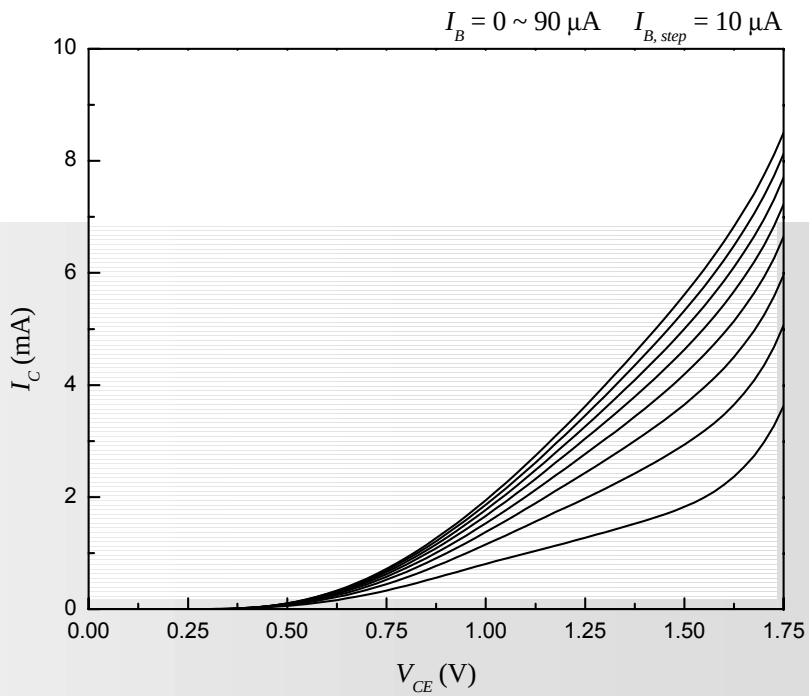
Key Differences of Gen I HBT

- Lower doping in base and emitter
- 2000 Å collector

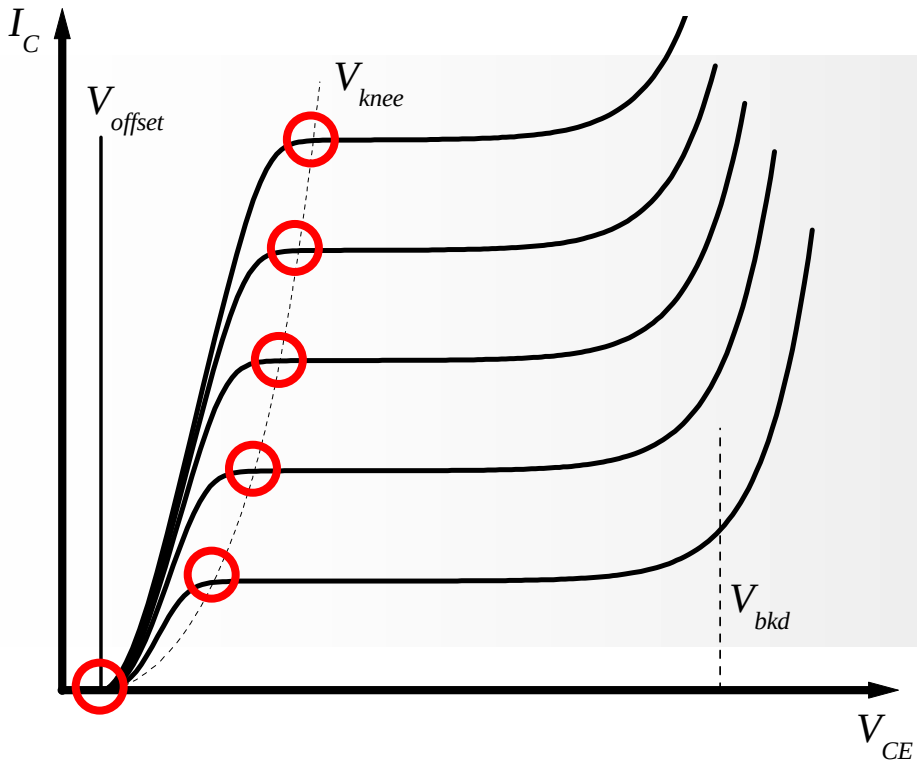
Fabricated from same material as the oxide diodes







V_{offset} and V_{knee}

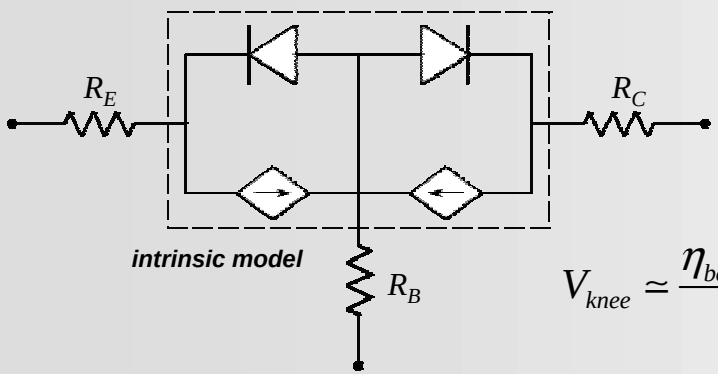


Definitions

V_{offset} : V_{CE} at which I_C = 0

V_{knee} : V_{CE} at which the device switches between forward-saturation and forward-active operation ($V_{BC} \approx 0$)

Modified Ebers-Moll Model

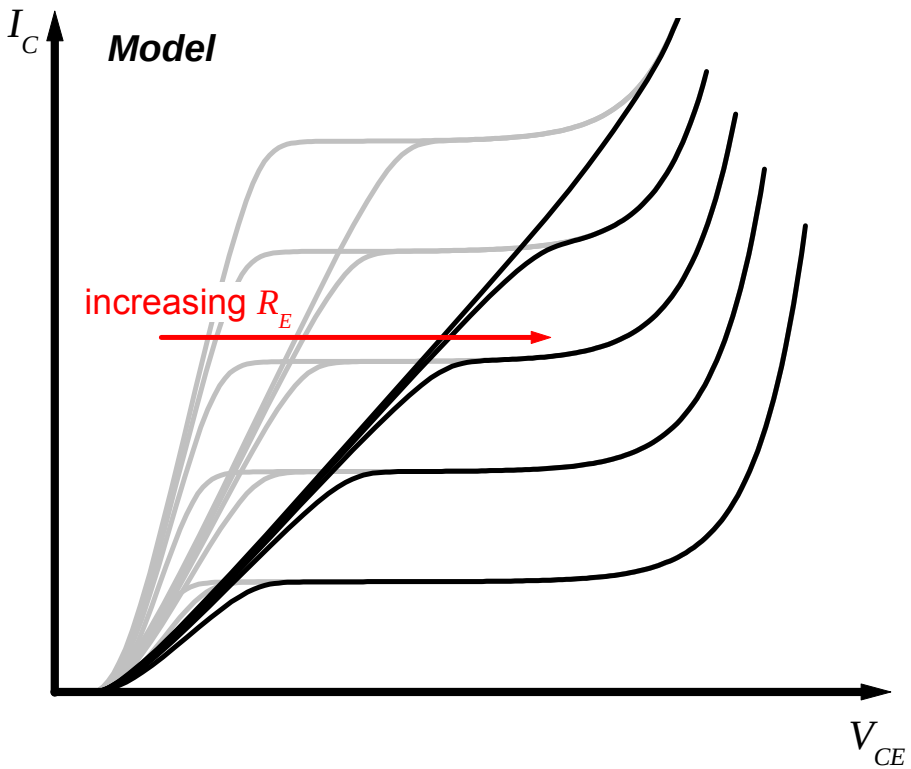


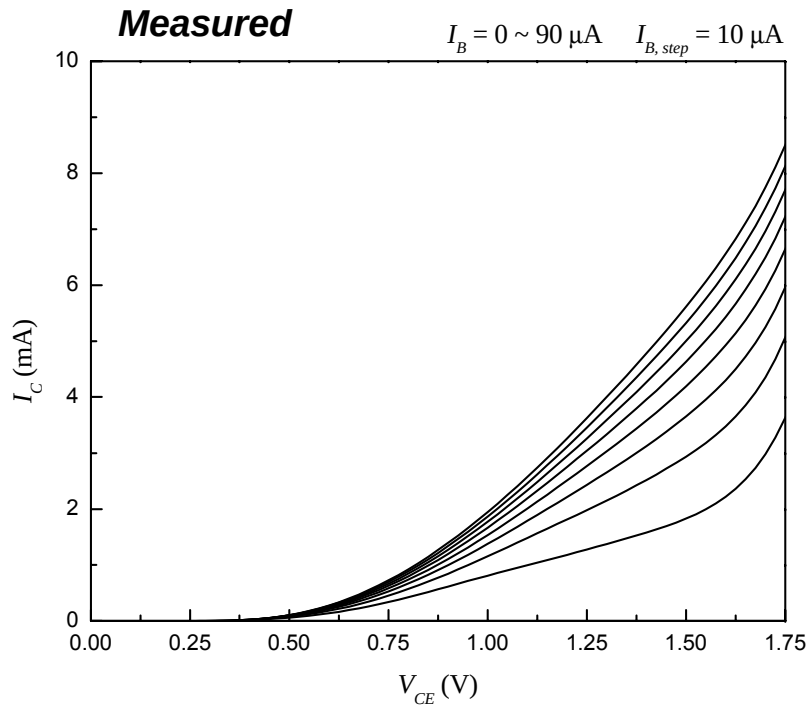
$$V_{offset} \simeq \eta_{bc}\frac{kT}{q}\ln\left(\frac{I_{bc,sat}}{\alpha_F I_{be,sat}}\right)+\left(1-\frac{\eta_{bc}}{\eta_{be}}\right)\left(V_{BE}-I_B R_B\right)+\frac{\eta_{bc}}{\eta_{be}}I_B R_B$$

$$V_{knee} \simeq \frac{\eta_{be}kT}{q}\ln\left[\frac{I_E-\alpha_R I_C}{I_{be,sat}\left(1-\alpha_F\alpha_R\right)}\right]-\frac{\eta_{bc}kT}{q}\ln\left[\frac{\alpha_F I_E-I_C}{I_{bc,sat}\left(1-\alpha_F\alpha_R\right)}\right]+I_E R_E+I_C R_C$$

The Knee Voltage: V_{knee}

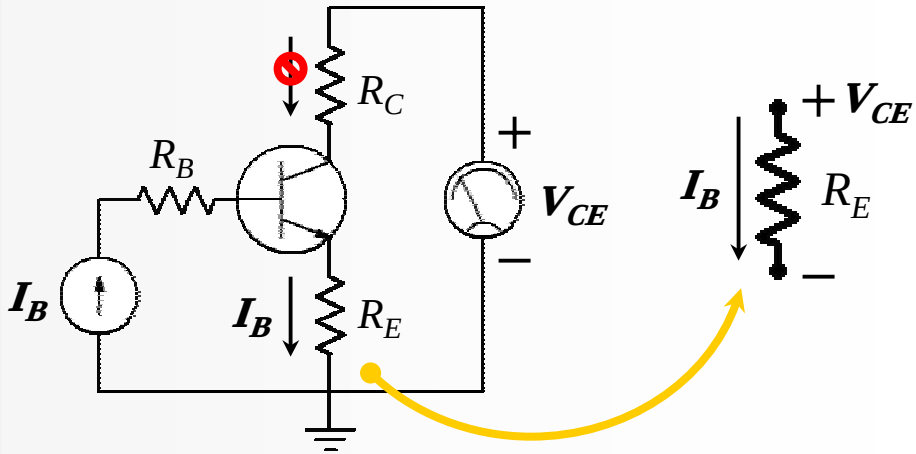
$$V_{knee} \simeq \frac{\eta_{be} kT}{q} \ln\left[\frac{I_E - \alpha_R I_C}{I_{be,sat}\left(1-\alpha_F \alpha_R\right)}\right] - \frac{\eta_{bc} kT}{q} \ln\left[\frac{\alpha_F I_E - I_C}{I_{bc,sat}\left(1-\alpha_F \alpha_R\right)}\right] + I_E R_E + I_C R_C$$



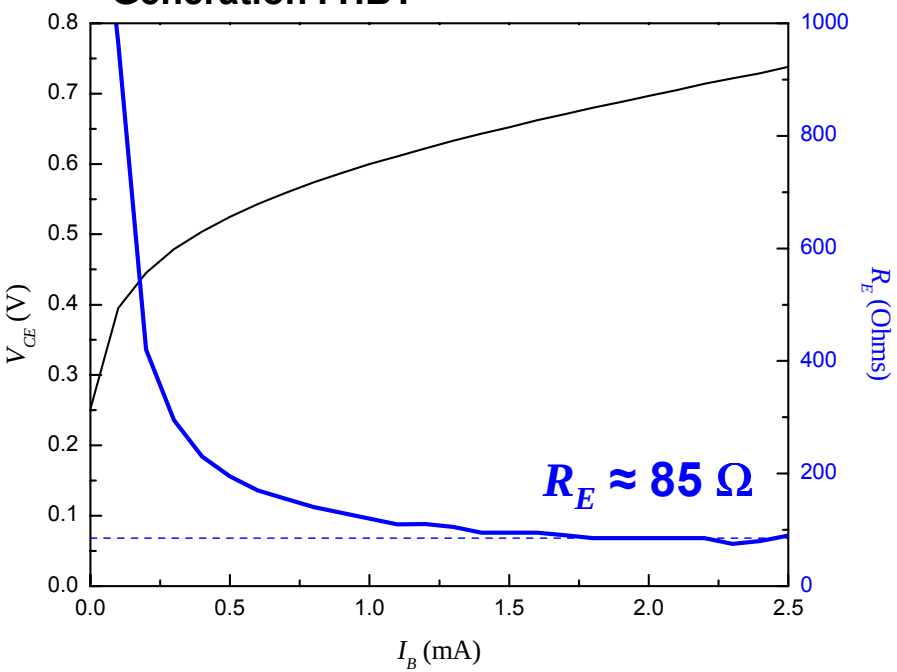


Generation I: Emitter Resistance

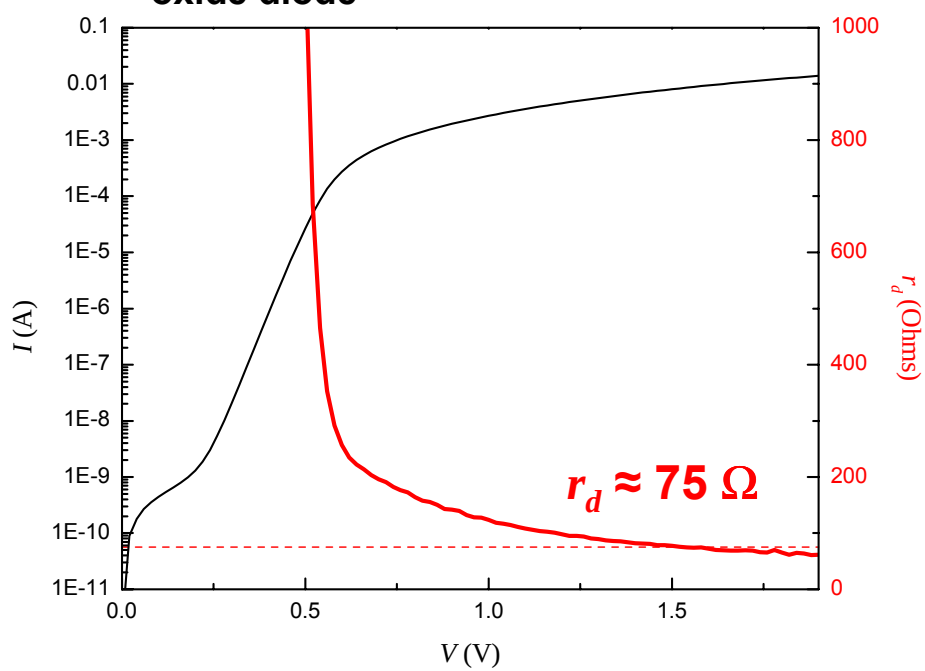
The **emitter resistance** (R_E) of a bipolar transistor can be measured by **floating-collector measurements**



Generation I HBT



oxide diode



At a current level of **~4 mA** with $R_E \approx 85\ \Omega \rightarrow V_{knee} \geq 0.34$ V

Oxide HBTs: Generation II

What have we learned so far…

Generation Ø and oxide diodes

Oxide aperture placement is critical

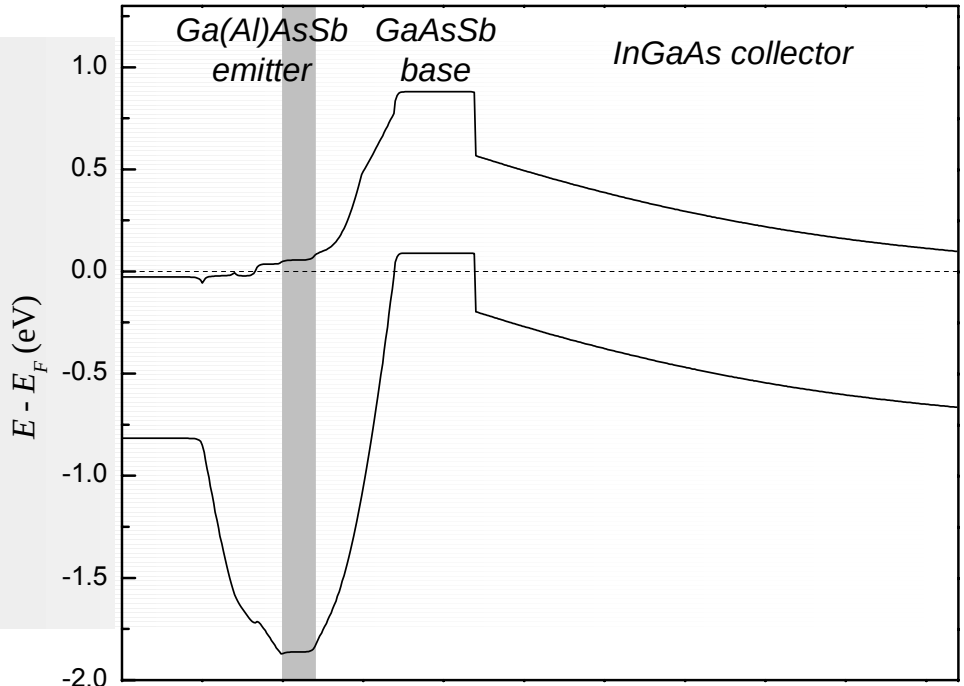
"The Three Bears": can't be **too close**, can't be **too far**, has to be **just right**

Generation I

Resistance in the emitter due to the **low electron mobility** in $AlAs_{0.56}Sb_{0.44}$ is a problem (high V_{knee})

Generation II

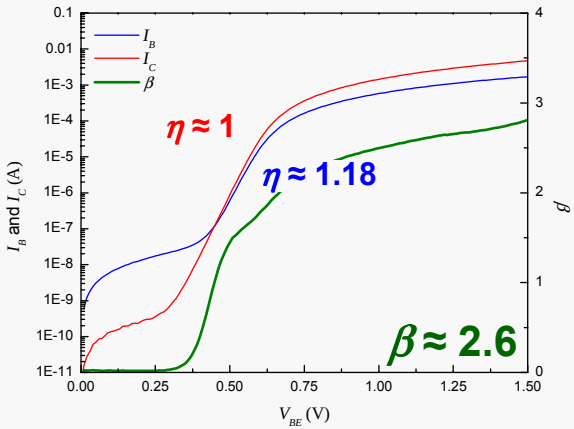
- Oxide aperture is located 500 Å from the *pn* junction (same as Gen I)
- Increased doping in the emitter and base
- Increased collector width to 3000 Å

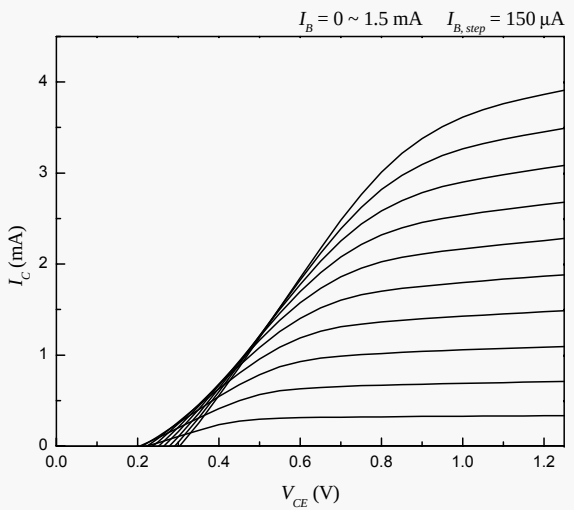


Generation II: Gummel and CE

1 x 10 HBT

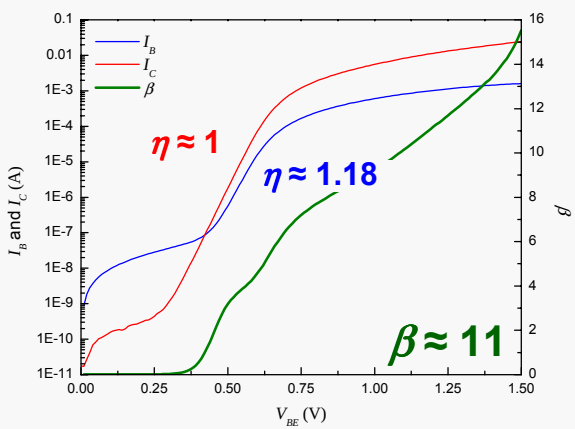
A_E = 0.5 x 9.5 μm²
A_C = 1 x 10 μm²

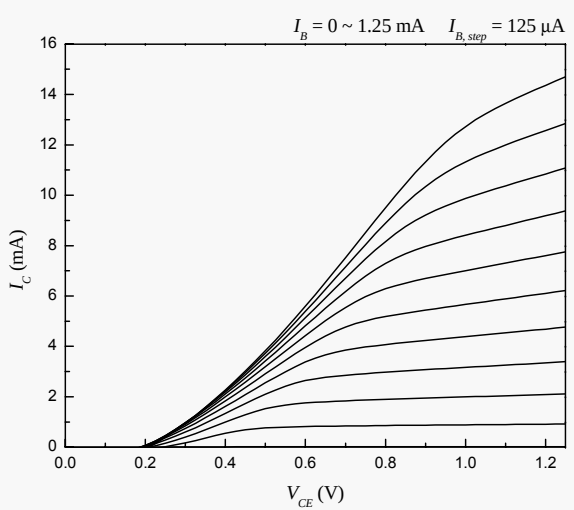




2 x 10 HBT

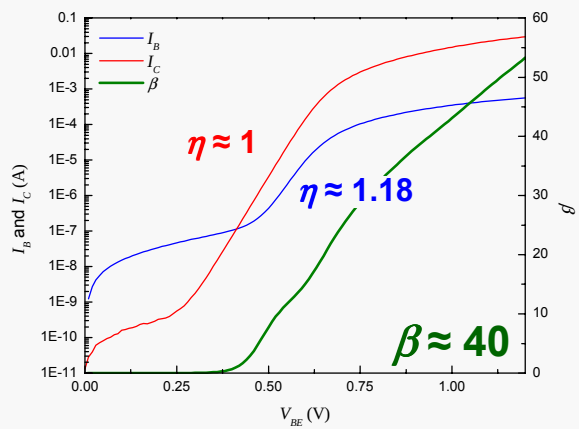
A_E = 1.5 x 9.5 μm²
A_C = 2 x 10 μm²

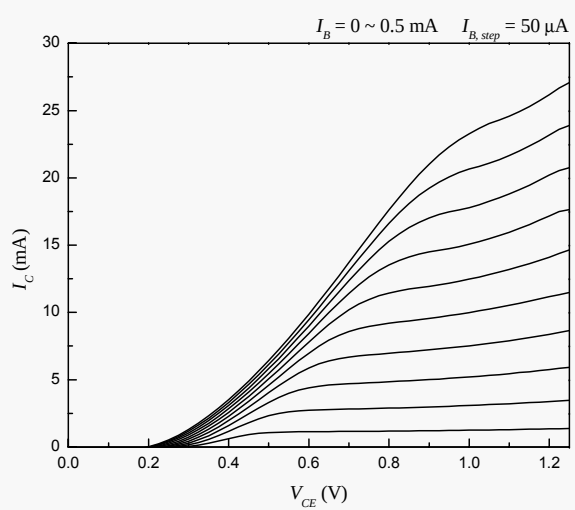




4 x 10 HBT

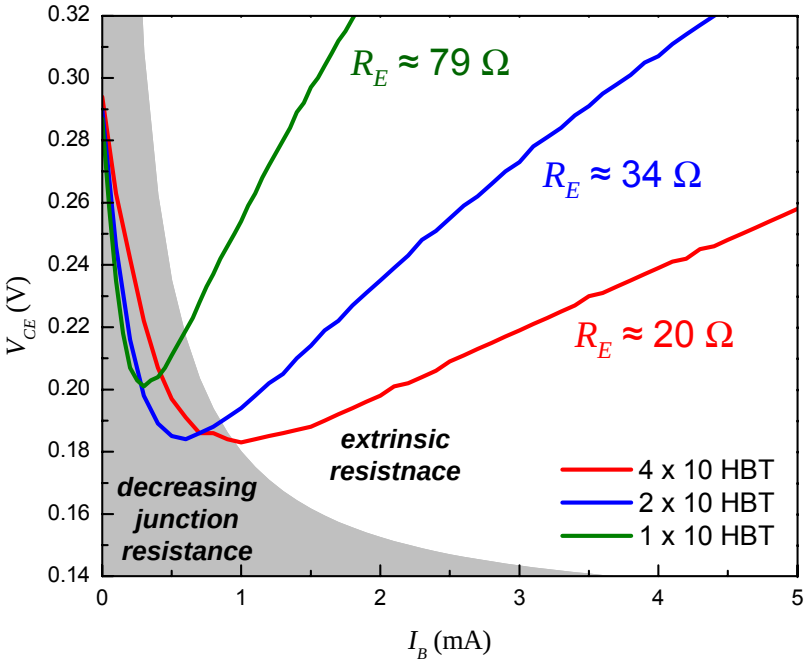
A_E = 3.5 x 9.5 μm²
A_C = 4 x 10 μm²

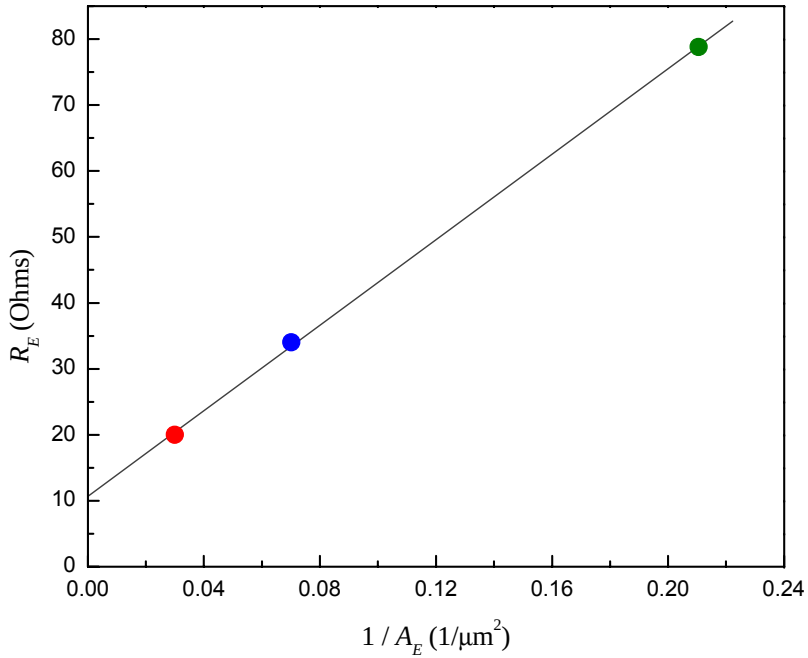




Generation II: Emitter Resistance

Floating-collector measurements

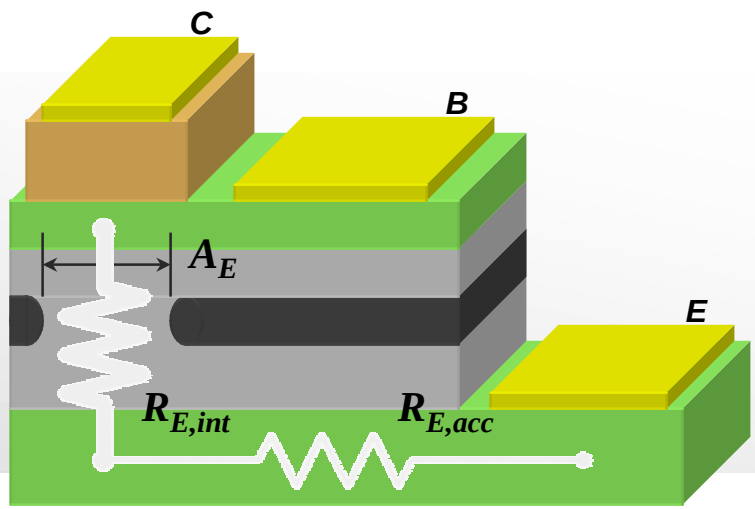




Emitter resistance (R_E) has **reduced** as a direct result of increased doping

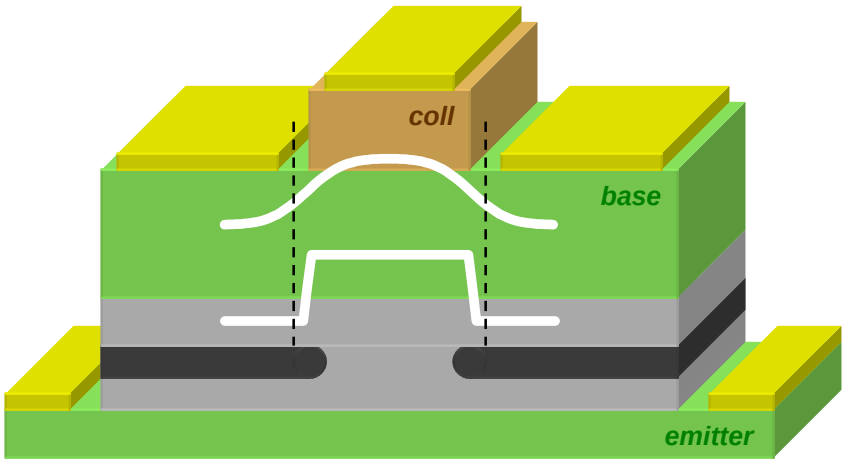
R_E **increases linearly** with **1 / A_E**

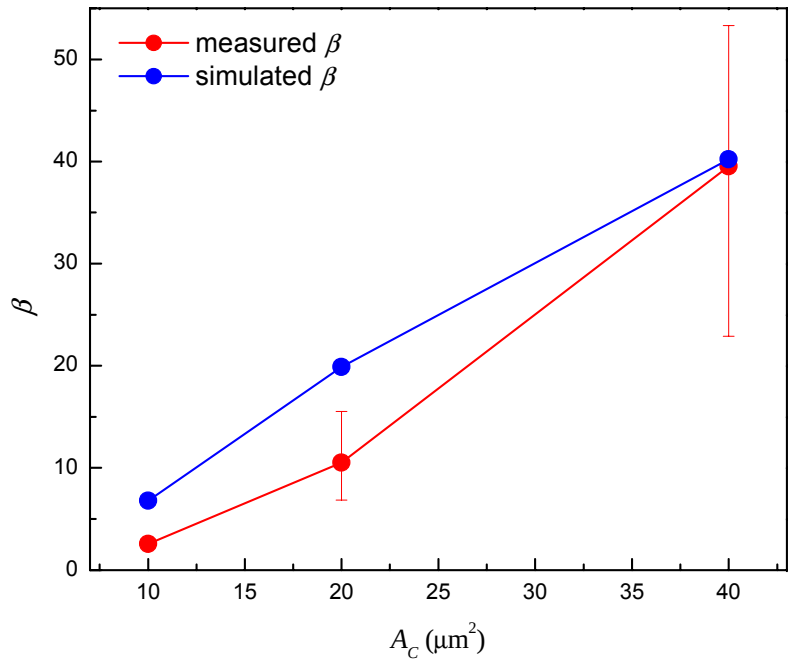
- Suggests **internal resistance** ($R_{E,int}$) **dominates** of lateral access resistance ($R_{E,acc}$)



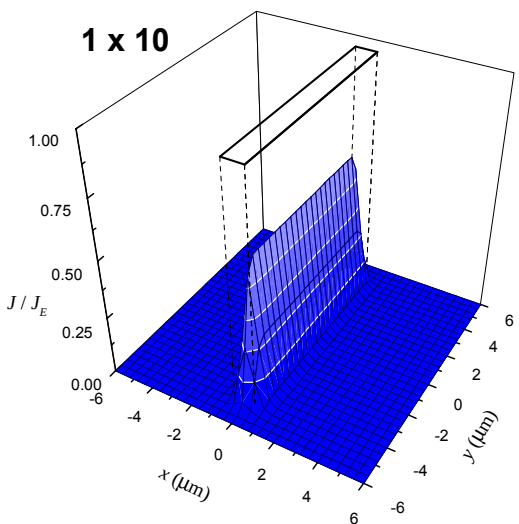
Generation II: Gain Variation

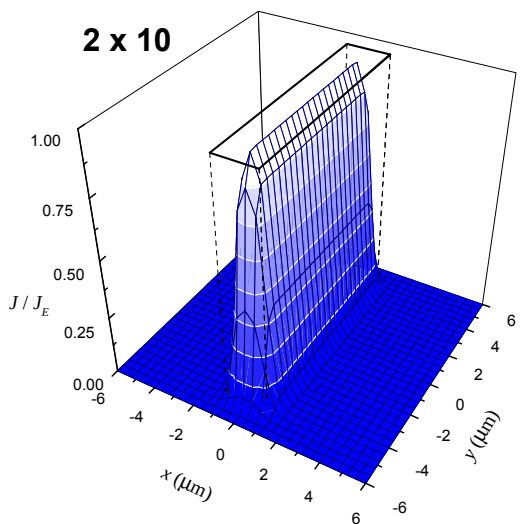
The reduced gain with decreasing emitter/collector area is most probably a result of **lateral diffusion of carriers**

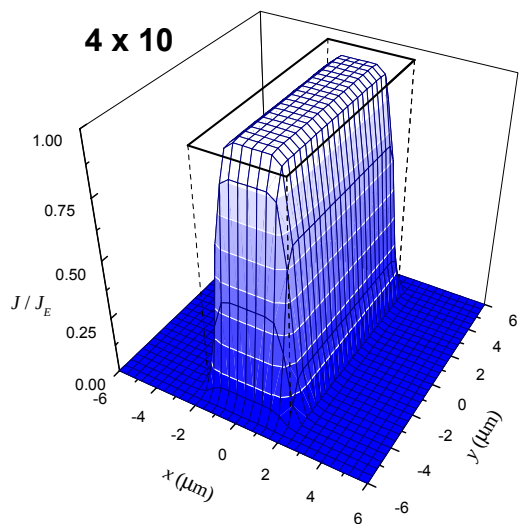




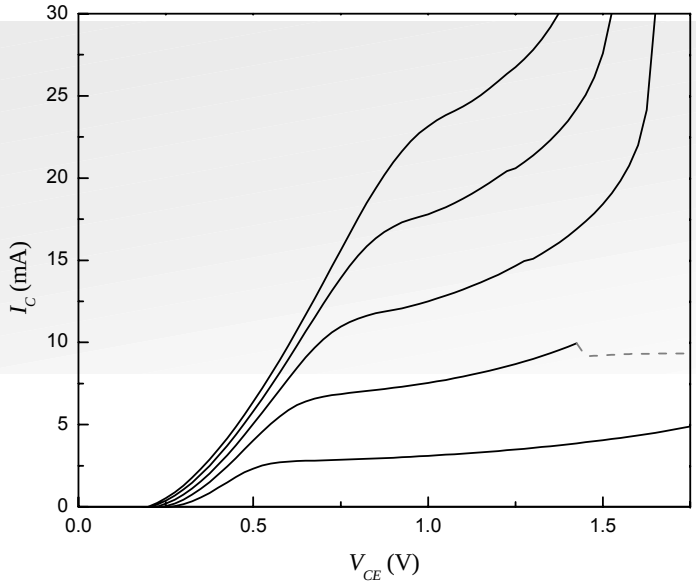
Simulations







Generation II: Output Conductance

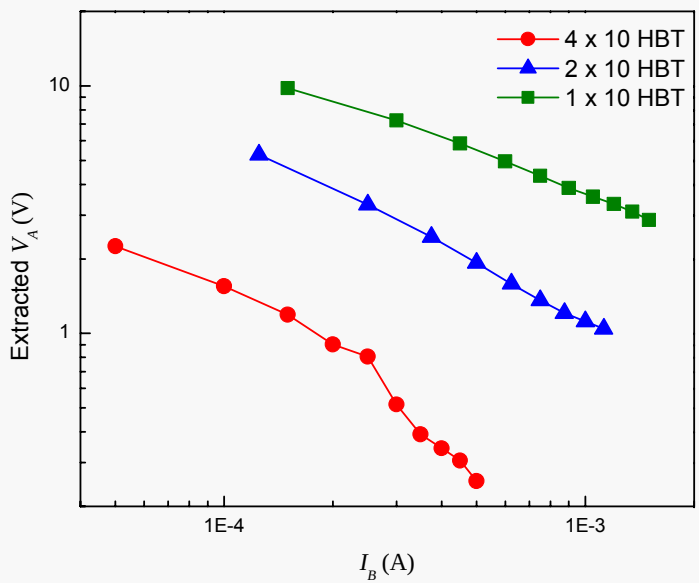


The **output conductance** (g_o) of the oxide aperture HBT is much **higher than expected**

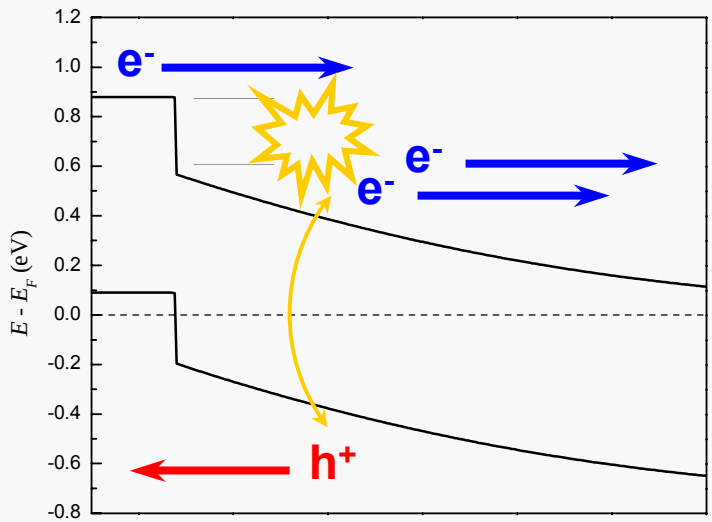
The common-emitter **breakdown voltage** (V_{bkd}) is **lower than expected**

Impact Ionization

Early Effect

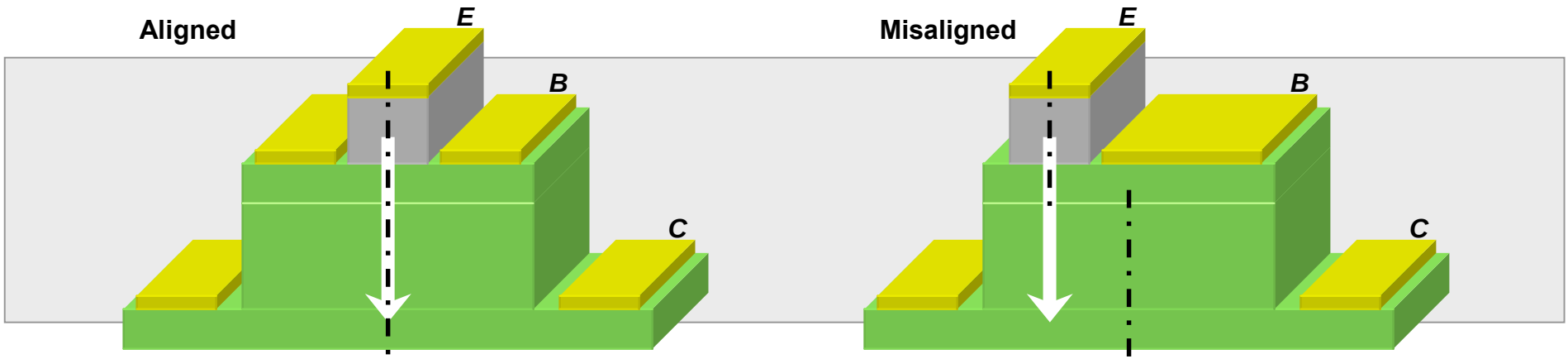


Impact Ionization

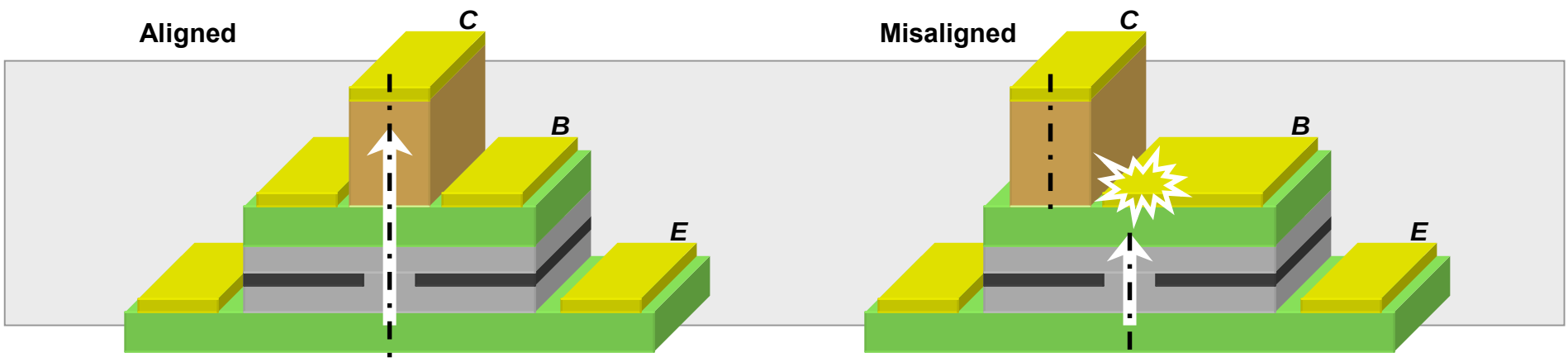


Generation II: Misaligned HBTs

In **conventional HBTs**, the active **collector area** is **larger** than the active **emitter area**



In **oxide aperture HBTs**, the active **collector area** and **emitter area** are roughly the **same size**

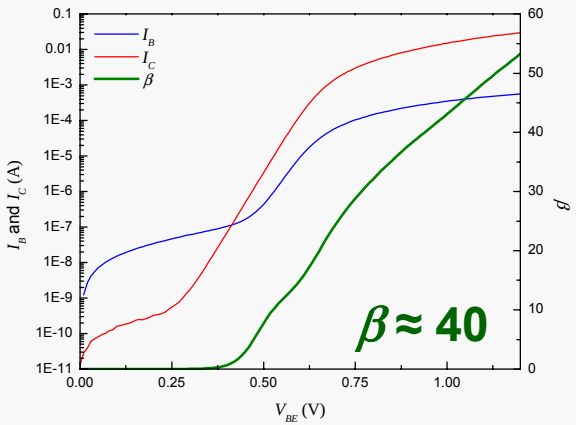


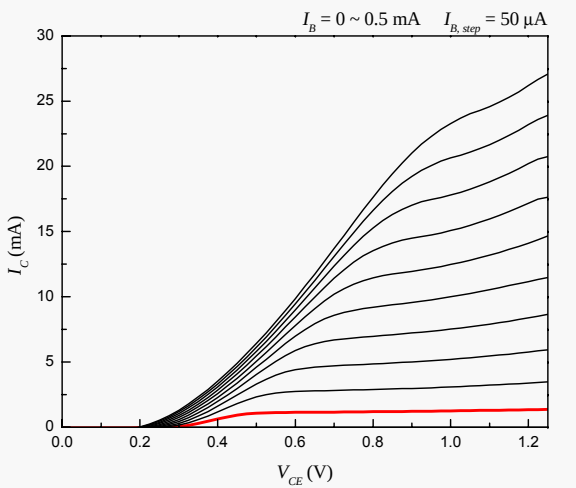
Generation II: Misaligned HBTs

A_C = 4 x 10 μm² and A_E = 3.5 x 10 μm² for all HBTs

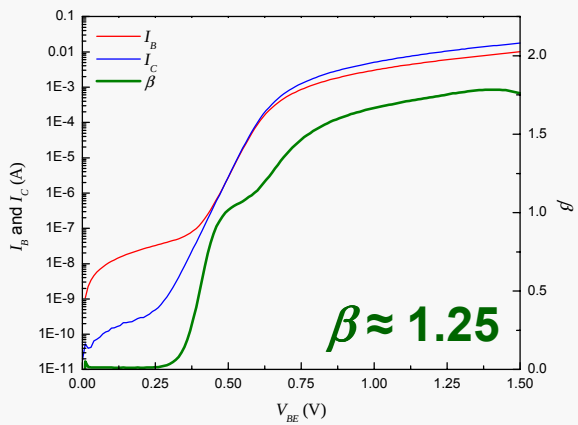
I_B = 0 ~ 0.5 mA at 50 μA steps

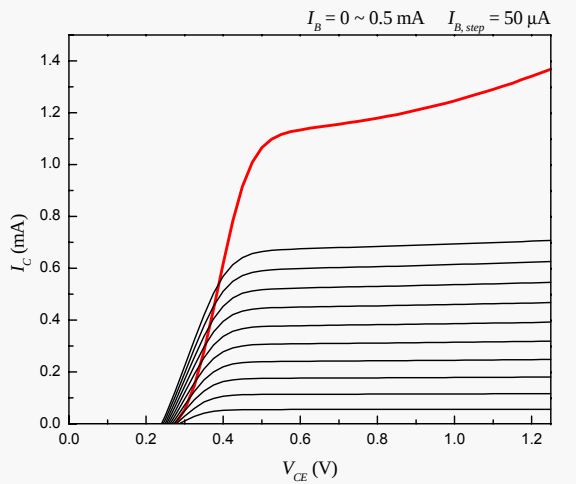
+ 0 μm



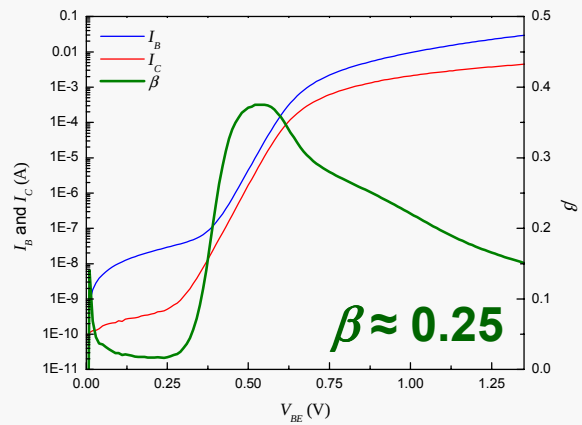


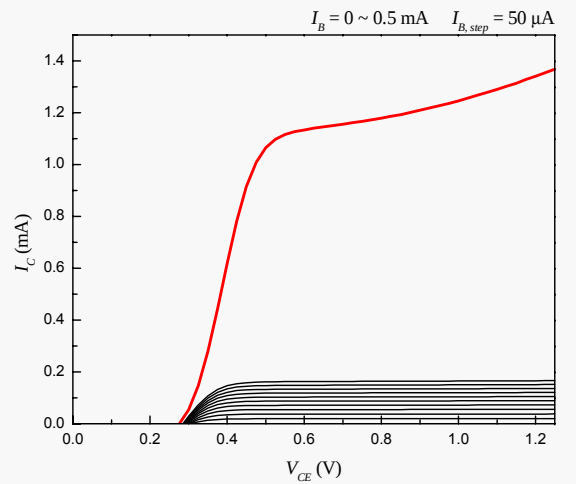
+ 1 μm





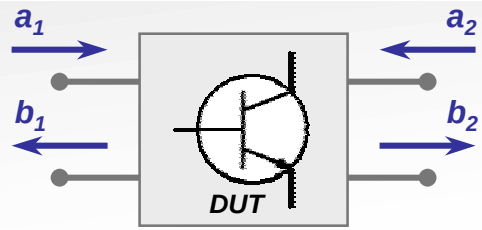
+ 2 μm



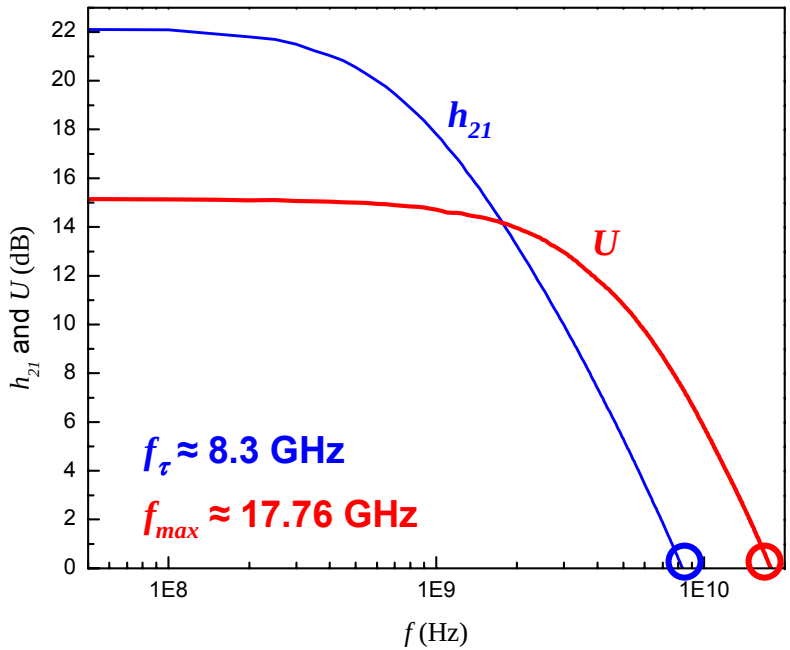


RF Measurements

Scattering parameter (***S*-parameter**) measurements were performed on the Generation II HBTs in order to evaluate the transistor's **frequency performance**



From *S*-parameters, characteristics like the **short-circuit current gain** (h_{21}) and **unilateral power gain** (U) can be extracted



Subsequently, the **current-gain cutoff frequency** (f_τ) and **maximum frequency of oscillation** (f_{max}) can be determined

Measured f_τ and f_{max}

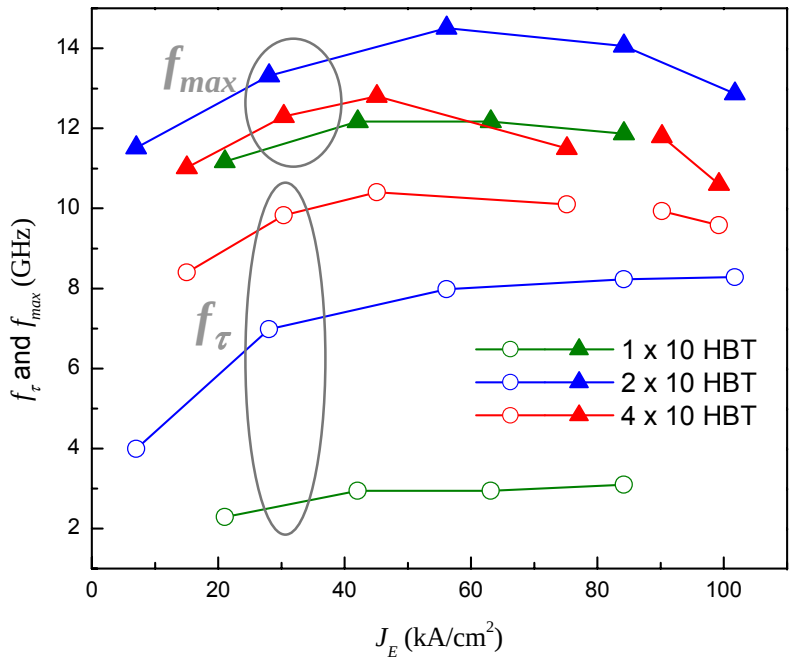
Measured f_τ and f_{max}

The measured values of f_τ and f_{max} for the oxide aperture HBTs were lower than expected

Maximum measured f_{max}

f_{max} = 17.76 GHz f_τ = 8.3 GHz

for a 2 x 10 HBT ($I_C \approx 9$ mA, $V_{CE} = 2$ V)



Calculated f_τ and f_{max}

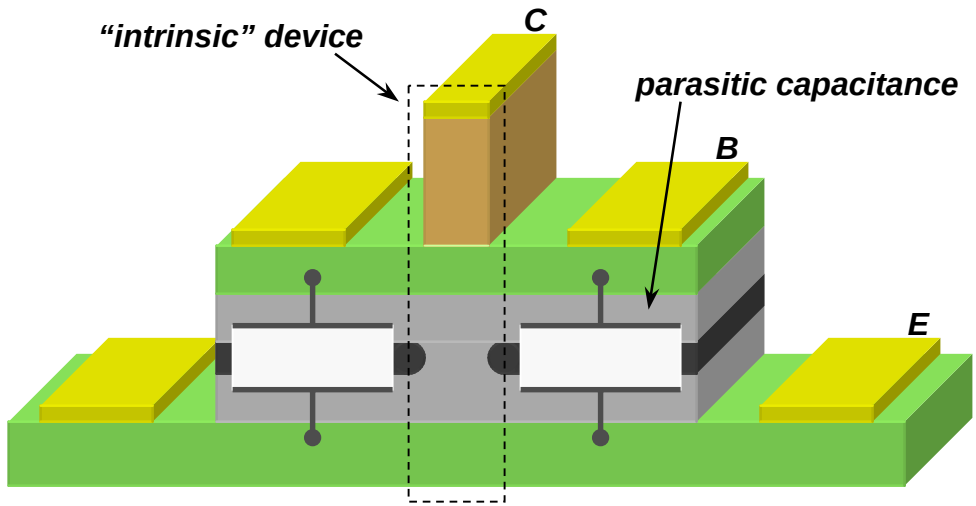
Calculations using the measured R_E, R_B, and assuming a fully depleted collector suggest: **$f_\tau \approx 25$ GHz $f_{max} \approx 35$ GHz**

f_τ and f_{max} were calculated using the **classical** hybrid-π model for a bipolar transistor

$$f_\tau = \frac{1}{2\pi}\left[\frac{\eta V_T}{I_C}\left(C_{BE}+C_{BC}\right)+\tau_B+\tau_C+\left(R_E+R_C\right)C_{BC}\right]^{-1} \qquad f_{max} = \sqrt{\frac{f_\tau}{8\pi R_B C_{BC}}}$$

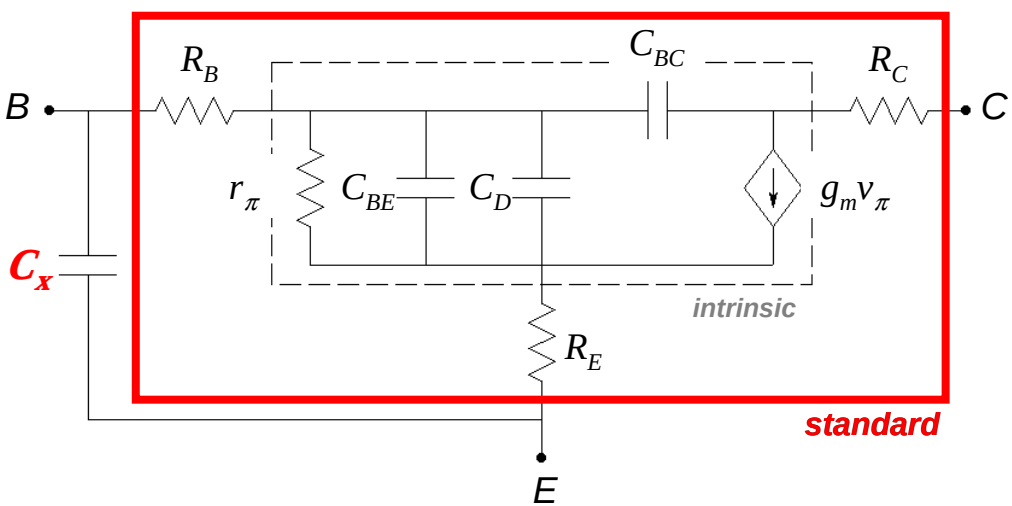
Parasitic Base-Emitter Capacitance

Re-examining the of the oxide aperture HBT structure suggests the presence of a **parasitic capacitance** in the base-emitter resulting from the **collector-up design**



Modified model

By using MoTC, the **parasitic capacitance** leads to an **additional delay time** within f_τ



$$f_{\tau,x} = \frac{1}{2\pi}\left[\tau_{\tau,std} + \left(\frac{\eta V_T}{I_C} + \frac{R_B}{\beta_o} + R_E\right)C_x\right]^{-1}$$

$$\tau_{\tau,std} = \frac{1}{2\pi f_{\tau,std}}$$

$$f_{max,x} = \sqrt{\frac{f_{\tau,std}}{8\pi R_B C_{BC}}} \neq \sqrt{\frac{f_{\tau,x}}{8\pi R_B C_{BC}}}$$

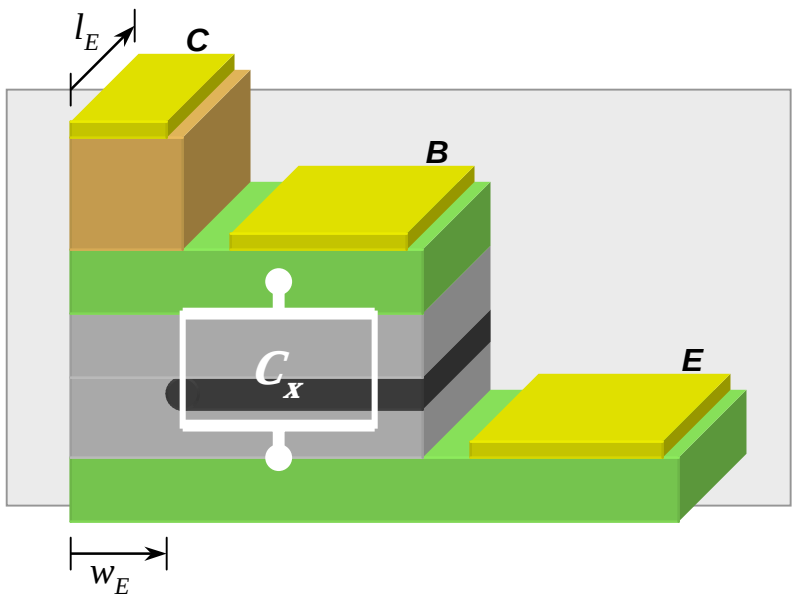
f_τ Scaling

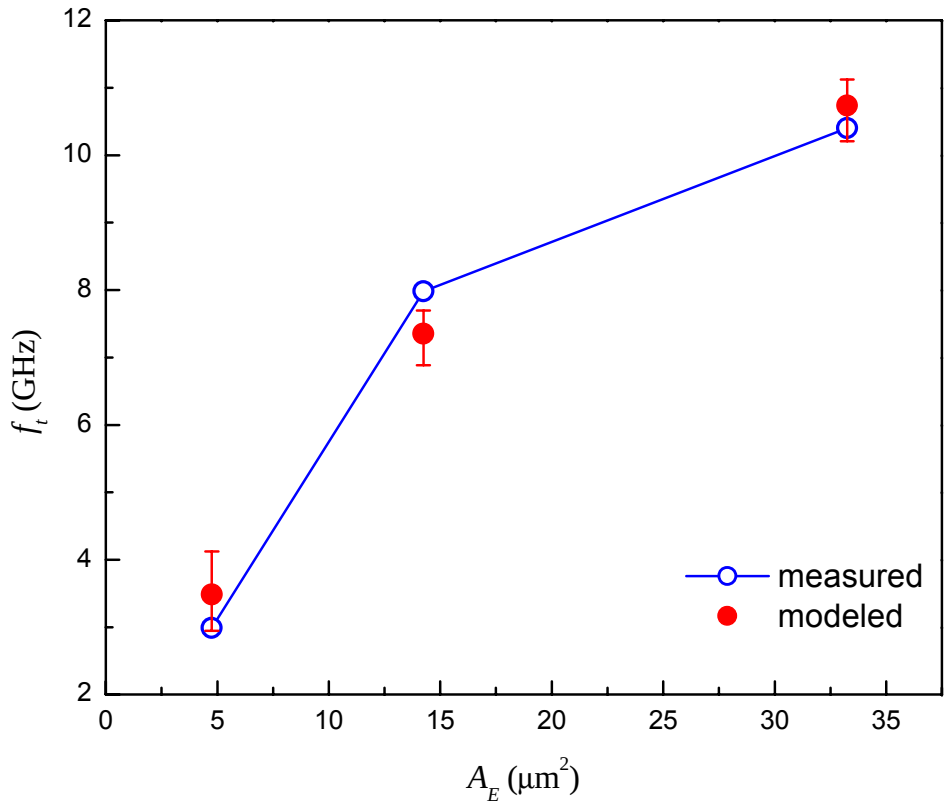
In a transistor where $A_C \approx A_E$, f_τ should be essentially **independent of emitter size**

$$f_\tau = \frac{1}{2\pi}\left[\frac{\eta V_T}{J_C}\left(c_{BE}+c_{BC}\right)+\tau_B+\tau_C+\left(r_E+r_C\right)c_{BC}\right]^{-1}$$

In the oxide aperture HBT, this is not true

$$f_{\tau,x} = \frac{1}{2\pi}\left[\tau_{\tau,std}+\left(\frac{\eta V_T}{I_C}+\frac{R_B}{\beta_o}+R_E\right)C_x\right]^{-1}$$





By applying the above equation, $f_{\tau,std} = 1/2\pi\tau_{\tau,std} \approx$ **26.3 GHz** and $C_x \approx$ **345 fF**

Circuit designers require device models in order to design accurately and model circuits

Device models are useful to device engineers because they can lend insight into the operation of the device, in addition to verifying proposed phenomenon

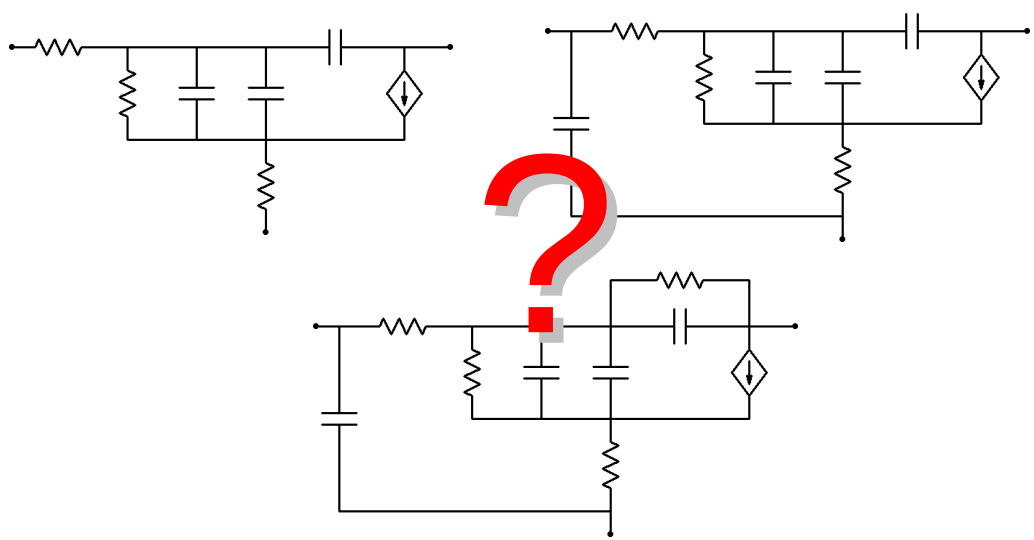
Model Extraction

Proper high-frequency model extraction requires:

(*1*) A well-behaved, stable device

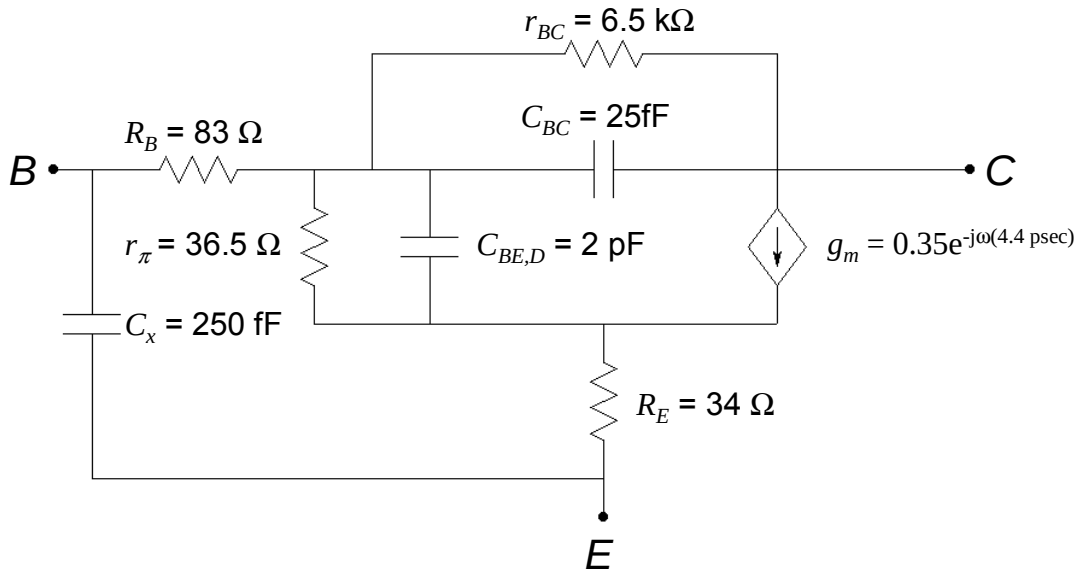
(*2*) Y-parameters that accurately represent the device

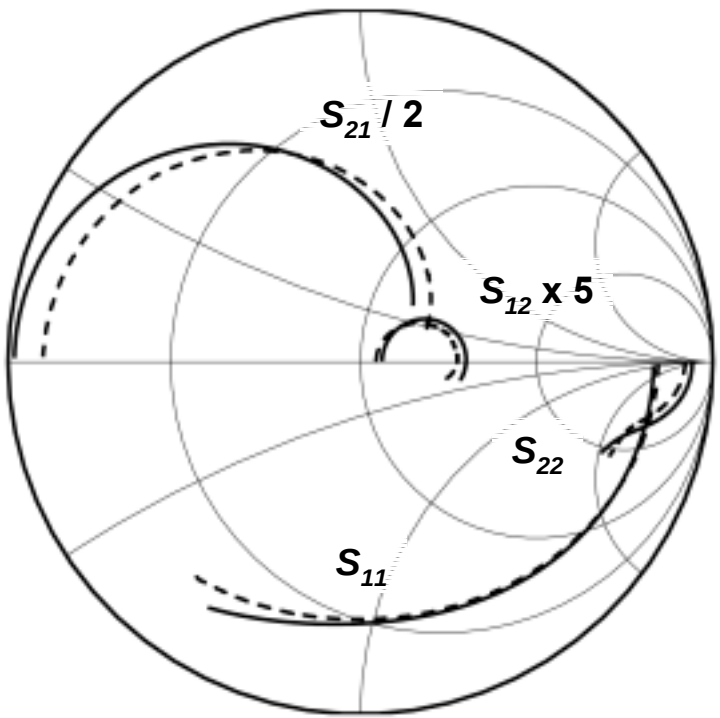
Y-parameters that accurately represent the transistor require prior knowledge of the model

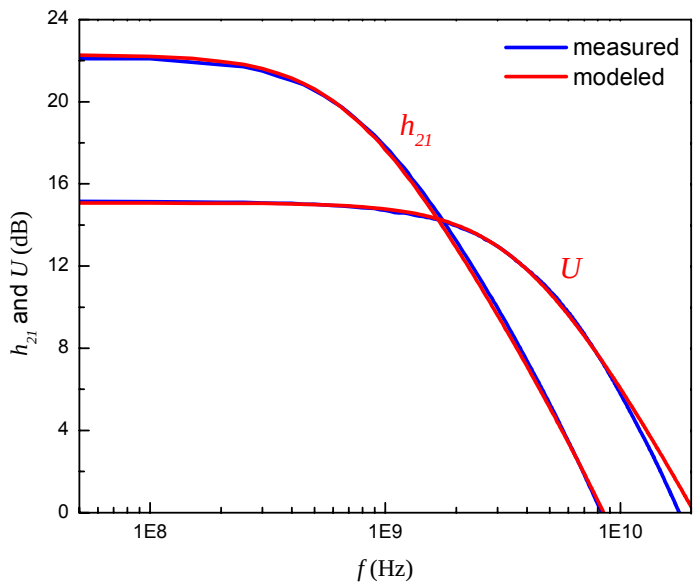


Device Model

Using measured characteristics (R_B, R_E, β_o, g_m) and initial estimates of other characteristics (r_{BC}, C_{BC}, C_x) a **simple model** was generated

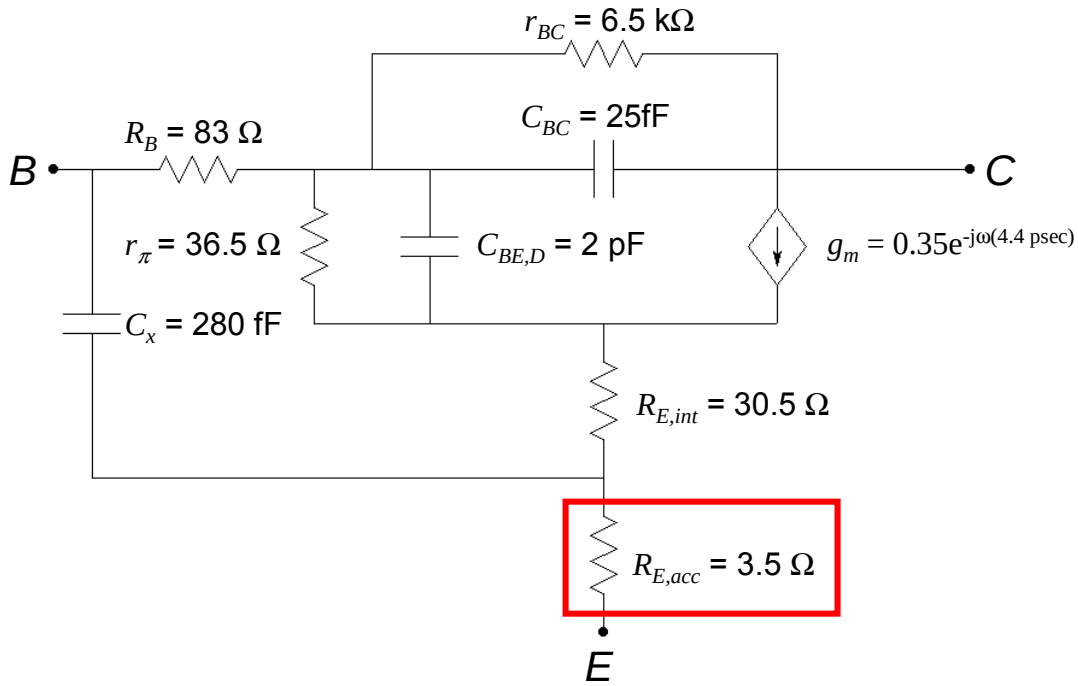


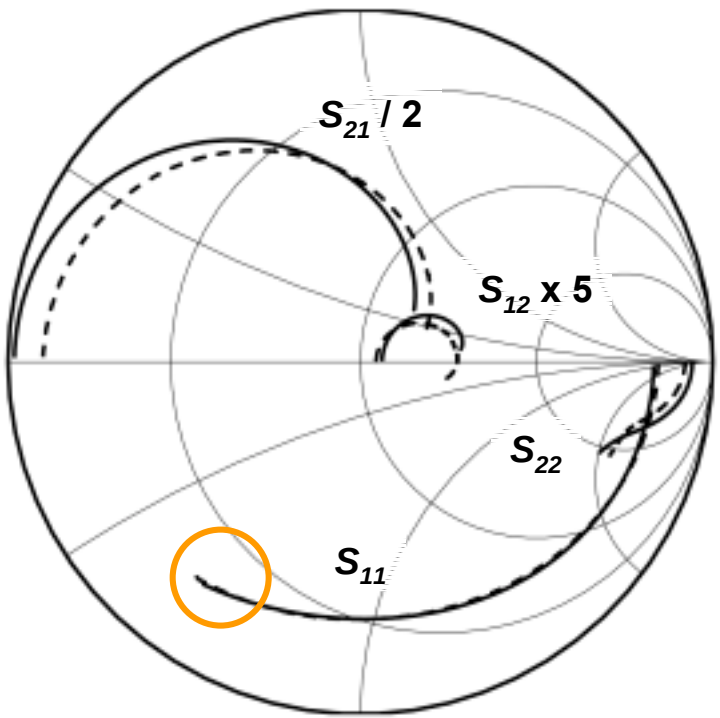


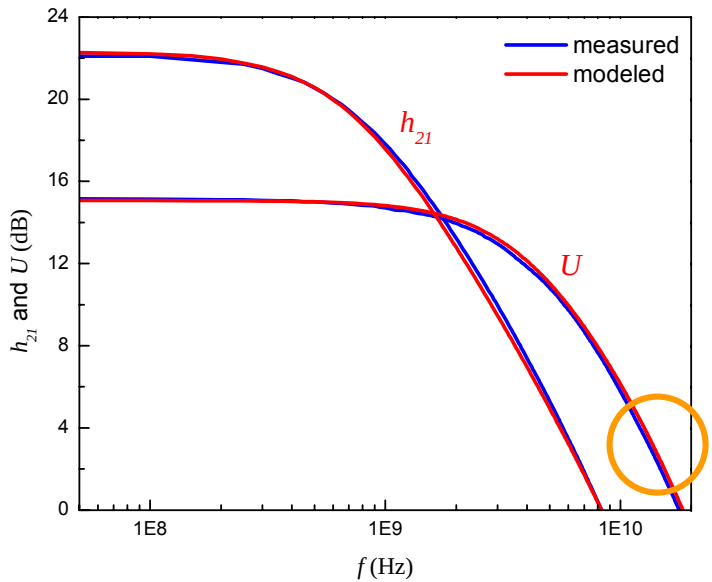


Modified Device Model

A model which includes the **lateral emitter access resistance** ($R_{E,acc}$)results in a slightly more accurate model

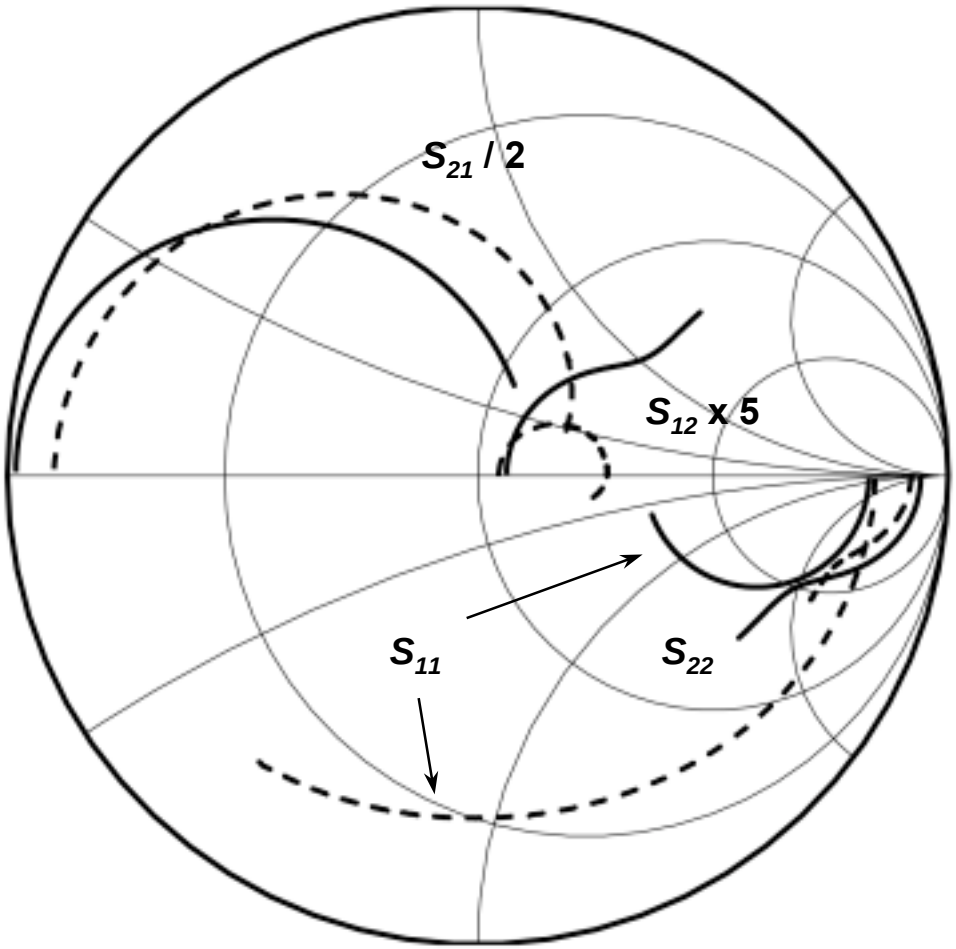


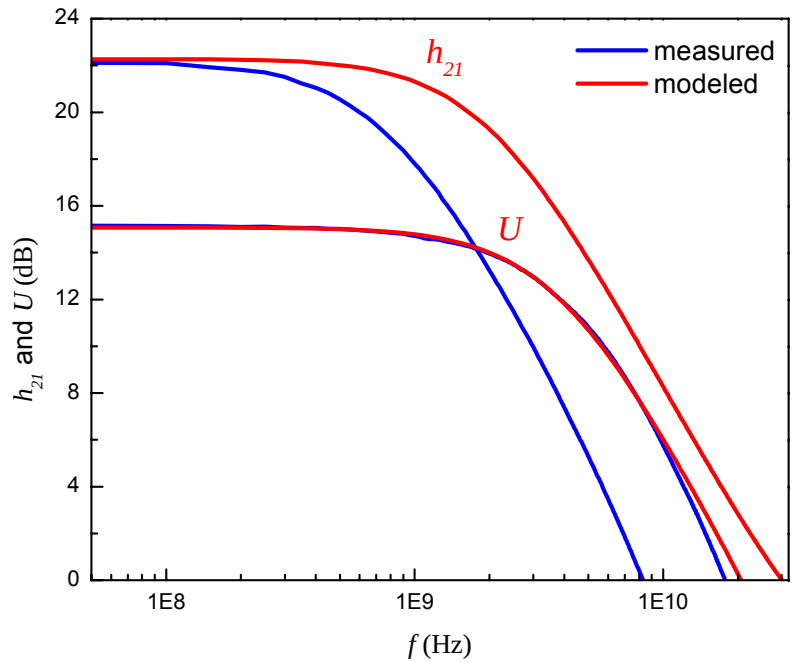




Model without C_x

Removal of the parasitic capacitance radically affects the S-parameters, resulting in a marked increase in f_τ with a minimal perturbation in f_{max}





Overview

Introduction

Transistor Design and Growth

- Growth as related to bipolar transistors
- Growth of $GaAs_{0.49}Sb_{0.51}$, $AlAs_{0.56}Sb_{0.44}$, and $Al_xGa_{1-x}As_ySb_{1-y}$
- n-type doping of arsenide-antimonides

Oxide Aperture Diodes

- Current density: area versus perimeter
- Aperture placement
- Diode Selection Rules

Oxide Aperture HBTs

- Generation Ø
- Generation I
- Generation II
- RF results

Conclusions and Future Work

Conclusions

The **validity and application** of the oxide aperture HBT design for high maximum frequency of oscillation (f_{max}) was examined

The work culminated with the fabrication of an oxide aperture HBT with an f_τ on the order of 8 ~ 10 GHz and f_{max} of 12 ~ 17 GHz, with the maximum measured f_{max} being **17.76 GHz**

Two critical aspects concerning the design and fabrication of the oxide aperture HBT became apparent:

(*1*) The **impact of the oxide aperture** on the DC operation of the BE junction and thereby the HBT

"The Three Bears"

(*2*) The **effect of the parasitic BE capacitance** on the high-frequency performance of the HBT

$$f_{\tau,x} = \frac{1}{2\pi}\left[\tau_{\tau,std} + \left(\frac{\eta V_T}{I_C} + \frac{R_B}{\beta_o} + R_E\right)C_x\right]^{-1}$$

Future Work

The research presented here represents a foundation

Suggested areas of research:

sub-micron scaling

for reduced base-collector capacitance and increased f_{max}

bandgap graded base layers

for reduced base transit times and increased f_{τ}

Specific areas that **must** be examined in future research:

(*1*) collector design

for reduced output conductance and increased common-emitter breakdown

(*2*) base-emitter junction optimization

for reduced emitter resistance and improved performance

(*3*) self-limiting oxidation

for sub-micron scaling and reduced parasitic base-emitter capacitance

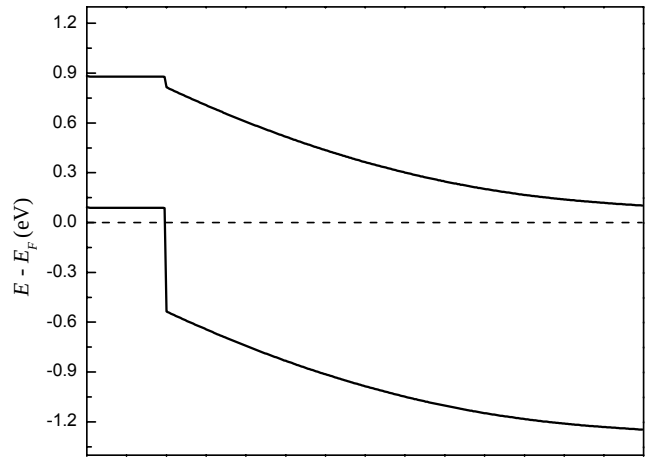
Future Work

collector design

The high output conductance in the devices in this work were attributed to **impact ionization** in the **InGaAs collector**

A simple solution is to use an **InP collector**

Experiments by other groups have shown devices fabricated with this BC combination have **increased output resistances** and **breakdown voltages**



base-emitter junction design

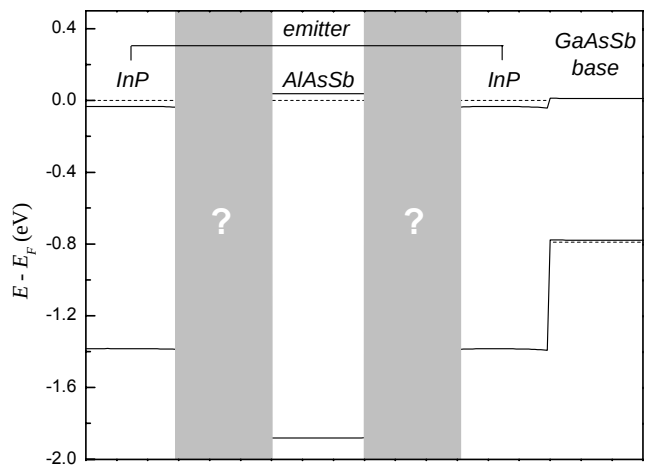
The BE junction in this work is not the optimum design

High R_E due to **low mobility AlAsSb** in the emitter

Alternatives:

InP-based emitter

Alternative oxide source material: **AlInAs**

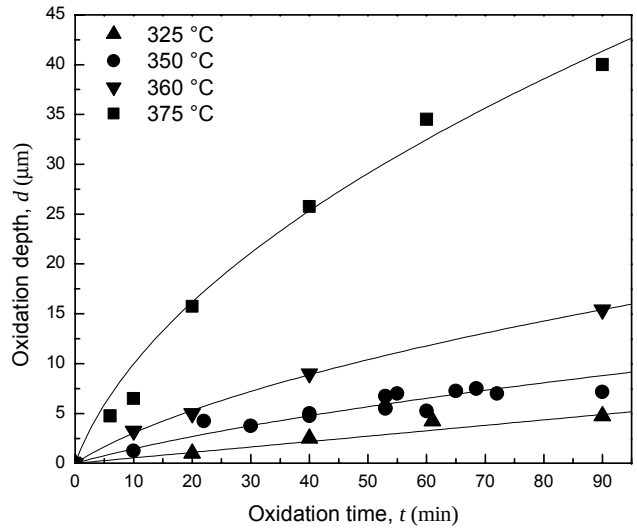


self-limiting oxidation

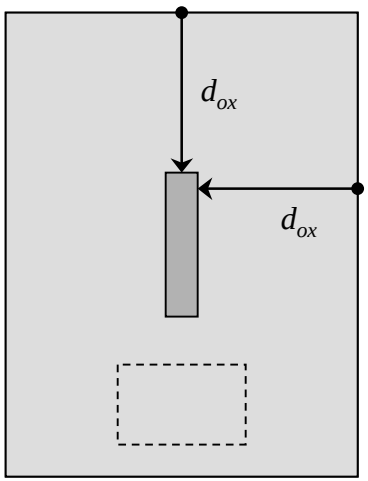
The only means to control oxidation depth currently is **time and temperature**

As a result, the oxide depth is **equidistant** from the outside edge of the oxidation mesa

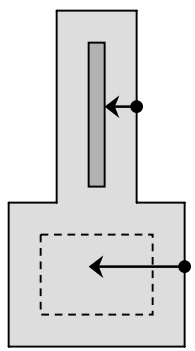
This required the base mesa to be **similar to and centered on** the collector mesa



oxide aperture HBT



conventional HBT



Possible Solutions

Stress/Strain Engineering:

By inducing strain selectively under the collector, it may be possible to alter the oxidation conditions

Selective Disordering:

By generating disorder only outside of the collector, it may be possible to increase the oxidation outside of the collector