Oxidation Control of GaAs/AlGaAs/InGaAs pHEMT for High Efficiency and Low Voltage Wireless Applications

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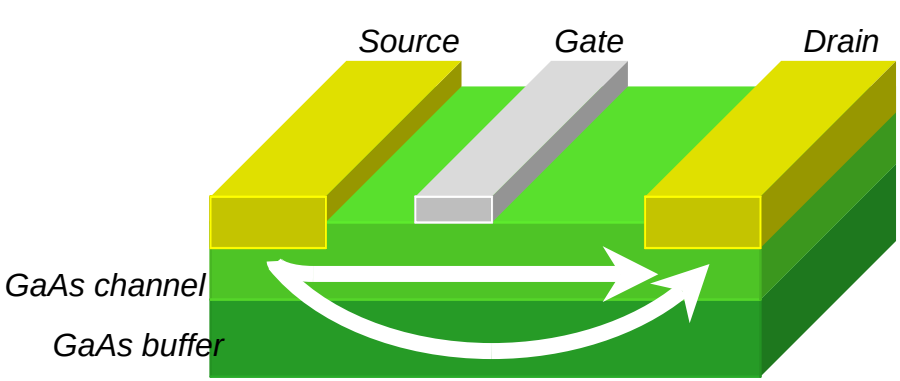
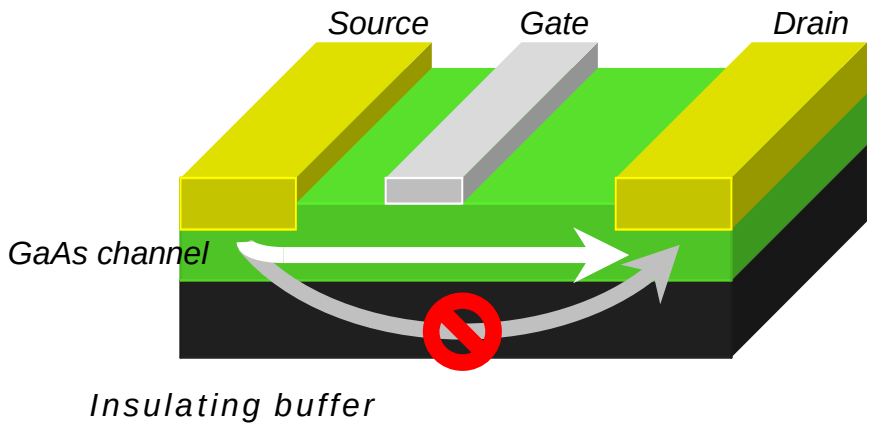
GaAs on Insulator (GOI)



Conventional FET



GOI FET

Advantages of GaAs On Insulator (GOI):

- **Elimination of substrate leakage current**
- **Reduced output conductance**
- **Excellent charge control**
- **High efficiency**

Insulating buffer can be obtained by the lateral wet oxidation of $Al_{0.98}GaAs$ layer

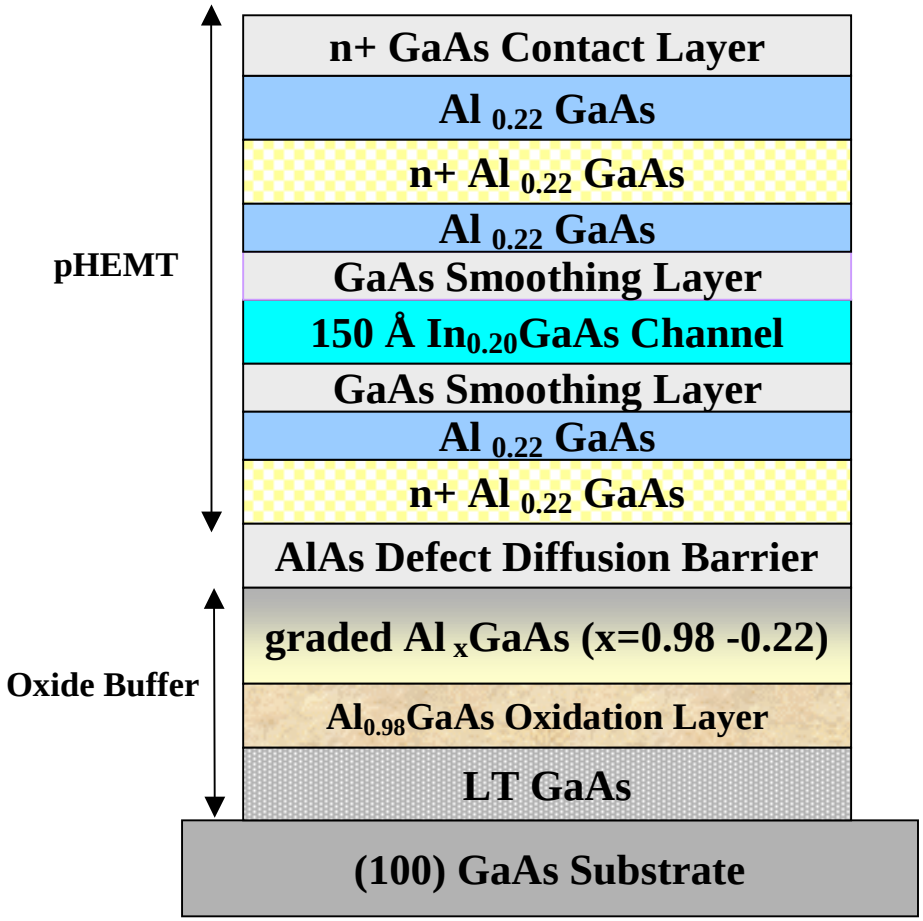
GOI pHEMT

Advantages of GaAs On Insulator (GOI):

- **Elimination of substrate leakage current**
- **Reduced output conductance**
- **Excellent charge control**
- **High efficiency**

Advantages of pHEMT:

- **Higher mobility of InGaAs channel**
- **Increased sheet carrier concentration due to the large conduction band discontinuity between InGaAs/AlGaAs**
- **Superior power and efficiency performance**
- **low noise**

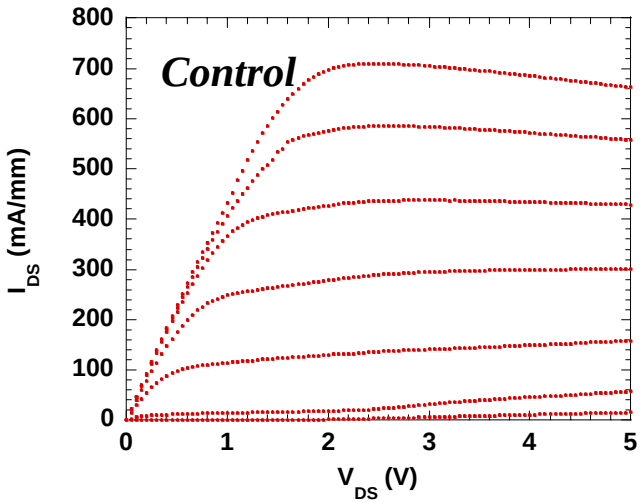


MBE Grown GOI pHEMT Structure

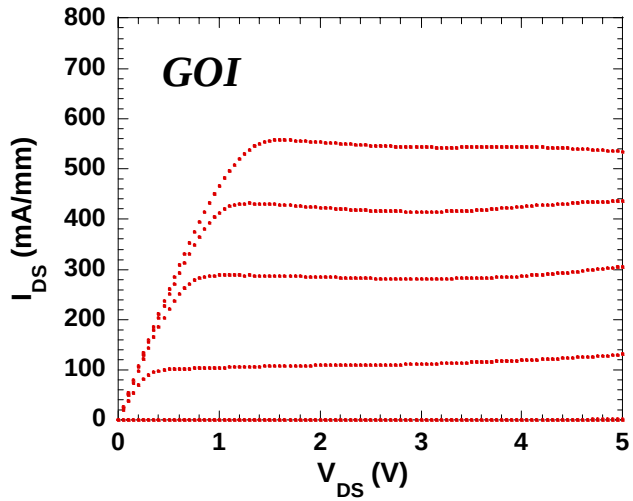
DC I-V Characteristics of Fully Oxidized GOI & Control pHEMTs

GOI and Control pHEMTs: 0.7 µm long, 150 µm wide

Vgs = 0.5 to – 2.5V, step = 0.5 V

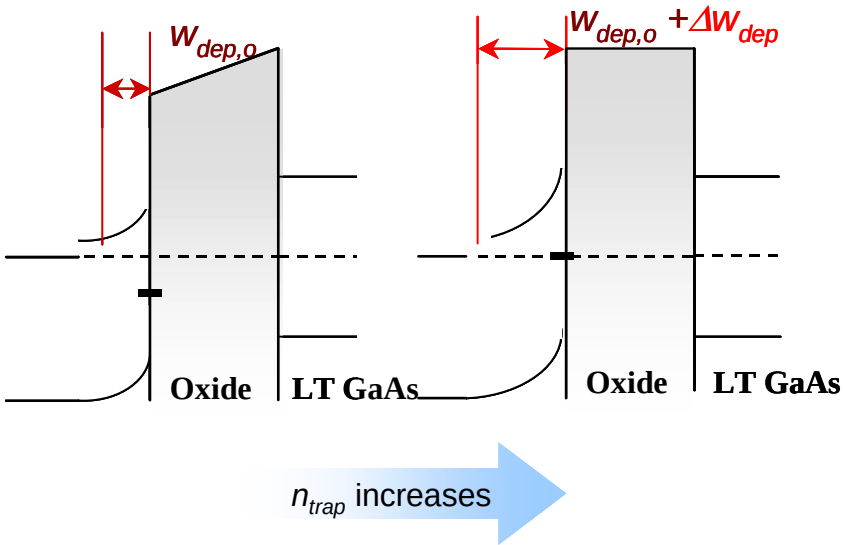


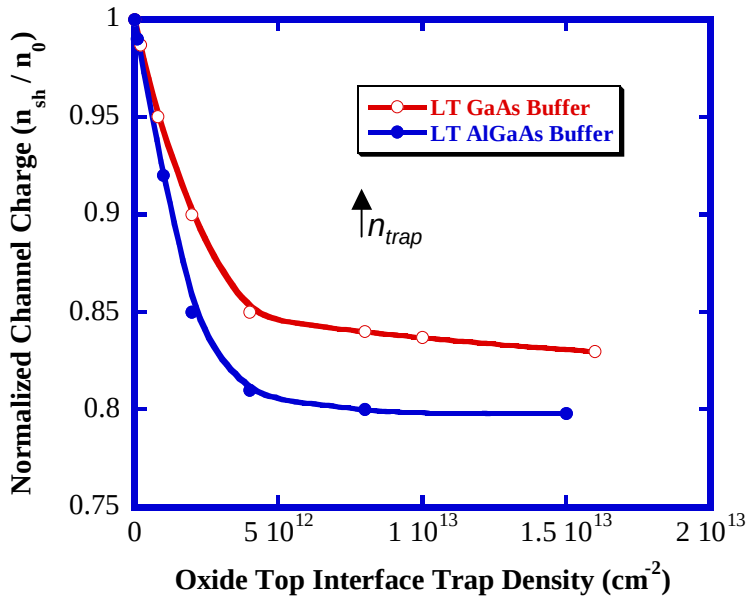
Vgs = 0.5 to – 2.5V, step = 0.5 V



- **I_{DSS} (GOI) ~ 436 mA/mm, I_{DSS} (Control) ~ 586 mA/mm.**
- **Decreased current level in fully oxidized GOI sample is due to back depletion from high defect density oxide-semiconductor interface and charge compensation.**

The Effect of Traps: Back Depletion





- 1D Poisson simulation indicates more charge loss with increased oxide-semiconductor interface defect density, causing up to 20% charge loss for GOI MESFETs grown on LT AlGaAs or GaAs buffer.

- MESFETs grown on LT GaAs buffer shows charge loss up to 30 ~ 40% after the oxidation.

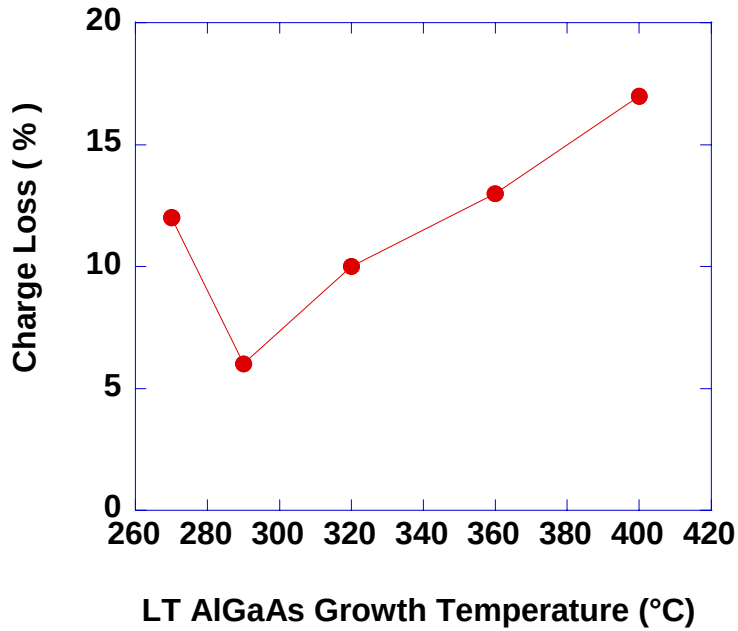
- Additional charge loss can be contributed to charge compensation during the oxidation process.

Minimize Charge Loss by Growing LT AlGaAs Buffer

Charge Loss of fully oxidized GOI MESFET

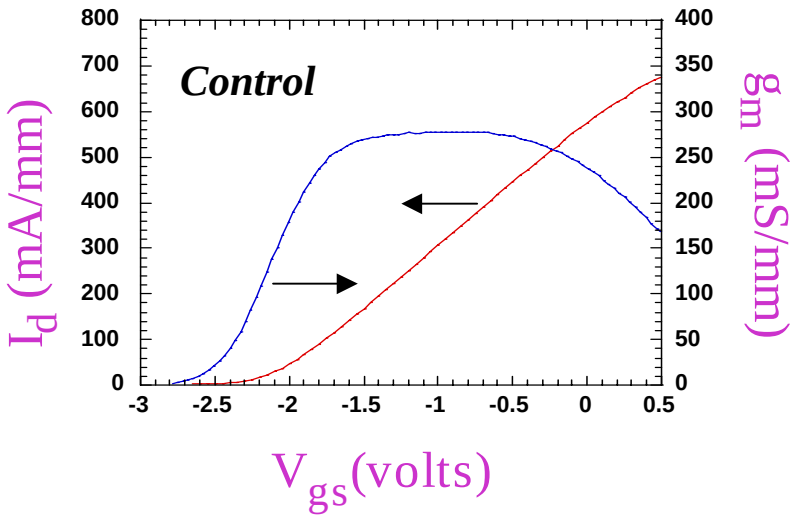
- **GOI MESFET directly grown on GaAs substrate: 80%.**
- **GOI MESFET on LT Grown GaAs buffer (Tg = 270 ºC): 35 ~ 40%.**
- **GOI MESFET on LT $Al_{0.3}Ga_{0.7}As$ buffer (Tg = 270 ~ 400 ºC): 6 ~ 17 %**

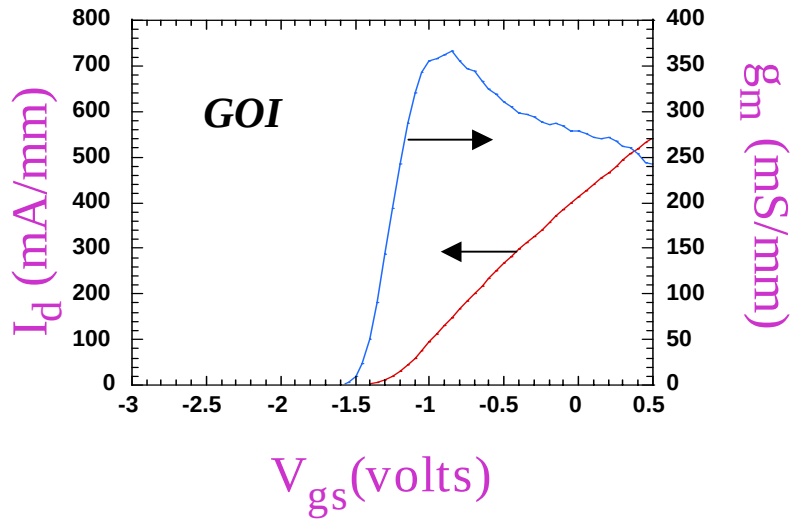
The growth and anneal temperature of the LT $Al_{0.3}Ga_{0.7}As$ buffer is critical to obtain the minimized charge loss.



g_m Characteristics of Fully Oxidized GOI & Control pHEMTs

GOI and Control pHEMTs: gate 0.7 µm long, 150 µm wide, V_{ds} = 2.5 V

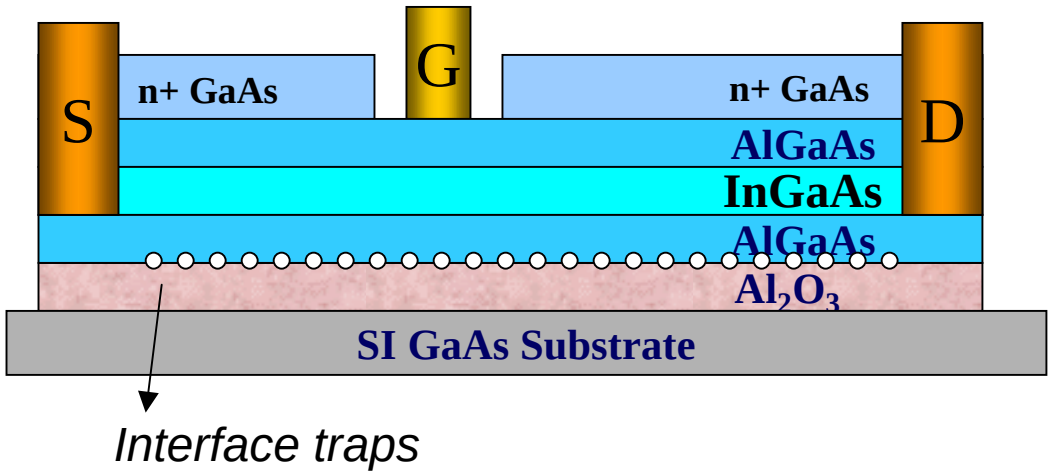


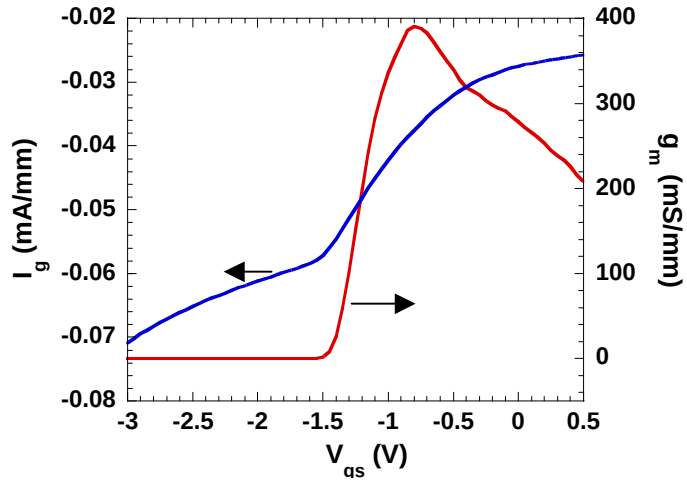


- **g_m(GOI) ~ 366 mS/mm, g_m (Control) ~ 280 mS /mm**
- **GOI sample has sharper turn-on and higher g_m near pinch-off**
- **g_m peaking was observed for GOI pHEMT due to impact ionization**
- **Control sample showed constant g_m curve**

$$g_m = C_g \frac{v_s}{l} = \frac{\varepsilon}{d} \bullet \frac{v_s}{l}$$

g_m peaking in Fully Oxidized GOI pHEMT

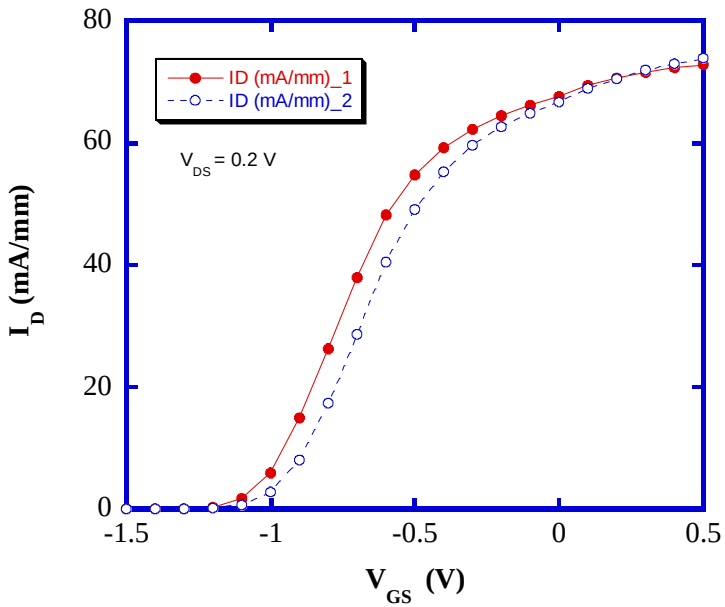




- Traps are generated during the oxidation process at the oxide semiconductor interface and in the adjacent layers.
- Impact ionization of the traps underneath the gate by hot electrons can take place at substantially lower drain bias compared to the electron-hole pair generation by band to band ionization.
- Electrons removed from the deep levels shift the threshold voltage to the negative direction, therefore causing the increase in current.

Gain peaking is attributed to an increase in drain current induced by trap-related threshold voltage shift.

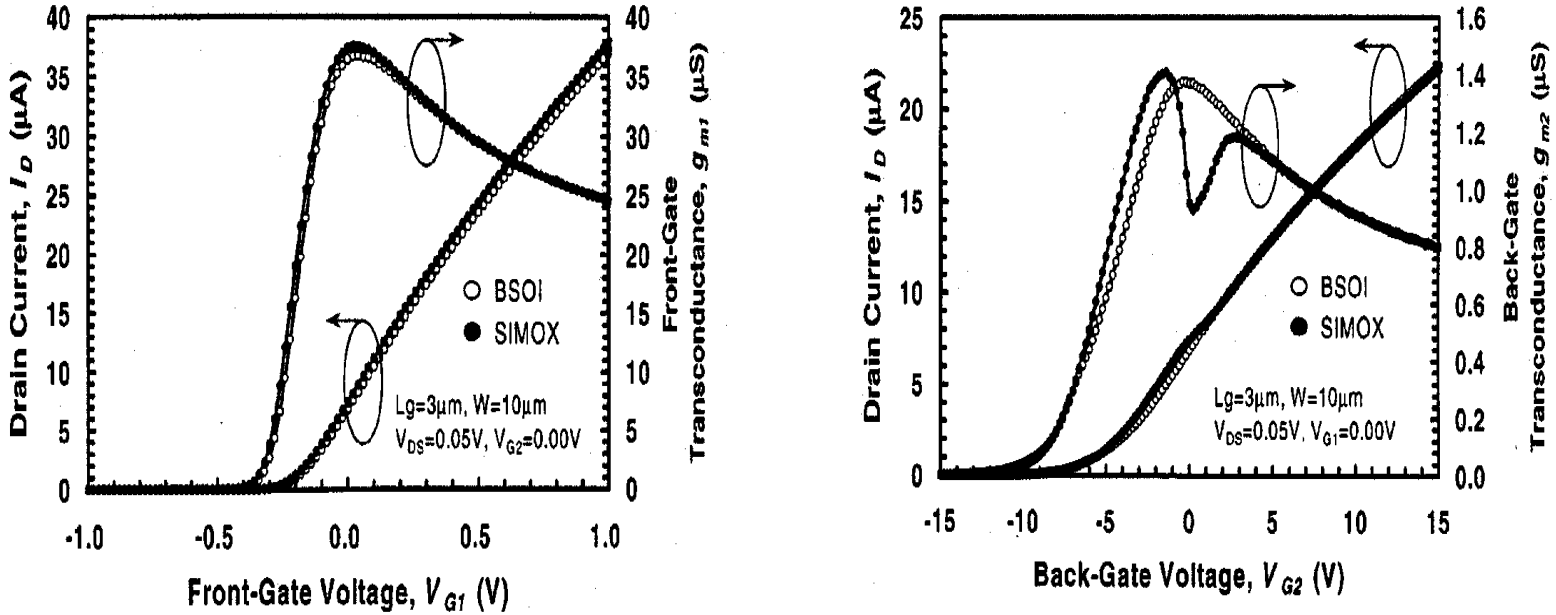
Threshold Voltage Shift in GOI pHEMT



Threshold Voltage of GOI pHEMT before and after high bias applied.

- The threshold voltage of a GOI pHEMT was measured in the dark at a low V_{DS} of 0.2V.
- The 80mV threshold voltage shift toward the positive voltage direction was observed after up to 5V V_{DS} applied to the GOI pHEMT.
- The threshold voltage shift can be contributed to the negatively charged trap states underneath the gate.

Transconductance Characteristics in SOI MOSFET's

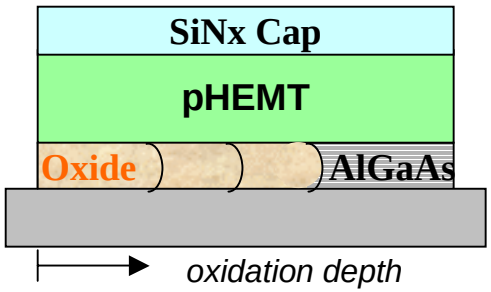


Front gate and back-gate characteristics in NMOS SOI transistors for both high-does SIMOX wafers or BSOI wafers

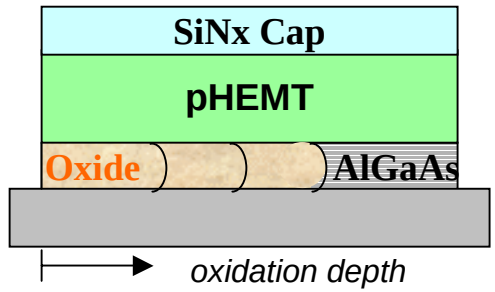
- *The rapid kink phenomenon has been contributed to the presence of energetically – localized trap states at SOI/BOX interface.*

Takeo Ushiki, Koji Kotani, et al. IEEE Transactions on Electron Devices, Vol. 47, 2000, P360

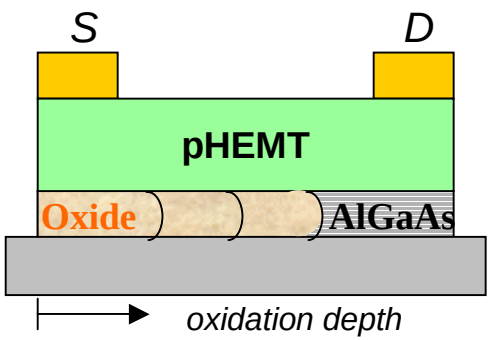
Partially Oxidized pHEMT Process Flow



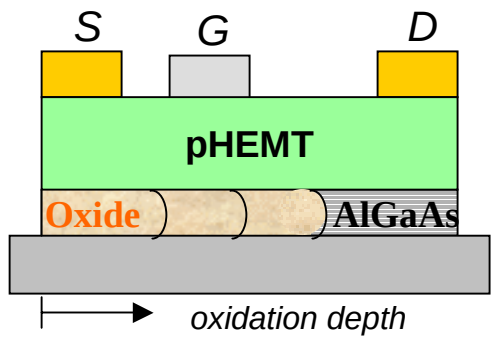
1. Controlled Wet Oxidation of AlGaAs



2. Anneal (600°C/3min)

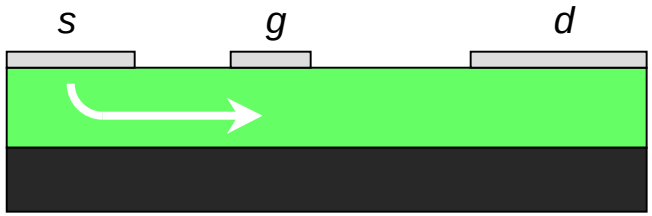


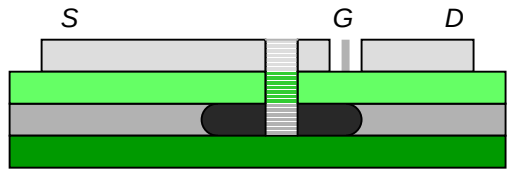
3. Mesa Isolation and S/D Ohmic Contact



4. Gate recess etch and gate metallization

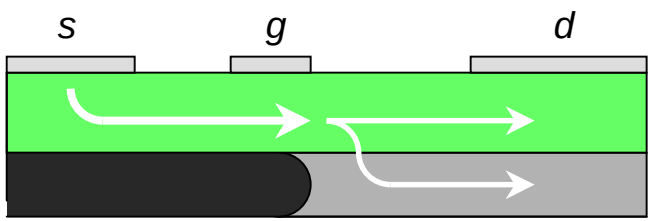
Partially Oxidized pHEMTs





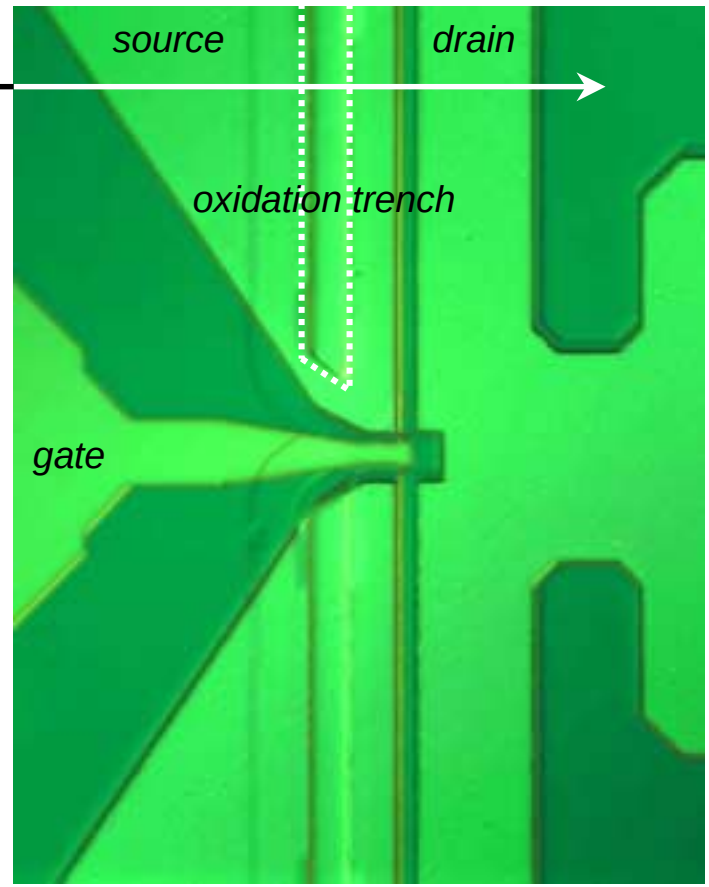
Fully oxidized devices

- *Truly insulating buffer*
- *charge loss*
- *g_m peaking*

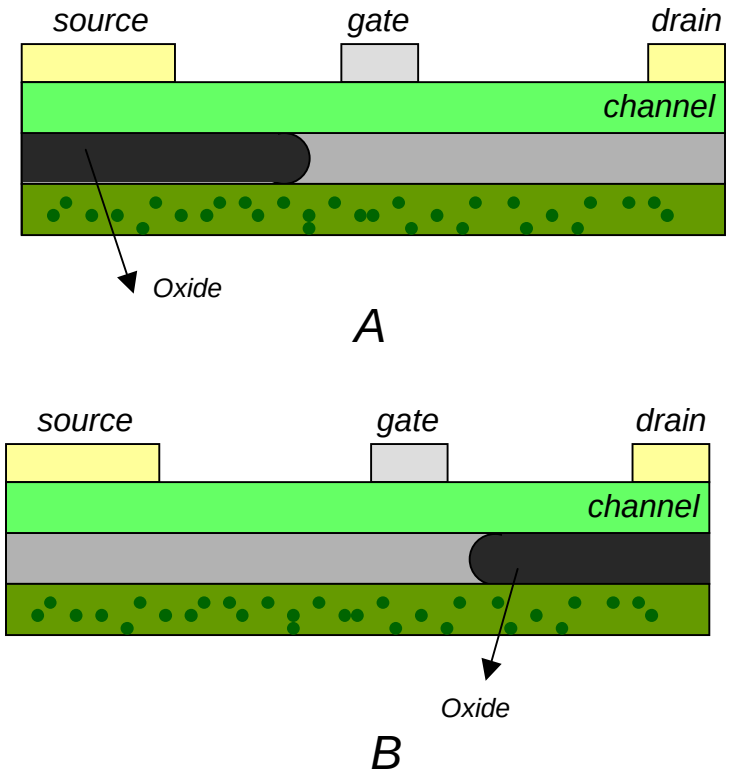


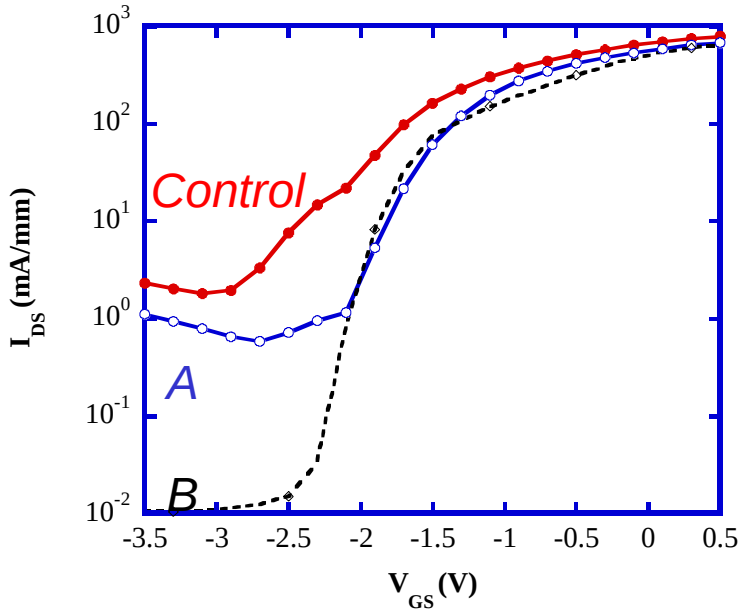
Partially oxidized devices

- *insulating buffer underneath the source*
- *reduced charge loss*
- *no g_m peaking*



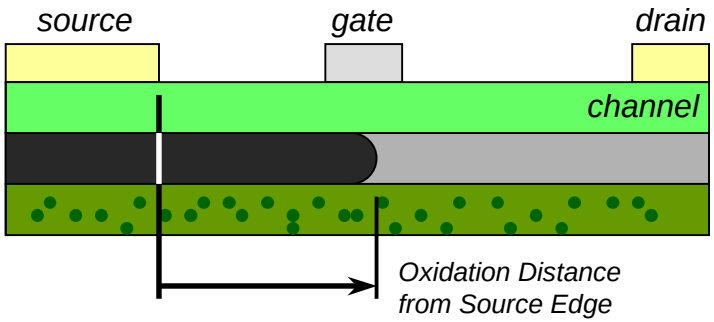
Subthreshold Leakage Current





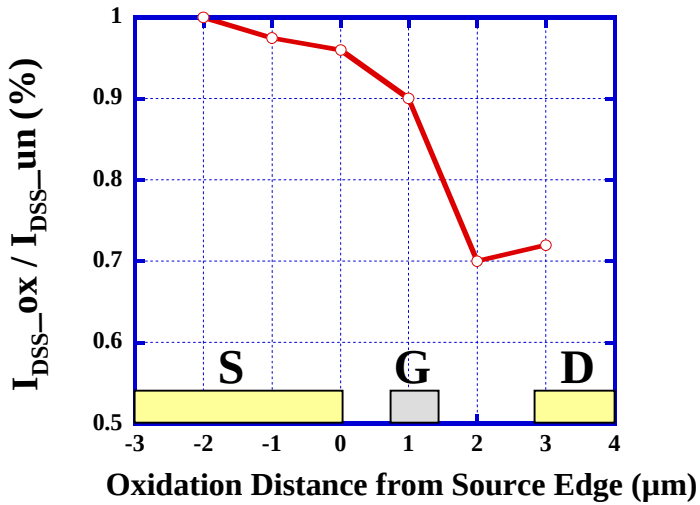
Partially oxidized pHEMT can effectively block the subthreshold leakage current compared with the un-oxidized control sample, especially when the high field drain side of the gate edge is blocked by the oxide.

Partially Oxidized & Control pHEMTs DC Characteristics

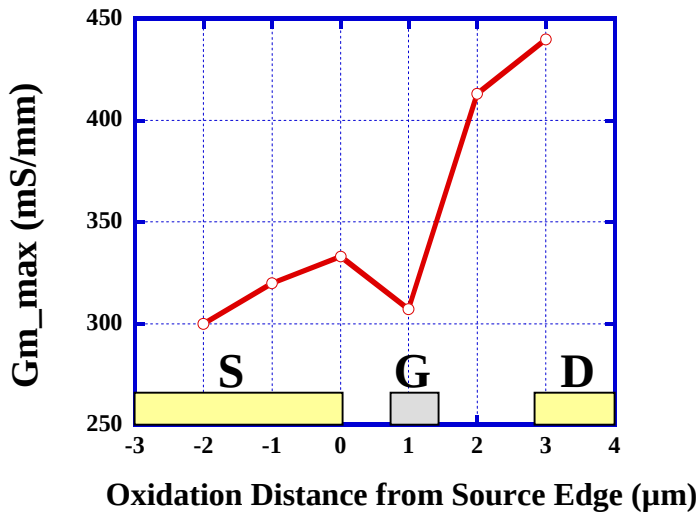


GOI and Control pHEMTs: gate 0.7 µm long, 150 µm wide

- ***Hall measurement shows charge density of 3.54 x 10^{12}/cm^2 and mobility of 6467cm^2/(v.sec)***
- ***Oxidation conditions : 400ºC, 30 minutes, oxidation depth 5 µm***
- ***Charge loss up to 30% for fully oxidized sample was observed***
- ***High g_m peaking was observed for samples with the oxide extending beyond the drain edge of the gate***

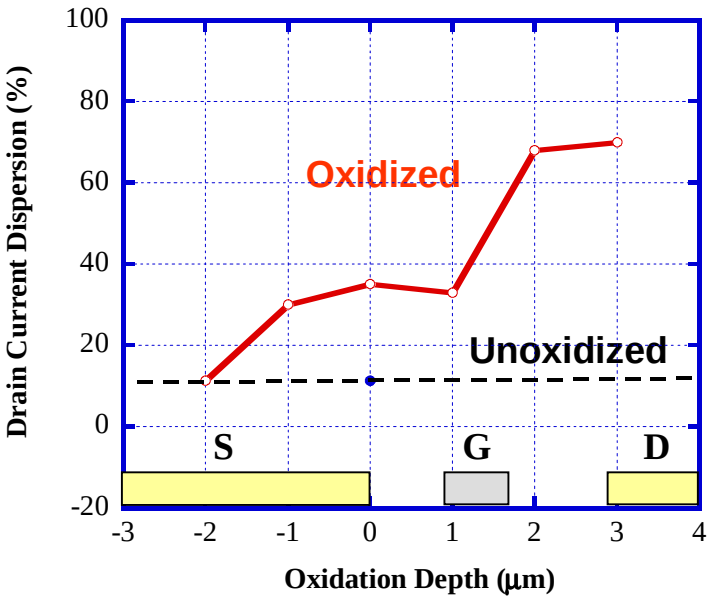


I_{DSS}_unoxidized = 667 mA/mm

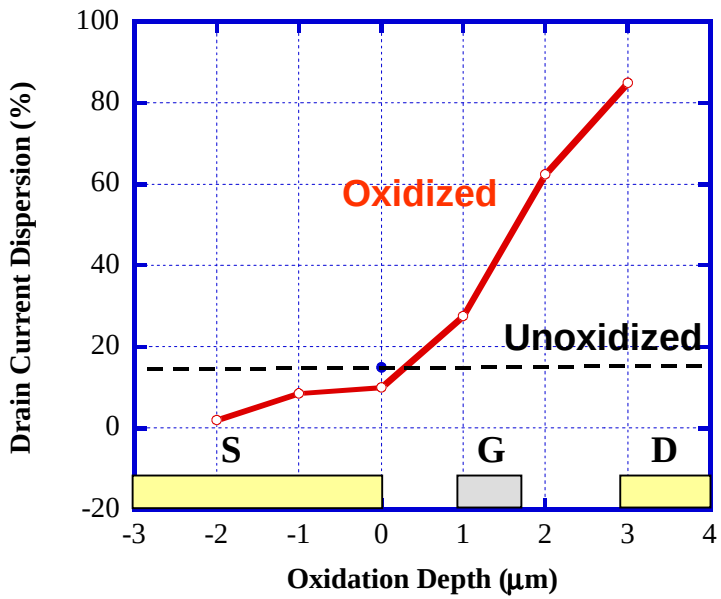


Gm_max_unoxidized = 341 mS/mm

Dispersion in Partially Oxidized pHEMTs



LT GaAs buffer *(001235_2)*

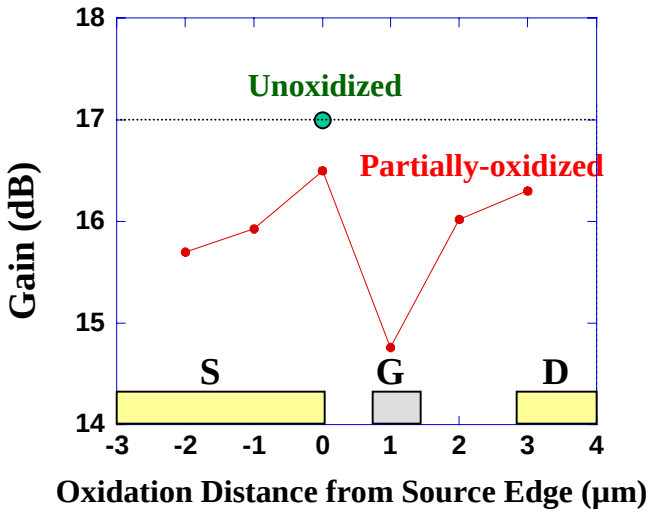


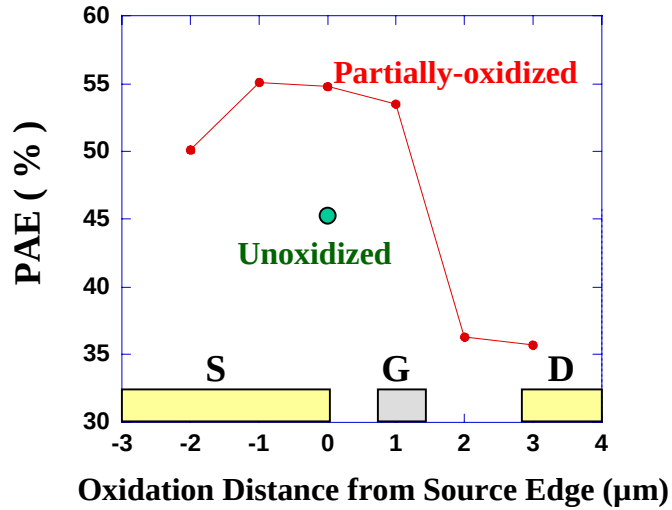
LT AlGaAs buffer *(010882_2)*

Serious dispersion was observed for the pHEMTs with oxide extending beyond the gate region. The pHEMTs with an LT AlGaAs buffer showed lower dispersion compared to the pHEMTs with an LT GaAs buffer when oxide is around the source region.

Submicron GOI & Control pHEMTs RF Characteristics

GOI and Control pHEMTs: gate 0.7 µm long, 150 µm wide





- *ATN loadpull measurement: 8 GHz, Class AB bias, 3.5 V V_{DS}*
- *Lower gain is observed for the partially oxidized sample due to the reduction in channel charge after the oxidation*
- *Highest power added efficiency was observed for samples with oxide front terminated around source edge due to decreased subthreshold leakage current*
- *RF measurement is limited by the available matching states of our Loadpull system*

Conclusions

- Oxidized $Al_{0.98}Ga_{0.02}As$ offers an insulating buffer for MESFETs and pHEMTs, increasing the efficiency of the device.
- Partially oxidized devices retain the benefits of the oxide buffer, while not suffering as greatly from the charge loss problem.
- Partially oxidized pHEMTs with oxidation stopped around the source region showed improved power added efficiency at low power supply.
- Transconductance peaking due to impact ionization of the traps underneath the gate was observed when oxide extended beyond the gate.
- Serious dispersion was observed for the pHEMTs with oxide extending beyond the gate region. The pHEMTs with an LT AlGaAs buffer showed lower dispersion compared to the pHEMTs with an LT GaAs buffer when oxide is around the source region.