Oxidation Control of GaAs pHEMTs for High Efficiency Applications

C. Zheng, R. Coffie, D. Buttari, J. Champlain, U. K. Mishra

Abstract

In this paper, for the first time, an investigation of partially oxidized GaAs-on-insulator (GOI) AlGaAs/InGaAs/GaAs pseudomorphic HEMTs is reported. Fully oxidized pHEMTs demonstrated minimized substrate leakage current, high output impedance, but suffered from 30 ~ 40% charge loss. Fully oxidized devices also showed transonductance peaking that could be removed by controlled partial oxidation. Partially oxidized pHEMT devices showed improved power added efficiencies (PAEs) at a low supply voltage of 3.0 V compared to fully oxidized or unoxidized devices and negligible charge loss (<10 %).

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I. INTRODUCTION

High efficiency components are key elements of solid state amplifiers for wireless application. Portable applications require reduced supply voltages to minimize weight and size, and enhanced efficiency to ensure long battery lifetime. GOI MESFET technology has been shown to provide ultrahigh efficiencies [1]. This was due to the enhanced charge control provided by the GOI technology, which reduced the parasitic substrate leakage and increased transconductance near pinchoff as compared to a conventional MESFET. Extending the GOI technology to pHEMTs is of great interest since pHEMTs are widely used for low noise and high power applications in the microwave and millimeter wave frequency ranges due to their superior power, efficiency, and linearity performance.

Charge loss in fully oxidized GOI MESFETs, which has detrimental effects on current and output power, has been a serious problem for the practical application of GOI technology [2]. The charge loss was believed to be due to the depletion of charge by the high defect density oxide-semiconductor interface. The stresses developed as a result of the volume shrinkage of the oxidized layer, as well as As accumulation appear to contribute to the formation of defects close to the interface and in the layers adjacent to the oxide layer [3]. There are several ways to minimize the charge loss. It was observed that the presence of LT GaAs layer in the vicinity of the oxidized layer enhances the oxidation rate and develops better oxide/GaAs interfaces compared to reference samples without an LT GaAs layer [4,5]. A thin layer of AlAs can be used as a defect diffusion barrier above the oxidation layer to minimize the diffusion of point defects generated during the oxidation into the active channel region [6,7]. Partial oxidation of the active channel was explored here to take advantage of the insulating oxide buffer, while minimizing the charge loss.

II. EPITAXIAL STRUCTURE AND DEVICE FABRAICATION

The epitaxial structure of the double-side doped AlGaAs/InGaAs/GaAs GOI pHEMT is shown in Figure 1. The pHEMT material was grown by MBE on a semi-insulating GaAs substrate with the following growth sequence: a 2000Å GaAs buffer, a 2000Å low temperature (LT) GaAs grown at 270ºC, a 500Å $Al_{0.98}Ga_{0.02}As$ oxidation layer, a 150Å graded $Al_xGa_{1-x}As$ with Al composition (x) graded from 0.98 to 0.22, a 50Å AlAs defect diffusion barrier, a 100Å n^+ $Al_{0.22}Ga_{0.78}As$ bottom electron supply layer, a 20Å $Al_{0.22}Ga_{0.78}As$ / 20Å GaAs spacer, a 150Å $In_{0.2}Ga_{0.8}As$ channel, a 20Å GaAs / 20Å $Al_{0.22}Ga_{0.78}As$ spacer, a 150Å n^+ $Al_{0.22}Ga_{0.78}As$ top electron supply layer, a 150Å $Al_{0.22}Ga_{0.78}As$ barrier, a 30Å AlAs etch stop layer, a 200Å n^+ GaAs Ohmic contact layer. The growth was finished with a 50Å AlAs etch stop layer and a 200Å GaAs layer to protect the sample surface during the oxidation process. Hall measurement showed an electron sheet charge density of 3.5 x $10^{12}/cm^2$ and a mobility of 6467 $cm^2/V{\cdot}s$ at room temperature after the removal of the n^+ GaAs Ohmic contact layer.

GOI pHEMT process flow is similar to the conventional FET process with an additional oxidation process. First a 2000Å Si_xN_y mask is deposited by PECVD, then patterned, and selectively removed using a CF_4 based RIE etch. Next a Cl_2 based RIE etch is used to open the oxidation window in the exposed semiconductor surface to allow lateral oxidation of the $Al_{0.98}Ga_{0.02}As$ layer from the sidewall [8]. The oxidation was carried out at 400ºC with N_2 bubbling through 80ºC DI water. After oxidation, the sample was annealed at 600ºC for 3 minutes to annihilate point defects generated during the oxidation process. The Si_xN_y mask was then completely removed. Mesa isolation was obtained by a Cl_2 based RIE etch. Ni/AuGe/Ni/Au were deposited for the source/drain ohmic contacts and annealed at 430ºC for 30 seconds. Finally, a 0.7 μm long gate was defined and a single recess to remove the n^+ GaAs was

performed using a citric acid based selective wet etch. Ti/Pt/Au gate metals were deposited to complete the GOI pHEMT process.

III. RESULTS AND DISCUSSION

Fully oxidized pHEMTs and unoxidized control sample were fabricated at the same time. Low subthreshold leakage current, sharp transconductance turn on near pinch-off and high output impedance were observed for fully oxidized GOI pHEMTs due to the introduction of the insulating oxide buffer. But compared with the unoxidized devices, fully oxidized pHEMTs showed transconductance peaking up to 50% near pinch off voltage (see Figure 2), as well as charge loss up to 30% due to back depletion from the oxide-semiconductor interface. Gain peaking could be due to an increase in drain current induced by threshold voltage shift. The threshold voltage shift is attributed to impact ionization of the traps underneath the gate by hot electrons, which can take place at substantially lower drain bias compared to the electron-hole pair generation by band to band ionization [9]. Electrons removed from the deep levels shift the threshold voltage to the negative direction, therefore causing the increase in current [10]. This is analogous to the phenomena responsible for the kink effect in SOI MOSFETs [11]. In this study partial oxidation was investigated to minimize the charge loss and gain peaking associated with the fully oxidized pHEMTs.

A series of partially to fully oxidized pHEMTs were fabricated with the edge of oxidation front varying from below the source contact to beyond the drain contact. The unoxidized pHEMTs was also fabricated on the same wafer. The extent of the oxide formed by lateral wet oxidation of the AlGaAs underneath the device active region was controlled by varying the distance between the edge of the oxidation window and the source contact edge as shown in Figure 3. It was found that the largest transconductance peaking and charge loss occurred for

devices with an oxidation front extending beyond the gate region (Figure 4 (1)). This is consistent with the threshold voltage shift due to impact ionization of traps underneath the gate as the cause for the transconductance peaking. Devices with the oxidation front stopped around the source edge showed flat transconductance curves and negligible charge loss of less than 10%. An ATN load-pull system was used for the large signal continuous-wave (CW) measurements at 8 GHz and devices were tuned for maximum efficiency. As shown in Figure 4 (2), improved power added efficiencies (PAEs) as high as 55% have been achieved with class AB bias condition. The associated power gains were around 15 to 17 dB at a low V_{DS} bias of 3.0V. Repeated experiments of various pHEMT samples showed improved PAE by 5 ~ 10% for partially oxidized samples with oxidation front stopped around the source edge compared with an un-oxidized control sample. The improved PAE can be contributed to decreased substrate leakage current and improved g_m near pinch-off. These preliminary results indicated partially oxidized pHEMTs are promising for high efficiency and low voltage wireless application.

IV. CONCLUSION

In conclusion, low subthreshold leakage current, sharp transconductance turn on near pinch-off and high output impedance were observed for fully oxidized GOI pHEMTs due to the introduction of the insulating oxide buffer. Fully oxidized pHEMTs suffered from transconductance peaking and charge loss up to 30%. Partially oxidized pHEMT devices still benefited from the insulating oxide buffer and showed improved power added efficiency (PAE) with oxidation front stopped around the source edge at a low supply voltage of 3.0 V and negligible charge loss.

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Figure Captions

Figure 1 The epitaxial structure of the double-side doped GaAs on Insulator (GOI) AlGaAs/InGaAs/GaAs pHEMT.

Figure 2 Drain current and transconductance versus gate bias at 2.5V drain bias of (1) an un-oxidized sample with a maximum g_m of 280 mS/mm and (2) a fully oxidized sample with a peaked transconductance as high as 370 mS/mm near the pinch off voltage.

Figure 3 The pHEMT device layout and cross-section.

Figure 4

(1) Normalized I_{DSS} and maximum transconductance at 2.5V V_{DS} of partially oxidized pHEMTs.

(2) Power added efficiency of pHEMTs at 8 GHz with a bias near class AB operation. The drain bias was 3.0V.

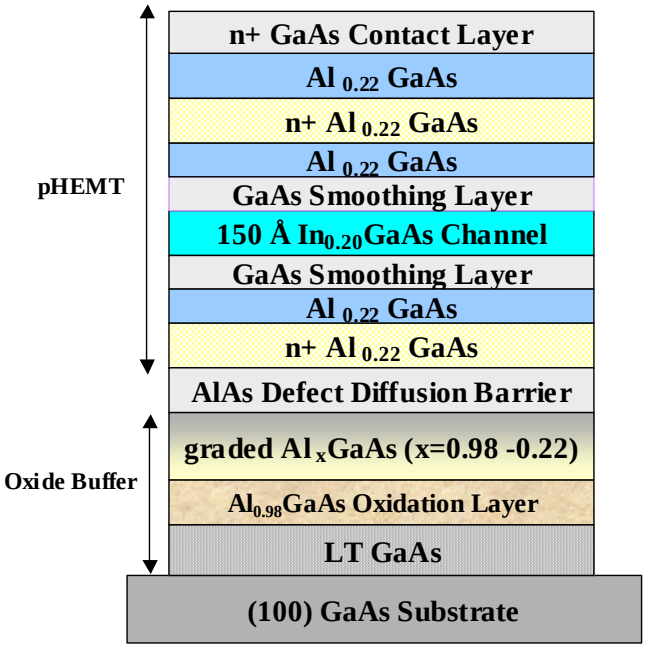
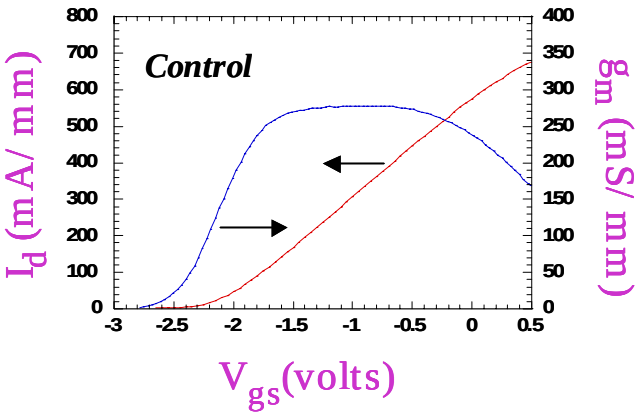
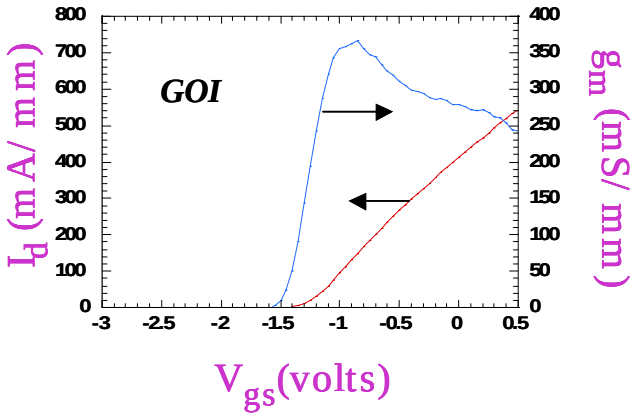

n+ GaAs Contact Layer
Al 0.22 GaAs
n+ Al 0.22 GaAs
Al 0.22 GaAs
GaAs Smoothing Layer
150 Å In0.20GaAs Channel
GaAs Smoothing Layer
Al 0.22 GaAs
n+ Al 0.22 GaAs
AlAs Defect Diffusion Barrier
graded AlxGaAs (x=0.98 -0.22)
Al0.98GaAs Oxidation Layer
LT GaAs
(100) GaAs Substrate
pHEMT
Oxide Buffer

Figure 1


Control
I_d (mA/ mm)
g_m (mS/ mm)
V_{gs}(volts)
800
700
600
500
400
300
200
100
0
400
350
300
250
200
150
100
50
0
-3
-2.5
-2
-1.5
-1
-0.5
0
0.5

(1)


GOI
I_d (mA/ mm)
g_m (mS/ mm)
V_{gs}(volts)
800
700
600
500
400
300
200
100
0
400
350
300
250
200
150
100
50
0
-3
-2.5
-2
-1.5
-1
-0.5
0
0.5

(2)

Figure 2

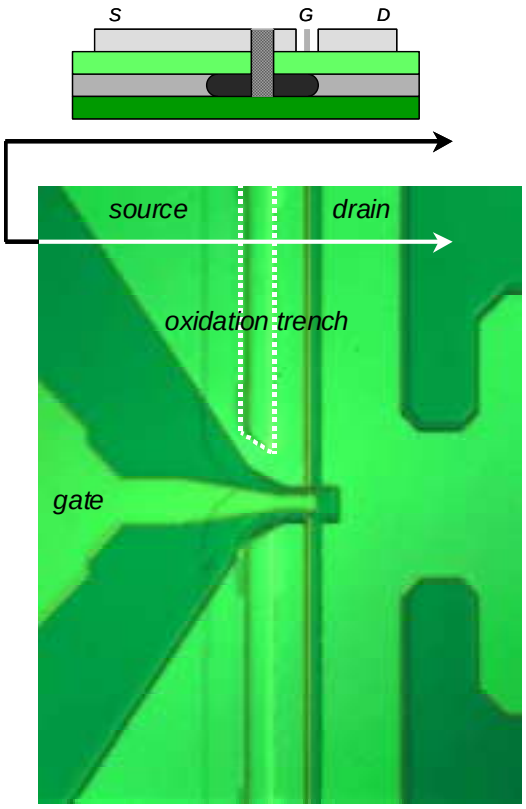
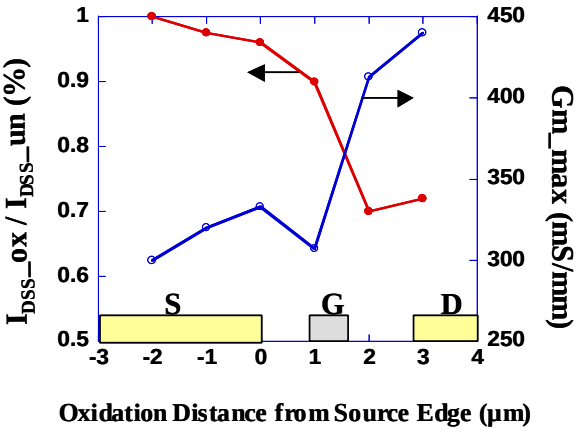
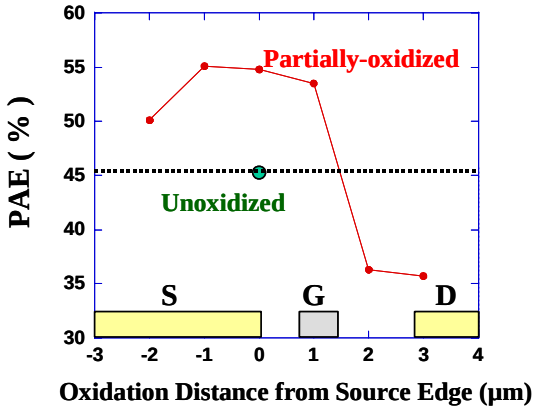


Figure 3


1
0.9
0.8
0.7
0.6
0.5
450
400
350
300
250
S
G
D
-3
-2
-1
0
1
2
3
4
I_{DSS_ox} / I_{DSS_un} (%)
Gm_max (mS/mm)
Oxidation Distance from Source Edge (µm)

(1)


60
55
50
45
40
35
30
Partially-oxidized
Unoxidized
S
G
D
-3
-2
-1
0
1
2
3
4
PAE (%)
Oxidation Distance from Source Edge (µm)

(2)

Figure 4

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Abstract

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Index Terms

Semiconductor defects, Impact ionization, Heterojunctions, MODFETs, Oxidation

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