University of California Santa Barbara

Lattice Engineered Substrates Using Lateral Oxidation of AlAs

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in
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by

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Abstract

Lattice Engineered Substrates Using Lateral Oxidation of AlAs

by Prashant Chavarkar

This thesis documents the invention, development and demonstration of a new approach to relaxed heteroepitaxy – the lattice engineered substrate (LES). This approach is based on the process of lateral oxidation of Al-containing III-V compound semiconductors. The process of lateral oxidation besides changing a crystalline semiconductor to an amorphous oxide, converts a rigid epitaxial interface to a porous oxide/semiconductor interface. This results in significant structural changes in the semiconductor structure. The most significant of these are the reduction in thickness of the oxidizing semiconductor and the relaxation of strain in lattice-mismatched (strained) semiconductor overlayer. This results in an epitaxial template with a different lattice constant that is mechanically supported on a commercially available binary III-V substrate, effectively generating a new (quasi)-substrate.

One of the main prerequisites for a lattice-engineered substrate is the growth of thick highly strained semiconductor overlayers (like InGaAs on GaAs) with a low threading dislocation density. This is achieved by growth at a low temperature and by maintaining the growth in a layer-by-layer mode. The strain relaxation in these overlayers upon lateral oxidation is dependent on the oxidation temperature and the lattice mismatch between the strained overlayer and the substrate. The enhanced strain relaxation upon oxidation is attributed to the stress generated during the lateral oxidation process and the removal of misfit dislocation segments at the strained overlayer – oxide interface.

The structural, electronic and optical properties of epitaxial layers grown on lattice-engineered substrates is sensitive to surface preparation

techniques that are used prior to regrowth. Pure thermal desorption of a lattice-engineered substrate that is protected with a thin GaAs cap layer was found to be the best technique. Epitaxial layers grown on lattice-engineered substrates had higher strain relaxation than those grown directly on GaAs substrates. InGaAs pn junction diodes grown on lattice-engineered substrates had lower reverse leakage current that can be attributed to lower dislocation density. The GaAs based lattice-engineered substrate technology enables the growth of high band-offset quantum wells, which are necessary for uncooled operation of long wavelength lasers. Room temperature photoluminescence was observed at 1.3 μm from InGaAs and GaAsSb based multiple quantum wells grown on GaAs lattice-engineered substrates.

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Chapter 1.
Introduction

1.1. Introduction

Information technology has played a major role in today's world. Electronic and optoelectronic systems based on semiconductor devices have made this possible. Increasing bandwidth and volume demands on these systems have been the driving force for continual improvement in semiconductor device performance. Of the numerous types of semiconductors in existence, Si and GaAs can be considered as the two most important ones. In the 1950s and 1960s semiconductor devices were mainly fabricated by ion implantation and/or diffusion of various dopants in a bulk semiconductor wafer. However this approach limits the minimum vertical and lateral features that can be achieved and excludes the possibility of fabricating devices where small features or precise layer thicknesses are required. Also the entire device consists of a single semiconductor material. Significant improvement in device performance is enabled by precise control of vertical features, which is achieved by deposition additional semiconductor material on the substrate by a process known as epitaxy.

Crystal Growth techniques like Liquid Phase Epitaxy and Vapor Phase Epitaxy which were developed in 1960s and 1970s enabled the fabrication of

the first semiconductor lasers. However the real potential of epitaxy was realized by the development of atomically precise growth techniques like Molecular Beam Epitaxy (MBE) and Metal Organic Chemical Vapor Deposition (MOCVD). A major advantage of using epitaxy is the ability to fabricate semiconductor heterostructure based devices that consist of two or more semiconductors. Improved performance of heterostructure devices is due to their ability to confine electrons and/or photons in a particular region of the device.

Despite the rapid pace of improvement in epitaxial growth techniques, the semiconductor substrate and its lattice parameter have decided the fate of many semiconductor technologies. The semiconductor substrate has two functions; the first is mechanical support and the second is to provide lattice registration to the epitaxial layers grown on it. Substrate size and quality are major factors governing the economics and feasibility of a particular semiconductor technology. The widespread use of silicon-based devices is a testimony to advances in the Silicon substrate size and quality. In recent years similar improvements in the case of GaAs substrates have transformed III-V compound semiconductor devices from research curiosities to production commodities. High quality epitaxial growth is possible only if the lattice constant of the desired epitaxial material is nearly the same as that of the substrate. Also production costs can be reduced if the growth and processing is done on cheap large area substrates. Hence the substrate has been a major factor that governs both the economics and performance of a semiconductor technology. This is most evident in the recent developments in GaN based semiconductor devices, where no suitable lattice-matched substrate exists and progress has been limited to device structures most forgiving of lattice-mismatch related structural defects.

In many cases the performance of electronic and optoelectronic devices can be improved through the use of new semiconductor materials for which no suitable lattice-matched substrate exists. Therefore these materials have to be deposited on available substrates (which have a different lattice constant). Hence the process is termed as heteroepitaxy. In recent years, there has been extensive research in the heteroepitaxy of semiconductor materials on Si and GaAs substrates. However epitaxial deposition of a semiconductor material on a substrate with a different lattice constant initially results in deformation of the semiconductor lattice (build up of strain). Further deposition results in the reduction of deformation in the deposited material, with the strain energy stored in the epitaxial layer acting as a driving force (strain relaxation). This process is facilitated by the formation of crystal defects of dislocations, which degrade the electronic and optoelectronic properties of the deposited semiconductor. Hence the major goal in heteroepitaxy is to either minimize the formation of these dislocations or minimize their impact on the deposited semiconductor layers.

This thesis documents the invention, development and demonstration of a new approach to relaxed heteroepitaxy – the lattice engineered substrate (LES). This approach is based on the process of lateral oxidation of Al-containing III-V compound semiconductors. The process of lateral oxidation besides changing a crystalline semiconductor to an amorphous oxide, results in significant structural changes in the semiconductor structure. The most significant of these are the reduction in thickness of the oxidizing semiconductor and conversion of a rigid epitaxial interface to a porous oxide/semiconductor interface. The structural changes caused during the process of lateral oxidation result in the relaxation of strain in lattice-mismatched (strained) semiconductor overlayer. This results in an epitaxial

template with a different lattice constant that is mechanically supported on a commercially available binary III-V substrate, effectively generating a new (quasi)-substrate. Also the conversion of the Al-containing semiconductor to a porous-amorphous material epitaxially decouples this template from the underlying binary substrate.

Hence the major prerequisites of the LES approach are the growth of highly quality strained semiconductor overlayers of significant thickness on Al-containing oxidation layers on binary III-V substrates. The structural changes occurring during the process of lateral oxidation result in strain relaxation with the strain energy acting as the driving force. The goal is to minimize the strain relaxation during the initial growth of the strained semiconductor overlayer and achieve maximum strain relaxation through the process of lateral oxidation.

1.2. Concepts in Epitaxy, Lattice Mismatch and Dislocations

Since this thesis deals extensively with the heteroepitaxial growth and strain relaxation in semiconductors, a brief description of various terms used in the thesis is given in this section for readers not familiar with these concepts. These concepts will be repeated in the forthcoming chapters for the sake of organization and continuity.

1.2.1. Lattice-Matched and Strain Epitaxy

Epitaxy is the defined as the process of depositing a *crystalline overlayer (epitaxial layer)* on a *semi-infinite crystal (substrate)*. In the case of *lattice-matched epitaxy, the lattice constant of the epitaxial layer is same as*

that of the substrate. The most common example of lattice-matched epitaxy is the AlGaAs/GaAs material system. Other examples are $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As/InP$ and the almost-lattice matched AlSb/GaSb/InAs material system. In the case of lattice-matched epitaxy, the epitaxial growth under appropriate conditions is dislocation free.

When the *epitaxial layer with a different lattice constant (referred to as heteroepitaxial layer)* is deposited on the substrate, the in-plane lattice constant is same as that of the substrate. Hence to preserve the unit crystal volume, the out-of-plane lattice constant is changed. When the *lattice constant of the epitaxial layer is greater than that of the substrate*, the layer is under *compressive stress*. When the *lattice constant of the epitaxial layer is smaller than that of the substrate*, the layer is under *tensile stress*. Figure 1.1 illustrates these concepts.

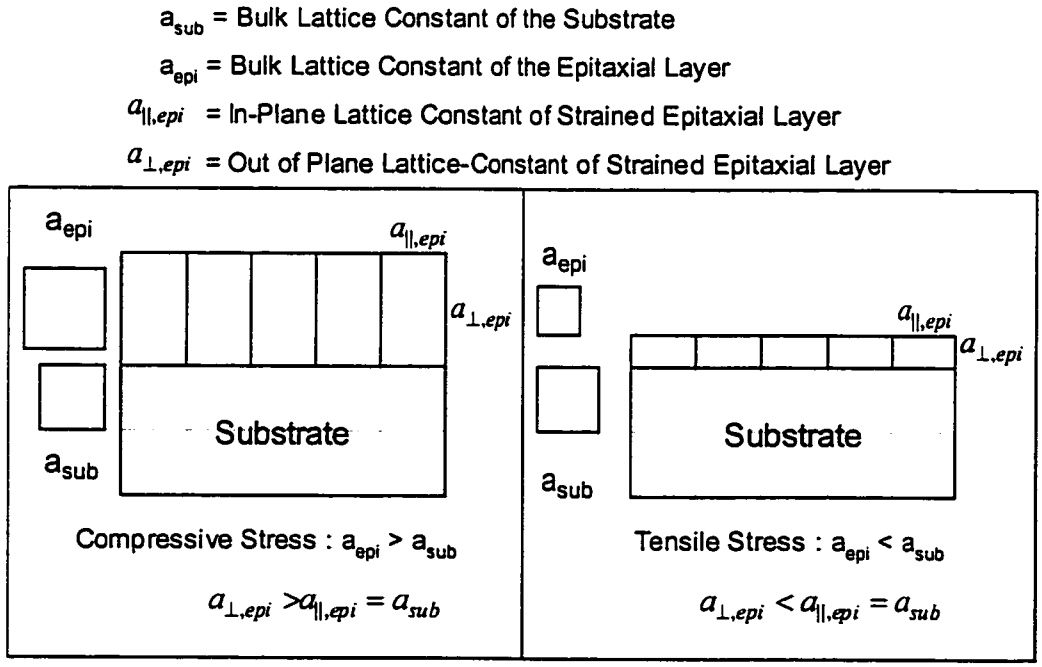

Figure 1.1: Heteroepitaxy under compressive and tensile strain

1.2.2. Dislocations

Lattice deformation results in build up of strain energy in the heteroepitaxial layer. Beyond a certain layer thickness defined as the critical thickness, it becomes energetically favorable to relieve this strain by formation of dislocations. A dislocation can be defined as a localized region of disregistry between crystal unit cells.

The two basic type of dislocations are edge type dislocations and screw type dislocations. As illustrated in Figure 1.2 an edge dislocation is formed by

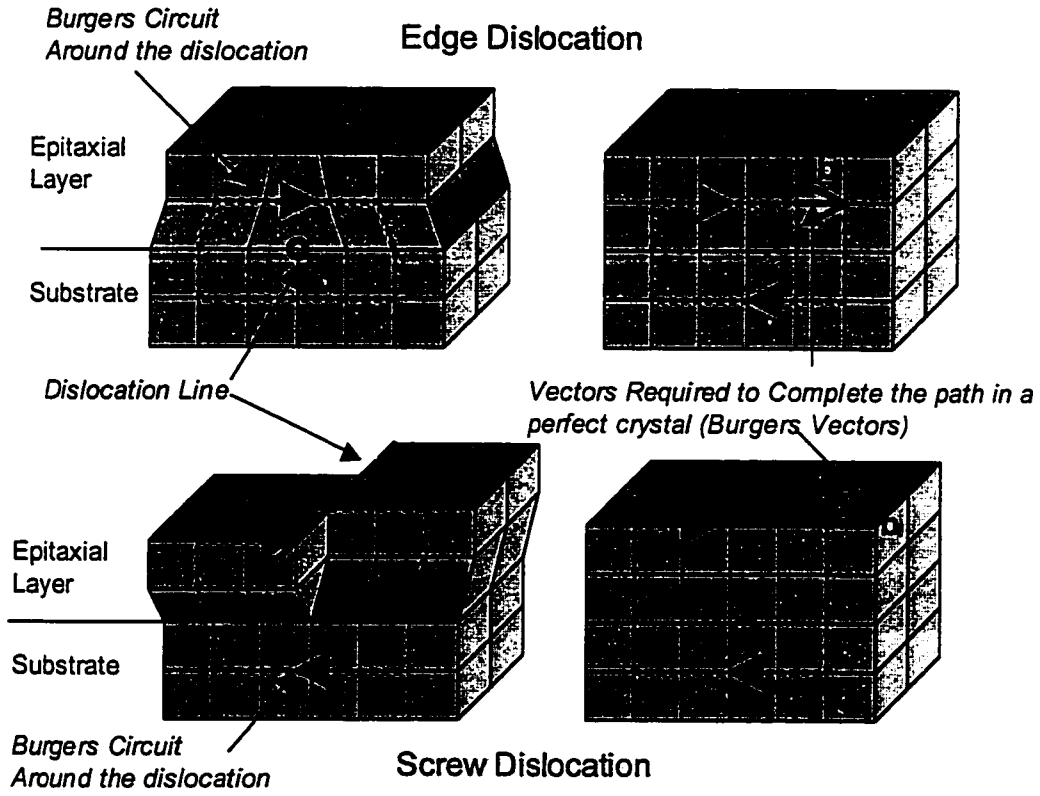

Figure 1.2: Schematic description of an edge dislocation and a screw dislocation and their associated Burgers vectors

insertion of an extra half plane in the crystal lattice. The edge dislocation is characterized by a dislocation line lying along the inserted half plane. *The Burgers vector of a dislocation is defined as the linear displacement that is required to complete a closed path in the crystal when the dislocation is removed.* The Burgers vector of an edge dislocation is perpendicular to the dislocation line.

A screw dislocation is characterized by having its Burgers' vector parallel to the dislocation line. As seen from Figure 1.2 the Burgers vector of a screw dislocation is parallel to the dislocation line. *Edge dislocations are the most efficient dislocations that can accommodate lattice mismatch, where as screw dislocations do not accommodate any lattice mismatch.* A dislocation that has both the edge and screw character is termed as a mixed dislocation.

Figure 1.3 depicts a 3-dimensional illustration of dislocations and their glide planes as observed in cubic semiconductors.

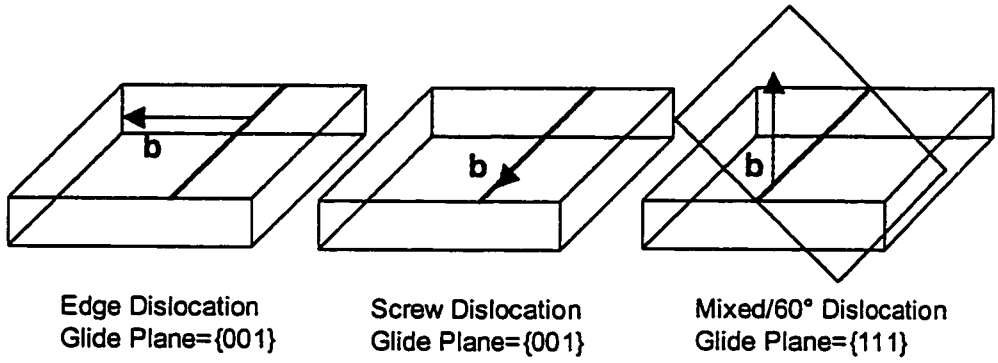

Figure 1.3: Schematic illustration of dislocations with their Burgers vectors and glide planes

The glide plane of a dislocation is defined as the plane that contains the Burgers vector and dislocation line. Only the component of applied force along the Burgers vector results in dislocation movement that can occur only

on the glide plane. The glide planes of pure edge and screw dislocations in cubic semiconductors are {001}, whereas the glide plane for Mixed Dislocations is {111}. The mixed or 60° dislocations are the most prevalent dislocations observed in cubic semiconductors. Also the only possible glide direction is the {111} direction, hence pure edge and screw dislocations cannot glide and are immobile or sessile. *Since these dislocation line segments assist in accommodating the lattice mismatch they are termed as misfit dislocation segments.*

1.2.3. Dislocation Sources and Strain Relaxation Mechanisms

The various sources that result in the formation of misfit dislocation segments include substrate-threading dislocations, and half loops that nucleate at the growth surface. The real dislocation sources remain elusive. *Substrate threading dislocations (TD) are dislocations found in semiconductor substrates.* The typical density of these threading dislocations varies from 10 /cm^2 for Si substrates to 10^5 /cm^2 for GaAs substrates. These dislocations are mixed or 60° dislocations. Figure 1.4 illustrates the mechanism of creation of misfit dislocation segment from a substrate TD. The force due to misfit strain acts to extend the misfit dislocation line segment through the motion of the threading dislocation. The force opposing the creation of the misfit dislocation segment is line tension in the misfit dislocation segment. The line-tension in a dislocation segment is analogous to the elastic tension in a rubber band that opposes its extension.

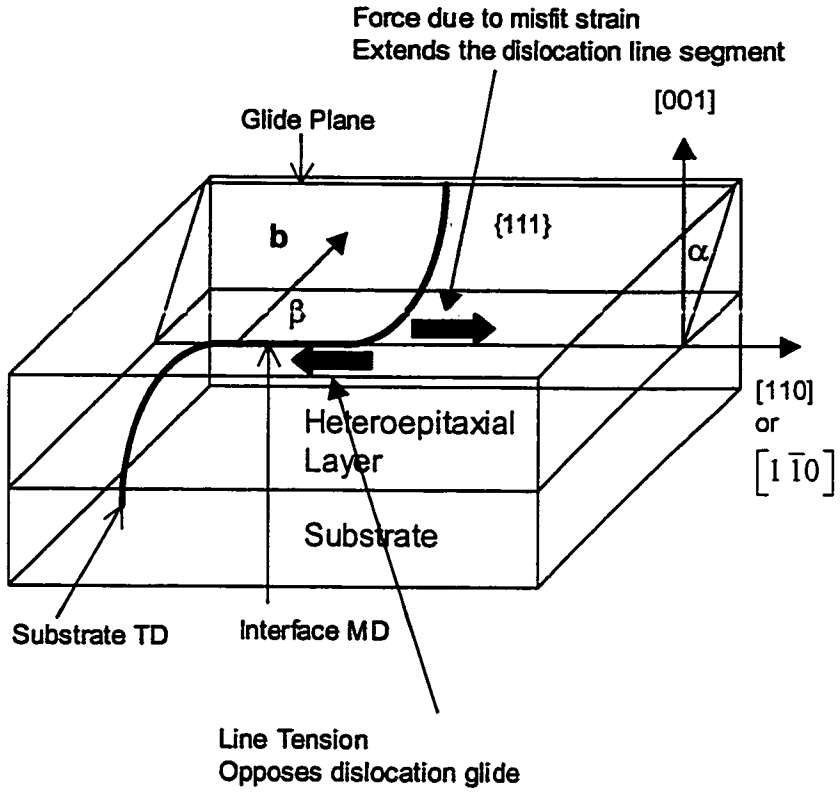

Figure 1.4: Mechanism of Misfit Dislocation segment from a substrate threading dislocation

Since the Burgers vectors of these dislocations lie on the {111}glide plane the dislocation glide occurs along the {111} planes. The misfit dislocation line segments lie along the orthogonal <110> directions, which are the intersection of {111} glide plane and the {001} surface.

Another mechanism that creates misfit dislocation segments is surface half-loop nucleation as illustrated in Figure 1.5. In this mechanism a half-loop is nucleated at the growing surface and propagates towards the interface along the {111} glide plane. When this loop reaches the epitaxial layer substrate

interface, it results in the formation of two threading dislocation segments connected by a misfit dislocation segment.

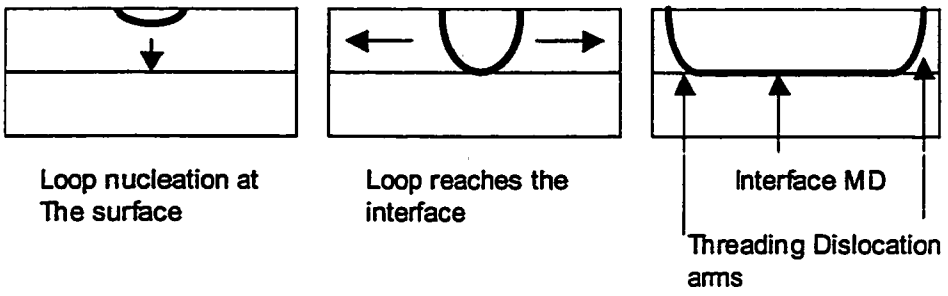

Figure 1.5: Misfit Dislocation Formation by Surface Half-Loop Nucleation and Propagation to the interface

Since misfit dislocation formation by these mechanisms involves dislocation glide on {111} planes, the misfit dislocations generated are mixed type dislocations that can glide (glissile dislocations) and contribute to further strain relaxation.

The driving force for dislocation glide (and strain relaxation) is the strain energy due to the lattice mismatch. This process is mainly impeded by the presence of other dislocations that inhibit the dislocation glide.

1.2.4. Heteroepitaxial Growth Modes and Strain Relaxation

The growth mode of an epitaxial layer can also affect the dislocation generation and strain relaxation process. Figure 1.6 illustrates the various growth modes observed in semiconductor epitaxy.

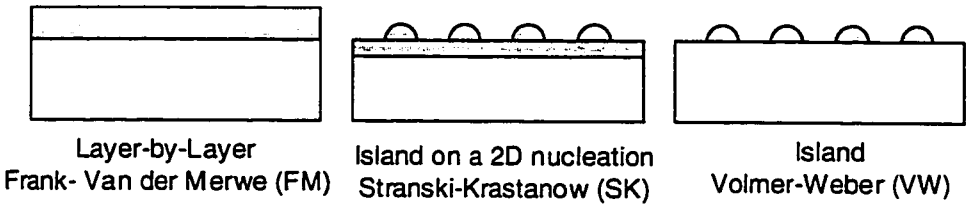

Figure 1.6: Growth Modes observed in semiconductor epitaxy

The Frank-van der Merwe (FM) growth mode is typically observed for low lattice mismatches (~ 1%) whereas the Stranski-Krastanow (SK) growth mode is observed for higher lattice mismatches (upto 7%). For higher lattice mismatches it is impossible to achieve layer-by-layer or 2D growth for any thickness and the growth is initiated in the island or 3D mode. Under lattice mismatch strain, the equilibrium growth surface is rough or consists of islands. The rough surface can also act as dislocation sources as seen in Figure 1.7.

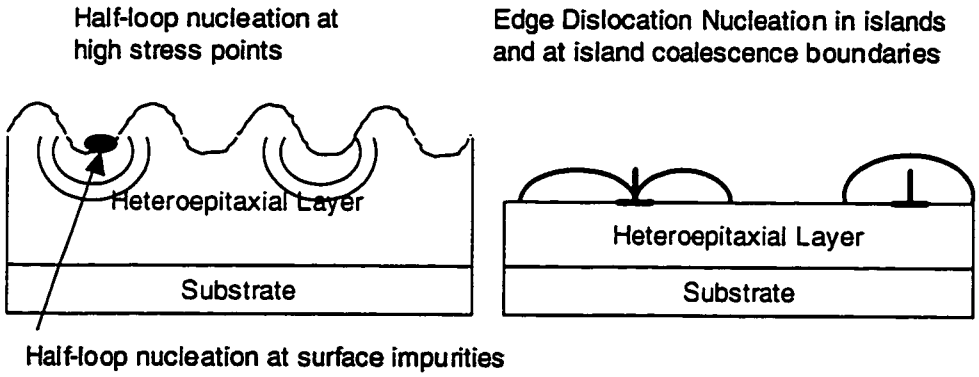

Figure 1.7: Dislocation generation mechanisms due to heteroepitaxial growth modes

To summarize, lattice-mismatch in heteroepitaxy can be accommodated by formation of misfit dislocations. The dislocations can be generated from

various sources that include substrate dislocations, impurities and high stress points in the 3-D growth surface.

1.3. Strained Layer Epitaxy and Heteroepitaxy

The mechanics of accommodation of lattice-mismatch between an epitaxial layer and the substrate was first investigated by Frank and van der Merwe 50 years ago [1]. Significant improvement in semiconductor device performance can be achieved by the incorporation of strained semiconductor layers. In this case one or more thin semiconductor layers of a different lattice constant are incorporated in the semiconductor device structure. These semiconductor layers are under deformation, as their lattice has to conform to that of the substrate. The lattice deformation also changes the band structure of the semiconductor potentially leading to improved transport and optical gain properties. However when the thickness of the strained semiconductor is greater than a certain thickness (referred to as critical thickness) structural defects are introduced, which significantly affect device performance. In the last 20 years, strained layer epitaxy has been studied in great detail and significant advancements have been made in incorporating strained layers in semiconductor devices. The most notable of these are the SiGe/Si heterojunction bipolar transistor, the GaAs psuedomorphic HEMT and strained quantum well laser. A comprehensive review of strained layer epitaxy can be found in [2].

Figure 1.8 shows the lattice constants and bandgap of various semiconductor substrates in use. It is clear that for lattice constants ranging 5.451 Å (Si) to 6.47 Å

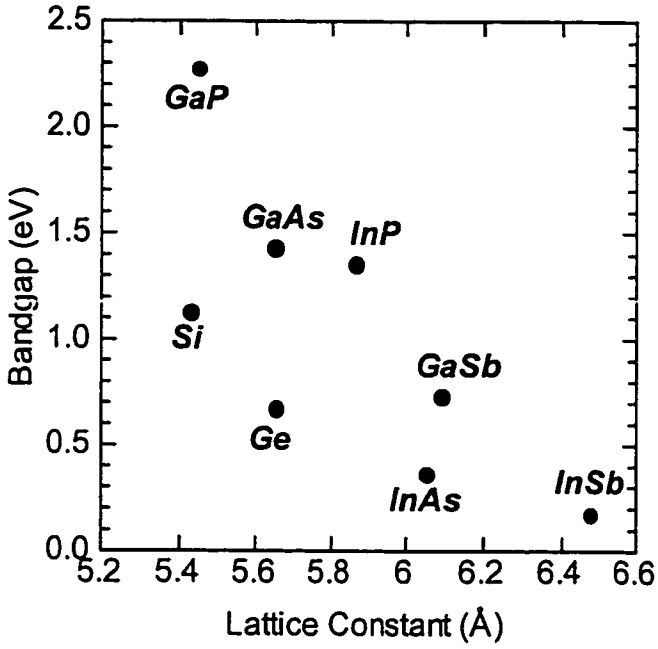

Figure 1.8: Lattice Constant and Bandgap of Commonly Used Semiconductor Substrates

(InSb), high quality epitaxy is possible only at discrete lattice constants that correspond to an available semiconductor substrate. Unlike Si and GaAs, development of semiconductor technologies on other substrates like InP, GaSb and InSb continues to be mainly limited by advances in substrate cost, size and quality. In the case of antimonide substrates absorption of light by the substrate is also a major obstacle in improving the performance of IR optoelectronic devices. Hence it is desirable to grow a semiconductor with an arbitrary lattice constant on a cheap large area substrate like Si or GaAs. For these reasons, the universal heteroepitaxial growth of semiconductors on Si or GaAs has been the holy grail of semiconductor epitaxy. Figure1.9 illustrates the difference between strain layer epitaxy and relaxed heteroepitaxy. Relaxed lattice mismatched growth is termed as heteroepitaxy.

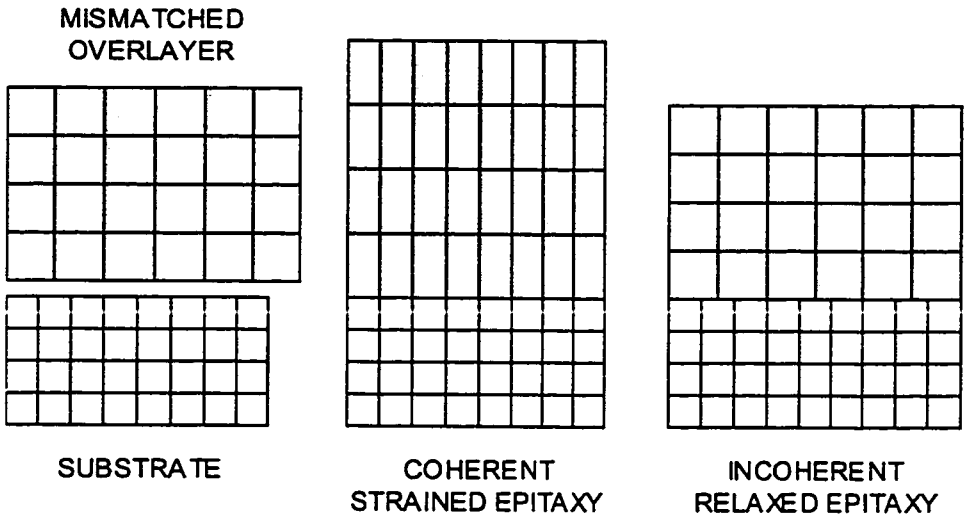

Figure1.9: Schematic Illustration of strained-layer epitaxy and relaxed heteroepitaxy

The goal in heteroepitaxy is not to grow a coherent strained epitaxial layer on a given substrate, but to obtain a relaxed or unstrained epitaxial layer with a different lattice constant on a substrate. This enables the growth of optimized semiconductor devices at hitherto unachievable lattice constants. As described before, the growth of an epitaxial layer whose lattice constant differs from that of the substrate results in lattice deformation of that epitaxial layer. The lattice deformation results in the build up of strain energy in the growing heteroepitaxial layer. Beyond the critical thickness, the mismatch strain is relieved by the formation of misfit dislocations at the epitaxial layer/substrate interface. These dislocations enable the heteroepitaxial layer to achieve its native or unstrained lattice constant. Misfit dislocation segments are created at the epitaxial substrate layer mainly by glide or movement of substrate threading dislocations [3]. The formation, movement and interaction of these dislocations decide how the mismatch strain between the epitaxial layer and

the substrate is relieved. This process will be described in detail in later chapters.

Under non-optimum conditions the process is impeded and the nucleation of additional dislocations to accommodate the mismatch strain is necessary. This increases the density of threading dislocations in the epitaxial layer. The threading dislocations act as traps and recombination centers and hence degrade the electronic and optical properties of the heteroepitaxial layer. Misfit dislocations are needed to accommodate the lattice mismatch between the epitaxial layer and the substrate, however the additional threading dislocations required to create the misfit dislocation segments are an unfortunate consequence of this process. Hence dislocations are necessary evils in heteroepitaxy and are best confined at the heteroepitaxial layer/substrate interface.

To summarize, lattice mismatched epitaxial growth can have two entirely opposite approaches. The first is strained heteroepitaxy, where the emphasis is to grow a coherent strained layer without the formation of dislocations. The second is the growth of a low threading dislocation density unstrained lattice-mismatched semiconductor, where the lattice-mismatch between the epitaxial layer and the substrate is accommodated by misfit dislocation at the epitaxial layer-substrate interface.

1.4. Conventional approaches for heteroepitaxy

There have been various approaches investigated to achieve high quality lattice mismatched growth of various semiconductors on the most commonly available substrates, Si and GaAs. Besides lattice mismatch, growth of III-V

compound semiconductors on elemental semiconductor substrates like Si or Ge, has to deal with issues related to interface polarity [4]. In addition to this, the thermal expansion mismatch between Si and many compound semiconductors also generates dislocations during the cool-down process after growth. These issues will not be discussed in this thesis.

When a significant difference exists between the epitaxial layer and the substrate, direct growth results in the formation of large numbers of dislocations that propagate in the epitaxial layer. This is because all the misfit dislocation segments are located at a single interface. This interaction between the strain-fields of these dislocations acts as a barrier to the formation of additional misfit dislocation segments. Also the large lattice mismatch (typically > 2%) may cause the epilayer to grow in a 3D or island mode. When the islands coalesce there is a large increase in threading dislocation density in the epitaxial layer. An approach to avoid this is the gradual change in lattice constant that distributes the misfit dislocation segments vertically and reduces the barrier creation of additional misfit dislocation segments by glide of threading dislocations [5]. This approach has led to the successful fabrication of majority carrier based devices like field effect transistors. However the thickness of the graded buffer is of the order of microns. Also elaborate growth techniques are required to maintain a low dislocation density, which has a lower minimum of $10^6/cm^2$.

Reducing the growth area can also reduce the interaction between the dislocations at the mismatched interface [6]. However large sized patterned areas (~100 μm) can accommodate lattice mismatches of the order of 0.5 %. For a larger lattice-mismatch (1-2 %), smaller sized patterned areas (~0.6-1.3 μm) have to be used [7]. This renders the approach unsuitable for device fabrication.

1.5. Novel Approaches for Heteroepitaxy

In recent years fused/bonded interfaces and amorphous materials like oxides have been incorporated in semiconductor devices for performance improvement [8, 9]. Not surprisingly these techniques have been applied to heteroepitaxial growth on GaAs and Si. These techniques modify the nature of dislocation nucleation and interaction at the fused interface or the oxide/semiconductor interface. Recently a "universal compliant" substrate was demonstrated which consisted of a thin GaAs film twist-bonded to a GaAs substrate [10]. In the twist bonding process, the in-plane crystallographic axes of the two wafers are at an angle (as opposed to the normal case where they are aligned). The twist-bonded interface is said to create a two-dimensional screw dislocation network that generates a correlated network of strain relieving misfit dislocations. The exact reason for compliance is still under investigation [11]. Here the term "compliant" refers to the phenomenon of the substrate adjusting itself to the native lattice-constant of the epitaxial layer by forming a suitable network of dislocations.

Amorphous materials like oxides have been increasingly integrated in semiconductor devices for performance improvement. In the case of Si based devices, buried oxides have been incorporated in the semiconductor structure by wafer bonding or implantation, resulting in a Silicon-On-Insulator (SOI) structure. In the case of III-V semiconductor devices, buried oxide layers are obtained by lateral oxidation of Al-containing III-V semiconductors. Electronic and optical confining properties of these oxides have been used to improve the performance of field effect transistors and semiconductor laser diodes [12, 13]. Compared to a rigid substrate/epilayer interface, incorporation of a structurally weaker amorphous interlayer is expected to change the nature of dislocation

nucleation, propagation and interaction in the heteroepitaxial structure. Approaches based on amorphous interlayers consist of a thin substrate mechanically supported by the amorphous oxide on a handle wafer that provides mechanical support. The heteroepitaxial layers are grown on a thin substrate supported by an amorphous interlayer that is supposed to be viscous at growth temperatures. The lattice mismatch is incorporated by the deformation in the substrate that is much thinner than the growing heteroepitaxial layer, which is aided by the viscous interlayer at high growth temperatures [14, 15].

1.6. Lattice Engineered Substrates Using Lateral Oxidation of AlAs

This thesis documents the invention, development and demonstration of a new approach to relaxed heteroepitaxy – the lattice engineered substrate (LES). This approach is also based on the use of an amorphous interlayer. The process of lateral oxidation besides changing a crystalline semiconductor to an amorphous oxide, results in significant structural changes in the semiconductor structure. The most significant of these are the reduction in thickness of the oxidizing semiconductor and conversion of a rigid epitaxial interface to a porous oxide/semiconductor interface.

On a GaAs substrate for example, the LES approach utilizes the process of relaxation of a coherent hypercritical thickness ($h > h_{critical}$) strained semiconductor over-layer (InGaAs) in direct contact with an oxidizing Al-containing semiconductor (e.g. AlAs or AlGaAs). The porous and reactive interface between the strained semiconductor overlayer and the oxide enables

extensive plastic strain relaxation due to efficient dislocation motion without interaction and generation of new dislocations. This results in the formation of a relaxed dislocation-free InGaAs template *(Lattice Engineered Substrate)* that is epitaxially decoupled from the underlying GaAs substrate, while still mechanically supported by the substrate. Subsequent regrowth on this template (lattice engineered substrate) enables the fabrication of relaxed low threading dislocation density InGaAs buffers and device structures.

In other approaches the process of lattice constant transformation by strain relaxation occurs during the growth of the desired heteroepitaxial layer. In the LES approach, strain relaxation during lateral oxidation creates a "quasi-substrate" having a different lattice constant than the substrate that supports it. Subsequent growth of the desired epitaxial layer on the quasi-substrate is strain free. (Lattice-engineered substrates are called quasi-substrates because the strain-relaxed semiconductor overlayer provides only epitaxial registration for subsequent growth, however, the whole structure is mechanically supported by the binary substrate) This approach differs from all other conventional and novel approaches in heteroepitaxy as it separates the process of strain relaxation and epitaxial growth. With the appropriate choice of semiconductor substrate and the oxidizing Al-containing semiconductor, this approach should enable the fabrication of quasi-substrates at lattice constants between the all commercially available III-V semiconductor substrates. Figure1.10 illustrates the implementation of the LES approach on various III-V semiconductor substrates. Thus it should be possible to achieve an arbitrary lattice constant ranging from GaP to InSb.

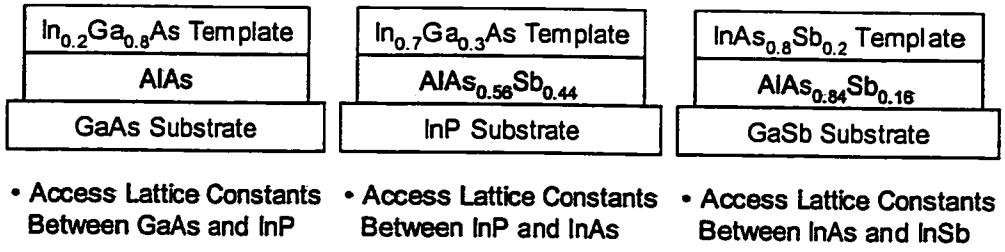

Figure1.10: Implementation of the LES Approach on Various III-V Semiconductor Substrates

1.7. Applications for Lattice-Engineered Substrates

Conventional approaches like graded buffers are adequate for fabrication of semiconductor devices that rely on majority carrier transport. However for devices where the presence of dislocations severely impacts the performance, low dislocation density materials are necessary. For example in semiconductor lasers, the dislocations act as non-radiative recombination centers and increase the amount of current required to achieve the lasing threshold. In bipolar transistors, the presence of dislocations results in increased recombination in the base. This reduces the current gain of the transistor. On the other hand in detectors that are reverse biased, dislocations acts as generation centers and result in increased dark currents. This adversely affects the noise performance of the detector.

There exist applications for low dislocation density materials with intermediate lattice constants ranging from Si to InSb. These applications are listed in Table 1.1. Column 1 lists the specific applications, column 2 lists the substrate on which the devices are fabricated at present, column 3 explains the limitations on growing on that substrate, column 4 lists the desired platform for

lattice engineered substrate and column 5 list the advantages of the LES approach for that device.

Device	Substrate	Problem	LES Platform	Advantage
AlInGaP LEDs	GaAs	Growth on a light absorbing substrate. Wafer bonding to transparent GaP substrates required for increased light output	GaP	Elimination of wafer bonding.
Solar Cells	GaAs/Ge	No material exists for utilizing solar radiation with wavelengths beyond 1 μm	GaAs/Ge	Enables growth tandem GaAs/Ge solar cells with InGaAs junctions. Higher efficiency
Long Wavelength Lasers	InP	Low Band offsets result in lower optical gain and carrier confinement.	GaAs	Enables High Temperature Operation Without TE Coolers
Low Power HBTs	InP	Minimum Junction Turn On Voltage=0.75 V Limits High Density Circuits	InP	Supply Voltage can be reduced to 0.5 V
IR Detectors	GaSb	Substrate Absorbs Wavelengths > 5 μm Conductive Substrate	InP	Enables integration with InP Electronics
IR Lasers	GaSb	Lossy Substrate	InP	Eliminates optical loss in the substrate

Table 1.1: Device Applications of Lattice-Engineered Substrates

Apart from affecting the epitaxial growth of the device structure, the substrate also effects back-end processing and operational characteristics of devices. The poor mechanical strength of InP substrates is a yield-limiting factor in InP-based MMICs. The inability to cleave sapphire limits the yield of GaN based semiconductor lasers. Also the performance of GaN based semiconductor devices is limited by poor thermal conductivity of sapphire

substrates, whereas IR optoelectronic devices on GaSb substrates are performance-limited by the IR-absorbing substrate. Hence development of alternative substrates promises to improve the device performance on many fronts.

1.8. Thesis Outline

This thesis is organized as follows. Chapter 2 discusses the MBE growth of templates for fabrication of lattice-engineered substrates. The highly strained epitaxial layer is a source of the driving force (in the form of mismatch stress energy) for the formation of the quasi-substrate upon oxidation. The lattice constant information is stored in the form of the composition of the strained epitaxial template. Since the LES approach requires the growth of strained epitaxial layers with thickness 10 times that of the equilibrium critical thickness, appropriate epitaxial growth techniques have to be used to minimize dislocation formation. These techniques and characterization of the MBE grown templates will be discussed in Chapter 2.

The process of lateral oxidation and the consequent process of strain relaxation is also an important aspect of the LES approach. Chapter 3 discusses the process of lateral oxidation and the various factors affecting strain relaxation. The LES approach is compared with conventional approaches for achieving low dislocation density strain relaxed materials.

Chapter 4 discusses the structural characterization of epilayers on lattice-engineered substrates. The surface morphology is analyzed using atomic force microscopy. X-Ray diffraction of epitaxial layers is used to calculate

strain relaxation. TEM characterization is used to evaluate the structural quality of epitaxial layers grown on lattice-engineered substrates

Chapter 5 discusses the electrical and optical properties of epitaxial layers grown on lattice-engineered substrates. PN junction diode structures were grown on lattice-engineered substrates. The magnitude of the reverse leakage current in a pn junction diode is a measure of the dislocation density in the epitaxial layers. Single and multiple quantum well structures with an emission wavelength of 1.3 μm were also grown. The intensity and the peak width of the PL emission is also dependent on the structural quality of the regrown epitaxial layers.

Chapter 6 summarizes the various aspects of the LES approach and discusses future directions.

1.9. References

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Chapter 2.
MBE Growth of Templates for Lattice-Engineered Substrates

Epitaxial growth of highly strained low threading dislocation density InGaAs layers is a major prerequisite for the fabrication of an InGaAs based lattice-engineered substrate (LES). Figure 2.1 shows the various epitaxial layers in a LES template. This chapter focuses on issues related to growth of highly strained InGaAs epitaxial layers by molecular beam epitaxy. The design of oxidation layers is discussed in Chapter 3. The cap layers are mainly for facilitating processing and their design is predicted in Chapter 4.

Section 2.1 discusses the basic mechanisms of strained layer epitaxy and is followed by the definition of Matthews-Blakslee critical thickness in Section 2.2. Growth mode, surface morphology and dislocation generation issues related to strained InGaAs growth on GaAs are discussed in section 2.3. Experimental growth conditions and structural characterization of LES templates InGaAs will be discussed in sections 2.4 and 2.5 of this chapter.

2.1. Lattice Mismatched Epitaxy: A basic model

In recent years, strained layer epitaxy has been extensively investigated for application in electronic and optoelectronic devices. The most basic model

of strained layer epitaxy is as follows. When a semiconductor with a different lattice constant is grown in Frank-van der Merwe (FM) or layer-layer growth mode on an infinitely thick substrate, initially the in-plane lattice constant of the semiconductor is same as that of the substrate and the out-of-plane lattice constant changes due to the in plane deformation ('Poisson' effect). This lattice deformation results in build-up of strain energy in the epitaxial layer. Beyond a certain thickness defined as the critical thickness ($h_{critical}$), the partial release of strain energy results in the formation of local regions of lattice misregistry known as misfit dislocations at the epitaxial layer-substrate interface. The misfit dislocations enable the epitaxial layer to achieve its native lattice constant, as the constraint of perfect registry at the interface is relaxed[1].

The source of misfit dislocations occurring during lattice-mismatched epitaxy has been a topic of great controversy [2]. Most semiconductors substrates are not perfect crystals and contain threading dislocations or defects. For low mismatch strains (Misfit < 4%) and FM growth mode, the substrate threading dislocations can be considered as the major source for formation of misfit dislocations. A misfit dislocation (MD) can be considered as a remnant of the glide process of a threading dislocation (TD). As illustrated in Figure 2.1, the strain energy in the mismatched epitaxial layer aids the glide process,

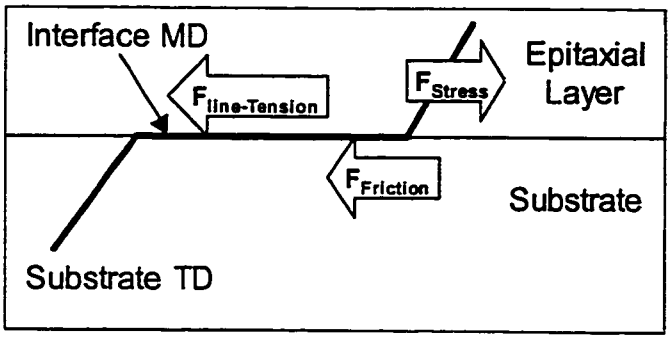


Figure 2.1: Schematic Illustration of Misfit Dislocation (MD) Formation at the Substrate-Epitaxial Layer Interface by extension of Substrate Threading Dislocation (TD) segments

whereas the line tension in the threading dislocation segment and Peierls stress or frictional force oppose this motion. Critical thickness is defined as the layer thickness when glide force on the TD segment balances the line tension and frictional force.

This is the most basic model for definition of critical thickness. In practice however, kinetic factors and other barriers may delay the formation of misfit dislocations. These factors are exploited in the growth of highly strained low dislocation density InGaAs layers with layer thickness exceeding the critical thickness by 20 times.

2.2. Matthews-Blakeslee critical thickness

Since the goal during the growth of a lattice-engineered substrate template is the minimization of strain relaxation in the as-grown film, it is essential to determine the layer thickness at which misfit dislocations are created. Consider an *epitaxial layer of thickness* h, having a *lattice mismatch* f

with the substrate. The driving force for glide on a threading dislocation, which is due to the misfit strain, is given by [1],[3]

$$F_{misfit} = 2G\varepsilon bh\cos\lambda\frac{1+\nu}{1-\nu} \tag{2.1}$$

Assuming that Peierls stress is negligible, the opposing force to glide of the TD is the line tension and is expressed as follows:

$$F_{line} = \frac{Gb^2}{4\pi}\frac{1-\nu\cos^2\theta}{1-\nu}\ln\left(\frac{h}{b}\right) \tag{2.2}$$

The various parameters in Equations (2.1) and (2.2) are defined as follows, G is the Shear modulus; b is the magnitude of the Burgers vector of the dislocation; ε is the elastic strain; ν is the Poisson ratio, λ is angle between the slip direction and the direction in the plane that is perpendicular to the line of interaction of the slip plane and the epitaxial surface, and θ is the angle between the misfit dislocation line and its Burgers vector. Equating the line tension to the glide force due to the misfit strain results in the following definition for the critical thickness, hence defined as $h_{critical}$,

$$\varepsilon = \frac{b}{8\pi h_{critical}\cos\lambda}\frac{1-\nu\cos^2\theta}{1+\nu}\ln\left(\frac{h_{critical}}{b}\right) \tag{2.3}$$

One important aspect of the above derivation is that it assumes that the strained layer is not capped. Growth of a capping layer that is lattice-matched to the substrate stabilizes a strained layer with respect to formation of misfit dislocations. Critical thickness of the strained layer with an infinitely thick cap is nearly twice that of an uncapped layer [4]. In the case of LES templates, the strained InGaAs layers are grown upto $20 \times h_{critical}$ thick, before the growth of a capping layer, which is 1/3 or 1/5 of the strained layer thickness. Therefore the capping layers have a negligible effect on stabilizing the structure. Hence for all practical purposes the critical thickness models used here will be those

for uncapped layers for the sake of simplicity. This analysis assumes that there are no other sources of dislocations in the substrates. However in reality dislocations can nucleate at surface defects and particulates and local stress concentrators. Also propagation of surface half loops to the interface can create misfit dislocation segments [2].

Figure 2.2 shows the variation of equilibrium critical thickness as a function of lattice mismatch (f) and Indium content (x) for the $In_xGa_{1-x}As/GaAs$ material system.

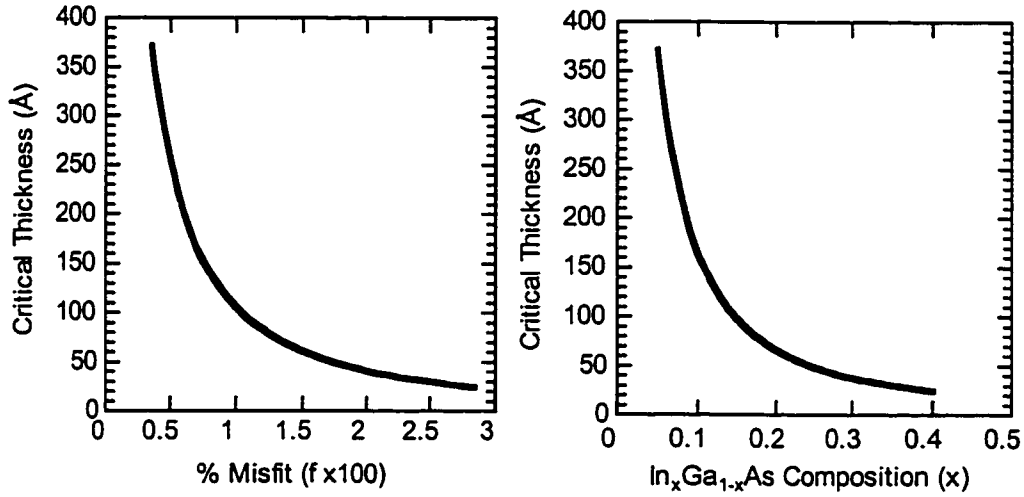


Figure 2.2: Variation of Critical Thickness as a Function of Misfit strain (f) and Indium Content (x) for $In_xGa_{1-x}As/GaAs$ material system

The critical thickness model presented above is an equilibrium model. There are kinetic limitations and heterogeneous barriers that result in a critical thickness much more than that given in equation (2.3). In the case of MBE grown InGaAs epitaxial layers, growth at temperatures ranging from 500 to 530 °C can be considered to be under equilibrium conditions [5].

There are various ways to characterize the strained semiconductor layers. These include structural methods like x-ray diffraction and transmission electron microscopy (TEM) and optical methods that consist of photoluminescence (PL) characterization of InGaAs/GaAs quantum wells.

Optical characterization of InGaAs/GaAs quantum wells shows that when the InGaAs quantum well thickness exceeds the critical thickness, the PL intensity decreases and FWHM increases [6]. The decrease in intensity is due

Indium Composition	Calc. $h_{critical}$	Exp. $h_{critical}$	Tech.	Structure	Reference
$In_{0.09}Ga_{0.91}As$	190 Å	300 Å	PL	GaAs/InGaAs/GaAs	[5]
$In_{0.10}Ga_{0.90}As$	166 Å		TEM	GaAs/InGaAs	[4]
$In_{0.11}Ga_{0.89}As$	147 Å	270 Å	PL	GaAs/InGaAs/GaAs	[7]
$In_{0.14}Ga_{0.86}As$	107 Å	200 Å	PL	GaAs/InGaAs/GaAs	[5]
$In_{0.19}Ga_{0.81}As$	71 Å	125 Å	PL	GaAs/InGaAs/GaAs	[5]
$In_{0.2}Ga_{0.8}As$	65 Å	200 Å	PL	GaAs/InGaAs/GaAs	[8]
		190 Å	PL	GaAs/InGaAs/GaAs	[9]
		160 Å	TEM	GaAs/InGaAs	[4]
$In_{0.28}Ga_{0.72}As$	41 Å	90 Å	PL	GaAs/InGaAs/GaAs	[5]
$In_{0.3}Ga_{0.7}As$	38 Å	28 Å	RHEED	GaAs/InGaAs	[10]
$In_{0.38}Ga_{0.62}As$	26 Å	15 Å	RHEED	GaAs/InGaAs	[10]
$In_{0.4}Ga_{0.6}As$	24 Å	28 Å	PL	GaAs/InGaAs/GaAs	[5]
$In_{0.5}Ga_{0.5}As$	17 Å	11 Å	RHEED	GaAs/InGaAs	[10]
InAs		0.9 ML	PL	GaAs/InAs/GaAs	[11]

Table 2.1: Comparison of theoretical and experimental critical thickness of InGaAs epitaxial layers on GaAs

to the formation of misfit dislocations that act as non-radiative recombination centers. The bandgap of strained InGaAs depends on the elastic strain. Hence

spatially non-uniform relaxation results in increased FWHM of the PL peak. Table 2.1 compares the calculated and reported experimental critical thickness for InGaAs layers grown at high growth temperatures (500-520 °C).

Before comparing the experimentally observed and the theoretically calculated critical thickness it is necessary to consider the advantages and limitation of various measurement techniques. In MBE, the Reflection High Electron Energy Diffraction (RHEED) can be used to monitor the changes in the epitaxial growth mode. A spotty RHEED pattern during heteroepitaxial growth indicates transition to the energetically favorable island growth mode. This does not necessarily imply the onset of dislocation generation. Hence critical thicknesses measured from RHEED are typically lower than the theoretical values. On the other hand detecting strain relaxation by techniques like TEM and PL requires the formation of large number of dislocations. Hence critical thickness as inferred from these techniques is much higher than the theoretically calculated values [12]. A more sensitive technique to detect the onset of misfit dislocation formation is photoluminescence microscopy. In this technique, dislocations that act as non-radiative recombination centers appear as dark line defects. For $GaAs/In_{0.2}Ga_{0.8}As$ structures dark line defects due to misfit dislocation formation appear at a layer thickness of 200 Å [8]. Even when highly sensitive characterization techniques are used to detect strain relaxation, the formation of dislocations themselves may be limited by kinetic factors and epitaxial growth conditions.

2.3. Growth of Highly strained InGaAs under Non-Equilibrium Conditions

As described in section 2.1, the template for a lattice-engineered substrate requires the growth of thick, highly strained InGaAs layers with a smooth surface morphology. Most critical thickness models assume a layer-by-layer or Frank-van der Merwe growth mode. However, in reality, the mismatch strain in the growing heteroepitaxial layer affects the surface morphology. Surface morphology and dislocations interact with each other to determine the microstructure of the heteroepitaxial layer. Figure 2.3 shows the various

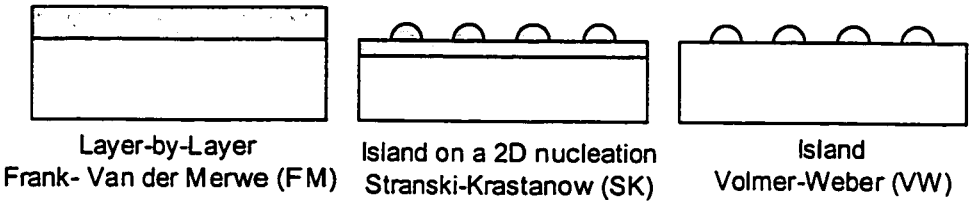


Figure 2.3: Growth modes observed in semiconductor epitaxy

growth modes observed in semiconductor epitaxy. For low mismatch strains (f < 1%), epitaxial growth is mainly in the FM mode. Strain relaxation occurs by formation of misfit dislocations (MD) at the epitaxial layer-substrate interface. The strain fields from the MDs result in the roughness of the surface. The heteroepitaxial layer is free of threading dislocations. For higher mismatch strains (f > 3.5 %), growth initially commences in layer-by-layer mode and then reverts to an island (Stranski-Krastanow) mode. In this case, strain relaxation occurs either by elastic deformation of the growing surface, or by generation of high density of threading dislocations during island coalescence. For extreme lattice-mismatches, layer-by-layer growth mode is not possible and the heteroepitaxial layer nucleates in an island mode (Volmer-Weber) on

the substrate. In both Stranski-Krastanow and Volmer-Weber growth modes the heteroepitaxial layer has a high density of threading dislocations originating from island coalescence.

Thus the surface morphology of a heteroepitaxial layer determines the mode of strain relaxation and density of dislocations in the epilayer. Hence the epitaxial growth of *highly strained* InGaAs has to be in a layer-by-layer or Frank-van der Merwe mode (FM), so that the formation misfit dislocations by the glide of threading dislocations is the only mode of strain relaxation. Further this mode of strain relaxation also has to be suppressed. The approaches used to achieve this are described in this section. It is important to note that in strained layer epitaxy, surface morphology and dislocation generation influence one another.

2.3.1. Controlling Surface Morphology

There are two factors that effect the surface morphology of a heteroepitaxial layer, the first is the elastic strain relaxation by formation of surface ripples and the second is formation of cross-hatch due to strain fields on dislocations at the heteroepitaxial layer – substrate interface [13].

For highly strained InGaAs, the equilibrium state of the growing surface is three-dimensional [14]. In MBE, the onset of three-dimensional growth can be detected by the transition from a streaky RHEED pattern to a spotted pattern [10]. Formation of islands is undesirable for two reasons; rough surface morphology results in elastic relaxation of strain and is also undesirable for regrowth. As described before, island coalescence can also lead to high density of threading dislocations. To prevent the transition to the 3D growth mode, surface migration of atoms has to be reduced. Therefore it is

necessary to rely on kinetic limitations to delay this transition. Atomic surface diffusion length (λ) on a growing InGaAs surface is given by,

$$\lambda = \sqrt{2D\tau} \qquad (2.4)$$

where D is the thermally activated surface diffusion coefficient and is dependent on the growth temperature according to the following equation,

$$D = D_o \exp(-E/kT) \qquad (2.5)$$

and τ is the mean residence time of group III adatoms on the growing surface [15]. The mean residence time is usually inversely proportional to the growth rate. Using equations (2.4) and (2.5), the appropriate growth conditions to delay the 2D to 3D transition can be arrived at. These approaches are summarized as follows.

Increased growth rate

Since the residence time τ is inversely proportional to the growth rate, surface diffusion of adatoms is reduced when the strained InGaAs is grown at high growth rates (~ 1.5 μm/hr). Grandjean et al. demonstrated that $In_{0.35}Ga_{0.65}As$/GaAs quantum wells grown at higher growth rates had improved optical properties both due to improved interface smoothness and delayed plastic relaxation [16]. Both these phenomena are a direct consequence of delaying the 2D-3D transition during growth. This is mainly due to suppression of dislocation generation processes at the surface.

Reduction of surface diffusion coefficient: Increasing the energy barrier for migration

Increasing the activation energy barrier E, can reduce the surface diffusion coefficient D. This is achieved either by the use of surfactants or by changing the surface reconstruction of the growing surface as in migration

enhanced epitaxy. Grandjean et al. demonstrated that psuedomorphic growth regime of InAs on GaAs is extended from 1.5 to 6 ML using Te as surfactant [17, 18]. Migration enhanced epitaxy has a cation-stabilized surface reconstruction which favors growth in 2 dimensional mode by increasing the energy barrier for surface diffusion. Strained InGaAs layers grown using MEE have demonstrated better electrical properties than those grown by MBE [19]. Growing at low temperatures can also reduce the surface diffusion coefficient.

Reduction of Indium Surface Segregation

During the growth of InGaAs on GaAs by molecular beam epitaxy, a fraction of the Indium flux incident on the surface is not incorporated in the growing layer and segregates on the surface. At typical growth temperatures of 520°C the segregation ratio is 0.85. That is only 15 % of the incident atoms on the growing surface are incorporated. Due to the segregation effect, the Indium composition reaches asymptotically towards the desired composition as additional layers are deposited. If at any point the total thickness of the segregated Indium exceeds 1.7 ML and the Indium composition in the growing layer is > 25 %, the growth mode changes from 2D to 3D. Hence minimization of Indium surface segregation is required. Growth at low temperature reduces Indium segregation [20, 21]. Indium surface segregation is also reduced by high Arsenic flux (beam equivalent pressure ~ 10^{-5} torr) and high growth rates (~1-1.5 μm/hr) [22].

These techniques to control the surface morphology are effective in reducing the onset of 3D growth when the equilibrium island size L in the layer-by-layer growth mode is larger than the surface diffusion length λ. However for highly strained layers (Misfit > 3.5 %), the equilibrium island

size L is comparable or even less than λ. In this case these techniques are not effective.

2.3.2. Reducing Strain Relaxation during Strained InGaAs growth

As discussed in the previous section, maintaining a 2D surface morphology minimizes the dislocation generation processes occurring at the epitaxial surface. However, as described before, strain relaxation also occurs due to formation of misfit dislocations at the heteroepitaxial layer/substrate interface. In this section, approaches used to minimize this mode of strain relaxation will be discussed.

Effect of growth mode on strain relaxation

Growth of highly strained InGaAs (f > 2 %) at high temperatures (~500 °C) results in strain relaxation by growth in 3D mode. The roughening of the growth surface also allows partial relaxation of strain by purely elastic deformation of the film. Dislocation nucleation can also occur due to the change in growth mode. This is because dislocation nucleation is easier at high stress points in the rough surface. The dislocation nucleation rate at a rough surface, $R_{surface}$ can be approximated as [23],

$$R_{surface} \propto De^{-U_{surface}\varepsilon^{-4}/kT} \tag{2.6}$$

whereas the dislocation nucleation rate in the bulk, R_{bulk} can be approximated as,

$$R_{bulk} \propto e^{-U_{bulk}\varepsilon^{-1}/kT} \tag{2.7}$$

In the above equations, $U_{surface}$ and U_{bulk} are the activation energies, D is the surface diffusion coefficient and ε is the lattice-mismatch. Therefore at high lattice mismatches, dislocation nucleation at high stress points exceeds the

dislocation nucleation in the bulk or at the interface. This has been experimentally demonstrated in the case of $In_{0.3}Ga_{0.7}As$ growth on GaAs at a growth temperature of 510 °C [24].

It has been shown that most of the misfit dislocations generated in highly strained InGaAs grown at high temperature are pure edge type misfit dislocations. Highly strained InGaAs grows in an island mode. High stress concentrations at island edges result in the formation of dislocation half-loops that give rise to 60° or mixed misfit dislocations. Edge type dislocations are formed by interaction of the 60° dislocations during the coalescence of 3D islands [25, 26]. These dislocations are sessile that is, they cannot glide on the {111} plane. Hence they will not contribute to strain relaxation. Therefore it is necessary to minimize the formation of edge type dislocations by maintaining a 2D growth mode. Also as a consequence of being sessile, the thread ends of these edge type dislocations cannot glide. Therefore this results in an epitaxial layer with high threading dislocation density.

Conventional models for critical thickness assume a FM or layer-by-layer growth mode. However for highly mismatched layers which typically have critical thicknesses < 50 Å, the contribution of surface energies to the process of dislocation generation and strain relaxation is significant. The equation for calculation of critical thickness that includes surface energy effects is given as follows [10],

$$\varepsilon = \frac{(1-\nu)}{2\mu(1+\nu)h\cos\lambda}\left\{\frac{\mu b\left(1-\nu\cos^2\alpha\right)}{4\pi(1-\nu)}\left[\ln\left(\frac{h}{b}\right)+1\right]-\sigma b\sin\alpha\right\} \quad (2.8)$$

In the above equation all the parameters are same as those in equations 2.1-2.4. The term σ is the surface energy term and has a value of 0.5 to 1.0 J/m^2. The term σb sin α can be interpreted as the energy lost by the creation of

a surface step when a misfit dislocation is formed. Figure 2.4 shows the variation of critical thickness as a function of Indium composition taking into account surface energy effects. The lower curve takes into account surface energy effects. From the percentage difference in the two models it is clear that at high lattice mismatches the contribution of the surface energy term is significant. It is important to consider that any model that is used to calculate the critical thickness inspite of its elaborateness is an equilibrium model. On the other hand epitaxial growth by techniques likes MBE and MOCVD are highly non-equilibrium processes and hence under the right conditions dislocation generation can be suppressed, thus resulting in an experimental critical thickness that is higher than theoretically calculated values.

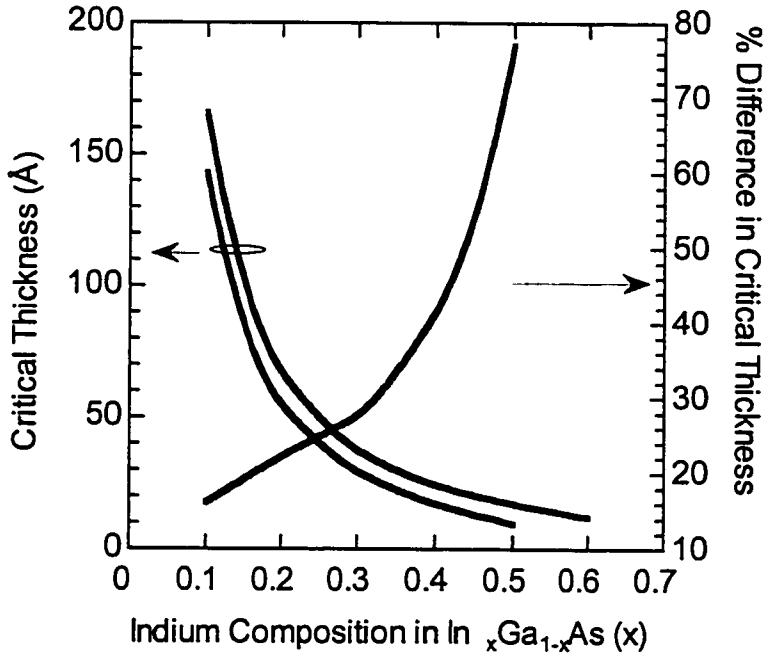


Figure 2.4: Comparison of Calculated Critical Thickness of InGaAs on GaAs with and without surface energy consideration. Also shown is the % difference in calculated critical thickness between the two models

Effect of growth temperature on strain relaxation

The growth temperature affects the strain relaxation in three ways, through surface morphology and thermally activated nucleation and propagation of defects. The 2-D to 3-D growth mode transition is delayed by reducing the growth temperature to maintain the 2D growth mode. The onset of 2D-3D growth transition for $In_{0.36}Ga_{0.64}As$ is increased from 15 Å to 55 Å when the growth temperature is reduced from 570 °C to 470 °C [27]. The persistence of 2D growth mode ensures that edge-type dislocations are not nucleated. Also surface related dislocation generation mechanisms are suppressed.

Under these conditions, thermally activated glide of substrate threading dislocations to form misfit dislocation segments at the substrate-epitaxial interface is the most dominant mechanism of strain relaxation. The most obvious way to minimize strain relaxation is to prevent this process. Price has shown that critical thickness of InGaAs (x>0.25) increases rapidly with the reduction of growth temperature below 480 °C [28]. This is due to Peierls-Nabarro friction stress that impedes dislocation movement at low growth temperatures [1]. The Peierls-Nabarro frictional force that opposes dislocation motion is expressed by the following equation.

$$F_{friction} = Ahe^{-U/kT} \tag{2.9}$$

where A is a constant, h is the film thickness and U is the activation energy which is typically 2.3 eV. Figure 2.5 shows the variation of calculated critical thickness as a function of growth temperature for various InGaAs compositions on GaAs.

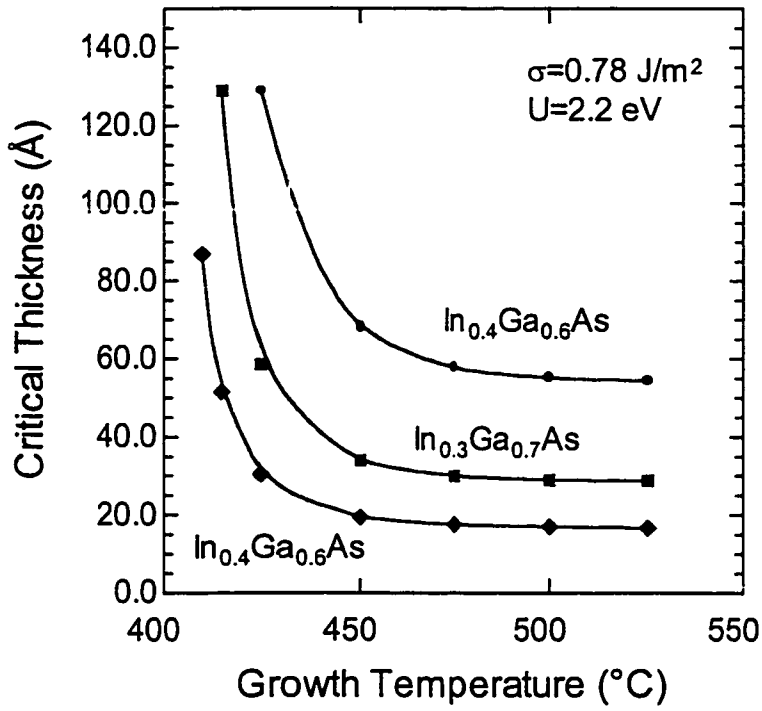


Figure 2.5: Variation of calculated critical thickness of $In_xGa_{1-x}As$ on GaAs substrate as a function of growth temperature

Also a low growth temperature reduces the probability of thermally activated nucleation sources.

Reducing Dislocation Sources

As described before, in the case of highly strained layers where the growth mode is 3D, dislocation nucleation can occur at surface pits and grooves since these are points of large stress. The control of the growth mode and the use of low growth temperatures ensures that nucleation of new dislocations is minimized. Hence under these conditions, strain relaxation in

heteroepitaxial layers is mainly limited by the nucleation of dislocations [23]. This is due to the high activation energy barrier to the nucleation of homogeneous dislocations [29]. In practical cases, most dislocations are generated at heterogeneous sources like particulates or by extension of substrate threading dislocations. These particulates and threading dislocations (TD) are a low-activation-energy nucleation source of dislocations.

Assuming that all other heterogeneous sources of dislocation nucleation are suppressed, the only way misfit dislocations can form is by the glide of substrate threading dislocations. Hence to minimize strain relaxation it is necessary to use low TD density substrates. The TD density in GaAs substrates depends on the method of crystal growth. The etch-pit density (EPD) in a substrate is a measure of TD density in a substrate. Table 2.2 compares the EPD counts of GaAs substrates grown by various techniques like Liquid Encapsulated Czochralski (LEC) and Vertical Gradient Freeze (VGF) [30].

Substrate Type	Defect Density (Typical)	Defect Density (Substrates used at UCSB)
Si Wafer	100 / cm^2	
N-type GaAs VGF substrate	200 /cm^2	200 /cm^2
P-type GaAs VGF substrate	2000 /cm^2	1400 /cm^2
SI GaAs VGF substrate	4000/cm^2	1100/cm^2
SI GaAs LEC substrate	70000 /cm^2	50000 /cm^2

Table 2.2: Comparison of TD/Defect Densities in GaAs Substrates grown by different methods. Note that the defect densities are much higher than elemental Si semiconductor substrates.

The superior quality of VGF substrates is due to low thermal gradient during crystal growth and a more thermodynamically stable mode of crystal growth [31]. X-ray diffraction shows that VGF substrates have smaller mosaic

spread than LEC substrates. Klem et al. demonstrated that for highly metastable structures, the MD density is a sensitive function of substrate quality [32]. Kui et al. observed that during growth of $In_{0.1}Ga_{0.9}As$ epilayers on a GaAs substrate, a crosshatched surface morphology was observed on substrates with higher EPDs (10000 /cm^2), whereas no cross-hatching was observed on lower EPD substrates (< 1000 /cm^2) [33]. Misfit dislocation density in GaAs pHEMT channel layers is lower on low threading dislocation substrates, indicating that substrate-threading dislocations are a major source of misfit dislocation [34]. Misfit dislocations have also been shown to originate from inhomogeneous sources like particulates on the wafer surface and oval defects caused by Ga spitting. The inhomogeneous sources can give rise to more than one misfit dislocation segments [35]. Unless misfit dislocation from inhomogeneous sources is reduced, using low TD substrates does not help in reducing the strain relaxation in as-grown LES templates.

Other Approaches

Critical thickness can also be increased by growing on patterned substrates [36]. Patterning a substrate isolates the epitaxial growth between regions with dislocation sources and those without dislocation sources. The absence of low activation energy dislocation sources in these areas delays the formation of dislocations thereby increasing the critical thickness. Growing at a higher growth rate can also minimize strain relaxation. This reduces the total time that the strained layer spends at a high growth temperature. Thus even if the process of glide of TD is started; there is not enough time for the creation of MD segments and cause strain relaxation.

2.4. Growth conditions for LES Templates

All the techniques discussed above were used to minimize the strain relaxation in the as-grown InGaAs Lattice-Engineered Substrate (LES) templates. The epitaxial structures investigated consisted of strained $In_xGa_{1-x}As$ template layers grown on AlAs oxidation layer on a n-type GaAs substrate in a Varian Gen II molecular beam epitaxy system. After oxide desorption from the GaAs substrate, a high temperature GaAs buffer was grown at 580 °C. After this a low-temperature (LT) GaAs buffer is grown at 250 °C and a 500 Å AlAs oxidation layer grown at 650 °C. The LT GaAs buffer was grown beneath the AlAs layer to assist in oxidation.

2.4.1. $In_xGa_{1-x}As$ Lattice Engineered Substrates

The strained $In_xGa_{1-x}As$ layers were grown directly on the AlAs oxidation layers. The thicknesses of the different $In_xGa_{1-x}As$ layers used were 1000 Å $In_{0.2}Ga_{0.8}As$, 760 Å $In_{0.3}Ga_{0.7}As$ and 480 Å $In_{0.4}Ga_{0.6}As$ respectively. These thicknesses are roughly 20 times the Matthews-Blakslee critical thickness of $In_xGa_{1-x}As$ (x=0.2, 0.3, 0.4) on GaAs substrate. As described before, the $In_xGa_{1-x}As$ template layers were grown at low temperature to minimize the formation of threading dislocations and maintain a two-dimensional growth-front. The growth temperature was varied from 300 °C to 400 °C.

The $In_xGa_{1-x}As$ layers were capped with a 30 Å AlAs etch stop layer and 200 Å GaAs cap layer to protect it during oxidation. The etch stop and cap layers are grown at the same temperature as that of the InGaAs template. It was observed that the use of growth interrupts during the growth of the thick,

highly strained InGaAs layers resulted in a spotty RHEED pattern. This is possibly due to formation of 3D islands by the segregated Indium on the growing surface. This is undesirable as this may result in the generation of dislocations at the surface and also result in a rough surface that is not ideal for subsequent regrowth. To prevent this, no growth interrupts were used after the growth of the strained InGaAs layer was initiated. As a result the segregated Indium on the surface is incorporated to some extent in the AlAs etch stop and the GaAs cap layers. Table 2.3 summarizes the growth conditions for InGaAs LES Templates. This chapter will mainly concentrate on the growth conditions and their effect on the characteristics of the InGaAs layers. The discussion on the design of the oxidation layer and the effect of the LT GaAs buffer can be found in Chapter 3. Processing considerations determine the design of the AlAs etch stop layer and the GaAs cap layer and are discussed in Chapter 4.

Layer Description	Thickness	Growth Temperature	Growth Rate
GaAs Buffer	2000 Å	580 °C	1.0 μm/hr
LT GaAs Buffer	2000 Å	250 °C	1.0 μm/hr
AlAs Oxidation Layer	500 Å	630 °C	0.5 μm/hr
Summary of Growth Conditions for $In_xGa_{1-x}As$ Lattice Engineering Layers			
$In_{0.2}Ga_{0.8}As$ Template	1000 Å	375, 400, 430 °C	1.0 μm/hr
$In_{0.3}Ga_{0.7}As$ Template	760 Å	375, 400, 430 °C	1.14 μm/hr
$In_{0.4}Ga_{0.6}As$ Template	480 Å	300, 375, 430 °C	1.33 μm/hr
AlAs Etch Stop Layer	30 Å	Same as InGaAs Template	0.5 μm/hr
GaAs cap Layer	200 Å	Same as InGaAs Template	0.8 μm/hr

Table 2.3: Summary of Growth Conditions for InGaAs LES Templates

Note that the growth temperature has to be progressively lowered with increasing lattice mismatch to suppress formation of threading dislocations and

prevent islanding. Further lowering of the growth temperature is undesirable as it results in a rough surface morphology due to the low mobility of atoms on the growing surface.

2.4.2. $GaAs_{1-y}Sb_y$ Lattice Engineered Substrates

Like the InGaAs alloys, GaAsSb alloys are also capable of covering lattice constants from GaAs to GaSb (InAs). Hence lattice-engineered substrates are also be made with GaAsSb template layers. There have been very few reports of GaAsSb growth on GaAs substrates; this is mainly due to the inability to control the Sb_4 fluxes in the conventional effusion cells in molecular beam epitaxy. However with the introduction of the valved cracker cell for Sb, it is possible to control the composition of GaAsSb alloys precisely. It is important to note that unlike InGaAs growth, the Sb composition also depends on the growth temperature. In contrast to low temperature growth of InGaAs, there are very few reports of low temperature growth of mixed arsenide-antimonide materials [37].

All the strained GaAsSb layers were grown at a temperature of 400 °C, the growth conditions for other layers in the LES template are same as that of the InGaAs LES templates. Table 2.4 summarizes the growth conditions for GaAsSb epitaxial layers.

Sample #	As_2 Flux	Sb_2 Flux	Growth Temperature	Sb mole fraction
991102	5.22×10^{-6}	9.36×10^{-8}	400 °C	0.09
991103	4.87×10^{-6}	1.4×10^{-7}	400 °C	0.12
991104	4.12×10^{-6}	1.9×10^{-7}	400 °C	0.25
991117	4.12×10^{-6}	1.9×10^{-7}	400 °C	0.25
991214	4.12×10^{-6}	1.9×10^{-7}	375 °C	0.23

Table 2.4: Growth Conditions for GaAsSb Template Layers

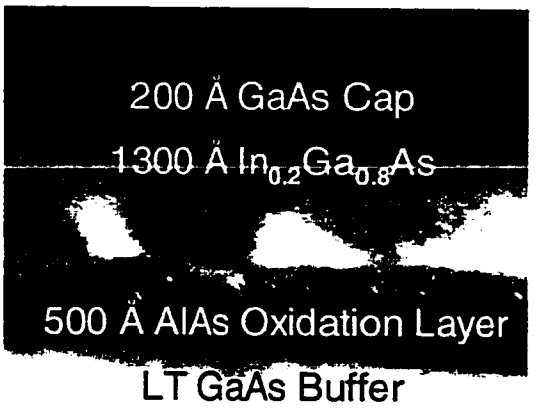
2.5. Structural Characterization of LES Templates

2.5.1. TEM Characterization of LES Templates

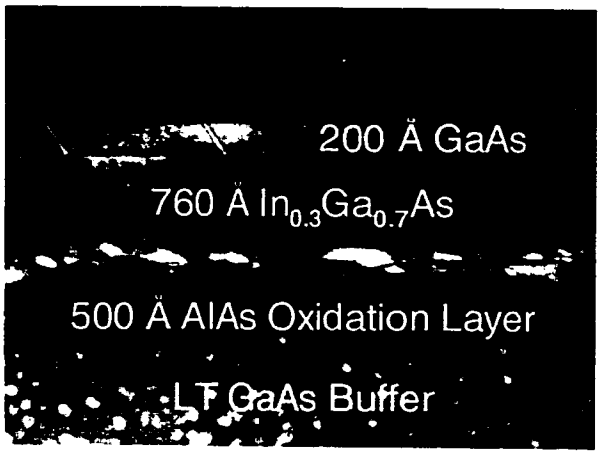
Cross-sectional TEM Analysis

Figure 2.6 shows the cross-sectional TEM micrographs of an $In_{0.2}Ga_{0.8}As$, $In_{0.3}Ga_{0.7}As$ and $In_{0.4}Ga_{0.6}As$ LES Templates respectively. Though a few misfit dislocations are observed at the AlAs/InGaAs interface, there are no threading dislocations in the InGaAs template layers. The contrast in the TEM micrograph indicates that the InGaAs epitaxial layer is under strain. These particular LES templates were grown at 430 and 400 °C respectively. Hence it can be concluded that InGaAs epitaxial layers grown at lower growth temperatures also have low threading dislocation density. Cross-section TEM micrographs of a 120 Å thick $In_{0.3}Ga_{0.7}As$/GaAs heterostructure grown at 550 °C shows inhomogeneous strain contrast [38]. The upper interfaces are inhomogeneously strained indicating 3D island growth. However in Figure 2.6 no such strain contrast is observed at the upper interface indicating that the growth mode is still 2-dimensional. It can also be seen that

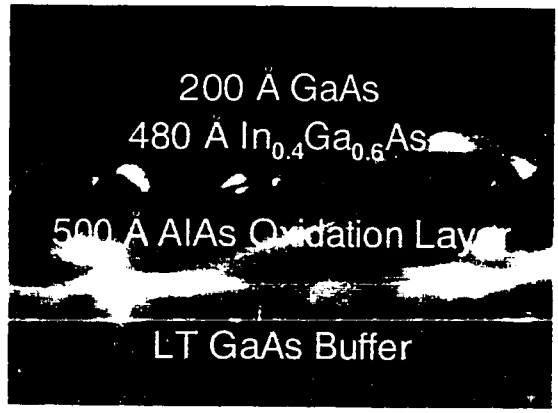
as the lattice-mismatch is increased strain contrast is observed in the lattice-matched AlAs oxidation layer.



$In_{0.2}Ga_{0.8}As$ LES Template – T_{growth}= 430 °C



$In_{0.3}Ga_{0.7}As$ LES Template – T_{growth}= 430 °C



$In_{0.4}Ga_{0.6}As$ LES Template – T_{growth}= 400 °C

Figure 2.6: Cross-sectional TEM Micrographs of InGaAs LES Templates

(Sample Preparation and TEM Analysis done by Dr. Lijie Zhao)

Plan View TEM Analysis

While cross-sectional TEM is useful to observe the vertical distribution of dislocations in a heterostructure, plan view TEM (PVTEM) enables the investigation of the misfit dislocation network at a lattice-mismatched interface. Figure 2.7 shows the plan-view TEM micrograph of a 1000 Å thick $In_{0.2}Ga_{0.8}As$ LES template grown at 430 °C. The misfit dislocation density at the $In_{0.2}Ga_{0.8}As$/AlAs interface as calculated from the PVTEM is 1.3 x 10^5 /cm. No threading dislocations were observed in the PVTEM image indicating that the TD density in these layers is below 10^5 /cm^2. These dislocation densities are typical of those observed in literature. The MD density for 750 Å $In_{0.25}Ga_{0.75}As$ epitaxial layers grown at 500 °C is 1.2-1.4 x 10^5/cm [39]. Misfit dislocations were first observed at an epilayer thickness equal to $5h_{critical}$. Lavoie et al. reported an MD density of 9 x 10^4 /cm in 830 Å $In_{0.18}Ga_{0.82}As$ (~$10h_{critical}$) epitaxial layers grown at 490 °C [40].

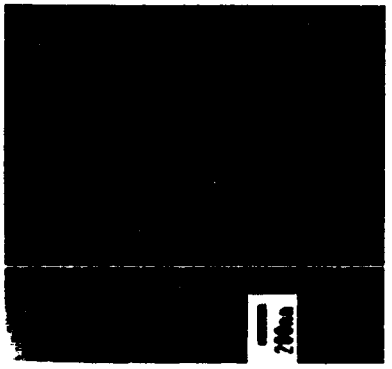


Figure 2.7: Plan-View TEM Micrograph of $In_{0.2}Ga_{0.8}As$ LES Template

(Sample Preparation and TEM Analysis done by Sheila Mathis)

2.5.2. Surface Morphology of LES Templates

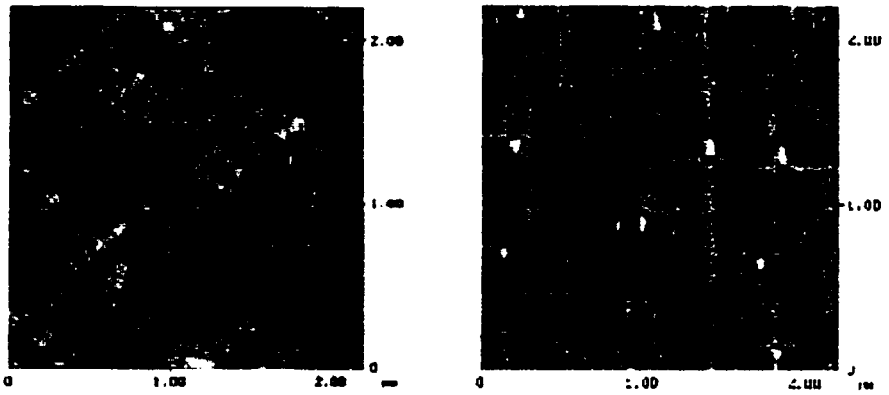
Since there is a close correlation between surface morphology and strain relaxation, surface morphology is a good indicator of material quality. The dislocation generation and glide processes occurring at the substrate-heteroepitaxial layer interface influence the surface morphology. The two types of surface morphologies observed in moderately lattice-mismatched epitaxial systems are the cross-hatched surface morphology which is observed when the growth mode is layer by layer and a rough surface morphology which is indicative of growth in island mode.

Various models have been proposed to explain the occurrence of crosshatched surface morphology in lattice-mismatched epitaxial systems. Lutz et al. proposed that surface steps arising from formation of 60° misfit dislocations result in a crosshatched surface [41]. Albrecht et al. proposed that the crosshatched surface is due to locally enhanced growth rate above the

misfit dislocation. Thus the crosshatched surface morphology is a consequence of plastic relaxation i.e. strain relaxation due to the formation of dislocations.

However a rough or undulating surface also enables the accommodation of lattice mismatch by elastic relaxation [13]. Elastic strain relaxation by means of a surface undulation is also a function of lattice mismatch and growth conditions.

Figure 2.8 shows the AFM scan of $In_{0.2}Ga_{0.8}As$ templates and Table 2.5 lists the surface roughness and peak-to-peak values obtained from the AFM scan.



1300 Å $In_{0.2}Ga_{0.8}As$ Epitaxial Layer
T_{growth}=430 °C/SI-VGF Substrate

1000 Å $In_{0.2}Ga_{0.8}As$ Epitaxial Layer
T_{growth}=430 °C/n-VGF Substrate

Figure 2.8: AFM Scans of $In_{0.2}Ga_{0.8}As$ LES Templates

(AFM Scans done by Dr. Stacia Keller)

As expected, crosshatched surface morphology is observed for the thicker $In_{0.2}Ga_{0.8}As$ template. However there is no evidence of island growth mode (as seen later for higher lattice mismatches). No crosshatched surface morphology is observed when the layer thickness is reduced to 1000 Å as seen

on the right hand side of Figure 2.8. This may be due to a combination of two factors, the first being the lower layer thickness and second being the n-VGF substrates which has a lower defect density and consequently lower MD nucleation sites.

Layer Composition (Sample #)	Growth Temperature	Thickness	RMS Roughness	Peak to Peak
$In_{0.2}Ga_{0.8}As$ (980705)	430 °C	1300 Å	4.6 Å	48 Å

Table 2.5: AFM Analysis of $In_{0.2}Ga_{0.8}As$ LES Templates

The surface roughness values are much lower than the values reported for low-mismatch InGaAs epitaxial layers on GaAs substrates in the literature. Lavoie et al. reported a RMS surface roughness of 10.2 Å for $In_{0.2}Ga_{0.8}As$ epitaxial layers grown 490 °C [40]. Samonji et al. have reported rms roughness

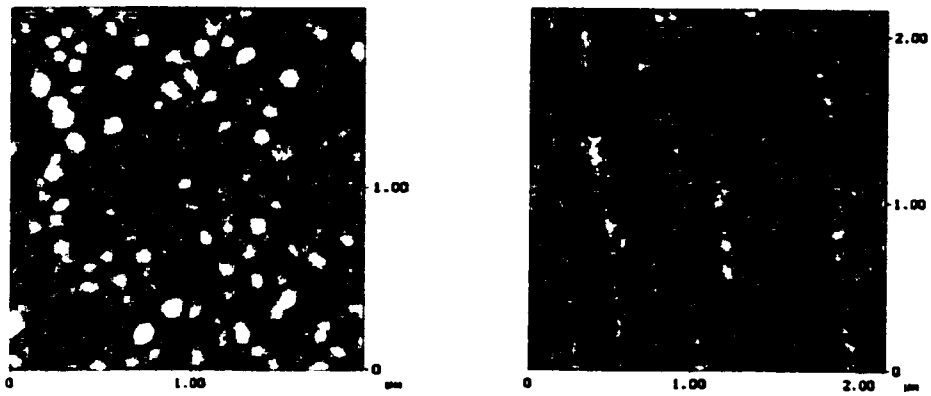


Figure 2.9: AFM Scans of $In_{0.3}Ga_{0.7}As$ LES Templates (AFM Scans done by Dr. Stacia Keller)

of 10 Å for 2000 Å $In_{0.2}Ga_{0.8}As$ layers grown at 420 °C [42]. They observed a crosshatched surface morphology when the layer thickness exceeded 500 Å.

Figure 2.9 shows the surface morphology of $In_{0.3}Ga_{0.7}As$ LES templates and Table 2.6 lists the surface roughness and peak-to-peak values as obtained from the AFM scans.

As seen from the above figure, island growth mode is observed for $In_{0.3}Ga_{0.7}As$ epitaxial layers at 430 °C. Reducing the growth temperature to 400 °C results in reduction in size and density of these islands. The surface morphology is now crosshatched and similar to that of the $In_{0.2}Ga_{0.8}As$ LES Templates. However the density of the crosshatched lines is higher in the $In_{0.3}Ga_{0.7}As$ templates, which is an obvious consequence of the higher mismatch.

Layer Composition (Sample #)	Growth Temperature	Thickness	RMS Roughness	Peak to Peak
$In_{0.3}Ga_{0.7}As$ (980702)	430 °C	760 Å	6.4 Å	51 Å
$In_{0.3}Ga_{0.7}As$ (981005)	430 °C	910 Å	7.3 Å	133 Å
$In_{0.3}Ga_{0.7}As$ (990310)	400 °C	760 Å	4.0 Å	70 Å
$In_{0.3}Ga_{0.7}As$ (991116)	375 °C	760 Å	3.0 Å	24 Å

Table 2.6: AFM Analysis of $In_{0.3}Ga_{0.7}As$ Templates

From the roughness analysis of the AFM scans, it is clear at as the growth temperature is reduced the rms surface roughness is reduced. This is due to a reduction in strain relaxation and also reduced Indium surface segregation. Cullis et al have investigated the surface morphology of $In_{0.3}Ga_{0.7}As$ epitaxial layers grown on GaAs substrates at a growth temperature of 580 °C [43]. AFM analysis of these layers showed a rippled surface morphology that is consequence of island growth mode and the consequent

elastic relaxation. The surface morphology of thin layers (50 Å) consists of elongated islands that coalesce to form an array of linear ridges. The typical height of surface features is 100-200 Å. Lower growth temperatures in the LES templates results in the suppression of these effects. Also the peak-to-peak height variation for much thicker layers (760 Å v/s 50 Å) is significantly lower.

Increasing the lattice-mismatch make it difficult to maintain layer-by-layer growth mode as seen in the case of $In_{0.4}Ga_{0.6}As$ LES templates. Figure 2.10 shows the

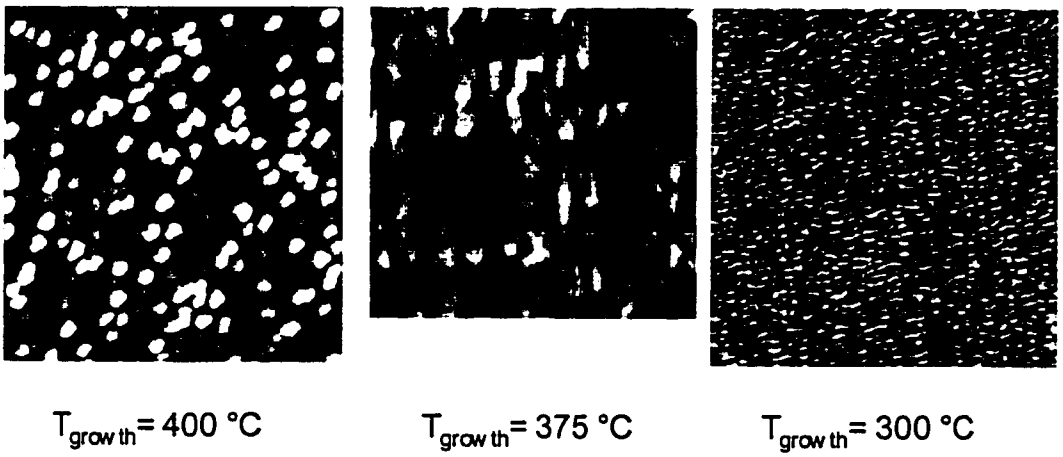


Figure 2.10: AFM Scans of $In_{0.4}Ga_{0.6}As$ LES Templates (AFM Scans Done by Dr. Stacia Keller)

AFM scans of $In_{0.4}Ga_{0.6}As$ LES Templates grown at various temperatures.

As seen from the figure above, a rough surface morphology is observed even at growth temperatures as low as 400 °C. Note at these growth temperatures LES templates with lower Indium compositions displayed layer-by-layer growth mode. Lowering the growth temperature to 375 °C eliminates the rough growth surface, but in this case a ripple surface is observed, which

indicates some degree of elastic strain relaxation. At growth temperatures of 300 °C again a rough surface morphology is observed which is a consequence of low adatom mobility on the growing surface. Table 2.7 lists the surface roughness and peak-to-peak heights as obtained from the AFM scans.

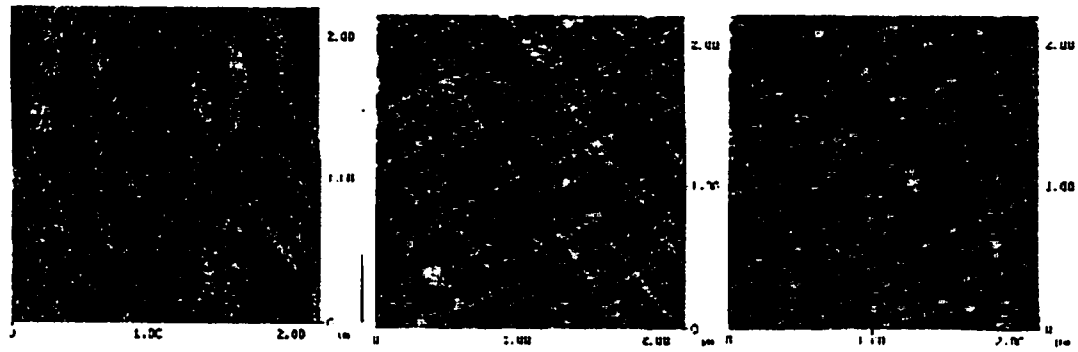
Layer Composition (Sample #)	Growth Temperature	Thickness	RMS Roughness	Peak to Peak
$In_{0.4}Ga_{0.6}As$ (980704)	400 °C	480 Å	24 Å	204 Å
$In_{0.4}Ga_{0.6}As$ (981004)	375 °C	480 Å	8.3 Å	77 Å
$In_{0.4}Ga_{0.6}As$ (990139)	300 °C	480 Å	7.0 Å	79 Å

Table 2.7: Analysis of AFM Scans of $In_{0.4}Ga_{0.6}As$ LES Templates

The rms surface roughness and the peak-to-peak height are both reduced as the growth temperature is lowered. From the analysis of surface morphology of InGaAs LES Templates it is clear that as the lattice mismatch is increased three factors impact the surface morphology. The first is the generation of misfit dislocations, the strain fields of which impact the surface morphology. The second is the occurrence of the 3D or island growth mode which the equilibrium growth mode for lattice mismatched systems. The third is the phenomenon of Indium segregation on the surface that results in a rough surface.

Lowering the growth temperature aids in suppression of dislocation formation and island growth mode, however it does not prevent Indium segregation that has been observed at growth temperatures as low as 300 °C. One way to suppress the Indium segregation is using a high V/III flux ratio, but this reduces the mobility of adatoms on the growing surface that results in a rough surface.

Replacing the Group III In atom by the group V Sb atom to achieve the same lattice constant can eliminate the tradeoff associated with lower growth temperatures. To investigate this GaAsSb LES Templates with various Indium compositions were grown at 400 °C. The other layers in the LES Template were grown under the same condition as before. Figure 2.11 shows the AFM scans of GaAsSb templates with various Sb compositions.



$GaAs_{0.91}Sb_{0.09}$ $GaAs_{0.88}Sb_{0.12}$ $GaAs_{0.75}Sb_{0.25}$

Figure 2.11: AFM Scans of $GaAs_{1-y}Sb_y$ LES Templates grown at 400 °C

(AFM Scans done by Dr. Stacia Keller)

For lower lattice mismatches step flow growth mode is observed, however as the lattice mismatch is increased a crosshatched surface morphology is observed. Table 2.8 shows the rms roughness and peak-to-peak surface roughness values obtained from the AFM scans for the GaAsSb LES Templates.

Layer Composition (Sample #)	Growth Temperature	Thickness	RMS Roughness	Peak to Peak
$GaAsSb_{0.10}$ (991102)	400 °C	1300 Å	2.4 Å	18 Å
$GaAsSb_{0.13}$ (991103)	400 °C	760 Å	2.9 Å	24 Å
$GaAsSb_{0.27}$ (991104)	400 °C	480 Å	5 Å	41 Å
$GaAsSb_{0.27}$ (991117)	400 °C	760 Å	5 Å	39 Å

Table 2.8: Analysis of AFM Scans for $GaAs_{1-y}Sb_y$ LES Templates

From the above table it is clear that much lower rms surface roughness values are obtained for GaAsSb templates compared to the InGaAs templates. For example the peak-to-peak height variation of a 20 $h_{critical}$ thick $GaAs_{0.73}Sb_{0.27}$ template (991117) is only 39 Å compared to 70 Å for an $In_{0.3}Ga_{0.7}As$ template grown at the same temperature. Though the same dislocation generation and growth mode effects hold in the case of GaAsSb template, there is no segregation of Sb on the surface. The alloy component deciding the composition is now a group V element, hence any unincorporated Sb will result only in excess V/III ratio and also may act as a surfactant resulting in a smooth surface morphology.

2.5.3. X-Ray characterization of LES Templates

The LES templates were characterized by X-ray diffraction to determine the extent of strain relaxation. The degree of strain relaxation can be calculated by finding the in-plane and out-of-plane lattice constant of the strained epilayer. The procedure is calculated from the peak separation of the off-axis 115 and $\overline{1}\overline{1}5$ reflections. The in-plane and out-of-plane lattice constants are calculated as follows [44],

$$\Delta\phi = \frac{1}{2}(\Delta\omega_A - \Delta\omega_B) \tag{2.10}$$

$$\Delta\theta = \frac{1}{2}(\Delta\omega_A + \Delta\omega_B) \tag{2.11}$$

where $\Delta\omega_A$ and $\Delta\omega_B$ are the separations between the substrate and epilayer peak for $\bar{1}\,\bar{1}5$ and 115 diffraction conditions respectively. From $\Delta\Phi$ and $\Delta\theta$, the in-plane and perpendicular lattice constants are calculated as follows,

$$\left(\frac{\Delta a}{a}\right)_{\perp} = \Delta\phi\tan\phi - \Delta\theta\cot\theta \tag{2.12}$$

$$\left(\frac{\Delta a}{a}\right)_{\parallel} = -\Delta\phi\cot\phi - \Delta\theta\cot\theta \tag{2.13}$$

For the 115 off-axis reflections, θ=45.071° and Φ=15.79°, the angle between the 001 and 115 planes. From the in-plane and out-of-plane lattice constants the lattice constant of the relaxed epitaxial layer is calculated as follows,

$$\left(\frac{\Delta a}{a}\right)_r = \left(\frac{1-\nu}{1+\nu}\right)\left(\frac{\Delta a}{a}\right)_{\perp} + \left(\frac{2\nu}{1+\nu}\right)\left(\frac{\Delta a}{a}\right)_{\parallel} \tag{2.14}$$

In the above equation v is the Poisson ratio. Therefore the percentage strain relaxation is given by,

$$R = \left(\left(\frac{\Delta a}{a}\right)_{\parallel} \Big/ \left(\frac{\Delta a}{a}\right)_r\right) \times 100 \tag{2.15}$$

The full-width at half-maximum width (FWHM) of the epitaxial layers is also an indicator of material quality. In the case of LES templates the FWHM increases from 339 arcsec for an $In_{0.2}Ga_{0.8}As$ template to 513 arcsec for an $In_{0.3}Ga_{0.7}As$ template. For an $In_{0.4}Ga_{0.6}As$ template the FWHM is 992 arcsec. The increase in FWHM is due to broadening associated with the decreasing layer thickness. Broadening may also be due non-uniform strain

relaxation and tilting associated with strain relaxation and higher dislocation densities as the lattice mismatch increases [45].

From the x-ray diffraction data misfit dislocation (MD) density at the InGaAs/AlAs interface can be calculated. Table 2.9 shows the critical thickness of the InGaAs templates and the predicted equilibrium MD density for the given layer thickness. The equilibrium MD density is given by the following equation,

$$\rho_{MD} = \frac{f}{b\cos\lambda}\left[1 - \frac{h_c}{h}\right] \qquad (2.16)$$

where f is the misfit strain, b is the Burgers vector, $\lambda = 60°$, h_c and h are the critical thickness and layer thickness respectively. Here the most comprehensive model for critical thickness that considers temperature and surface energy effects is used.

	Critical thickness (h_c)	*Layer thickness*	*Equilibrium MD density*
$In_{0.2}Ga_{0.8}As$	77 Å	1000 Å	9.8×10^5 /cm
$In_{0.3}Ga_{0.7}As$	39 Å	760 Å	1.01×10^6 /cm
$In_{0.4}Ga_{0.8}As$	23 Å	480 Å	1.35×10^6 /cm

Table 2.9: Critical Thickness and Equilibrium MD Density of LES Templates

Since the growth conditions are far from equilibrium the InGaAs layers do not relax completely. Hence the equilibrium MD density cannot be achieved. Table 2.10 lists the observed MD density and the predicted MD density based on strain relaxation of as-grown InGaAs LES templates. It is also important to note that the equilibrium MD densities can never be achieved due to dislocation interaction effects (discussed in Chapter 3). The maximal MD

density that was achieved in the $In_{0.2}Ga_{0.8}As/GaAs$ structure was 6.1 x 10^5 /cm [46].

	Observed MD Density (From PVTEM)	*Calculated MD Density (From X-Ray Diffraction)*	*Equilibrium MD density*
$In_{0.2}Ga_{0.8}As$	1.67 x 10^5/cm	1.05 x 10^5 /cm	9.8 x 10^5 /cm
$In_{0.3}Ga_{0.7}As$	*NA*	1.47 x 10^5 /cm	1.01 x 10^6 /cm
$In_{0.4}Ga_{0.8}As$	NA	3.64 x 10^5 /cm	1.35 x 10^6 /cm

Table 2.10: Comparison between calculated and observed MD Densities in LES Templates

Effect of growth temperature and substrate quality on strain relaxation in LES Templates

Table 2.11 compares the strain relaxation data for $In_{0.2}Ga_{0.8}As$ LES Templates as a function of growth temperature and substrate type.

Sample #	Layer Thickness	Substrate Type	InGaAs Growth T	% Strain relaxation
990138	1300 Å	SI-VGF	430 °C	48 %
990320	1300 Å	SI-VGF	400 °C	40 %
980418	1000 Å	SI-VGF	430 °C	48 %
980725	1000 Å	n-VGF	430 °C	27 %
991148	1000 Å	n-VGF	375 °C	19 %

Table 2.11: Strain Relaxation Data for $In_{0.2}Ga_{0.8}As$ LES Templates

It is clear that the strain relaxation in the as-grown LES template reduces with growth temperature and the degree of strain relaxation is smaller in LES templates grown on low defect density (n-type VGF) substrates. The strain relaxation values reported here are similar to those obtained for

$In_{0.2}Ga_{0.8}As$ epitaxial layers grown at 420 °C, where 1000 Å thick layer had a strain relaxation of 42% [42]. Table 2.12 compares the strain relaxation data for $In_{0.3}Ga_{0.7}As$ LES Templates.

Sample #	Layer Thickness	Substrate Type	InGaAs Growth T	% Strain relaxation
980702	760 Å	SI-VGF	430 °C	47 %
980735	760 Å	n-VGF	430 °C	28 %
990527	760 Å	n-VGF	400 °C	25 %
990528	760 Å	n-VGF	350 °C	17 %

Table 2.12: Strain Relaxation Data for $In_{0.3}Ga_{0.7}As$ LES Templates

Strain relaxation follows similar trends as in the case of the $In_{0.2}Ga_{0.8}As$ LES Templates. The large difference in the degree of strain relaxation for similar epitaxial layers grown on SI-VGF (EPD=1200 /cm^2) and n-VGF (EPD=200 /cm^2) substrates suggests the dominant role of dislocation nucleation sources in the process of strain relaxation.

Sample #	Layer Thickness	Substrate Type	InGaAs Growth T	% Strain relaxation
980704	480 Å	SI-VGF	400 °C	51 %
981004	480 Å	n-VGF	375 °C	43 %
990139	480 Å	n-VGF	300 °C	38 %

Table 2.13: Strain Relaxation Data for $In_{0.4}Ga_{0.6}As$ LES Templates

Table 2.13 shows the strain relaxation data for $In_{0.4}Ga_{0.6}As$ LES Templates. Due to the increased lattice mismatch the strain relaxation is higher for the same growth temperature. Also the reduction of growth temperature is

not as effective in reducing dislocation generation as seen in the case of lower Indium composition LES templates.

Sample #	Layer Thickness	% Strain relaxation
991102 ($GaAs_{0.91}Sb_{0.09}$)	1000 Å	0 %
991103 ($GaAs_{0.88}Sb_{0.12}$)	760 Å	9 %
991104 ($GaAs_{0.75}Sb_{0.25}$)	480 Å	14 %
991117 ($GaAs_{0.75}Sb_{0.25}$)	760 Å	31 %

Table 2.14: Strain Relaxation Data for GaAsSb LES Templates

Table 2.14 shows the strain relaxation data for GaAsSb LES templates grown at 400 °C. The degree of strain relaxation is comparable to InGaAs LES templates with the same lattice mismatch.

Tilt in LES Templates

During the lattice-mismatched growth of cubic semiconductor on (001) oriented substrates, MD segments are formed along the (110) and $(1\bar{1}0)$ directions. Dislocations lying along (110) have group III atoms at the core (α type) and those lying along $(1\bar{1}0)$ have group V atoms at the core (β type). Tilt in partially relaxed lattice mismatched layers is due to the abundance of one type of dislocations with respect to the other [47]. X-Ray diffraction in as-grown LES Templates revealed no such tilt.

2.6. Conclusions

This chapter discussed the MBE growth of LES Templates. Under the appropriate growth conditions the control of growth mode and dislocation

sources, the process of dislocation generation and propagation can be suppressed. This enables the growth of thick low threading dislocation density strained layers. Since these templates act as quasi-substrates for epitaxial regrowth, maintaining a smooth surface morphology is essential. Fortunately due to the interplay between strain relaxation and surface morphology, growth conditions which lead to reduced strain relaxation also result in a smooth surface morphology. The strain energy stored in the epitaxial layers can now act as a driving force for strain relaxation when the underlying AlAs layers are oxidized. This will be the subject of the next chapter.

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Chapter 3.

Strain Relaxation During Lateral Oxidation of AlAs

The lattice engineered substrate (LES) approach utilizes the process of relaxation of a coherent hypercritical thickness ($h >> h_{critical}$) strained semiconductor over-layer (InGaAs) in direct contact with an oxidizing Al-containing semiconductor (i.e. AlAs or AlGaAs). Figure 3.1 illustrates the schematic description of this process.

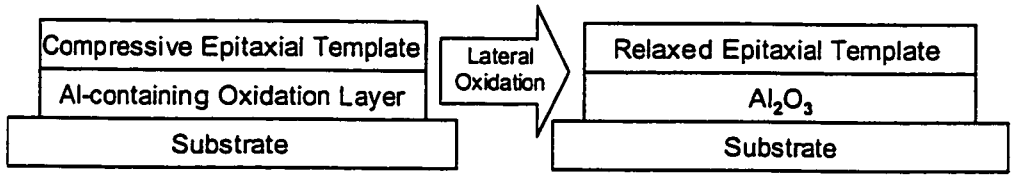


Figure 3.1: Schematic of LES Process

The process of lateral oxidation coverts the rigid epitaxial interface between the strained overlayer and the oxidation layer to a porous and reactive interface that enables extensive plastic strain relaxation due to efficient dislocation motion without interaction and generation of new dislocations. This results in the formation of a relaxed InGaAs template **(Lattice Engineered Substrate)** that is epitaxially decoupled from, but mechanically supported by the

underlying GaAs substrate. The structural changes in the semiconductor structure during lateral oxidation play an important role in the process of strain relaxation. The process of strain relaxation and the various factors affecting it will be discussed in this chapter.

The important factors affecting the process of strain relaxation are the lattice mismatch stress in the strained InGaAs overlayer, structural changes occurring during the process of lateral oxidation and the nature of dislocation interactions at the InGaAs/oxide interface. Section 3.1 discusses the basic mechanisms involved in the process of strain relaxation during heteroepitaxy, with the experimental observations for the InGaAs/GaAs and SiGe/Si material systems discussed in section 3.2. The conventional approaches to improve the efficiency of strain relaxation are discussed in section 3.3. In the recent past, other approaches like wafer bonding and amorphous interlayers have been investigated to improve heteroepitaxial growth. These approaches are discussed in section 3.4. Section 3.5 begins with a discussion the various structural changes occurring during the process of lateral oxidation. The oxidation kinetics of AlAs oxidation layers and the effect of addition of Group V elements like Sb are also presented. Section 3.6 discusses in detail the various factors affecting the strain relaxation during the process of lateral oxidation. The various approaches investigated to improve this process are presented. Also this approach is compared with other conventional approaches for heteroepitaxy.

3.1. Strain Relaxation Phenomena in Heteroepitaxy

3.1.1. Basics of Strain relaxation

The most benign process of strain relaxation occurs by glide of threading dislocation (TD) segments that creates misfit dislocation (MD) segments. The driving force for this glide is the lattice mismatch strain between the heteroepitaxial layer and the substrate. However misfit dislocations formed by other means can also relieve the mismatch. New misfit dislocations can be created by the interaction of two existing misfit dislocations. The process of island coalescence during 3-dimensional heteroepitaxial growth can also create dislocations.

However the most commonly observed dislocations in low-mismatch heteroepitaxial systems are 60° or mixed dislocations. Since they have both the edge and screw components, mixed dislocations can also accommodate lattice mismatch but are less efficient. Since strain relaxation occurs by glide process of TD ends of MD segments, it is important to consider which dislocations can glide and which cannot. In cubic semiconductors, the glide plane is {111}. Hence edge type dislocations cannot glide and cause further strain relaxation. Hence formation of 60° dislocations though less efficient is desired as their thread ends can glide and contribute to strain relaxation.

The lattice mismatch strain in a heteroepitaxial layer is distributed as

$$f = \varepsilon + \delta \qquad (3.1)$$

where ε is the residual elastic strain and δ is the plastic strain accommodated by misfit dislocations at the epilayer-substrate interface. For an unstrained (completely relaxed) heteroepitaxial layer, there is no in-built elastic strain

(ε=0), The lattice mismatch is entirely accommodated by dislocations at the epitaxial layer substrate interface. Therefore the interface misfit dislocation density p is given by

$$p = \frac{b}{2\delta} = \frac{b}{2f} \tag{3.2}$$

Here b is the magnitude of the Burgers vector and is typically 4 Å. As described before, the misfit dislocations are created by glide of TDs. Assuming that there are no other dislocation sources, the TD density (ρ_{TD}) does not depend on the lattice mismatch but depends on the average MD length $\langle L \rangle_{MD}$ and is given by the following expression [1],

$$\rho_{TD} = \frac{8f}{b\langle L \rangle_{MD}} \tag{3.3}$$

Therefore to achieve a low threading dislocation density, the average MD length should be very long. Since mismatch is relieved by glide of TDs that is possible only on the {111} plane, it is desirable that the dislocations be 60° or mixed dislocations. Also other TD nucleation sources like edge dislocations that cannot glide and in addition act as barriers to the glide of mixed dislocations are to be suppressed. This can be achieved by maintaining a layer-by-layer or Frank – van der Merwe (FM) growth mode.

3.1.2. Driving Forces for Strain Relaxation

The process of strain relaxation is a dynamic process that depends on dislocation nucleation and propagation rates. Growth under non-equilibrium conditions where dislocation nucleation and interaction are minimized can

prevent strain relaxation. The strain energy built up in the mismatch layer acts as a driving force for strain relaxation and is termed as excess stress. Hence is process of strain relaxation is initiated at layer thicknesses beyond the critical thickness.

The excess stress is used to quantify the tendency for a threading dislocation to glide and create misfit dislocation segment. The rate at which a TD glides defines the rate at which a MD segment is created. This is termed as dislocation glide velocity. The relation between the excess stress τ_{eff} and dislocation glide velocity V is given by [2],

$$V = B\tau_{eff} \exp(-U/kT) \tag{3.4}$$

where U is the activation energy and B is a constant. The dislocation glide velocity can also be expressed in a semi-empirical equation as follows [3],

$$V = V_o \left(\frac{\tau_{eff}}{\tau_o} \right)^m \exp(-U/kT) \tag{3.5}$$

where V_o = 8 m/s, τ_o=1 MPa, m=1.4 and U=1.1 eV. The typical values of dislocation glide velocities in zinc-blende semiconductors (like SiGe) range from 2nm/s to 25 nm/s [4]. Dislocation velocity increases with temperature due to increased thermal energy. Hull et al. have reported a misfit dislocation velocity of 5 μm/s at 545 °C and 100 μm/s at 830 °C in a $Si_{0.7}Ge_{0.3}$/Si heterostructure [5]. Since the dislocation glide creates new MD segments, the equation of threading dislocation multiplication is given by,

$$\frac{d\rho_m}{dt} = K\rho_m V \tau_{eff} \tag{3.6}$$

where ρ_m is density of mobile threading dislocations and K is a phenomenological parameter. The rate of strain relaxation ($d\gamma(t)/dt$) depends on the rate of MD segment formation and is as follows,

$$\frac{d\gamma(t)}{dt} = b\frac{d\rho_m}{dt} \tag{3.7}$$

where b is the Burgers vector. Here $\gamma(t)$ is the amount of plastic strain, that is, the amount of lattice mismatch accommodated by misfit dislocations. As strain relaxation proceeds, the strain energy in the heteroepitaxial layer reduces, hence the excess stress that is the driving force for strain relaxation reduces with proceeding strain relaxation and is expressed as,

$$\tau_{eff} = 2\mu\frac{1+\nu}{1-\nu}\left[f_o - \gamma(t) - r(h)\right] \tag{3.8}$$

where f_o is the mismatch strain and r(h) is the degree of strain retained by the heteroepitaxial layer, v is the Poisson ratio and μ is the shear modulus. Substituting equations, and in equation, the following non-linear differential equation is obtained,

$$\frac{d\gamma(t)}{dt} = C\mu^2\left[f_o - \gamma(t) - r(h)\right]^2\left(\gamma(t) + \gamma_o\right) \tag{3.9}$$

where C is a constant and γ_o is termed as the dislocation source density.

Since excess stress is the driving force for strain relaxation, excess stress evaluated at zero MD density gives the degree of metastability of the strained layer. Consider the process of strain relaxation in the growing heteroepitaxial layer. Initially the thickness of the strain layer is small, hence the lattice mismatch can be accommodated by elastic deformation and the excess stress is low, hence the rate of strain relaxation is low. As the thickness of strained layer reaches the critical thickness, there is sufficient excess stress to cause strain relaxation. Once strain relaxation is initiated the excess stress is reduced as dislocations formed as a result of this process accommodate some of the lattice mismatch. Hence the strain relaxation rate is high only for a short

time. As a result, it is not possible to reduce the elastic strain in a heteroepitaxial layer to zero.

The strain relaxation rate can be increased by various methods. The most obvious way is to maintain a high level of excess stress. In conventional approaches to heteroepitaxy, this is achieved by high temperature annealing that provides increased energy for dislocation movement. In the LES approach, the structural changes occur in the InGaAs/AlAs structure as the oxidation front passes through it. These changes may provide an additional stress that acts as driving force for strain relaxation. The above analysis assumes that there are no barriers to the creation of MD segments by glide of TDs.

3.1.3. Effect of strain relaxation on surface morphology

Surface morphology of heteroepitaxial layers has a significant effect on the device performance in FETs and lasers. A rough surface morphology can result in low mobility due to interface roughness scattering in HEMTs. In the case of lasers it results in increased optical losses due to scattering. The generation of dislocations at the epitaxial-layer substrate interface results in the modification of the growing surface. The introduction of a misfit dislocation produces a step on the surface with a height equal to Burgers vector b. Initially this was proposed to be the reason for the crosshatched surface morphology observed in low-mismatch heteroepitaxial layers [6]. Recently an alternative mechanism was proposed to explain this. The strain fields of dislocations at the epitaxial layer – substrate interface result in a non-uniform chemical potential at the growing surface. This non-uniform chemical potential increases the adatom incorporation rate in some areas, while suppressing it in others. This results in a wavy or crosshatched surface morphology. If the screw

components (which are non-strain relieving) of 60° dislocations cancel, the strain field decays rapidly, but this does not happen in reality [1]. Experimental observations on heteroepitaxial growth support the second model. Another factor that may result in surface roughness is partial elastic strain relief by surface deformation.

The crosshatched or rough surface morphology also affects the subsequent dislocation nucleation and glide. Formation of deep surface troughs creates regions with high stress where additional dislocations can form as the dislocation nucleation barrier is lowered [7]. The surface morphology also affects strain relaxation by blocking dislocation glide. These effects are illustrated in Figure 3.2.

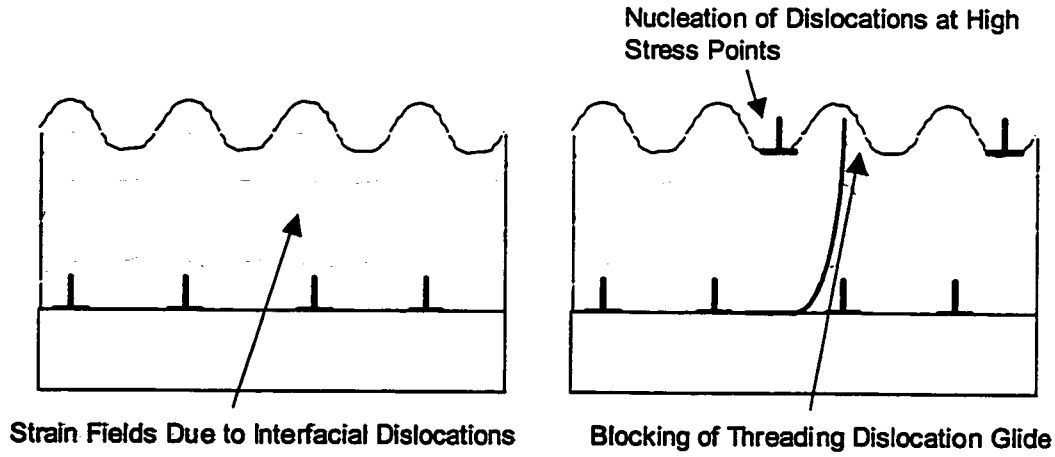


Figure 3.2: Evolution of surface morphology and dislocation generation in heteroepitaxial growth

Hence it is clear that the processes of strain relaxation and surface evolution in heteroepitaxial layers are closely coupled to each other.

3.1.4. Effect of Misfit Dislocation Interactions on Strain Relaxation

However the most dominant factor affecting the process of strain relaxation is the presence of existing dislocations that affect the process of dislocation glide.

Strain relaxation in low misfit systems

From equation (3.2) it is clear that for a low lattice mismatch the spacing between misfit dislocation (MD) segments should be large. Hence heteroepitaxial layers with low threading dislocation (TD) density and long MD segments are observed. Most of the MD segments are 60° or mixed dislocations that can glide on the {111} plane. The relation between TD density and MD density for low misfit systems is given by the following equation,

$$\rho_{TD} = \frac{4}{S_{MD}}\left(\frac{1}{\langle L\rangle_{MD}} - \frac{1}{L}\right) \qquad (3.10)$$

where S_{MD} is the MD spacing, $<L>_{MD}$ is the average MD length and L is the width of the sample. Therefore to minimize the TD density, long MD segments are required. This criterion is usually satisfied, as there are very few barriers to the glide of TD.

However in experimental observations for low misfit systems, the degree of strain relaxation is much lower than theoretically predicted values [8, 9]. Strain relaxation in this case is limited by dislocation nucleation and lack of excess stress required to cause TD glide to create MD segments. Hence efficient strain relaxation for low misfit systems requires high annealing/growth temperatures. This however is undesirable in the case of the III-V arsenide and antimonide materials due to the low volatility of the Indium and Antimony atoms.

Strain Relaxation in High Misfit Systems

As the lattice mismatch increases, the required spacing between the MD segments has to be reduced to accommodate the mismatch. The heteroepitaxial layers in this case exhibit short MD segments and typically have a high TD density. Also for high misfit systems edge type MDs are prominent at the interface and 60° MDs are a minority. This is because for higher lattice mismatches, the heteroepitaxial layer grows in a 3D or island mode. A majority of dislocations in the 3D islands are of the edge type, which generate threading dislocations when these islands coalesce. In this case strain relaxation is not efficient as most of the MDs are sessile and there are too many barriers to the movement of the small number of 60° dislocations.

In conventional epitaxial growth techniques, the only way to reduce threading dislocation density is through the growth of a thick buffer layer, which enables the reduction of TD density through annihilation. However, this method is highly inefficient. For example, the TD density in an InAs/GaAs structure (Misfit =7%) reduces from 2.1×10^9 /cm^2 to 1.9×10^8 /cm^2 when the layer thickness increases from 0.47 μm to 4.38 μm [10].

Another approach is to use a graded structure, where a series of layers with increasing misfit are grown. In this the lattice-mismatch is distributed among several epitaxial interfaces to reduce the dislocation interaction. However in this case, a careful design of the epitaxial structure is required to maintain a 2D growth mode and minimize dislocation blocking.

Strain relaxation and work hardening

To summarize, strain relaxation in low misfit systems is limited by nucleation of new dislocations, whereas in high misfit systems it is limited by glide of dislocations. As a result the residual strain in a heteroepitaxial layer

can never be reduced to zero. This phenomenon is known as work hardening. In this section, various mechanisms that lead to the formation of immobile dislocations are discussed.

The first mechanism that creates immobile dislocations is the annihilation of two dislocations. For example two gliding threading dislocations with complementary Burgers vectors can react to form a sessile threading dislocation as shown in Figure 3.3,

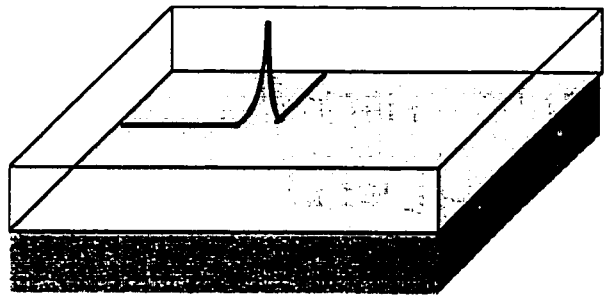


Figure 3.3: Interaction of two gliding TDs to create a sessile (immobile) TD

In this case, though the TD density is reduced by a factor of 2, subsequent strain relaxation does not occur as no new MD segments can be created.

The second mechanism that impedes strain relaxation is the blocking of the movement of TDs. A gliding threading segment is impeded when it crosses a perpendicular MD segment. This is because the background stress in a vicinity of MD segment is reduced as a consequence of its existence. Hence the driving force for a crossing TD is reduced and this inhibits its glide across the MD segment. Plan view TEM analysis of InGaAs layers by MacPherson et al. showed that for layers grown well beyond critical thickness two parallel 60° dislocations can react to form a edge type dislocation. An edge dislocation generated in this manner was shown to be

very effective in blocking the glide of orthogonal MD segments [11]. The phenomenon can be modeled using various approaches.

The effect of an existing network of MDs can be quantified in terms of an effective stress σ_n which is given by the following equation [12],

$$\sigma_n \simeq 2\sum_{i=1}^{n} \frac{\sigma_d}{i} \tag{3.11}$$

where σ_d is the stress resulting from interactions between neighboring MDs and is given by,

$$\sigma_d = \frac{\mu(\varepsilon_o - \varepsilon)}{2\pi} \tag{3.12}$$

Figure 3.4 illustrates the effect of the strain field of a MD on the glide of a crossing TD.

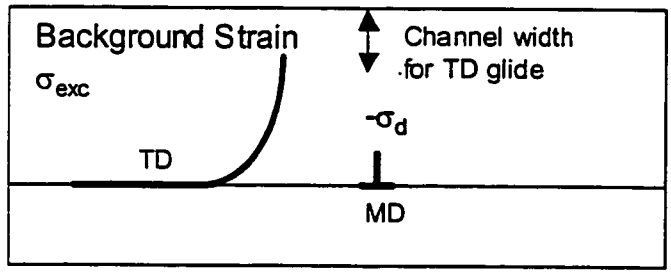


Figure 3.4: Blocking of TD glide by the strain field of a preexisting perpendicular MD segment. The background stress σ_{exc} is reduced by σ_d in the vicinity of the MD

Strain relaxation ceases to occur when the excess stress due to lattice mismatch in the structure equals the background stress due to MDs. Hence a higher density of existing MDs will result in blocking the strain relaxation process much earlier.

An alternate approach to account for the effect of existing MD segments on strain relaxation is proposed by Fischer and Richter [13]. The

concept of self-stress due to an orthogonal array of MDs is introduced. The resolved shear stress on a TD due to lattice mismatch is given by

$$\tau_{exc} = \cos\lambda\cos\phi\frac{2G(1+\nu)}{(1-\nu)}(f-\delta) \qquad (3.13)$$

where λ is the angle between the Burgers vector and the direction in the interface, normal to the dislocation line, φ is the angle between the slip plane and direction normal to the interface, f is the lattice mismatch, G is the shear modulus and δ is the plastic strain. The plastic strain is related to the mean MD spacing p by equation (3.2). The self-stress of a MD network with an average spacing p is given by,

$$\tau_{self} = \cos\phi\frac{Gb(1-(\nu/4))}{4\pi p(1-\nu)}2\ln\left(\frac{p}{2b}\right) \qquad (3.14)$$

Using equations (3.2), (3.13) and (3.14), the net stress on a misfit dislocation is given by,

$$\tau = \tau_{exc} - \tau_{self} = \cos\lambda\cos\phi\frac{2G(1+\nu)}{(1-\nu)}\left(f-\left[\delta(1+\beta)\right]\right) \qquad (3.15)$$

where

$$\beta = \frac{(1-\nu/4)}{2\pi\cos\lambda(1+\nu)}\ln\left(\frac{p}{2b}\right) \qquad (3.16)$$

The term δβ can be interpreted as the decrease in active stress due to the elastic interactions between the existing MDs. Strain relaxation ceases to occur when the self-stress of the misfit dislocation network equals the excess stress due to the lattice mismatch. Using the above analysis the observed MD density in a relaxed SiGe/Si structure could be accounted for.

As discussed above the presence of a MD decreases the background strain that acts a driving force for the glide of the TD. Also the layer thickness

through which the TD can glide is reduced as shown in Figure 3.5. In addition to background stress reduction due to existing MDs, the crosshatch surface morphology that is a result of strain relaxation can also impede TD glide. Under extreme conditions these troughs in the surface may further reduce the layer thickness through which the TD can glide [14]. It is also possible that the combination of a crosshatch surface and strain field of existing misfit dislocation completely blocks the movement of other TDs. These interactions between misfit dislocations can restrict their threading segments from reaching the edge of the sample. This dislocation interaction increases the TD density because the TD segments cannot reach the edge of the sample. Also as the strain cannot be relieved by creation of MD segments, additional dislocation nucleation is necessary, which further increases the TD density.

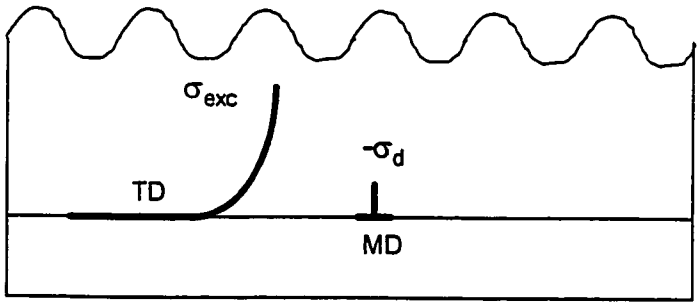


Figure 3.5: A rough surface morphology combined with presence of existing misfit dislocations can enhance the blocking of TD

3.2. Strain Relaxation Phenomena in InGaAs/GaAs and SiGe/Si material systems

According to equilibrium theories as predicted by Matthews-Blakeslee the elastic strain ε in a strained layer with misfit f and thickness h grown beyond critical thickness can be expressed as [15],

$$\varepsilon = f - \frac{b}{4\pi h}\left(\frac{1-\nu\cos^2\beta}{1+\nu}\right)\ln\left(\frac{4h}{b}\right) \qquad (3.17)$$

However, experimentally observed strain relaxation in the InGaAs/GaAs material system is dependent only on the layer thickness and is much lower than that predicted by the equilibrium theories. For low mismatch layers strain relaxation is observed only upon annealing at high temperatures of the order of 700 °C [16]. High temperature annealing results in only a minor reduction in the elastic strain [9]. This is mainly because for low misfit systems, strain relaxation is limited by nucleation of new dislocations.

Various models have been considered to explain the experimentally observed strain relaxation data. Dunstan et al., define a relaxation critical thickness t_{cr} in nm which is given by the following equation [17],

$$t_{cr}(nm) = \frac{0.8nm}{f} \qquad (3.18)$$

Beyond t_{cr}, the residual strain ε varies as,

$$\varepsilon(d) = \frac{0.8}{d(nm)} \qquad (3.19)$$

until the layer thickness is $10t_{cr}$. At this point strain relaxation is impeded due to dislocation blocking or work hardening. Krishnamoorthy et al. observed that strain relaxation for 1 μm thick InGaAs layers is 70 % irrespective of composition [18]. The rate of strain relaxation is sluggish for layer thicknesses greater than 30 h_c. This again suggests that blocking of dislocation glide is the main mechanism impeding strain relaxation.

Strain relaxation of metastable SiGe layers grown on Si substrates also has been studied extensively. Strain relaxation of metastable SiGe layers requires annealing temperatures of the order of 650-750°C. Longer misfit dislocation

lengths observed for $Si_{0.85}Ge0_{.15}$ films indicate the presence of 60° dislocations that glide efficiently without any significant interactions. For higher lattice mismatches 90° edge dislocations are observed [19]. The typical dislocation velocities vary from 1nm/s @ 540 °C to 10 μm/s @ 870 °C, with an activation energy of 2.2 eV [20]. As in the case of the InGaAs/GaAs material system, strain relaxation is impeded by interactions between dislocations.

3.3. Conventional approaches to improve strain relaxation efficiency

The various approaches to improve strain relaxation efficiency are clear if the factors affecting strain relaxation are considered. As described before, the excess stress σ_{exc} is a measure of driving force for strain relaxation by means of thermally activated glide of TDs. Scaling relations for strain relaxation state that strain relaxation is proportional to the square of the initial excess stress [21].

The TD glide velocity that determines the length of the MD created varies with temperature as exp (-E/kT) where E is the dislocation glide activation energy (typically ~ 2.0 eV). The activation energy for glide is also dependent on the excess stress and is expressed in the following equation [21],

$$E(\sigma_{exc}) \approx E_o(1-\sigma_{exc}/\tau_o) \qquad (3.20)$$

where E_o is the glide activation energy with zero excess stress and τ_o is the value of the stress where the glide activation energy goes to zero. Therefore is clear that under conditions of high excess stress and high temperature strain relaxation will be maximized. The other principal requirement is the removal of barriers to the TD movement. Various experimental approaches pursued to

this date try to achieve one or more of the above criteria and are summarized below.

3.3.1. Graded Layers

Grading splits the large lattice mismatch in a series of low mismatched interfaces. Grading helps TD glide in two ways. At low mismatch, TDs can glide without obstruction. If a TD has stopped gliding due to lack of excess stress, grading provides fresh interfaces for the TD to glide [22]. Compositional grading is to be adjusted so that, dislocation nucleation is suppressed but there is enough force to glide TDs and result in strain relaxation. However, the effect of surface morphology on strain relaxation also has to be considered. Increasing the grading rate results in the formation of misfit dislocations close to the growing surface. The strain fields from these dislocations cause surface roughening, which may impede dislocation glide. This has been one of the major obstacles in the growth of highly mismatched heteroepitaxial layers using the graded buffer approach. One solution to this problem is to interrupt the growth and use chemical-mechanical polishing to reduce the surface roughness and facilitate dislocation glide during subsequent continued growth, as seen the case of SiGe layers grown on Si substrates [23]. However it is not clear if this approach is feasible for III-V compound semiconductors.

3.3.2. Growth on Patterned Substrates

Another approach to prevent dislocation interactions is to limit the growth area by the use of patterned substrates. In the case of patterned substrate, the dislocations have to glide only to the edge of the mesa, as

opposed to the edge of the wafer. Also interaction between dislocations on different mesas is eliminated [24]. However to prevent the dislocation interaction within a mesa, the mesa size has to be reduced as the lattice-mismatch increases. This limitation limits the use of this technique to very low lattice-mismatched epitaxial systems (lattice mismatch ~ 0.5 %).

3.3.3. Other Approaches

Some of the other approaches investigated to minimize dislocation interaction are growth on offcut substrates. This results in the formation of a non-parallel misfit dislocation network which results in reduces dislocation pileups [25].

3.4. Compliant Substrates

As seen in the previous section, conventional approaches to heteroepitaxy attempt to minimize dislocation interaction without substantially changing the nature of the heteroepitaxial layer – substrate interface. In recent years, advances in field of semiconductor wafer fusion and wafer bonding have made it possible to engineer epitaxial interfaces. As a result a number of approaches incorporating wafer bonding and fusion in heteroepitaxial growth were investigated in the recent past. These approaches are discussed in this section.

During heteroepitaxial growth, dislocation generation and propagation occurs mainly in the epitaxial layers. This is because the epitaxial layer, which much thinner than the substrate accommodates most of the mismatch strain. If the thickness of the substrate is reduced such that it is thinner than the epitaxial

layer, then most of the mismatch strain is accommodated in the substrate [26]. This is the basic concept behind most "compliant" substrate approaches to heteroepitaxy. One advantage of having a free surface or interface near the epitaxial-substrate interface is that the threading dislocations can be attracted towards this interface instead of propagating in the heteroepitaxial layer as shown in Figure 3.6.

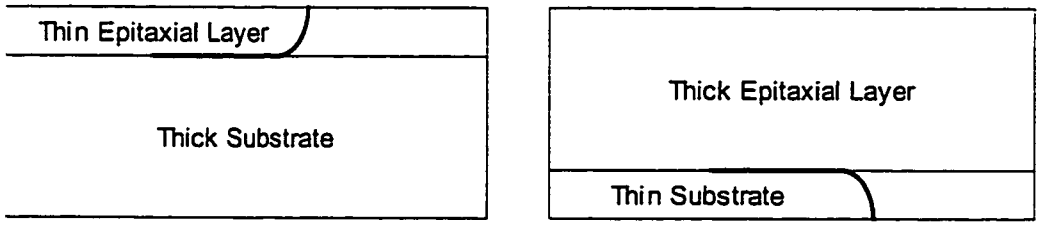


Figure 3.6: Reducing the substrate thickness causes the threading dislocations to bend into the substrate instead of the epitaxial layer

3.4.1. Wafer Bonding Approaches

However it is technologically difficult to fabricate freestanding substrates [27]. Also the biaxial strain causes warping of the epitaxial layer-substrate bilayer as it is no longer rigid [28]. This problem is solved by bonding two semiconductor wafers at an angle (twist-bonding). Low dislocation density growth of 1 % tensile strained InGaP layers and 14.7 % compressive InSb epitaxial layers was demonstrated on twist-bonded GaAs based compliant substrates [29, 30]. The bonding two semiconductor wafers results in a twist boundary consisting of a cross grid of screw dislocations. It is predicted that during the growth of the heteroepitaxial layer, strain relaxation occurs by correlated generation of edge type misfit dislocations [31]. However all other attempts to reproduce low dislocation density growth on "compliant"

twist-bonded substrates have not been successful. Formation of pinholes or voids during twist-wafer bonding results in the growth of a polycrystalline structures where epitaxy occurs in some areas on the twist-bonded GaAs template and on the mechanical GaAs substrate in other areas [32].

Growth of $In_{0.07}Ga_{0.93}As$ layers (Misfit=0.5 %) on mechanically bonded GaAs templates also has demonstrated increased critical thickness and reduced strain relief due to strain partitioning between the epitaxial layer and the thin substrate [33].

Another approach is described by Damlencourt et al. achieves strain relaxation in a film by releasing it from the substrate and bonding it to another substrate [34]. 300 Å $In_{0.65}Ga_{0.35}As$ (Misfit = 1%) epitaxial layers were grown on AlInAs sacrificial layers on InP substrates. Undercut etching of the AlInAs etch layers releases the $In_{0.65}Ga_{0.35}As$ epitaxial layers from the substrate and results in elastic relaxation. The elastically relaxed layer is then bonded at room temperature (Van der Waals bonding) to another substrate and $In_{0.65}Ga_{0.35}As$ layers are grown on this layer. PL emission from epitaxial layers grown on the elastically relaxed platforms had higher intensity and lower FWHM than those grown on directly on InP substrates.

3.4.2. Amorphous Interlayer Approaches

Instead of a freestanding membrane, a thin substrate supported by a viscous interlayer can be expected to behave in a similar manner. Powell et al. demonstrated the growth of low dislocation density relaxed SiGe epitaxial layers on a Silicon-on-Insulator (SOI) substrate [35]. A strained SiGe layer grown on a SOI substrate relaxes through the formation of dislocations in the thin Si substrate upon thermal annealing. The dislocations at the SiGe/Si

interface are attracted towards the Si/oxide interface instead of propagating in the SiGe layer. Annealing at 1050 °C reduces the strain to 25 % of the misfit. Growth of low TD density 1.0 μm thick $Si_{0.6}Ge_{0.4}$ layers (Misfit=1.6 %) has been demonstrated on a SOI substrate with a 200 Å thick Si template [36].

In the case of III-V compound semiconductors, the viscous or amorphous interlayers can be implemented using many approaches. Lubyshev et al. demonstrated a compliant substrate consisting of a 100 Å GaAs epitaxial layer with a 1000 Å oxidized AlGaAs (Al_2O_3) underneath it [37]. Reduced tilt was observed in 2 μm $In_{0.15}Ga_{0.85}As$ (Misfit=1%) epitaxial layers grown on a 150 Å $In_{0.15}Al_{0.85}As$ nucleation layer. Also the FWHM of the epitaxial layers was ¼ of those grown on a GaAs substrate. However crosshatched surface morphology indicated strain relaxation by misfit dislocations at the epitaxial layer-compliant layer interface.

As in the case of Si substrates, compliant substrates can also be fabricated by bonding a GaAs template to a GaAs substrate with a borosilicate glass viscous interlayer [38-41]. $In_{0.44}Ga_{0.56}As$ epitaxial layers (Misfit = 3%) grown on the compliant substrate had narrower X-Ray FWHM than those grown on GaAs substrates. However in both cases both the surfaces had a poor surface morphology. The ability of the glass interlayer to flow under shear strain is expected to aid in strain relaxation. However similar results were obtained with interlayers that viscosity that differed by 5 orders of magnitude.

Gaseous atom implantation and subsequent annealing has been used to induce layer splitting in semiconductor substrates. The layer splitting is induced by formation of cavities at the implantation depth. These cavities can also enhance strain relaxation by enhancing misfit dislocation creation. Strain relaxation was enhanced in a $Si_{0.86}Ge_{0.14}$/Si heterostructure by helium implantation at the heterointerface and subsequent high temperature annealing

[42]. The degree of strain relaxation in a 1000 Å thick $Si_{0.86}Ge_{0.14}$ layer after Helium implantation and annealing at 900 °C was 54 %. No strain relaxation was observed in un-implanted structures upon annealing.

Most of the above approaches rely on the fact that slippage occurs at the compliant layer-mechanical substrate interface. However in reality none has been observed. In comparison the LES approach utilizes the structural changes occurring during the process of lateral oxidation to enhance strain relaxation in heteroepitaxial layers above the oxide. Subsequent regrowth on the LES template does not rely on the weakness of the LES template/oxide interface. In the following section the lateral oxidation of Al-containing semiconductors will be reviewed.

3.5. Lateral Oxidation of Al-containing semiconductors

Oxidation of Al-containing semiconductors was originally used to improve the environmental stability of AlAs layers in semiconductor heterostructures [43, 44]. In this process, when AlAs is exposed to steam at temperatures ranging from 400 to 500 °C, it is converted to Al_2O_3. The reactions can be expressed as follows [45],

$$2\ AlAs + 6\ H_2O\ (g) = Al_2O_3 + As_2O_3\ (l) + 6\ H_2;\ \Delta G^{698} = -473\ kJ/mol$$

$$As_2O_3\ (l) + 3\ H_2 = 2\ As + 3\ H_2O\ (g);\ \Delta G^{698} = -131\ kJ/mol$$

$$As_2O_3\ (l) + 6\ H = 2\ As + 3\ H_2O\ (g);\ \Delta G^{698} = -1226\ kJ/mol$$

In recent years, it is the electronic and optical confining properties of the oxide that have found increasing use in optoelectronic devices. Oxidation of other Al containing semiconductors like AlGaInP, AlInAs and AlAsSb has also been investigated [46-48]. Initial application of oxides in heterostructure lasers

involved surface oxidation of $Al_xGa_{1-x}As$ ($x > 0.8$) layers [49]. Lateral oxidation of buried AlGaAs layers was first used for current and optical mode confinement in vertical cavity surface emitting lasers, field effect transistors and heterostructure bipolar transistors [50, 51]. Unlike surface oxidation, lateral oxidation results in selective conversion of a buried semiconductor layer to an amorphous/polycrystalline material. The resulting structural changes have important implications in VCSEL reliability and are used to advantage in the lattice-engineered substrate approach. Since the major focus is the structural changes in the semiconductor heterostructure as a result of the oxidation process, the electronic and optical confining aspects of oxides will not be discussed here.

3.5.1. Structural properties of oxide-semiconductor structures

Since the process of lateral oxidation involves conversion of a crystalline semiconductor to an amorphous/polycrystalline material, it results in major structural changes. The crystallographic phase of the oxide is polycrystalline γ-Al_2O_3. The crystal structure of γ-Al_2O_3 is cubic Fd 3m with Al_2MgO_4 spinel-like structure. One unit cell consists of 32 atoms of oxygen, 21(1/3) atoms of Al and 2(2/3) vacancies with a cube edge of 7.9 Å [52]. The volume per molecule of Al_2O_3 is 46.2 $Å^3$. Thus the conversion of AlAs to Al_2O_3 corresponds to volume shrinkage of 50% and a linear shrinkage of 20%. This corresponds to a hydrostatic stress of 80 GPa. However in practice linear shrinkage from 6.7 % to 13 % has been reported [53, 54]. This contraction in the layer thickness has significant impact on the thermal stability of device structures having buried oxide layers. Choquette et al. demonstrated that partially oxidized AlAs layers were unstable to thermal cycling and the addition of 2% Ga to the AlAs oxidation layer improved the thermal stability

[55]. Oxidation of AlAs results in a volume contraction of 12 %, whereas that of $Al_{0.92}Ga_{0.08}As$ results in a volume contraction of only 6.7 % [56]. Hence the improved thermal stability of AlGaAs oxides is due to reduced contraction that results in lesser residual stresses in the epitaxial structure. The thermal instability of a partially oxidized AlAs layer is due to strain at the oxide/AlAs terminus, which is a result of the greater volume shrinkage. This volume shrinkage of the oxide introduces a small tensile stress in GaAs layers above the oxide [57]. These stresses created in a semiconductor multilayer containing buried oxide layers can be used as additional driving forces to enhance strain relaxation in strained overlayers.

During the process of lateral oxidation, AlAs is initially converted to an amorphous AlOH phase and then transforms to the γ-Al_2O_3 [53]. The lower value of observed shrinkage compared to the expected theoretical shrinkage indicates that the oxide layer is porous. TEM analysis of oxide shows "cavity-like" regions within 1 μm of the reaction front. These "cavities" are not voids but are amorphous $Al(OH)_3$ distributed among γ-Al_2O_3 grains. This was observed only in high Al content AlGaAs oxidation layers that had a high oxidation rate [53]. The nature of the oxide semiconductor interface also plays a major role in properties of semiconductor structures with buried oxide layers. Cross sectional TEM analysis of AlAs/GaAs multilayers oxidized at 450 °C for 1 hr shows that the oxide/GaAs interface is abrupt with a transition width of 20 Å [54].

The process of oxidation also affects semiconductor layers adjacent to the oxide. Oxidation creates a large number of interface states in the GaAs layers adjacent to oxide, which is mainly due to presence of elemental As in the oxide [58]. This increases the minority carrier recombination rate at the oxide/GaAs interfaces. reducing the minority carrier lifetime in the adjacent

layers [59]. The degradation is mainly attributed to presence of excess As at the oxide-semiconductor interface. Diffusion of As into GaAs layers adjacent to oxide was also observed [60]. In addition to the diffusion of Arsenic, Graham et al. also observed diffusion of oxygen into the adjacent semiconductor layer [61]. The diffusion of oxygen reduced the radiative carrier lifetime in an $In_{0.2}Ga_{0.8}As$/GaAs quantum well to less than 1ns, whereas InGaAs/GaAs quantum wells in an identical unoxidized structure had a radiative lifetime of 12 ns. Hence it is necessary to use a defect diffusion barrier to block the electrons from reaching the oxide/semiconductor interface and also to prevent excess As and other defects from diffusing into the layer above the oxide. Inserting AlGaAs, AlAs or GaInP barrier layers in the semiconductor adjacent to the oxidation layer will help in reducing the structural and electronic degradation of layers adjacent to the oxide. Insertion of AlGaAs barrier layers was shown to improve the luminescence of an InGaAs/GaAs quantum well adjacent to a laterally oxidized AlAs layer [62]. In the case of the LES substrates, the excess Arsenic and oxygen in the template will diffuse into the regrown epitaxial layers. This is prevented by insertion of a 50 Å thick AlAs defect diffusion barrier in the strained InGaAs layer. The InGaAs layers above the defect diffusion barrier are expected to be free of impurities and defects generated by the process of lateral oxidation.

Another way to prevent the diffusion of excess As and other defects in the InGaAs overlayers is to incorporate a defect gettering layer like LT GaAs underneath the oxidation layer. Growth of GaAs epitaxial layers at low temperatures (~250 °C) results in the incorporation of excess arsenic. Annealing at high temperatures (~ 600 °C) results in the formation of As precipitates [63]. These precipitates can also act as gettering centers for defects and excess As generated during the process of lateral oxidation. Hence in the

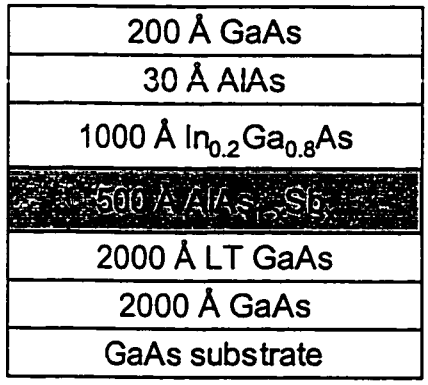
LES Template the AlAs(Sb) oxidation layers are grown above a 2000 Å thick LT GaAs buffer grown at 250 °C. However there is no separate annealing step for the LT GaAs buffer. This is because the growth of the AlAs(Sb) oxidation layers at high temperature (~580–620 °C) effectively anneals the underlying LT GaAs buffer.

3.5.2. Lateral Oxidation Kinetics of $Al_xGa_{1-x}As$

Lateral oxidation kinetics of AlGaAs has been extensively investigated and depends on numerous factors like the Al composition, type of doping, layer thickness, adjacent layers [64, 65]. Addition of Ga to AlAs decreases the oxidation rate. The addition of Ga reduces the oxidation reaction rate at the AlGaAs/oxide interface. This changes the oxidation mechanism from diffusion-limited to reaction-limited because the slow reaction at the interface is the limiting process in the oxidation. The oxidation rate is independent of the thickness for AlAs layers greater than 500 Å thick. Below 500 Å, the oxidation rate decreases with the layer thickness, with no observed lateral oxidation for AlAs layers less than 100 Å thick. This has been attributed to surface energy effects at the oxide/AlAs reaction interface [66]. Incorporation of LT GaAs also enhances the oxidation rates of AlAs oxidation layers adjacent to it [67]. This is probably due to enhancement of transport of As containing species which are a byproduct of the oxidation process. Based on this, the oxidation layers in LES substrates were 500 Å thick, also no Ga was added to these layers as the maximum possible oxidation rate was desired. Also these oxidation layers were grown on top of 2000 Å thick LT GaAs layers.

3.5.3. AlAs and AlAsSb Oxidation Layers for LES Substrates

Figure 3.7 shows the layer structure of templates used for study of oxidation kinetics of AlAsSb oxidation layers.



Layer Structure

Sb Composition	$P(As_2)$ (Torr)	$P(Sb_2)$ (Torr)	T_{growth}
x=0	7×10^{-6}	0	620 °C
x=0.03	9×10^{-6}	6×10^{-8}	570 °C
x=0.07	4×10^{-6}	6×10^{-8}	570 °C
x=0.10	4×10^{-6}	9×10^{-8}	570 °C

Growth Conditions for Oxidation Layers

Figure 3.7: Layer Structure and Growth Conditions for LES Templates used for Oxidation Kinetics Study

500 Å thick undoped $AlAs_{1-x}Sb_x$ (x=0.0, 0.03, 0.07, 0.10) oxidation layers were grown on GaAs substrates by solid-source molecular beam epitaxy (MBE) at a growth temperature of 570 °C. Both group V elements were used in dimer form (As_2 and Sb_2). The InGaAs epitaxial layers were grown at 430 °C. After growth, 100 μm x 100 μm mesas were defined by photolithography and reactive ion etching (RIE). The total etch depth was around 1 μm. These mesas were laterally oxidized in steam in a 3-zone quartz tube furnace at temperatures ranging from 390 to 450 °C. Steam was generated using N_2 carrier gas flowing at rate of 1.7 liter/min through a bubbler containing deionized water maintained at 90 °C.

Figure 3.8 shows the optical micrographs of partially oxidized $AlAs_{1-x}Sb_x$ layers. The AlAsSb oxidation layers are capped by 1000 Å thick $In_{0.2}Ga_{0.8}As$ and AlAs/GaAs sacrificial layers grown at 430 °C. The oxidation temperature is 410 °C and the oxidation time is 20 minutes. It has been reported previously that oxidation of $AlAs_{0.56}Sb_{0.44}$ lattice-matched to InP results in the formation of a uniform segregated layer Sb [48, 68]. A significant difference when compared to oxidation of $AlAs_{0.56}Sb_{0.44}$ lattice matched to InP is the non-uniform segregation of Sb observed for Sb compositions less than 10 %. The non-uniform segregation may be due to lower amounts of Sb compared to $AlAs_{0.56}Sb_{0.44}$. The segregated Sb is seen as dark spots in the oxidized region of the mesa. It is observed that the density of the Sb segregates increases with Sb composition. The segregation of Sb from the oxide may result in an oxide with higher porosity compared to one formed by oxidation of AlAs.

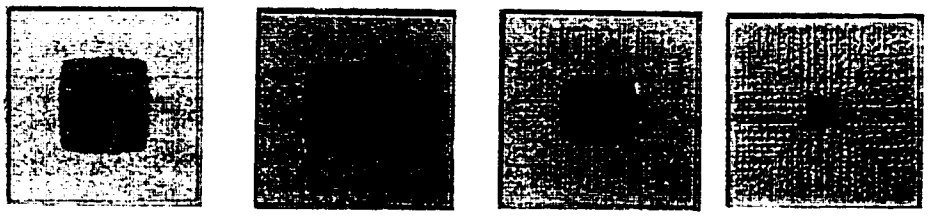


Figure 3.8: Optical Micrographs of AlAsSb Oxidation Layers Oxidation Temperature=410 °C, Time=20 minutes, Mesa Size=100 μm

The Sb segregation results in modification of oxidation kinetics. Figure 3.9 shows the variation of oxidation extent as a function of time for an oxidation temperature of 410 °C. It can be seen that the oxidation rate increases with the addition of antimony and the influence of the diffusion

process on the oxidation reaction is reduced. Thus it can be inferred that addition of Sb increases the reaction rate at the interface and also causes an increase in the permeability of the oxide. Hence the high oxidation rate does not result in a diffusion limited reaction mechanism as seen in the case of AlAs at temperatures greater than 500 °C [69].

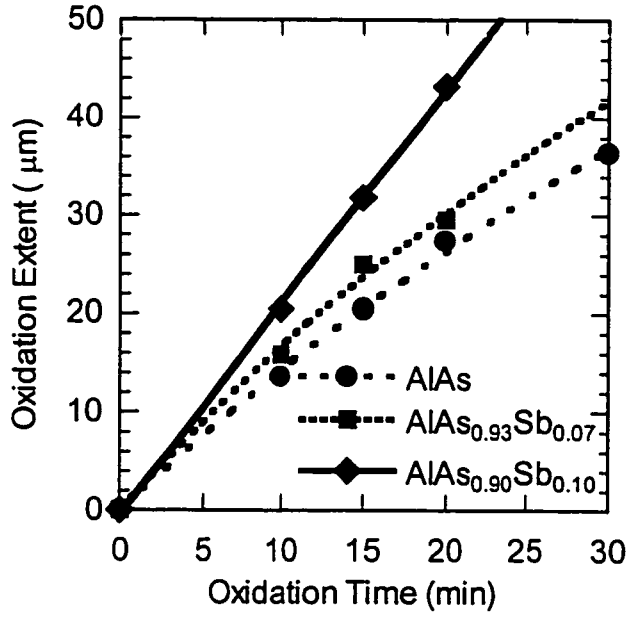


Figure 3.9: Variation of oxidation extent as a function of time for AlAsSb Oxidation Layers for an oxidation temperature of 410 °C

The oxidation data was fitted to the Deal-Grove model to determine the reaction rate ($k_{reaction}$) and diffusive rate ($k_{diffusion}$) constants respectively [70]. The extent of lateral oxidation x_{ox}, and the oxidation time t_{ox} are related as follows,

$$\frac{x_{ox}}{k_{reaction}} + \frac{x_{ox}^2}{k_{diffusion}} = t_{ox} \qquad (3.21)$$

The oxidation mechanism in AlAs is a combination of reaction-rate limited and diffusion limited mechanisms from 390 to 450 °C. On the other hand, the oxidation mechanism in $AlAs_{1-x}Sb_x$ is a combination of reaction-limited (linear) and diffusion-limited (parabolic) mechanisms at low temperatures and purely reaction limited at high temperatures. In contrast to AlAs, the diffusive rate constants ($k_{diffusion}$) for $AlAs_{1-x}Sb_x$ are much higher. For example, at an oxidation temperature of 410 °C, the diffusive rate constant, $k_{diffusion}$ for oxidation of $AlAs_{0.90}Sb_{0.10}$ is 161 μm^2/min, which is 2.5 times the value of AlAs (63 μm^2/min).

Figure 3.10 shows the reaction rate constant ($k_{reaction}$) and diffusion rate constant ($k_{diffusion}$) for lateral oxidation of $AlAs_{1-x}Sb_x$ as a function of inverse temperature for various compositions. The reaction rate constants for $AlAs_{1-x}Sb_x$ are higher than those for AlAs for the whole range of temperature. This may be due to higher free energy change for oxidation of $AlAs_{1-x}Sb_x$ compared to AlAs or due to the fact these layers are under compression. The diffusive rate constant for oxidation also increases with Sb composition that indicates increased porosity of the oxide. The increased porosity of the oxide may be due to the segregation of Sb and Sb-related byproducts from the oxide. The rapid increase in $k_{diffusion}$ at high temperature results in a reaction-rate-limited mechanism as reactant diffusion is no longer a limiting factor. It has been proposed for lateral oxidation of AlAs that the formation of a dense As_2O_3 layer near the oxidation reaction interface results in the parabolic dependence of the oxidation reaction [71]. The influence of the dense As_2O_3 layer on the oxidation process is significant at high oxidation rates/temperature. This is because the rate of formation of dense As_2O_3 layer is higher rate than its rate of reduction to As which results in a porous oxide. In the case of lateral oxidation of $AlAs_{1-x}Sb_x$, we believe that segregation of Sb from the oxide results in

increased permeability, which coupled with increased oxidation reaction rates for AlAsSb, results in high oxidation rates with linear time dependence.

The activation energy of $k_{reaction}$ for lateral oxidation of AlAs is 1.04 eV. This value is lower than the value of 1.6 eV reported in the literature [69]. This may be due to the presence of LT GaAs buffer beneath the oxidation layer,

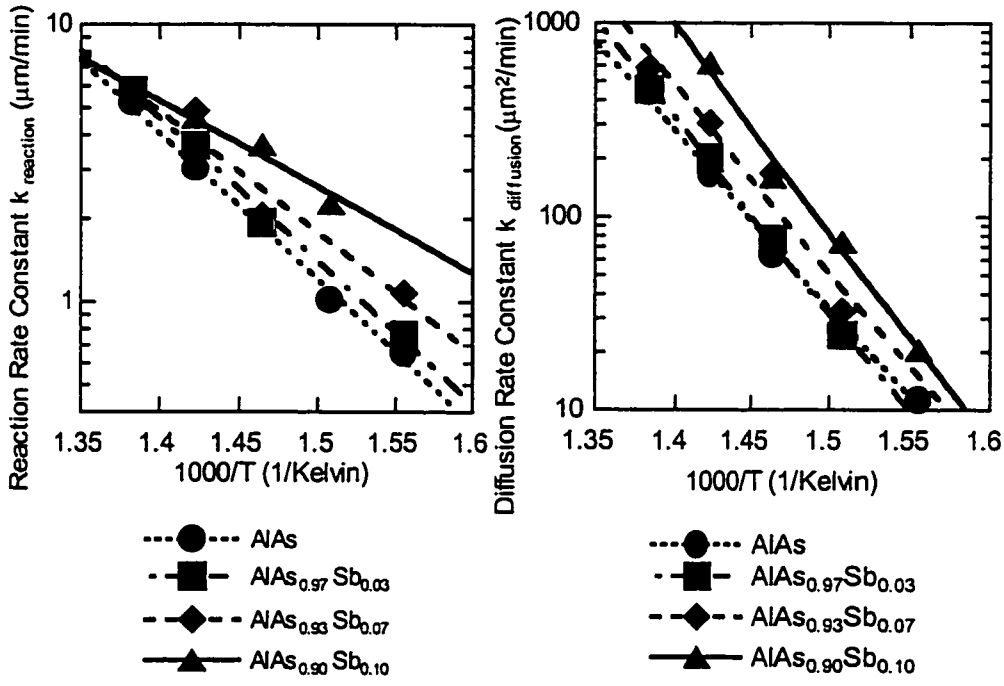


Figure 3.10: Variation of reaction rate constant ($k_{reaction}$) and diffusion rate constant ($k_{diffusion}$) as a function of inverse temperature

which is known to affect the oxidation rate of AlAs [67]. As seen from Table 3.1, the activation energy for the oxidation of $AlAs_{1-x}Sb_x$ reduces with addition of Sb to AlAs.

Oxidation Layer	E_A ($k_{reaction}$)	E_A ($k_{diffusion}$)
AlAs	1.04 eV	1.82 eV
$AlAs_{0.97}Sb_{0.03}$	1.02 eV	2.01 eV
$AlAs_{0.93}Sb_{0.07}$	0.93 eV	1.92 eV
$AlAs_{0.90}Sb_{0.10}$	0.61 eV	2.14 eV

Table 3.1: Activation Energies of $k_{reaction}$ and $k_{diffusion}$ for AlAsSb Oxidation Layers

Though the addition of Sb increases the oxidation rate and enables the use of larger sizes mesas for LES substrates, segregation of Sb is undesirable for regrowth as it creates an undulating surface. However as seen from Figure 3.11 oxidation at higher temperatures eliminates Sb segregation, as all the Sb byproducts of oxidation can be removed.

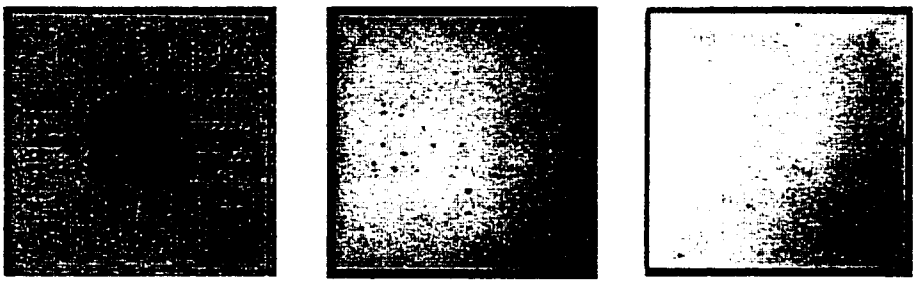


Figure 3.11: Oxidation of AlAsSb as a function of temperature. Oxidation at higher temperatures eliminates Sb segregation

3.6. Strain relaxation upon lateral oxidation

3.6.1. Strain Relaxation Mechanisms

The process of lateral oxidation results in linear contraction of the oxidation layer. Also rigid crystalline interfaces are converted to porous interfaces. Since the process of strain relaxation is driven by excess stress in the semiconductor heterostructure, stress created by the volume reduction during lateral oxidation is expected to enhance the process of strain relaxation. Strain relaxation is observed in InGaAs/GaAs superlattices upon oxidation [72]. The extent of strain relaxation was higher for superlattices with higher Indium mole fraction and for thicker oxidation layers. The driving force for strain relaxation comes from built up strain energy and the stresses generated as a consequence of lateral oxidation.

Figure 3.12 explains the difference in strain relaxation mechanisms in conventional substrates and lattice-engineered substrates. In conventional

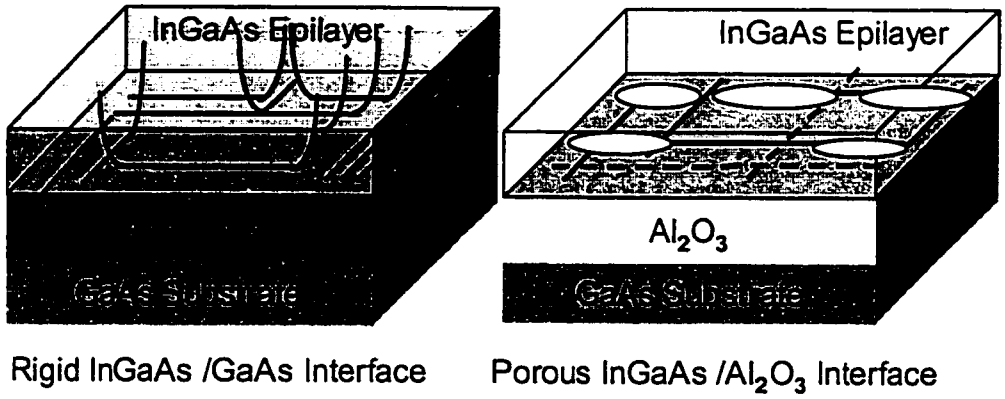


Figure 3.12: Comparison of Strain Relaxation Mechanisms in Conventional and Lattice-Engineered Substrates

heteroepitaxy (for example, InGaAs growth on a GaAs substrate) formation of misfit dislocation (MD) segments by the movement of threading dislocation (TD) ends relieves strain in the lattice-mismatched epilayer. However existing clusters of other MDs may block this motion. Therefore the existing dislocations cannot relieve the mismatch strain building up in the growing epitaxial layer. Hence generation of additional dislocations is required to relieve the strain in the epilayer. Thus a large number of dislocations are generated to accommodate the lattice mismatch. Conventional approaches like graded buffers reduce the TD/MD dislocation interaction by vertically distributing the MD segments over a large layer thickness. In a lattice-engineered substrate, enhanced TD movement at the template/oxide interface that is porous and has voids relieves the strain in the epitaxial template. Also core regions of existing MDs may be reactively removed during the process of lateral oxidation. As a result there are fewer barriers to increasing MD length, which prevents the generation of additional threading dislocations.

Kukta and Freund have proposed a model for strain relaxation in strained semiconductor structures with a viscous interlayer [73]. The most obvious mechanisms for strain relaxation in this case, are the movement of the viscous interlayer at high temperature or slippage at the viscous interlayer-semiconductor interface. Either of these processes enables the strained overlayer to expand or contract and achieve its natural lattice constant. However this process is extremely slow and therefore less probable. A much faster process of strain relaxation involves the glide of MD segments towards the viscous interlayer and their subsequent dissipation. Figure 3.13 shows the mechanism by which this process occurs.

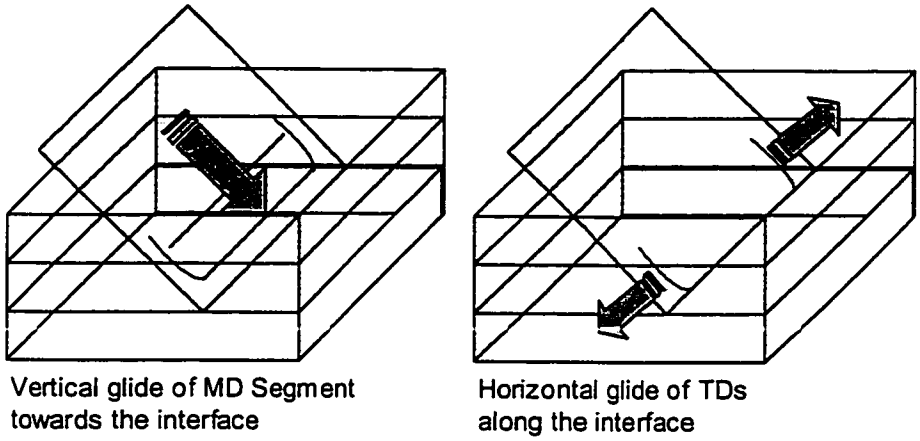


Figure 3.13: Mechanism for removal of MD segments near a weakly bonded interface as proposed by Kukta and Freund

Consider a MD segment close to a surface or a weakly bonded interface. There exists an attractive force on the MD segments that drive it towards the surface or an interface with a viscous/porous layer. Thus the MD segment, which is initially at the interface of epitaxial film and the compliant layer, glides towards the compliant layer-bonding layer interface. On reaching the interface, the MD segment and its associated strain field is dissipated in the viscous/porous interlayer The two thread ends of the misfit dislocation segment are further drawn out and remove additional segments the misfit dislocation in this process. This model is applied to the relaxation of metastable SiGe layers grown on a SOI substrate [35]. This process should be even more efficient in the case of the lattice-engineered substrates as the MD segments are at the semiconductor (InGaAs)- porous interlayer (Al_2O_3) interface. In addition to this reactive oxidation of the MD core region may also result in the removal of the MD segment.

To summarize strain relaxation occurs in InGaAs layers during lateral oxidation of underlying AlAs layers mainly due to two mechanisms. The first

is the increase glide force on the TD segments due to volume contraction. This results in strain relief due to the formation of additional MD segments. The second is the dissipation of the MD segments in the oxide. This improves the efficiency of TD glide by removing the barriers.

3.6.2. Plan View TEM Analysis of Lattice Engineered Substrates

Plan-view transmission electron microscopy (PVTEM) has been used to characterize the interface between oxidized AlAs and lattice-mismatched $In_{0.2}Ga_{0.8}As$. Figure 3.14 shows the layer structure of $In_{0.2}Ga_{0.8}As$ Lattice-Engineered Substrate. The substrate was patterned and oxidized at 450°C for one hour to a distance of 90μm.

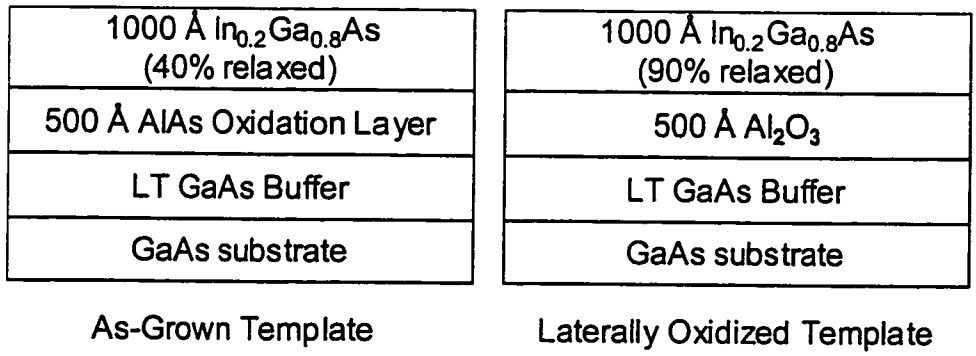


Figure 3.14: Layer Structure of InGaAs LES Template used for PVTEM Analysis

Figure 3.15 shows a strong-beam **g**=220 plan view TEM image of an area including the oxidation front as viewed along the substrate normal. In the region not yet oxidized, there is a dense network of misfit dislocations oriented along the two orthogonal <110> directions in the (001) plane. The oxidation front is indicated by the transition between the high and low misfit dislocation

density areas. The misfit dislocation density has been reduced from $1.67x10^5$/cm in the unoxidized region to less than ~$5x10^3$/cm in the oxidized region. At the same time, this percentage strain relaxation in the structure increases 40% before oxidation to 90% after oxidation at 450°C. This indicates the reduction in strain in the InGaAs layer without the creation of dislocations. This has not been observed in other compliant substrate approaches. However, reliable measurements of the threading dislocation density have not been possible since the density is quite low.

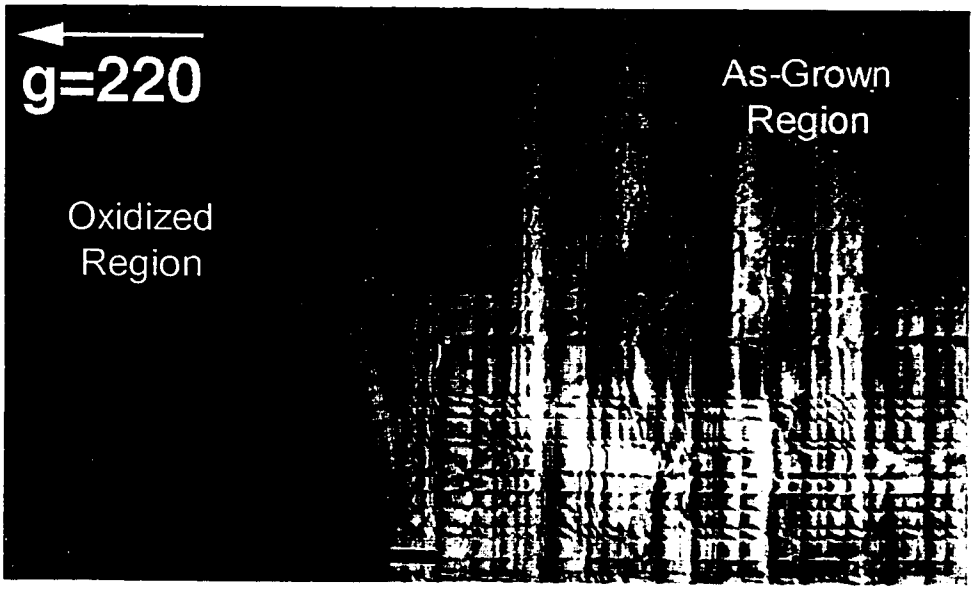


Figure 3.15: Plan-view, bright field g=220 TEM micrograph of GaAs-based, 20% InGaAs lattice-engineered substrate, showing oxidized and unoxidized areas of LES. The misfit dislocation density has been reduced from $1.67x10^5$/cm in the unoxidized region to less than ~$5x10^3$/cm in the oxidized region. (Plan View TEM Analysis done by Sheila Mathis)

The significant reduction in the MD density in the oxidized areas can be erroneously attributed to the delamination of the InGaAs epitaxial layer

from the oxide. However this is not the case, as evidenced from Moire fringes as observed in Figure3.16.

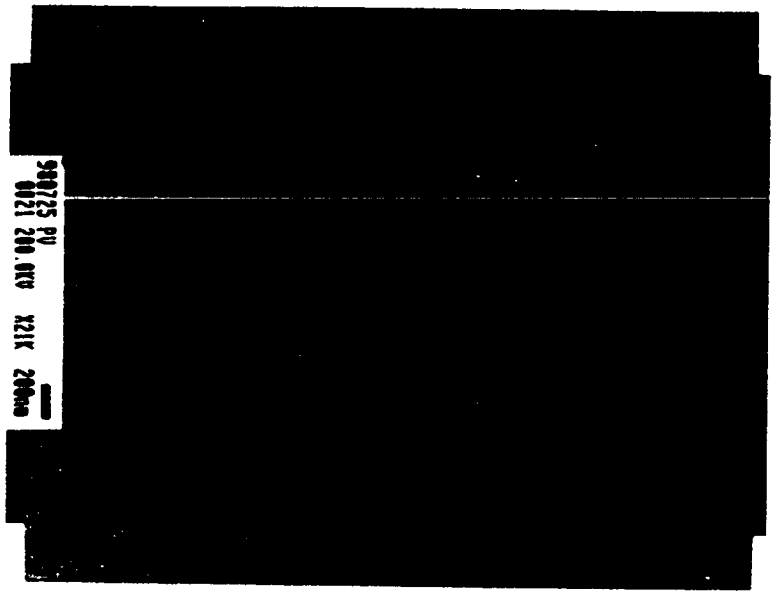


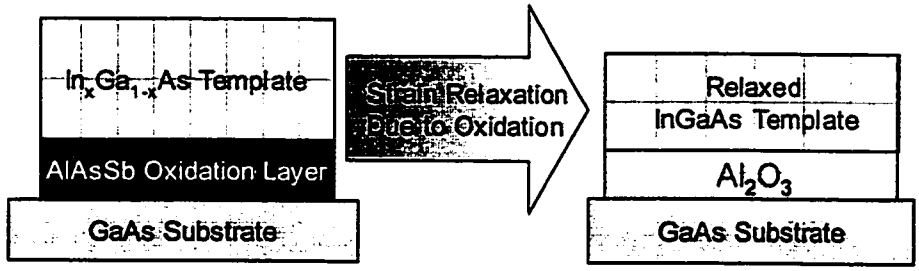
Figure3.16: PVTEM Micrograph of the oxidized InGaAs Lattice Engineered Substrate illustrating the Moire interference pattern from the GaAs and InGaAs lattices.

(Plan View TEM Analysis done by Sheila Mathis)

The Moire fringes observed in PVTEM are a result of electron beam interference between the GaAs substrate lattice and the InGaAs epitaxial layer lattice. Similar Moire fringes are observed in PVTEM of relaxed InAs islands on GaAs substrates [74]. This confirms that the removal of misfit dislocations is indeed a result of the lateral oxidation process and not a consequence of delamination during the TEM sample preparation procedures.

3.6.3. Dependence on Strain Relaxation on Lattice Mismatch and oxidation conditions

The process of strain relaxation during lateral oxidation is studied by varying the strain in the as-grown $In_xGa_{1-x}As$ template and by varying the nature of the $In_xGa_{1-x}As$/oxide interface. Changing the Indium composition in the template varies the mismatch strain in the template and the initial misfit dislocation density, whereas varying the oxidation temperature controls the nature of the InGaAs/oxide interface.



As grown template

Lattice Engineered Substrate

Strain relaxation affected by:

Initial Strain in InGaAs	- Vary Indium composition
Oxidation Process	- Vary oxidation temperature
	- Vary Sb content in $AlAs_{1-x}Sb_{1-x}$

Goal : Minimize relaxation of as-grown template
Maximize relaxation after oxidation

Figure 3.17: Factors affecting strain relaxation during lateral oxidation of AlAs

The goal is to minimize the relaxation of the as-grown InGaAs template and maximize the relaxation after the process of lateral oxidation as summarized in Figure 3.17.

After growth the substrate was patterned using photolithography and reactive ion etching into 100 μm x 100 μm square mesas to enable lateral oxidation of the AlAs layers. Lateral oxidation was carried out in a furnace

with steam generated by bubbling N_2 gas through water maintained at 90 °C. The oxidation temperatures of 410, 430 and 450 °C were used and the oxidation time was chosen so as to completely oxidize the mesas. There was no significant difference in oxidation rates of AlAs with different $In_xGa_{1-x}As$ overlayers. To ascertain whether strain relaxation is caused by lateral oxidation only and not by thermal annealing, a set of the patterned samples were annealed under same conditions, but in a non-oxidizing environment. The degree of strain relaxation was determined by X-Ray diffraction of as-grown, oxidized and annealed templates.

Figure 3.18 shows the extent of strain relaxation of the as grown and oxidized/annealed $In_xGa_{1-x}As$ templates as a function of oxidation temperature. As the Indium composition is increased, the relaxation of the as-grown epitaxial layers increases due to higher lattice-mismatch. This implies that the misfit dislocation density at the $In_xGa_{1-x}As$/AlAs interface increases with the Indium composition. The strain in the $In_xGa_{1-x}As$ template is relaxed after oxidation with the degree of relaxation increasing with oxidation temperature.

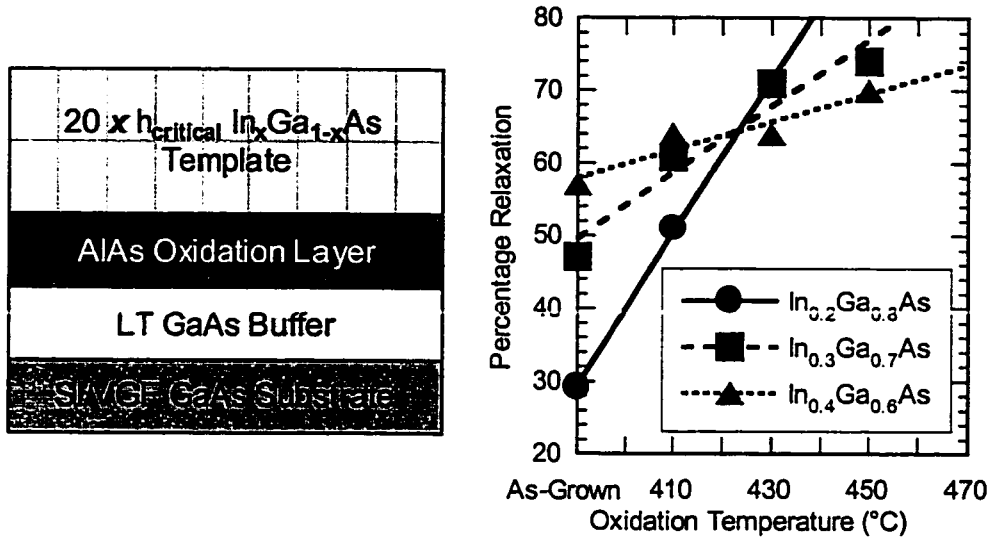


Figure 3.18: Strain Relaxation as a function of oxidation temperature for various $In_xGa_{1-x}As$ templates grown on SI/VGF GaAs substrates

During the process of AlAs oxidation, strain relaxation can occur in because of two different mechanisms. The first is the increased thermal energy available for threading dislocation movement; the other is change in the nature of the $In_xGa_{1-x}As/Al_2O_3$ interface. Data from the published literature for low Indium composition $In_xGa_{1-x}As$ epilayers indicates that strain relaxation due to thermal annealing occurs only at temperatures exceeding 650-700 °C [16]. Hence at oxidation temperatures of 410-450 °C, the thermal energy in the system appears to be insufficient to substantially enhance threading dislocation motion. This is corroborated by the fact that no strain relaxation is observed for the $In_{0.2}Ga_{0.8}As$ and $In_{0.3}Ga_{0.7}As$ structures annealed under

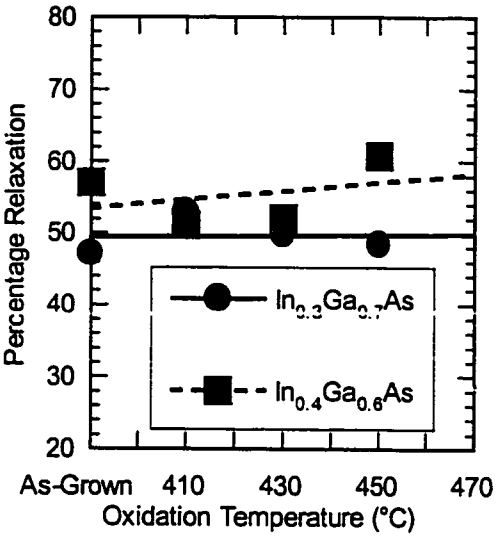


Figure 3.19: Strain Relaxation as a function of Annealing Temperature for InGaAs LES Templates grown on SI/VGF GaAs Substrates

the same conditions as seen in Figure 3.19. However in the case of $In_{0.4}Ga_{0.6}As$ structures relaxation is observed. This is due to the combination of high excess stress due to 2.8 % lattice mismatch, oxidation/annealing temperatures that are 100-150 °C higher than growth temperatures. On the other hand for the $In_xGa_{1-x}As$ (x=0.2, 0.3) structures the oxidation and annealing temperatures are nearly the same as the growth temperature. It has been reported previously that conversion of AlAs to Al_2O_3 results in volume contraction. Since the dislocation glide velocity is directly proportional to the effective stress, it is proposed that the stress generated at the oxidation front during volume contraction increases the threading dislocation glide velocity. Also from Figure 3.18, it is observed that strain relaxation can be greatly enhanced by increasing the oxidation temperature from 410 °C to 450 °C. Since the available thermal energy for threading dislocation glide does not increase appreciably for such a small change in temperature and effective stress due to volume contraction

does not change appreciably, the only possible reason for the enhanced strain relaxation is the change in the nature of the InGaAs/oxide interface. Oxidation kinetics of AlAs change from a diffusion limited mechanism to a reaction-limited mechanism as the oxidation temperature is increased from 410 °C to 450 °C. It is therefore proposed that the increase in strain relaxation with oxidation temperature is due to the increased porosity of the InGaAs/oxide interface, which reduces the misfit dislocation interaction. Also reactive removal of misfit dislocation cores is enhanced at higher oxidation temperatures. PVTEM analysis of oxidized $In_{0.2}Ga_{0.8}As$ lattice-engineered substrates supports this hypothesis.

The role of the initial dislocation density on the efficiency of relaxation is clear if the slope of the strain relaxation curve is examined. The barrier to threading dislocation movement is higher for higher Indium composition templates due to higher initial misfit dislocation density. Hence strain relaxation after oxidation is less efficient for the $In_{0.4}Ga_{0.6}As$ structure. The trend also points towards pathways to increase the degree of strain relaxation for higher Indium composition templates. Reducing the misfit dislocation density at the as-grown InGaAs/AlAs interface can enhance strain relaxation. An alternate way is to change the nature of the oxide and the InGaAs/oxide interface itself. Besides increasing the oxidation temperature, this can be achieved by addition of Sb (upto 10 %) to AlAs. Addition of Sb to AlAs has demonstrated a significant change in the oxidation mechanism and the InGaAs/oxide interface.

Figure 3.20 compares the theoretically predicted strain relaxation with the as-grown and oxidized LES templates as a function of misfit strain.

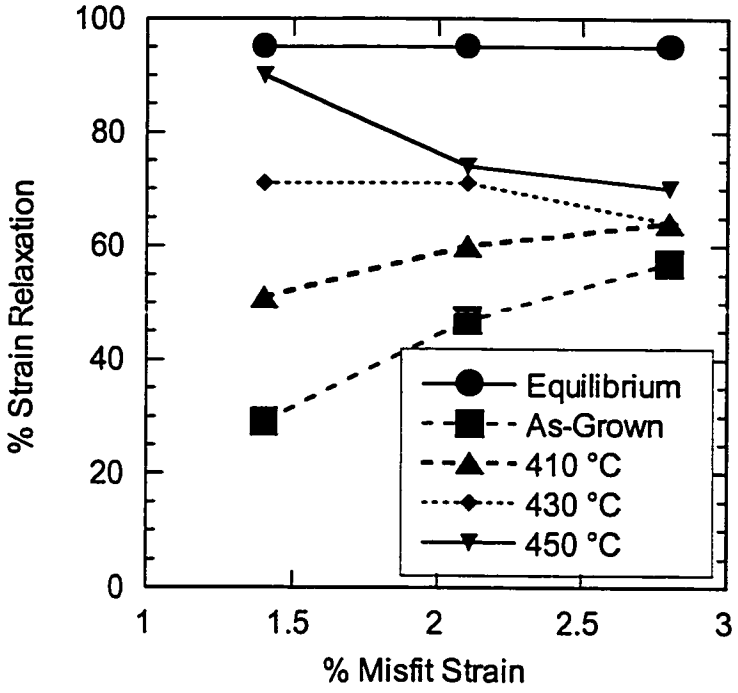


Figure 3.20: Strain relaxation as a function of misfit strain for lattice-engineered substrates

Under equilibrium conditions 95 % strain relaxation is observed in a heteroepitaxial layer that is 20 times its critical thickness. In the case of LES templates the % strain relaxation in the as-grown templates is much lower than expected which is a result of low temperature 2D growth, which suppresses strain relaxation. With the increasing oxidation temperature the observed strain relaxation is seen to increase. For an $In_{0.2}Ga_{0.8}As$ template the equilibrium value strain relaxation is achieved. As the lattice mismatch is increased the maximum observed strain relaxation reduces. However the observed strain relaxation is much higher than observed in InGaAs heteroepitaxial layers grown directly on GaAs substrates.

Figure 3.21 compares the percentage strain relaxation of InGaAs epitaxial layers as a function of the normalized layer thickness, ($h/h_{critical}$). Strain relaxation data for 2000 Å thick $In_xGa_{1-x}As$ layers of various compositions directly grown on GaAs substrate is used from data of Krishnamoorthy et al. [18]. Strain relaxation data for $In_{0.2}Ga_{0.8}As$/GaAs strain layer superlattices (SLS) from Bender et al. and Li et al. is also plotted for comparison [75, 76].

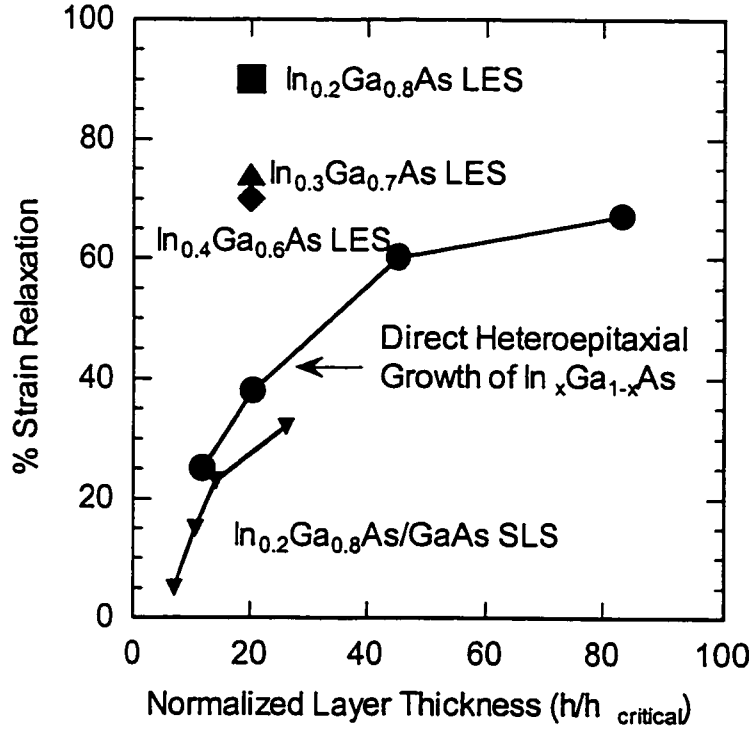


Figure 3.21: Comparison of observed strain relaxation as a function normalized layer thickness for LES Templates and InGaAs epitaxial layers grown by conventional techniques. Data for bulk InGaAs layers is from reference [18], data for InGaAs/GaAs SLS is from references [75] and [76].

It can been seen that strain relaxation for bulk InGaAs layers grown on GaAs substrates saturates to 70 % for large layer thickness. The observed strain relaxation in InGaAs/GaAs SLS is lower than in bulk layers but shows a similar trend. In contrast significantly higher strain relaxation is observed in InGaAs lattice-engineered substrates. The degree of the strain relaxation reduces with the increase in lattice mismatch. All the above observations highlight the dominant role of dislocation blocking in limiting strain relaxation in conventional approaches to heteroepitaxy. In the LES approach, the removal of misfit dislocations during the oxidation process, has a significant effect on this process and this explains the much higher observed strain relaxation.

Figure 3.22 shows the variation of the elastic strain as function of layer thickness for InGaAs lattice-engineered substrates and compares it with experimentally observed data. In the case of heteroepitaxial layers grown using conventional techniques, the residual elastic strain much higher than equilibrium model initially, however for increasing the layer thickness does not result in further reduction of elastic strain due to work hardening. The residual elastic strain increases with lattice mismatch, as the high density of dislocations generated in earlier stages of growth is very effective in preventing glide of dislocations.

In contrast, the residual elastic strains for a given layer thickness in InGaAs lattice-engineered substrates are much lower than InGaAs epitaxial layers grown by conventional approaches. This as described before is a combination of two factors. Structural changes occurring during lateral oxidation result in driving forces for strain relaxation that are much higher in the case of lattice-engineered substrates. The other factor is the reactive removal of majority misfit dislocations that enables the effective glide of remaining misfit dislocations. The reduction of elastic strain with layer

thickness increases with the oxidation temperature. Also in the case of the $In_{0.4}Ga_{0.6}As$ LES template, the residual elastic strain in the as-grown template is lower than that predicted by the model. This may be due to the low-growth

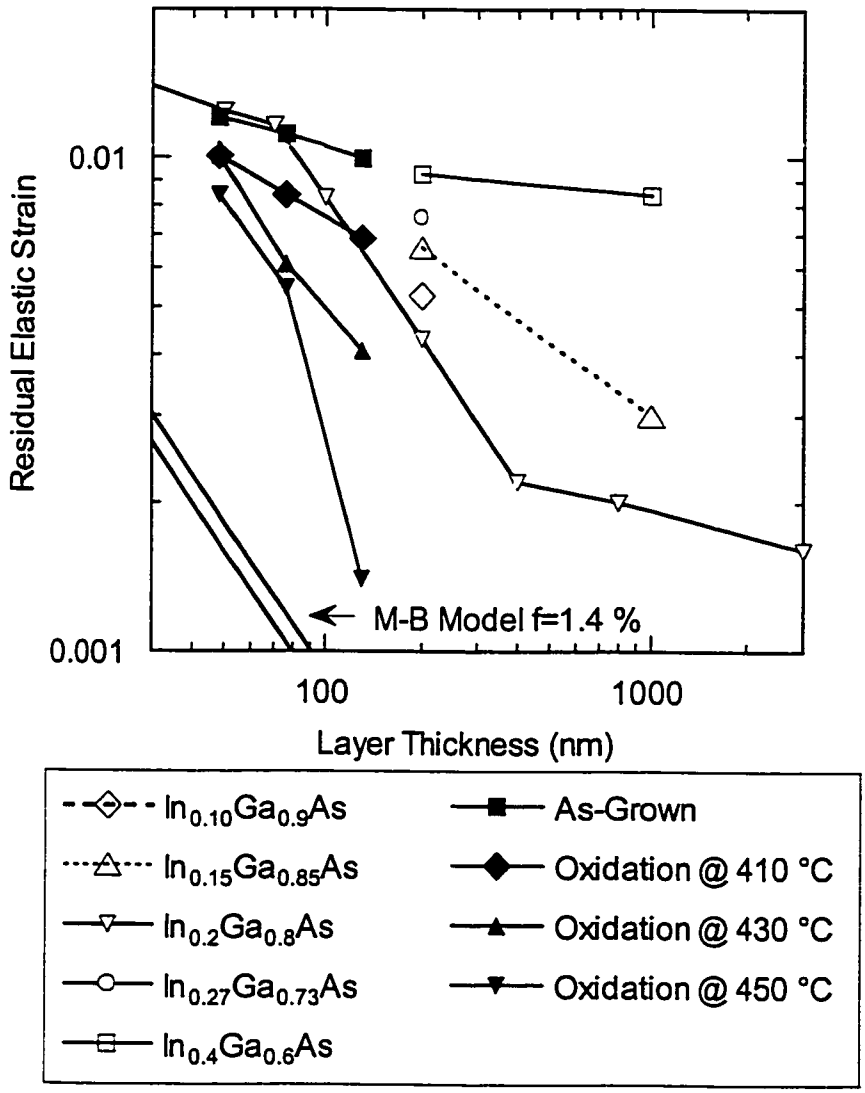


Figure 3.22: Variation of residual elastic strain as function of heteroepitaxial layer thickness. Filled symbols correspond to InGaAs lattice-engineered substrates (48 nm-$In_{0.4}Ga_{0.6}As$, 76 nm - $In_{0.3}Ga_{0.7}As$, 130 nm – $In_{0.2}Ga_{0.8}As$). Open symbols correspond to InGaAs layers grown directly on GaAs substrates. Data is for $In_{0.2}Ga_{0.8}As$ is from Dunstan et al. [77], data for all other compositions is from Krishnamoorthy et al. [18].

temperature that maintains a 2D growth mode and restricts the strain relaxation to be by misfit dislocation formation only. It is also observed that for a given oxidation temperature the residual elastic strain increases with the decrease in layer thickness (and Indium composition in $In_xGa_{1-x}As$). This can be a consequence of two different mechanisms. The first is that a heteroepitaxial layer with lower thickness can support a higher elastic strain without plastic deformation. The other reason for increase in residual elastic strain with Indium composition may be the increase in the yield strength of InGaAs with the Indium composition. Data presented by Krishnamoorthy et al. suggests that the yield strength of InGaAs increases with Indium composition from 0 to 50 % and then decreases from 50 % to 100 % [78].

3.6.4. Comparison with similar strain relaxation Approaches

Figure 3.23 compares the residual elastic strain in lattice-engineered substrates with various amorphous interlayer based approaches for enhancing strain relaxation. Compared to the $In_{0.2}Ga_{0.8}As$ LES, higher residual elastic strains are observed in the case of the SiGe based approaches [35, 42]. Also these structures have much lower lattice mismatch (0.6 % compared to 1.4 – 2.8%), hence the effect of dislocation blocking is less severe. Also the annealing temperatures used are much higher and about 500 °C higher than the growth temperatures. On the other in the lateral oxidation approach as used by Seo et al. has much higher residual elastic strain [72].

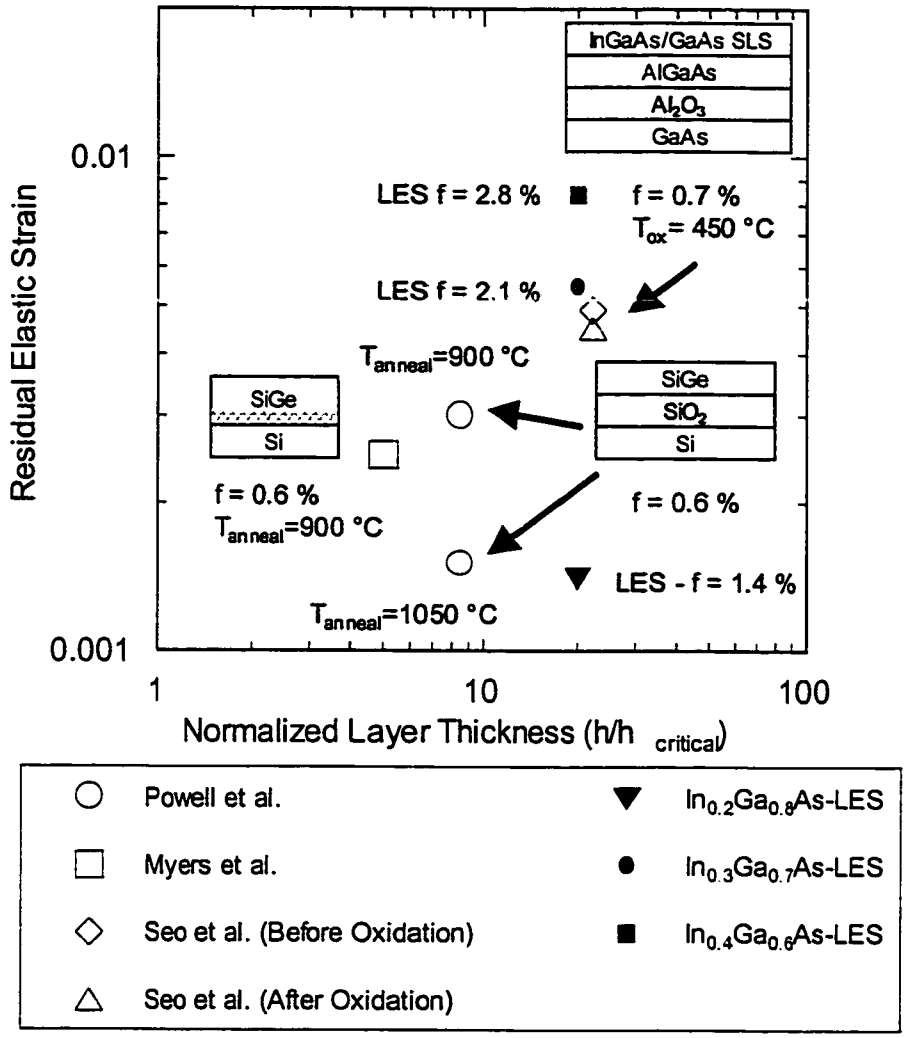


Figure 3.23: Comparison of residual elastic strains in LES and other amorphous interlayer based approaches for enhancing strain relaxation [35],[42],[72]

The SiGe based approaches have a porous and reactive interface between a strained overlayer and an amorphous interlayer. However the driving force for strain relaxation is mainly from thermal annealing. On the other hand, insertion of an AlGaAs spacer layer between the oxidation layer

and the strain overlayer eliminates the possibility of reactive removal of misfit dislocations during lateral oxidation. The only additional driving forces for strain relaxation are generated by structural changes occurring during lateral oxidation. In comparison, the lattice-engineered substrate approach incorporates the reactive and amorphous interface with the additional driving forces generated in the process of creating the interface. Hence the higher strain relaxation efficiency is observed for much higher lattice mismatch strains.

3.6.5. Pathways to Improve Strain relaxation efficiency

Reduction of Misfit Dislocation Density in As-grown LES Templates

As discussed in the previous section, one of the ways to improve the strain relaxation efficiency is to reduce the misfit dislocation density at the $In_xGa_{1-x}As$/AlAs interface in the template. An additional advantage is the improvement in the structural quality and surface morphology of the InGaAs template. This is achieved by reduction of the $In_xGa_{1-x}As$ template growth temperature. In the case of $In_{0.3}Ga_{0.7}As$ LES templates, reduction in the growth temperature for $In_{0.3}Ga_{0.7}As$ templates from 430 °C to 400 °C, reduces the strain relaxation of the as-grown sample, also the rms surface roughness reduces from 7 Å to 4 Å. In the case of $In_{0.4}Ga_{0.6}As$ LES templates, reduction in the growth temperature from 400 °C to 300 °C, reduces the strain relaxation of the as-grown sample, also the rms surface roughness reduces from 24 Å to 7 Å. The improvement in surface morphology is significant in the case of $In_{0.4}Ga_{0.6}As$ LES templates than the $In_{0.3}Ga_{0.7}As$ LES Templates. (For detailed discussion please refer to Chapter 2, Section 2.5).

Figure 3.24 compares the strain relaxation as a function of oxidation temperature for the $In_{0.3}Ga_{0.7}As$ and $In_{0.4}Ga_{0.6}As$ LES templates. The higher efficiency of strain relaxation as seen in templates grown at low temperature is a direct consequence of the lower misfit dislocation density in the template grown at lower growth temperature. Also the lower surface roughness is results in better regrowth of the desired epitaxial layers.

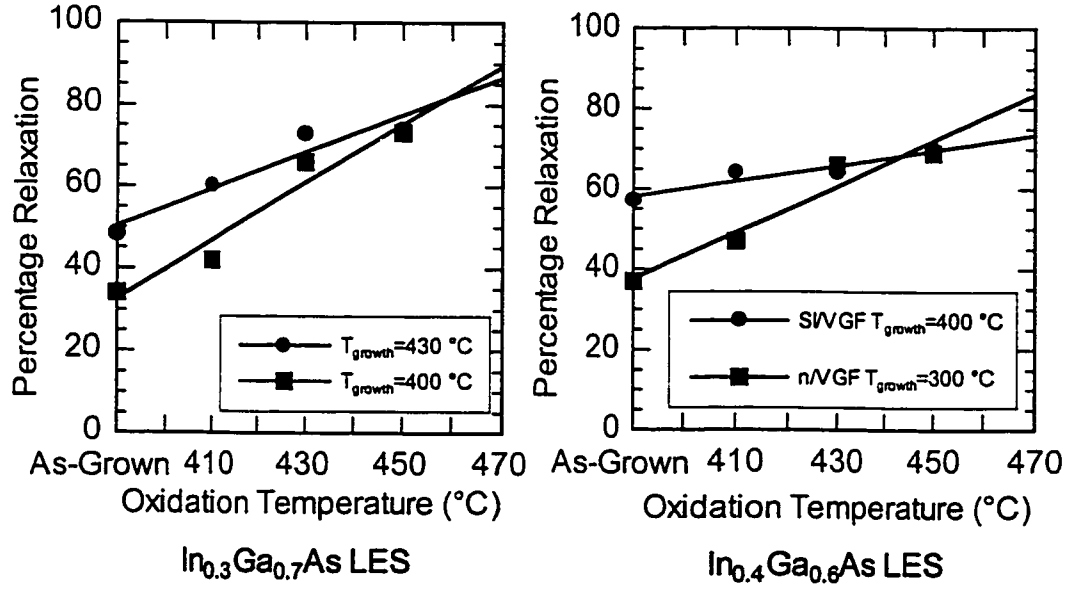


Figure 3.24: Comparison of strain relaxation as a function of $In_xGa_{1-x}As$ growth temperature

Changing the Nature of the oxide and the InGaAs/oxide interface

Another approach to increase the strain relaxation efficiency is to change the nature of the $In_xGa_{1-x}As$/oxide interface itself. This is achieved by addition of Sb (upto 10 %) to the AlAs oxidation layer. An important consequence of addition of Sb to AlAs is the segregation of Sb during lateral oxidation, which results in an increase in the porosity of the oxide. This

changes the oxidation kinetics from diffusion limited to reaction rate limited. Thus oxidation of larger size mesa is possible, as the oxidation reaction is no longer limited by the diffusion of the reactants through the oxide.

To investigate the effect of Sb addition on the strain relaxation process, $In_{0.2}Ga_{0.8}As$ template layers were grown on AlAsSb oxidation layers with Sb compositions of 0, 7 and 10%. Figure 3.25 shows the effect of Sb addition on the strain relaxation process during lateral oxidation.

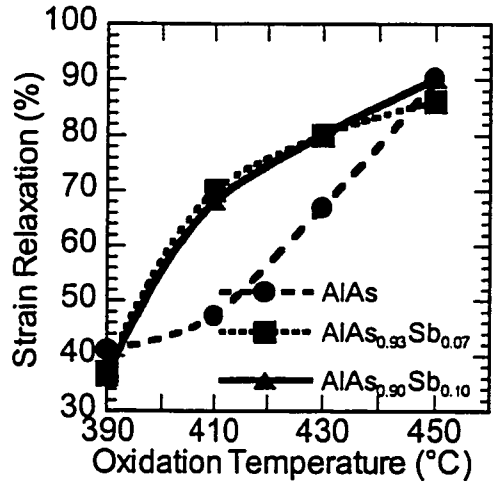


Figure 3.25: Strain relaxation as function of oxidation temperature for various $In_{0.2}Ga_{0.8}As$ templates with AlAsSb oxidation layers

As seen from Figure 3.25, addition of Sb to AlAs improves the strain relaxation efficiency at a given oxidation temperature when compared to AlAs. This is as mentioned before is a consequence of increased porosity of the oxide.

Strain Relaxation in GaAsSb LES Templates

As described in Chapter 2, low temperature growth of GaAsSb results in a surface morphology that has a lower surface roughness. This makes GaAsSb based lattice-engineered substrates desirable for regrowth purposes. Figure 3.26 shows the variation of strain relaxation as a function of lattice-mismatch and oxidation temperature of GaAsSb LES templates.

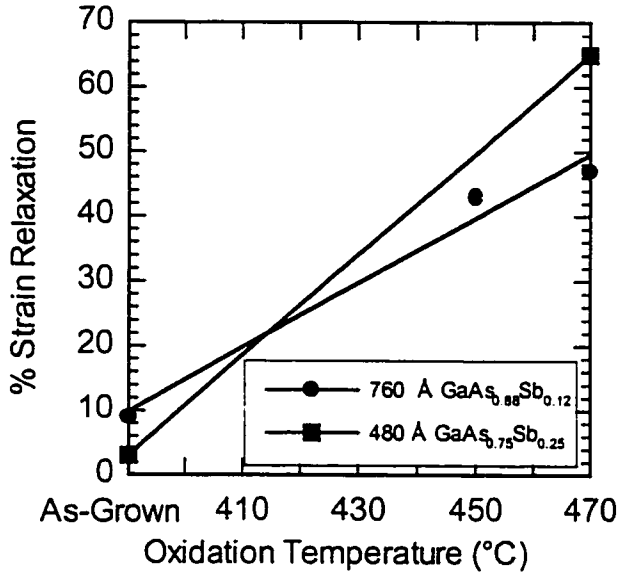


Figure 3.26: Strain relaxation as a function of oxidation temperature for GaAsSb LES Templates

Higher strain relaxation efficiency, that is change in strain relaxation as function of oxidation temperature is observed in GaAsSb LES Templates when compared to InGaAs LES Templates. However the main advantages of GaAsSb based lattice-engineered substrates are better resistance to high temperature oxidation when compared to InGaAs based lattice-engineered substrates as will be discussed in the next chapter.

3.7. Conclusion

To summarize, the process of strain relaxation of InGaAs and GaAsSb LES templates during lateral oxidation was studied in detail. Compared to conventional approaches for heteroepitaxy, significantly higher strain relaxation is achieved for a given heteroepitaxial layer thickness. The efficient accommodation of mismatch strain is a consequence of reduced dislocation blocking, which is a result of reactive removal of misfit dislocations at the InGaAs/oxide interface during lateral oxidation process. All the stresses generated by contraction during the lateral oxidation process provide additional driving forces for the process of strain relaxation.

To maximize the strain relaxation in the InGaAs template after lateral oxidation of the underlying AlAs layer, it is necessary to minimize the strain relaxation of the as-grown InGaAs template. This is achieved by lowering the InGaAs growth temperature. The strain relaxation efficiency can also be improved by changing the porosity of the oxide and the nature of the InGaAs/oxide interface. This can be achieved by the use of higher oxidation temperature and the addition of Sb to the AlAs oxidation layer. Since the process of strain relaxation is driven by excess stress present in the InGaAs template, it is not possible to achieve complete strain relaxation. This is because as the template relaxes the excess stress in the template that acts a driving force is reduced. Also below a certain value, a heteroepitaxial layer can accommodate the residual elastic strain without forming additional dislocations.

3.8. References

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Chapter 4.
Structural Characterization of Epitaxial Layers Grown on Lattice-Engineered Substrates

4.1. Introduction

The GaAs based lattice-engineered substrate (LES) technology enables the growth of material systems with lattice constants between GaAs and InP. The various III-V material systems that can be grown are $Al_xGa_yIn_{1-x-y}As$, $Al_xGa_{1-x}As_{1-y}Sb_y$, $Al_xGa_yIn_{1-x-y}P$ and $In_xGa_{1-x}As_{1-y}P$. The material systems enable the growth of long-wavelength optoelectronic devices on GaAs based LES and have many advantages compared to long-wavelength optoelectronic materials grown on InP substrates. In this chapter the structural properties of epitaxial layers grown on LES will be discussed. Compared to conventional epitaxy where the epitaxial growth is initiated on binary semiconductor substrate with the initial buffer layer being a binary semiconductor, epitaxial growth on LES involves the initiation of growth on a ternary semiconductor surface with a ternary semiconductor. As a result of this the quality of the epitaxial layers is mainly determined by surface preparation techniques. As

discussed in this chapter using ion based surface cleaning techniques that are common in semiconductor processing results in a high density of dislocations due to surface damage. Eliminating these processes is necessary to achieve good quality regrowth on LES. In general it is observed that the residual elastic strain and surface roughness in epitaxial layers grown on LES is lower than those grown on GaAs substrates under identical growth conditions.

Section 4.2 discusses the various issues involved in epitaxial regrowth on lattice-engineered substrates. These include the sacrificial cap layers that protect the InGaAs template during processing and lateral oxidation and AlAs defect diffusion barrier that prevent the diffusion of defects in the InGaAs template during the lateral oxidation process. The other important aspect of epitaxial regrowth is the removal of native oxides from the InGaAs surface before regrowth. In section 4.3, details of the various $In_xGa_{1-x}As$ and $GaAs_{1-y}Sb_y$ epitaxial layers grown on lattice-engineered substrates are given. In section 4.4, surface morphology of epitaxial layers grown on lattice-engineered substrates will be discussed. Section 4.5 deals with analysis of strain relaxation in the regrown epitaxial layers. Cross-sectional and plan-view TEM characterization of yields insights into the nature of dislocations in the epitaxial layers regrown on lattice-engineered substrates and is discussed in section 4.6

4.2. Issues in Epitaxial Regrowth on Lattice-Engineered Substrates

Since the Lattice-Engineered Substrates undergo a significant amount of processing prior to regrowth, it is important to consider the effect of these processes on the material quality of the InGaAs epitaxial template layers. The

two significant effects involved here are the diffusion of defects and vacancies during lateral oxidation and the formation of native oxides on the exposed surfaces of the lattice-engineered substrate.

4.2.1. Defect Diffusion During Lateral Oxidation

As discussed in the previous chapter, lateral oxidation of AlAs results in efficient relaxation of strained epitaxial overlayers. However the process of oxidation itself results in the formation of vacancies and electronic defects like elemental Arsenic, Ga vacancies and atomic Oxygen. Conversion of AlAs to Al_2O_3 results in a volume reduction up to 10%. This causes stress in the epitaxial layers above the oxidation layer, with the stress being maximum at the oxidation front where the byproducts of the oxidation process are generated. The diffusion of these defects into the InGaAs epitaxial template is enhanced due to the stress at the oxidation front. Thus the lattice-engineered substrate contains excess As and Ga vacancies which are incorporated in the regrown epitaxial layers (as shown in Figure 4.1). The defects result in

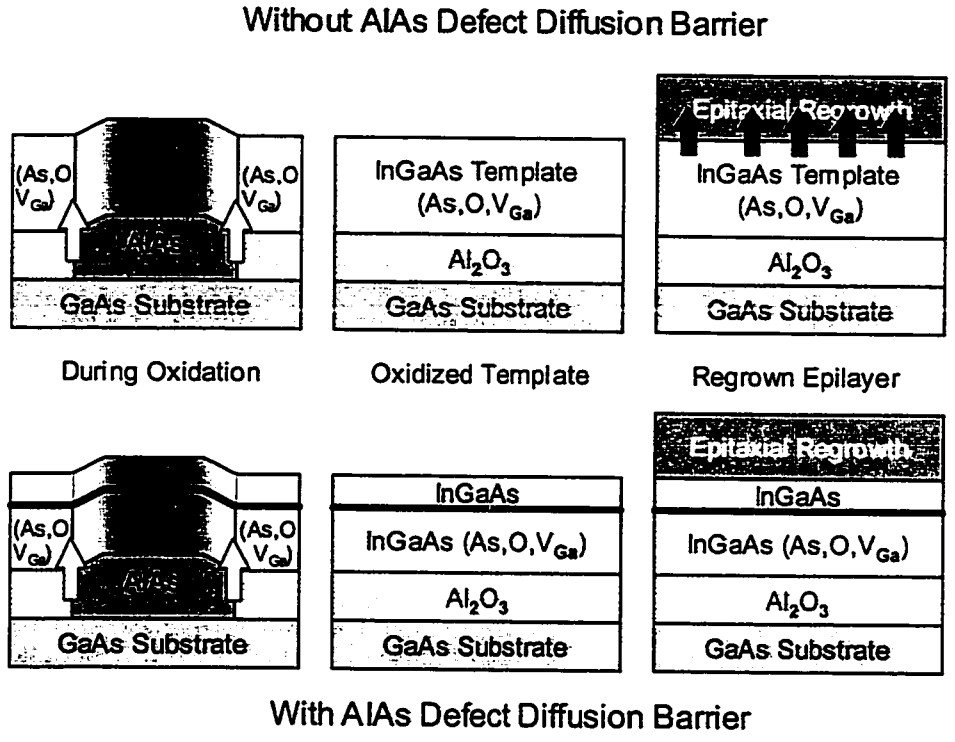


Figure 4.1 Stress Enhanced Diffusion of Defects During Lateral Oxidation of AlAs

degraded electronic and optical properties of epitaxial layers grown on lattice-engineered substrates.

This stress-enhanced diffusion of defects can be prevented by the insertion of a thin (50 Å) AlAs defect diffusion barrier in the InGaAs epitaxial template. AlAs defect diffusion barriers have been previously shown to be effective in blocking the diffusion of defects from LT GaAs layers into active device layers [1]. The thin AlAs defect diffusion barrier does not oxidize due to surface tension effects at the AlAs /oxide interface.

4.2.2. Surface Preparation For Epitaxial Regrowth on Lattice Engineered Substrates

Since a contaminant and native oxide free surface is desired for epitaxial regrowth, the InGaAs epitaxial layers are capped with sacrificial epitaxial layers which consist of a 30 Å thick AlAs etch stop layer and a 200 Å thick GaAs layer. The use of these layers ensures that the InGaAs epitaxial layers are not exposed to solvents and photoresist during the processing for mesa oxidation. These layers also eliminate the need for the commonly used SiO_2 or Si_3N_4 dielectric protective caps during lateral oxidation.

After lateral oxidation, the surface oxide on the sacrificial GaAs cap is removed by buffered HF solution. Then the GaAs cap is removed in a citric acid: H_2O_2 solution which stops on the AlAs etch stop layer. The AlAs etch stop layer is subsequently removed in a BHF solution which stops on the InGaAs epitaxial layer. The use of selective wet chemical etches is essential as the layer thicknesses involved here are small and a smooth surface morphology is desired after etching. Since the removal of sacrificial cap layers is done ex-situ, the removal of native oxides formed on the InGaAs surfaces is essential prior to regrowth.

Desorption of native oxides from binary III-V semiconductor substrates like GaAs and InP is relatively easy if sufficient Group V overpressure is maintained. Ga_2O_3 desorbs in the temperature range of 580-600 °C, whereas In_2O_3 desorbs at 520 °C. However desorption of native oxides from ternary semiconductor surfaces like InGaAs is difficult. This is because a minimum temperature of 580 °C is required to desorb all the native oxides and this temperature results in a significant desorption of Indium from the surface. This not only results in a change in surface composition but also degrades the

surface morphology. This is undesirable as the regrowth surface can now act as a source of dislocations. This has been verified by C-V and TEM analysis of regrown epitaxial layers on InGaAs surfaces thermally desorbed at 575 °C [2]. However desorption at this temperature results in a change in the surface composition as described before. This results in the generation of dislocations at the regrowth interface as seen from TEM.

The various processes investigated for the removal of native oxides from the surface prior to regrowth on lattice-engineered substrates are illustrated in Figure 4.2. In Process A, Ar ion sputtering was used to remove the native oxides from the InGaAs surfaces. The beam current was 20 mA and the sputtering time was 30 seconds. This process has been used previously on GaAs substrates. However Ar sputtering on InGaAs surfaces results in removal of the fragile Ga_2O_3 oxide whereas the In_2O_3 native oxide is still bound to the surface. Thermal desorption at a temperature of 520 °C was implemented. Unfortunately this does not result in complete removal of In_2O_3. As a result in process B, the thermal desorption temperature was increased to 630 °C. At this temperature, all the native oxides on the InGaAs surface are removed. However regrowth is still initiated on an ion damaged surface. This is a source of dislocations as demonstrated in the case of heteroepitaxial growth of InGaAs on ion-damaged GaAs surfaces [3], and for GaAs-on-GaAs homoepitaxy on surfaces that were exposed to a 200 W H_2 plasma to remove the native oxide [4]. Structural characterization of regrown GaAs/GaAs interface by Choquette et al. demonstrated that achieving surface reconstruction is essential for achieving dislocation-free regrowth interfaces even on oxide removed surfaces [5]. This is enabled by thermal desorption upto 630 °C.

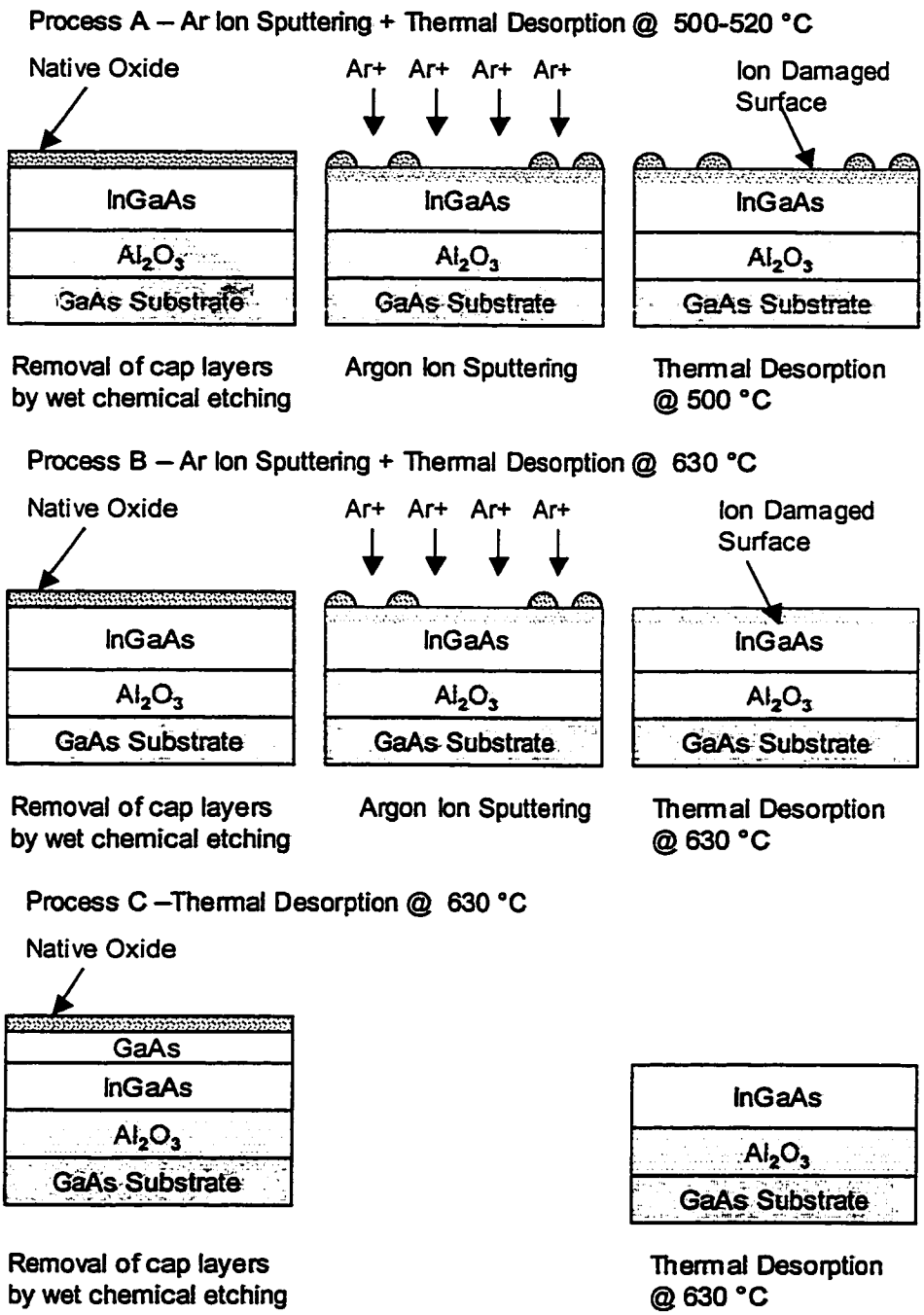


Figure 4.2: Various Processes Investigated for Removal of Native Oxides from Lattice-Engineered Substrates

The problem of initiating epitaxial growth on an ion-damaged surface can be eliminated by using only thermal desorption at high temperatures (~ 630 °C) to desorb the native oxides. However, exposure of InGaAs surfaces to high temperatures results in desorption of Indium from the surface and alloy decomposition. For example, desorption of $In_{0.53}Ga_{0.47}As$ at 565 °C, results in an InGaAs surface with an effective composition of 20 %. In the case of GaAsSb, desorption of As and Sb oxides occurs at much lower temperatures [6]. However, desorption of Ga_2O_3 requires the exposure of GaAsSb surfaces to Arsenic flux at high temperatures, which results in As/Sb exchange at the surface [7].

To eliminate this problem, a 20 Å GaAs cap was inserted between the InGaAs/GaAsSb layers and the AlAs etch stop layer. As a consequence, the ternary layers are never exposed to air. This enables high temperature thermal desorption without significant deterioration of the surface. It is estimated that after processing and thermal desorption about 10 Å or 2 monolayers of GaAs remains on the surface. This layer thickness is well below the critical thickness to cause dislocation generation. Figure 4.3 compares the RHEED patterns during desorption of an $In_{0.3}Ga_{0.7}As$ lattice-engineered substrate with a 20 Å cap. The use of Ar sputtering combined with high temperature desorption at 630 °C (Process B) yields smooth surface as evidenced by the streaky RHEED pattern prior to the initiation of regrowth. However this process results in a ion-damaged surface which is undesirable. Thermal desorption without the use of Ar sputtering (Process C) also results in surfaces of comparable quality as seen from the RHEED pattern. The presence of elongated spots indicates a slightly rougher surface. A similar RHEED pattern is observed during thermal desorption of epi-ready GaAs substrates. It is important to note that upon

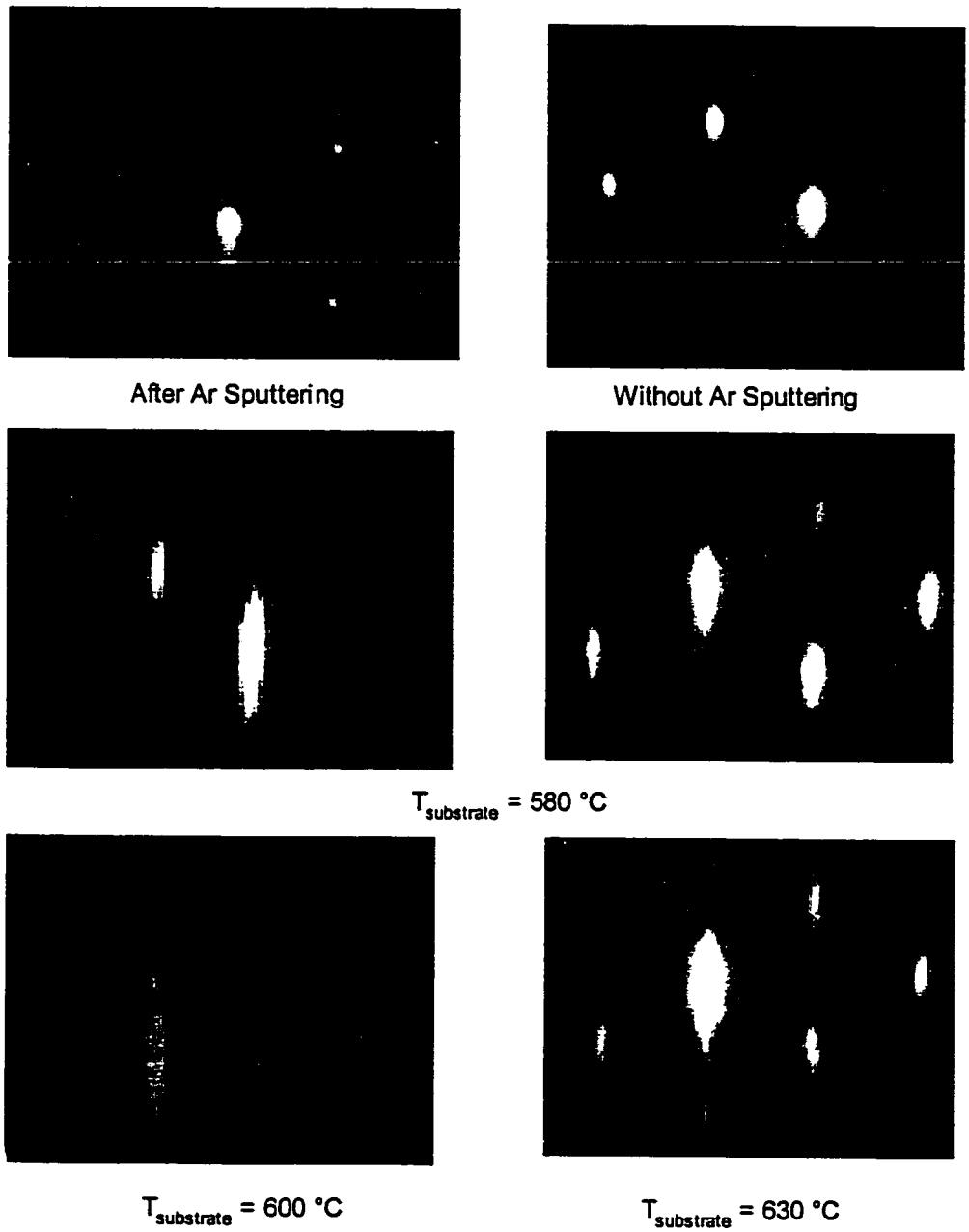
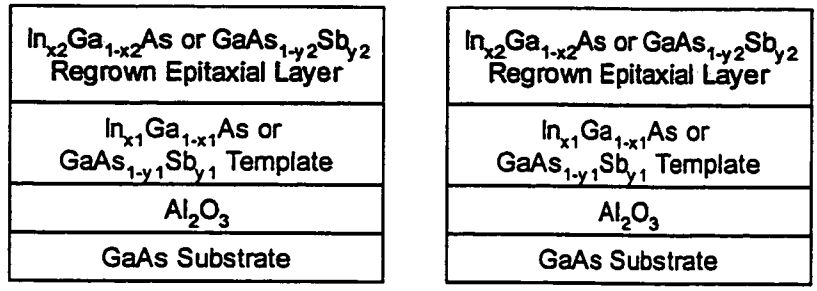


Figure 4.3: Comparison of RHEED Patterns of Lattice Engineered Substrates with and without Ar sputtering

initiation of regrowth, the RHEED patterns were similar after deposition of 500 Å of material on both Ar sputtered and non-Ar sputtered (Process B and C) surfaces. On the contrary RHEED pattern of Ar–sputtered InGaAs surfaces (Process A) were streaky but had low intensity.

4.3. MBE Growth of Epitaxial Layers on Lattice-Engineered Substrates

Lattice-engineered substrates (LES) offer the possibility of heteroepitaxial growth at lattice constants other than the conventional binary III-V substrates. Epitaxial growth on LES is possible in two different modes as illustrated in Figure 4.4. The first is strain-free growth of a semiconductor whose lattice constant is same as that of the in-plane lattice constant of the LES. In this case the Indium composition of the Sb composition of the regrown epitaxial layer is lesser than that of the LES epitaxial template layer The other



$a_{Regrowth} = a_{In-Plane(In_{x1}Ga_{1-x1}As/GaAs_{1-y1}Sb_{y1})}$ $a_{Regrowth} = a_{bulk(In_{x1}Ga_{1-x1}As/GaAs_{1-y1}Sb_{y1})}$

x2 < x1 ; y2 < y1 x2 = x1 ; y2 = y1

Figure 4.4: Schematic of Epitaxial Layers grown on Lattice-Engineered Substrates

is continued growth of the same semiconductor alloy as the LES epitaxial template layer.

In the first case the epitaxial layer grows in a strain-free condition and no dislocation generation due to lattice-mismatch is expected. In the second case, additional dislocation generation and propagation at the porous InGaAs/Al_2O_3 interface is expected as the epitaxial layer grows under strained conditions. This is so because the strain relaxation in the InGaAs LES is not complete.

4.3.1. Growth of InGaAs Epitaxial Layers on Lattice-Engineered Substrates

$In_xGa_{1-x}As$ epitaxial layers of various compositions were grown on

Lattice Engineered Substrate	Surface Prep Process	Regrowth
$In_{0.2}Ga_{0.8}As$ *(Equivalent to $In_xGa_{1-x}As$ x~ 11-15 % Depending on the oxidation conditions)*	Ar Sputter + Desorption @ 500 °C (Process A)	$In_{0.11}Ga_{0.89}As$, $In_{0.15}Ga_{0.85}As$ (Strain Free)
	Desorption @ 630 °C (Process C)	$In_{0.2}Ga_{0.8}As$
$In_{0.3}Ga_{0.7}As$ (Equivalent to $In_xGa_{1-x}As$ x~ 22-25 % Depending on the oxidation conditions)	Ar Sputter + Desorption @ 500 °C (Process A)	$In_{0.22}Ga_{0.78}As$, $In_{0.25}Ga_{0.75}As$ (Strain Free)
	Ar Sputter + Desorption @ 630 °C (Process B)	$In_{0.3}Ga_{0.7}As$
	Desorption @ 630 °C (Process C)	$In_{0.3}Ga_{0.7}As$
$In_{0.4}Ga_{0.6}As$	Ar Sputter + Desorption @ 500 °C (Process A)	$In_{0.3}Ga_{0.7}As$, $In_{0.35}Ga_{0.65}As$

Table 4.1: Details of InGaAs Epitaxial Layers Grown on Lattice Engineered Substrates

InGaAs and GaAsSb lattice engineered substrates. Table 4.1 lists the various epitaxial layers grown on LES. The growth temperature ranged from 490 – 510 °C and the growth rates ranged from 1.0 to 1.2 μm/hr.

4.3.2. Growth of GaAsSb Epitaxial Layers on Lattice-Engineered Substrates

Until now, antimonide based semiconductors have been mainly investigated for infrared devices on GaSb and InAs substrates. By varying the As/Sb ratio, mixed As-Sb compounds can be also grown at all lattice-constants ranging from GaAs to GaSb. The valved cracked antimony source enables precise control of composition [8]. Mixed As-Sb compounds on GaAs substrates were first investigated by Klem et al. [9]. Recently Sb-based DBRs have been used in long-wavelength lasers [10]. During the growth of GaAsSb, the Sb mole fraction is mainly determined by the Sb/Ga mole fraction, the requisite V/III overpressure is provided by the Arsenic flux. It is important to note the incorporation coefficient of Sb is not unity and depends on the

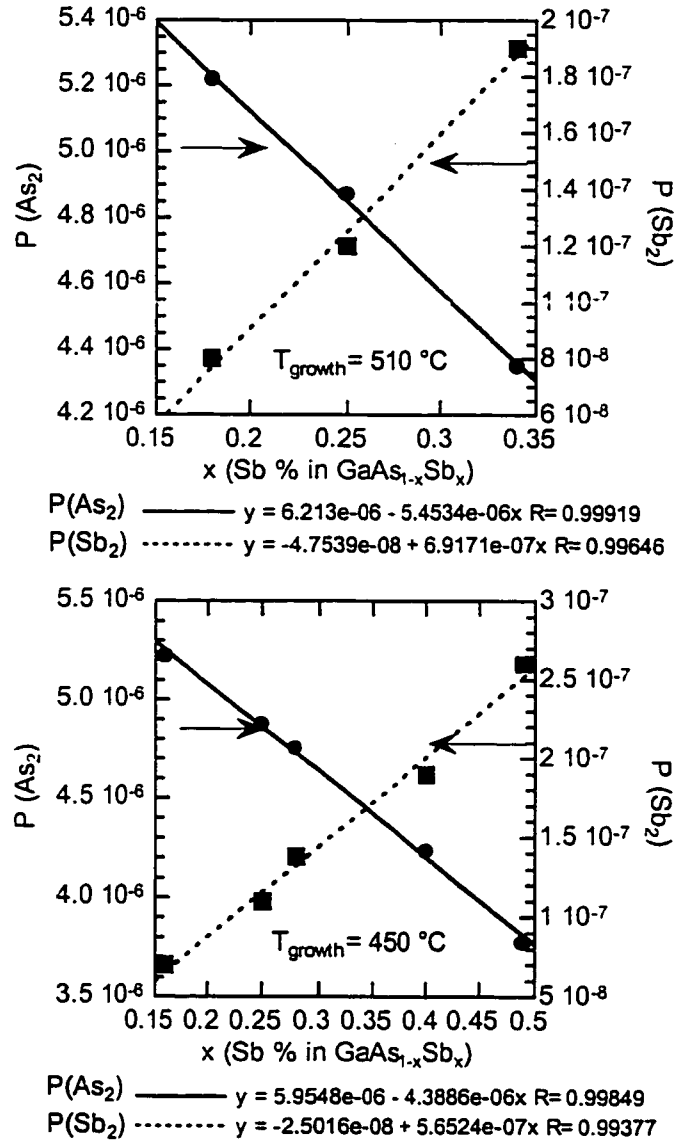


Figure 4.5: Dependence of Sb composition in $GaAs_{1-x}Sb_x$ on As and Sb Fluxes as a function of growth temperature

substrate temperature and the relative ratio of As and Sb fluxes. The Sb mole fraction also depends on substrate temperature as at high growth temperatures the reevaporation of Sb reduces the Sb mole fraction [11]. The growth of

GaAsSb layers on lattice-engineered substrates was investigated as function of As/Sb fluxes and growth temperatures. Figure 4.5 illustrates the variation of Sb composition in GaAsSb epitaxial layers as a function of As, Sb fluxes and growth temperatures. As seen from the figure, at higher temperatures, the incorporation efficiency of Sb is reduced due to Sb desorption from the growing surface. Low Sb fluxes are required as Sb has an incorporation coefficient close to unity.

Table 4.2 lists the various compositions of GaAsSb epitaxial layers grown on lattice-engineered substrates.

Lattice Engineered Substrate	Surface Preparation Process	Regrowth
$In_{0.2}Ga_{0.8}As$ *(Equivalent to* $In_xGa_{1-x}As$ *x~ 11-15 % Depending on the oxidation conditions)*	Desorption @ 630 °C (Process C)	$GaAsSb_{0.18}$ (Strained)
$In_{0.3}Ga_{0.7}As$ *(Equivalent to* $In_xGa_{1-x}As$ *x~ 25 % Depending on the oxidation conditions)*	Ar Sputtering + Desorption @ 500 °C (Process A)	$GaAsSb_{0.22}$ (Strain Free)
	Desorption @ 630 °C (Process A)	$GaAsSb_{0.22}$ (Strain Free)
$In_{0.4}Ga_{0.6}As$ *(Equivalent to* $In_xGa_{1-x}As$ *x~ 30 % Depending on the oxidation conditions)*	Ar Sputtering + Desorption @ 500 °C (Process A)	$GaAsSb_{0.31}$ (Strain Free)

Table 4.2: Details of GaAsSb Epitaxial Layers Grown on Lattice Engineered Substrates

4.4. Surface Morphology of Epitaxial Layers Grown on Lattice Engineered Substrates

Surface morphology is an important factor determining the performance of semiconductor heterostructure devices, as it can limit the mobility of 2DEG electrons, cause increased optical scattering in optical waveguides and increase the FWHM of quantum well emission due to lateral non-uniformities. The most dominant surface feature for low lattice mismatch ($f<1.5$ %) heteroepitaxial systems is the crosshatch patterned (CHP) surface. This consists of a series of intersecting ridges and valleys along the perpendicular [110] and [1 $\bar{1}$0] directions. There have been many attempts to explain the occurrence of this feature. One mechanism suggests that the CHP is developed due to generation of misfit dislocations at the epitaxial layer-substrate interface and surface step pileup that is caused by the glide of these dislocations along the {111} plane [12, 13]. The further development of the pattern is due the suppression of growth in the valley regions that are under high compressive stress and enhancement of growth in the peak regions that are under tensile stress [14, 15].

Zhou et al. proposed that the dislocation strain fields at the interface result in a varying chemical potential at the growing surface. This results in the variation of growth rate across the surface and the development of CHP [16]. Figure 4.6 shows the typical variation in the surface stress due to a misfit dislocation at the interface.

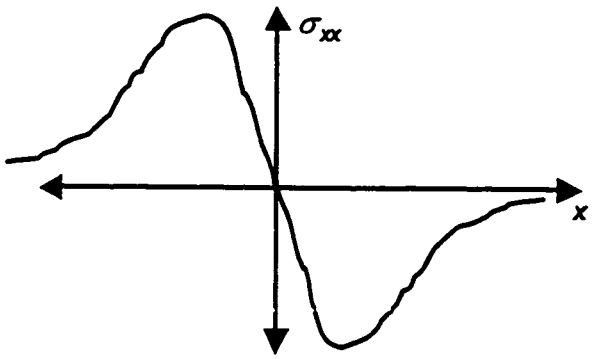


Figure 4.6: Typical variation of surface stress (σ_{xx}) due to a buried misfit dislocation at x=0. Positive values denote tensile stress and negative values denote compressive stress.

The adatom migration rate on a surface under compressive stress is enhanced, and is reduced on a surface under tensile stress. As a result, the growth rate is enhanced in the region under tensile stress and suppressed in the region under compressive stress. Thus a network of misfit dislocations will result in a series of ridges and valleys in the 110 and –1-10 direction giving rise to CHP. These surface undulations are aligned with interface misfit dislocations. The height of ridges depends on the elastic strain in the layer and the interface misfit dislocations [17].

Recent investigation of the surface morphology in the EuTe/PbTe epitaxial system also confirmed that the CHP is mainly due to strong lattice deformation fields produced by a non-uniform misfit dislocation network far below the growing surface [18]. The magnitude of the surface undulations is reduced if an epitaxial layer that is lattice matched to the substrate is grown above the heteroepitaxial layer. This is due to the decaying effect of the dislocation strain fields. This indicates that preferential growth is not the mechanism that gives rise to CHP. Thus for a low lattice mismatch, strain

fields created by dislocations far below the growing surface mainly determine the surface morphology.

For higher lattice mismatches (f > 2%), a rough surface morphology is observed. This is mainly due to 3-D island formation and coalescence. The surface is comprised of crests and deep troughs. While the material in the crest region is relaxed, the troughs are under compression and can act as dislocation nucleation sites [19]. In this case the surface processes that are related to the growth mode mainly determine the surface morphology.

The most common method surface analysis is Atomic Force Microscopy (AFM). This method has been used in this thesis for analyzing the surface morphology of epitaxial layers regrown on lattice-engineered substrates. All the AFM scans in this chapter were done by Dr. Stacia Keller at UCSB. Other methods of measure surface roughness include elastic light scattering [20].

4.4.1. InGaAs epitaxial layers

The surface morphology of lattice mismatched InGaAs layers grown on GaAs substrates has been studied extensively. For Indium compositions less than 15 % a crosshatched surface morphology is observed. The RMS roughness of 10.2 Å was measured on 830 Å thick $In_{0.18}Ga_{0.83}As$ epitaxial layers grown at 490 °C [21]. The surface morphology of relaxed InGaAs layers also depends on the growth conditions. The amplitude of the CHP was found to increase with the reduction of growth rate and increase of growth temperature [22, 23]. The rms surface roughness of 5000 Å thick $In_{0.2}Ga_{0.8}As$ epitaxial layers was reduced from 60 Å to 20 Å when the growth temperature was reduced from 500 °C to 350 °C [24]. This indicates the dependence of

surface mobility of adatoms on the surface morphology. For higher lattice-mismatch (f> 2%) a rough textured surface morphology is observed [12]. In the case of $In_{0.35}Ga_{0.65}As$ epitaxial layers grown at high temperature (~ 500 °C) on GaAs substrates, a rough islanded surface morphology is observed which indicates a 3D growth mode [25].

CHP is also observed in graded relaxed InGaAs layers on GaAs substrates. The surface amplitude of 1 μm graded InGaAs layers grown at 500 °C is 80 Å [26]. The rms surface roughness values of InGaAs buffer graded upto 9 % varies from 50 to 100 Å [27]. However the extension of graded buffer scheme beyond 40% Indium results in a rough surface morphology.

Strain Free Epitaxial Regrowth on LES

Figure 4.7 shows AFM scan of a 5000 Å thick $In_{0.11}Ga_{0.89}As$ layer grown on an $In_{0.2}Ga_{0.8}As$ lattice-engineered substrate and on a GaAs substrate. Surface

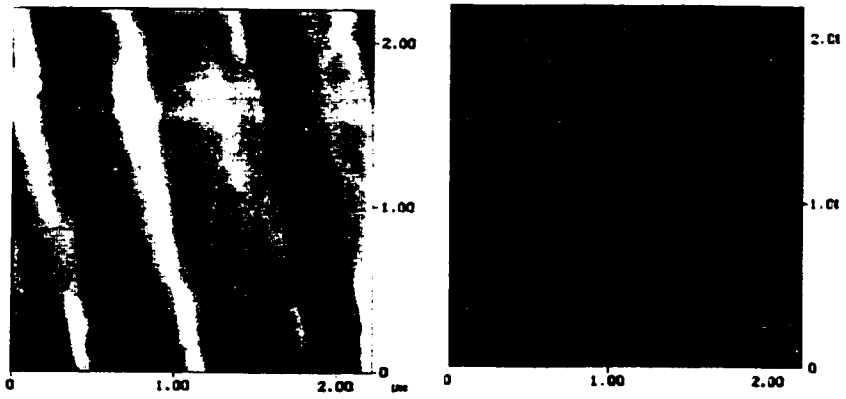


Figure 4.7: AFM Scans of InGaAs Epitaxial Layers grown on GaAs Substrate and Lattice-Engineered Substrate

preparation process A was used before regrowth (refer to Figure 4.2). The RMS roughness of InGaAs layer grown on the lattice-engineered substrate is 3 Å. The maximum height difference between the surface features is 32 Å. For comparison the $In_{0.11}Ga_{0.89}As$ layer grown on GaAs substrate has a RMS surface roughness of 9 Å with a maximum height difference of 50 Å. The AFM scan of $In_{0.11}Ga_{0.89}As$ layer on GaAs shows undulations associated with strain fields of clusters of misfit dislocations at the epitaxial layer substrate interface. These dislocations pileups at the InGaAs/GaAs interface also result in increased surface roughness. The reduced height difference and the surface roughness for InGaAs grown on lattice-engineered template is due to the

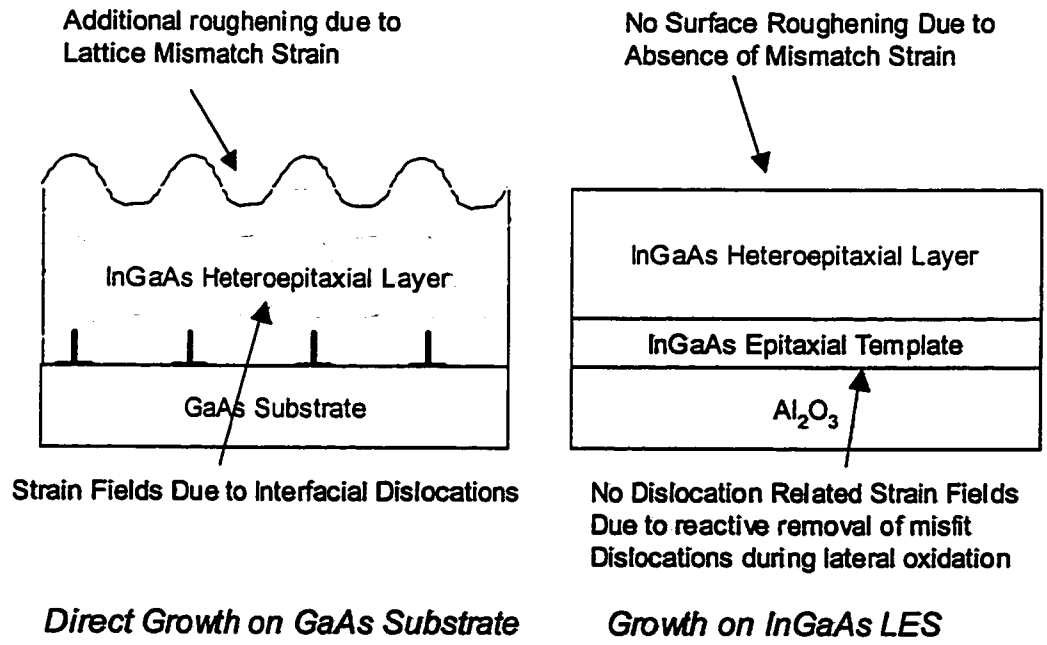


Figure 4.8: Factors affecting surface morphology for growth on GaAs and lattice-engineered substrates

absence of these misfit dislocation related strain fields and also due to the absence of any strain related surface roughening. Figure 4.8 illustrates the abovementioned concepts.

Strained Epitaxial Growth on LES

To investigate the effect of a porous InGaAs/Al_2O_3 interface during subsequent strained epitaxial regrowth on a lattice-engineered substrate, 5000 Å thick InGaAs epitaxial layers with the same alloy composition as the InGaAs template were grown at high growth temperature (~ 500 °C). For the

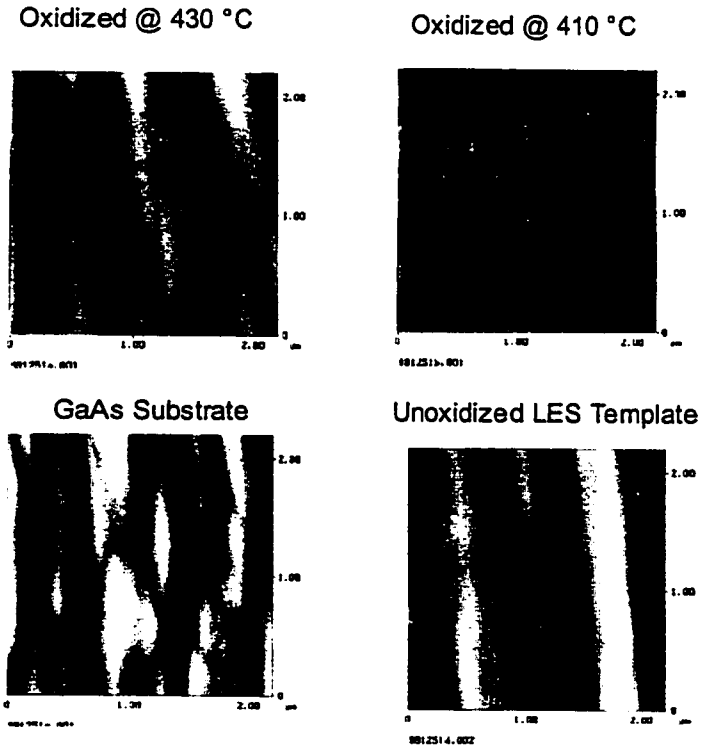


Figure 4.9: AFM Scans of 5000 Å $In_{0.2}Ga_{0.8}As$ Epitaxial Layers Grown on GaAs and $In_{0.2}Ga_{0.8}As$ Lattice Engineered Substrates

purpose of comparison, these layers were also grown on a GaAs substrate and an unoxidized (as-grown) LES template. Figure 4.9 shows the AFM scans of $In_{0.2}Ga_{0.8}As$ epitaxial layers.

As seen in the AFM scans, the surface morphology on a GaAs substrate shows uneven ridges and evidence of 3-D growth mode, which has been observed for similar lattice-mismatches for higher growth temperatures. Growth on an as-grown unoxidized $In_{0.2}Ga_{0.8}As$ LES occurs under conditions of lesser mismatch strain, however the strain fields due to misfit dislocations at the $In_{0.2}Ga_{0.8}As$ template, AlAs oxidation layer interface affect the surface morphology. In this case linear ridges are observed. In the case of growth on a lattice-engineered substrate, the effect of both the lattice-mismatch strain and the misfit dislocation related strain fields is diminished. Hence a smoother surface morphology is observed. Figure 4.10 compares the rms surface roughness and the maximum surface height as obtained from the AFM scans.

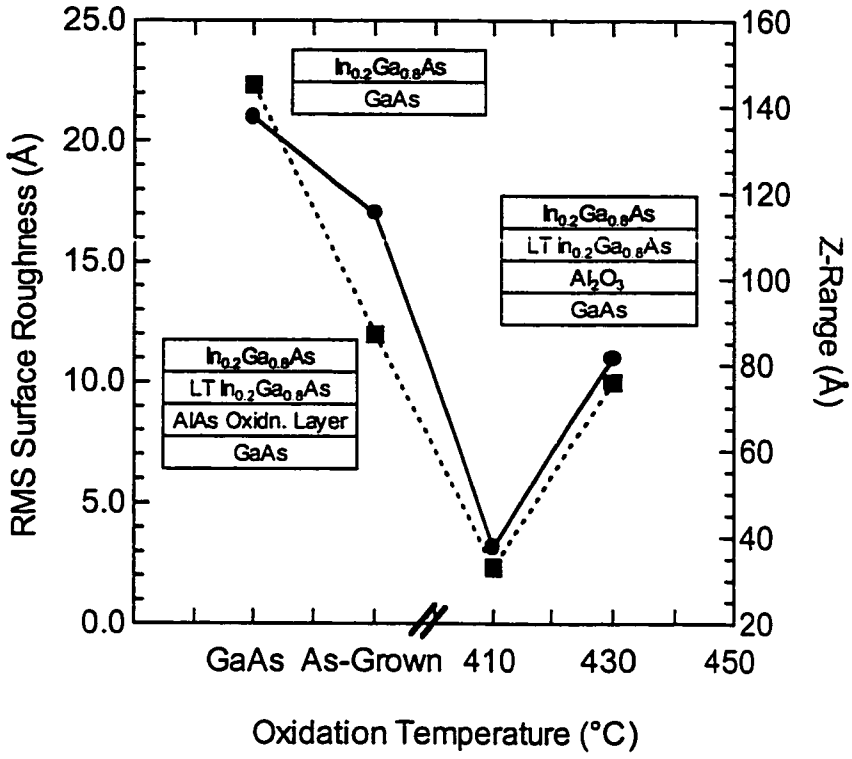


Figure 4.10: Comparison of RMS Surface Roughness and Maximum Height of $In_{0.2}Ga_{0.8}As$ Epitaxial Layers grown on GaAs, As-Grown LES Templates and Lattice-Engineered Substrates

As seen from the above figure, both the rms surface roughness and maximum surface height is lower for layers grown on LES. The improved surface morphology of epitaxial layers grown on lattice-engineered substrates is due to removal of misfit dislocation related strain fields and reduced elastic strain. The surface roughness is further increased with the increase in lattice mismatch as seen in Figure 4.11 for 5000 Å thick $In_{0.3}Ga_{0.7}As$ epitaxial layers grown on $In_{0.3}Ga_{0.7}As$ lattice engineered substrates.

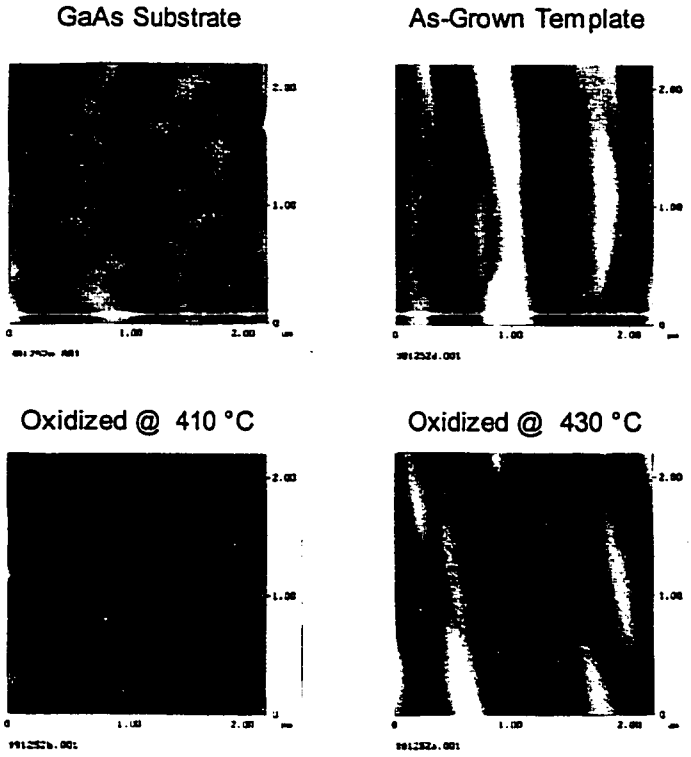


Figure 4.11: Surface Morphology of $In_{0.3}Ga_{0.7}As$ Epitaxial layers grown on GaAs and $In_{0.3}Ga_{0.7}As$ lattice-engineered substrates (AlAs oxidation @ 410 and 430 °C).

Growth of $In_{0.3}Ga_{0.7}As$ on GaAs substrates occurs in 3D mode due to high lattice mismatch. On the other hand, epitaxial growth on lattice-engineered substrates occurs under conditions of lesser lattice mismatch (due to strain relaxation of the $In_{0.3}Ga_{0.7}As$ template layer during lateral oxidation), this results in a lower surface roughness. Also the influence of misfit dislocation related strain fields on the surface morphology is reduced. Higher surface undulation is due higher magnitude of dislocation related strain fields.

4.4.2. GaAsSb Epitaxial Layers

As seen in the previous section, surface morphology of InGaAs epitaxial layer is strongly affected by conditions of lattice mismatch and dislocation related strain fields. This is mainly due to the higher mobility of the Indium adatom relative to the Ga adatom on the growing surface. In the case of GaAsSb, a smoother surface morphology is expected as there is only one Group III element in the alloy. Additionally, the surfactant effect of Sb is expected to result in a better surface morphology. However, unlike InGaAs the surface morphology of $GaAs_{1-x}Sb_x$ epitaxial layers grown on lattice-engineered substrates was found to be more sensitive to the growth temperature.

Strain Free Epitaxial Growth on LES

As seen from Figure 4.12, at higher growth temperatures (510 °C), the RMS surface roughness of the layer increases with Sb composition. However at lower growth temperatures (450 °C), the RMS surface roughness is independent of the Sb composition.

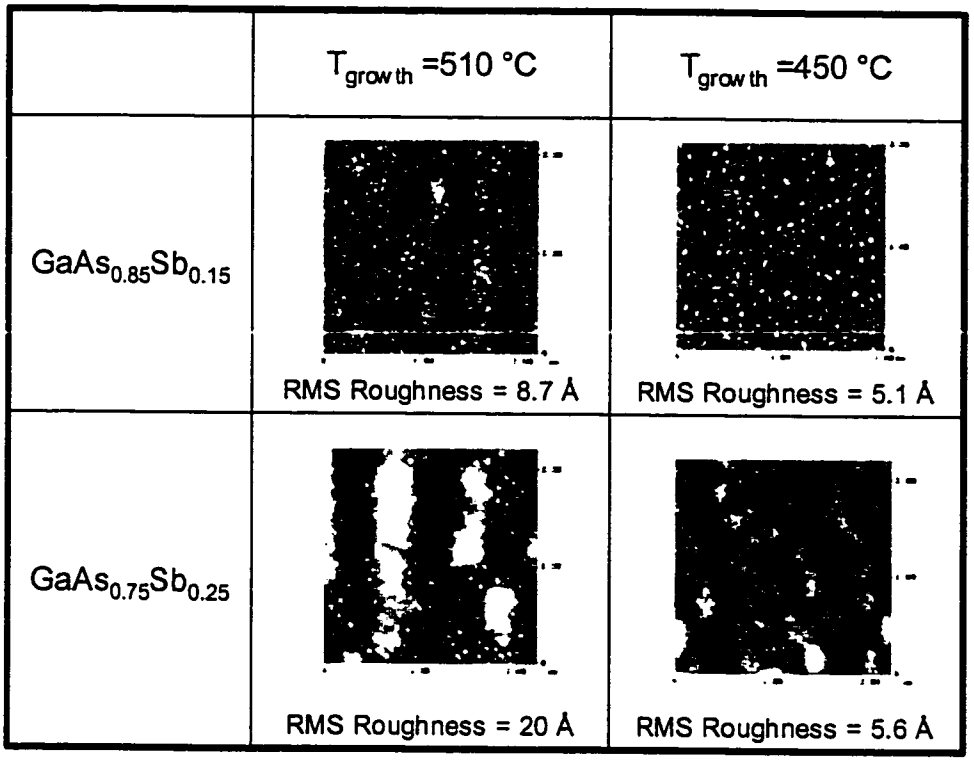


Figure 4.12: Surface Morphology of $GaAs_{1-x}Sb_x$ layers grown on lattice-engineered substrates as a function of Sb composition and growth temperature

Thus AlGaAsSb is a desirable material system for the implementation of long wavelength optoelectronic devices on GaAs based lattice-engineered substrates.

4.5. X-Ray characterization of Epitaxial Layers grown on LES

The extent of residual strain in epitaxial layers grown on lattice-engineered substrates was measured using on-axis (004) and off-axis (115 and $\overline{1}\overline{1}5$) x-ray diffraction scans. According to Matthews-Blakeslee, the plastic

strain (which is accommodated by misfit dislocations), in a heteroepitaxial layer of thickness is given as follows,

$$\delta = f\left[1 - \frac{h_{critical}}{h}\right] \qquad (4.1)$$

Here f is the lattice mismatch between the heteroepitaxial layer and the substrate and $h_{critical}$ is the Matthews-Blakeslee critical thickness. Consequently the residual elastic strain, is given by the following equation,

$$\varepsilon = f - \delta = f\left[\frac{h_{critical}}{h}\right] \qquad (4.2)$$

For efficient strain relaxation, the residual elastic strain in a heteroepitaxial layer should be as small as possible. According to the above equations, strain relaxation is expected to be complete for very thick heteroepitaxial layers. This however has been never observed experimentally. Just beyond the critical thickness, strain relaxation is rapid. However for thicker layers strain relaxation is sluggish. This is due to dislocation blocking that prevents the requisite dislocation glide for strain relaxation. Also interactions between glissile 60° or mixed dislocations results in sessile edge dislocations. In the case of large lattice-mismatches, the 3D growth mode results in a majority of interface dislocations being sessile edge dislocations.

Krishnamoorthy et al. reported that strain relaxation for 1-μm-thick InGaAs layers is 70 % irrespective of layer thickness [28]. 2 μm graded InGaAs layers grown by MOVPE at 700 °C have 80-85 % strain relaxation [27].

Figure 4.13 compares the residual elastic strain in InGaAs epitaxial layers grown on GaAs substrates and InGaAs lattice engineered substrates. As expected in all cases the residual elastic strain is lower for epitaxial layers grown on lattice-engineered substrates. Also the residual elastic strain

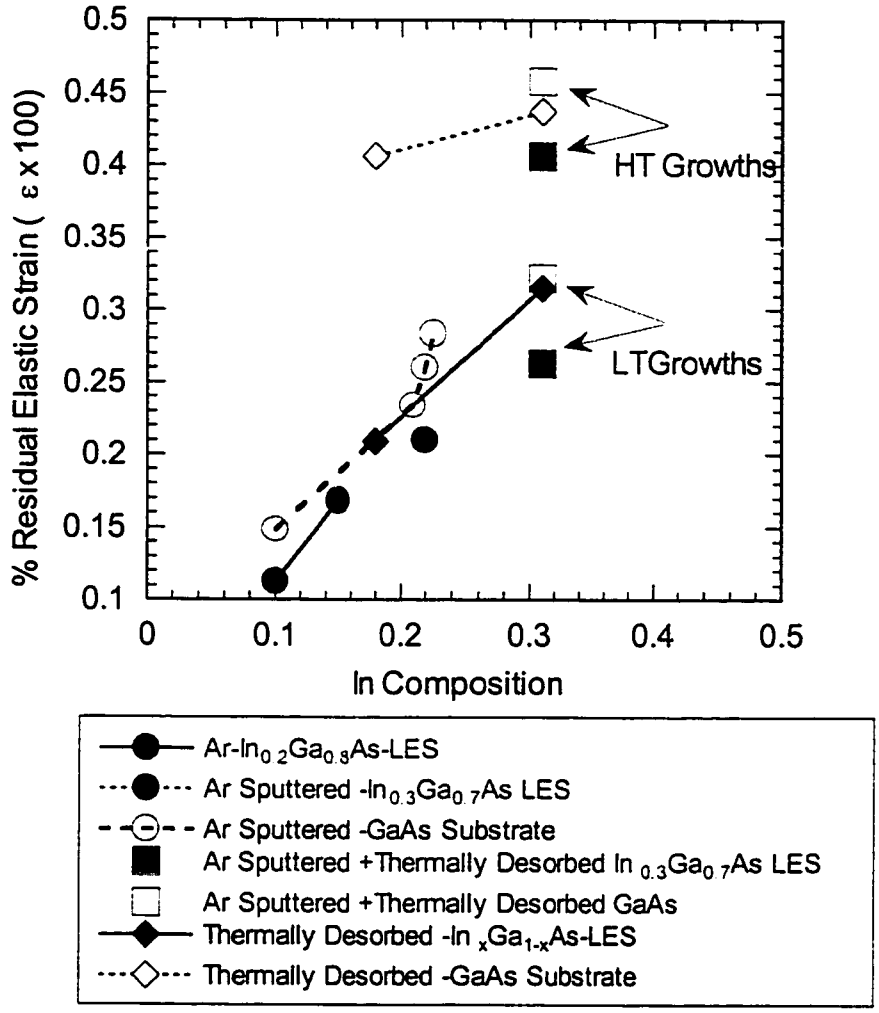


Figure 4.13: Comparison of residual elastic s train in InGaAs epitaxial layers grown on GaAs and lattice-engineered substrates. The Round symbols correspond to Surface Preparation Process A (Ar Sputter + Desorption @ 500 °C). Growth on lattice-engineered substrates in this case is strain free. The Square Symbols Correspond to Surface Preparation Process B (Ar Sputter + Desorption @ 630 °C), the diamond symbols correspond to Surface Preparation Process C (Thermal Desorption @ 630 °C). In the case of square and diamond symbols the regrown epitaxial layer has the same alloy composition as that of the lattice-engineered substrate. Therefore the growth is NOT strain- free

increases with the Indium composition of lattice mismatch. In the case of Ar sputtered lattice-engineered substrates, the difference between the residual elastic strains for growths on GaAs substrates and LES is not significant. This may be because the ion-damage surface may act as a source of additional strain relieving dislocations.

Comparing the residual elastic strains in $In_{0.3}Ga_{0.7}As$ epitaxial layers (process B denoted square symbols in Figure 4.13) grown at low temperature (375 °C) and high temperature (500 °C), it is seen that residual elastic strain is lower for low growth temperatures. This is because; the 3D growth mode is suppressed at low growth temperatures. This reduces the number of sessile edge dislocations that can impede dislocation movement.

However the advantage of the LES approach for heteroepitaxial growth is best seen in the case of thermally desorbed LES (process C denoted by diamond symbols in Figure 4.13). In this case the residual elastic strain for InGaAs epitaxial layers grown on GaAs substrates is much higher than those grown on LES. This is mainly attributed to the absence of ion-damage related dislocation sources. Figure 4.13 compares the strain relaxation as function of oxidation temperature for InGaAs epitaxial layers grown on thermally desorbed LES. It can be seen from that the % strain relaxation increases with the oxidation temperature. This is because (as seen in Chapter 3) strain relaxation increases with the oxidation temperature. Thus the in-plane lattice constant of the InGaAs LES is closer to its unstrained lattice constant. Also higher oxidation temperatures may result in more efficient removal of existing misfit dislocations. Hence the epitaxial growth on a LES oxidized at higher temperatures has reduced strain; hence fewer strain-relieving misfit dislocations are required. Furthermore, the barrier to the movement of these dislocations is reduced.

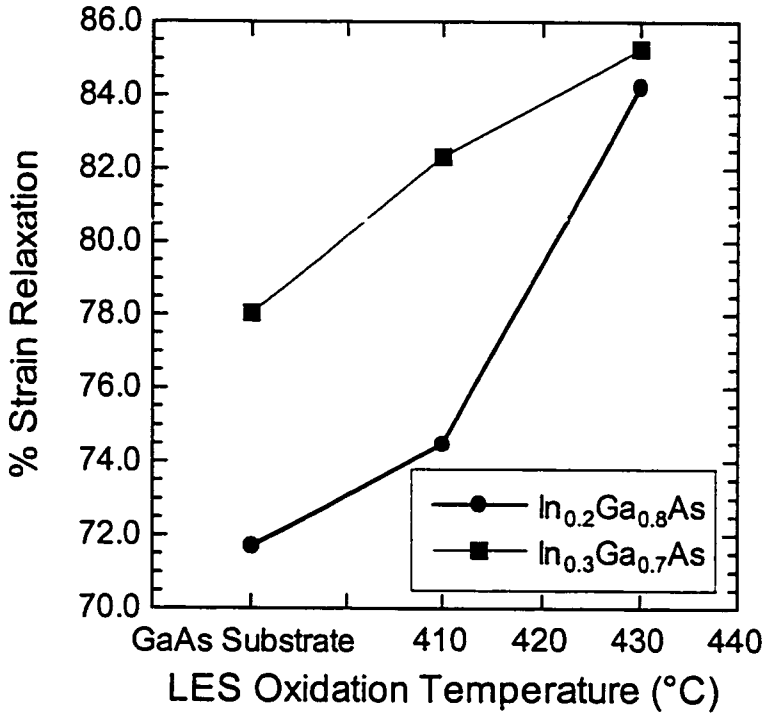


Figure 4.14: % Strain Relaxation in 5000 Å thick InGaAs epitaxial Layers as a function of LES Oxidation Temperature

Figure 4.15 compares the residual elastic strain in the LES and the regrown epitaxial layer with the theoretically predicted elastic strain by the Matthews-Blakeslee model. It can be seen that the residual elastic strain is high in the as-grown LES. This is mainly due to a low-growth temperature that suppresses strain relaxation by dislocation generation. Lateral oxidation results in a significant decrease in the elastic strain. Growth of InGaAs on this lattice-engineered substrate results in lower residual elastic strain than growth on a GaAs substrate. **Therefore the most efficient way to reduce the residual elastic strain is to achieve maximum strain relaxation during the process**

of lateral oxidation. This can be achieved by increasing the oxidation temperature or by addition of Sb to the AlAs oxidation layer.

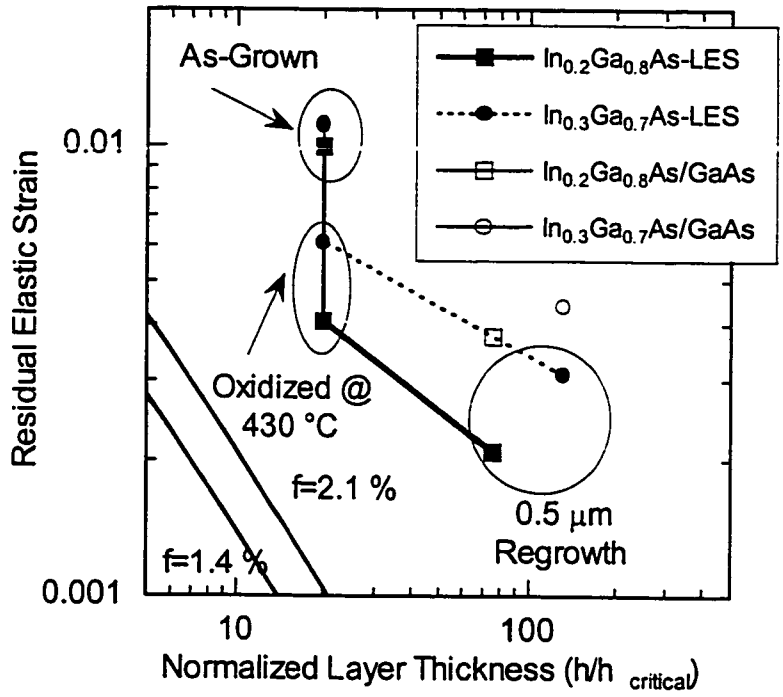


Figure 4.15: Variation of Residual Elastic Strain as function of Normalized Layer thickness. The straight lines in the bottom left hand corner represented the residual elastic strain as predicted by Matthews-Blakslee

Figure 4.16 compares the residual elastic strain in GaAsSb epitaxial layers as a function of Sb composition. In this case also the residual elastic strain increases with the Sb composition. Also the residual elastic strain in GaAsSb layers grown on GaAs is higher than those grown on lattice-engineered substrates.

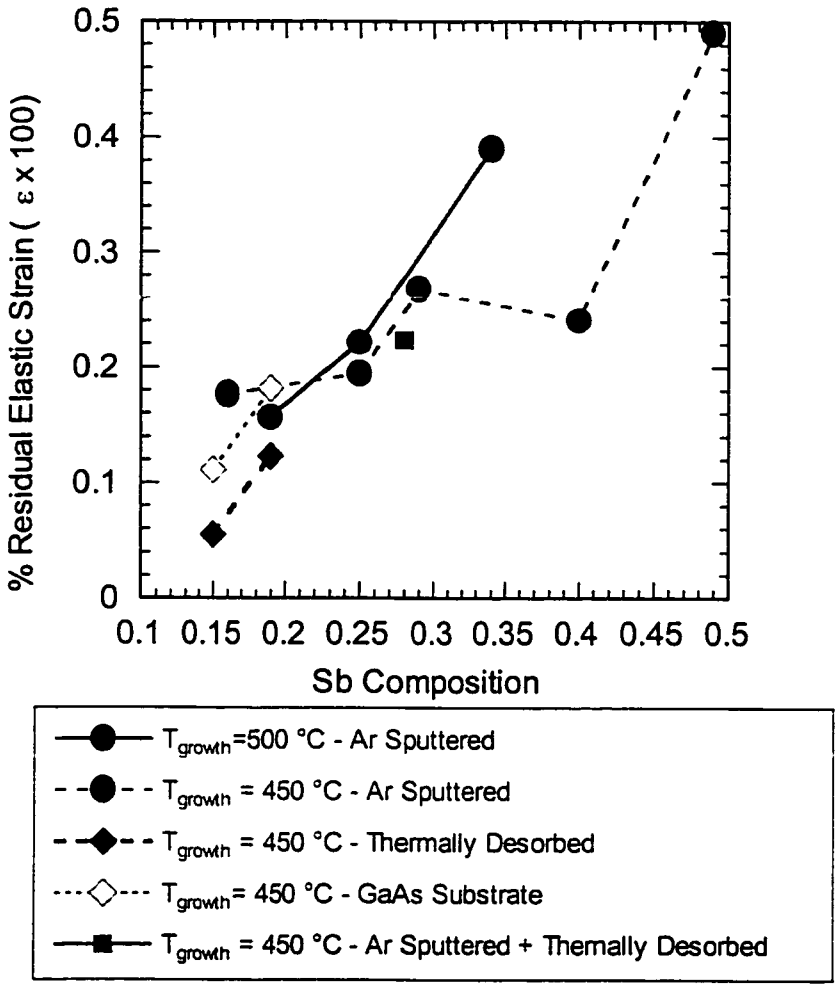


Figure 4.16: Comparison of residual elastic s train in GaAsSb epitaxial layers grown on GaAs and lattice-engineered substrates.

The Round symbols correspond to Surface Preparation Process A

(Ar Sputter + Desorption @ 500 °C).

The Square Symbols Correspond to Surface Preparation Process B

(Ar Sputter + Desorption @ 630 °C)

The diamond symbols correspond to Surface Preparation Process C

(Thermal Desorption @ 630 °C).

4.6. TEM Characterization of Epitaxial Layers Grown on Lattice-Engineered Substrates

In the InGaAs/GaAs material system, for low lattice mismatches, most of the dislocations are 60° or mixed dislocations that are introduced by glide of substrate threading dislocations. For large layer thicknesses. the interaction between mixed dislocations gives rise to sessile edge-type dislocations. In all cases in spite of increasing surface roughness, the growth mode is always 2D. Hence no threading dislocations are observed in TEM micrographs. However TEM micrographs do show misfit dislocations and their associated strain contrast at the epitaxial layer substrate interface.

For higher lattice mismatches, the epitaxial growth occurs in the Stranski-Krastanow mode. Island coalescence generates a high density of threading dislocations. Also a majority of misfit dislocations at the substrate-epilayer interface are sessile edge-type dislocations. These edge dislocations can thread up along the (001) direction by a climb process. Typically in the InGaAs/GaAs material system threading dislocations are generally observed for Indium compositions exceeding 20%, which is the onset of 3D growth mode. The typical threading dislocation densities observed are of the order of 10^8- 10^9 /cm^2. Since the substrate TD are less than 10^4 /cm^2, the high dislocation densities can be attributed dislocation multiplication mechanisms and other dislocation sources like surface impurities and native oxides.

Dr. Lijie Zhao and Sheila K. Mathis at UCSB did sample preparation and TEM analysis of all the epitaxial layers presented in this section.

4.6.1. Epitaxial Layers Grown on $In_{0.2}Ga_{0.8}As$ Lattice-Engineered Substrates (Low Indium Case)

Lattice-mismatched growth of $In_xGa_{1-x}As$ ($x \sim 0.10$) on GaAs results in the formation of misfit dislocations at the InGaAs interface and dislocation loops in the GaAs substrate when the $In_xGa_{1-x}As$ thickness exceeds the critical thickness. The strain due to lattice mismatch for these compositions of $In_xGa_{1-x}As$ is not enough to generate threading dislocations in the $In_xGa_{1-x}As$ epitaxial layers. Figure 4.17 shows cross sectional TEM micrographs of the partially relaxed 5000 Å $In_{0.11}Ga_{0.89}As$ layers grown on both the lattice-engineered substrate and directly on GaAs. Prior to initiating regrowth, Ar ion sputtering with desorption at 500 °C (Process A) was used. The cross sectional TEM images of $In_{0.11}Ga_{0.89}As$ grown directly on GaAs shows misfit dislocations and the characteristic strain contrast associated with misfit dislocations at or near the InGaAs/GaAs interface. For comparison, the thick $In_{0.11}Ga_{0.89}As$ layers grown on the lattice-engineered substrate shows neither misfit dislocations nor strain contrast at either the $In_{0.2}Ga_{0.8}As/Al_2O_3$ interface or the $In_{0.11}Ga_{0.89}As/In_{0.2}Ga_{0.8}As$ interface.

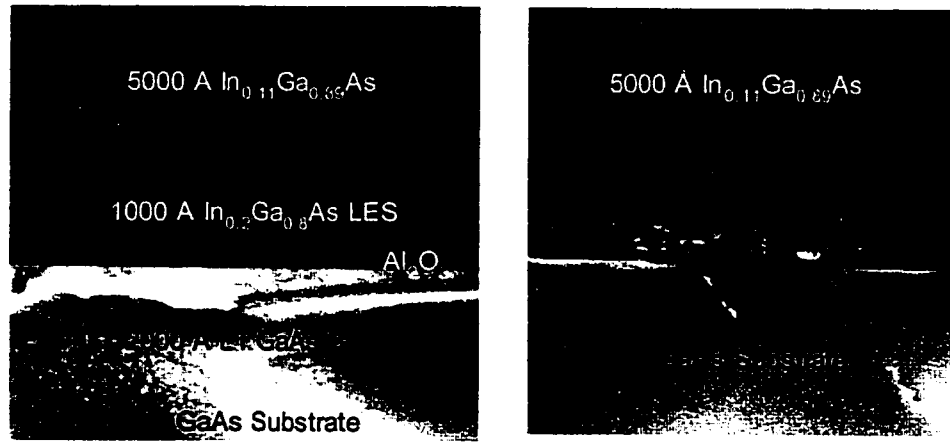


Figure 4.17: TEM Micrographs of $In_{0.11}Ga_{0.89}As$ grown on Lattice-Engineered Substrate and GaAs Substrate

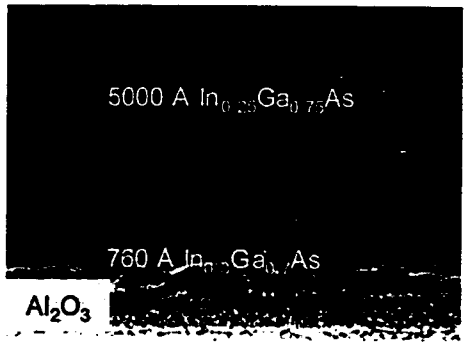
The absence of dislocation strain contrast in the TEM images of the $In_{0.2}Ga_{0.8}As/Al_2O_3$ interface is the remarkable feature of this new approach to strain relaxed layers. Normally in plastic relaxation of strained layer, misfit dislocations act as barriers to the further strain relaxation, by blocking the motion of threading dislocations, which must generate the misfit dislocations. The strain relaxation in $In_{0.2}Ga_{0.8}As$ is enhanced due to the absence of misfit dislocation at the $In_{0.2}Ga_{0.8}As/Al_2O_3$ interface. The absence of misfit dislocations or local strain contrast at the $In_{0.2}Ga_{0.8}As/Al_2O_3$ interface is attributed to both the reactive material removal during oxidation and the porous nature of the oxide itself. However the strain relaxation in the $In_{0.2}Ga_{0.8}As$ layers occurs by normal dislocation plasticity and not by any of the processes proposed for strain relaxation in compliant substrates. For both structures, no threading dislocations were observed in the cross-sectional TEM images. Thus the threading dislocation density in both cases was less than 10^7 $/cm^2$.

4.6.2. Epitaxial Layers Grown on $In_{0.3}Ga_{0.7}As$ Lattice Engineered Substrates (High Indium Case)

For Indium compositions exceeding 20 % heteroepitaxial layers with high threading dislocation density are generally observed. This is mainly due to island coalescence in the 3-D growth mode. Also the misfit dislocations generated in the island growth mode are edge type dislocations that cannot glide and relieve the misfit strain. Thus continual nucleation of dislocations is necessary to relieve the strain. Uppal et al. observed a threading dislocation density of 2×10^9 $/cm^2$ in 1 μm $In_{0.21}Ga_{0.79}As$ epitaxial layers [29]. Chang et al.

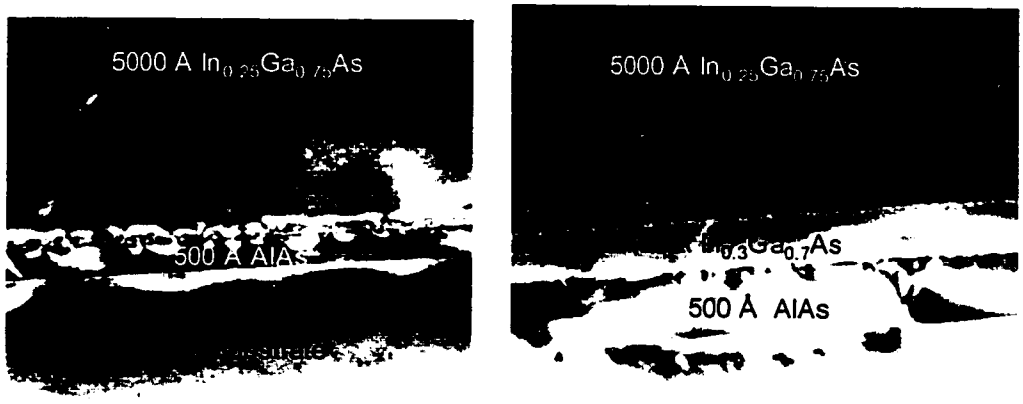
also observed a high TD density in $In_{0.3}Ga_{0.7}As$ epitaxial layers grown directly on GaAs [30].

Figure 4.18 shows cross sectional TEM micrographs of the partially relaxed 5000 Å $In_{0.25}Ga_{0.75}As$ layers grown on an $In_{0.3}Ga_{0.7}As$ lattice-engineered substrate, a GaAs substrate and an unoxidized $In_{0.3}Ga_{0.7}As$ lattice-engineered substrate. In this case also, argon ion sputtering with thermal desorption at 500 °C (Process A) was used. As in the case of $In_{0.11}Ga_{0.89}As$ epitaxial layer threading dislocations are not observed in the cross-sectional



2000 Å LT GaAs Buffer

Lattice-Engineered Substrate



GaAs Substrate

Unoxidized Substrate

Figure 4.18: Cross sectional TEM Micrographs of $In_{0.25}Ga_{0.75}As$ epitaxial layers grown on $In_{0.3}Ga_{0.7}As$ LES, GaAs substrate and $In_{0.3}Ga_{0.7}As$ Unoxidized Substrate

TEM micrograph. On the other hand, epitaxial layer grown on the GaAs substrate show a high density of threading dislocations and strain contrast at the $In_{0.25}Ga_{0.75}As$/GaAs interface. The TEM micrograph of $In_{0.25}Ga_{0.75}As$ epitaxial layers grown on an unoxidized $In_{0.3}Ga_{0.7}As$ LES substrate illustrates the importance of the porous InGaAs/Al_2O_3 interface in strain relaxation. In this case, due to the absence of lateral oxidation, the elastic strain in the

hypercritical $In_{0.3}Ga_{0.7}As$ template layer is not released, as evidenced by the strain contrast in the TEM image. Epitaxial regrowth on this substrate results in dislocation generation at the $In_{0.3}Ga_{0.7}As$/AlAs interface and these dislocations propagate into the regrown epitaxial layer. In this case also, no strain contrasts or dislocations were observed at the $In_{0.3}Ga_{0.7}As$ template/$In_{0.25}Ga_{0.75}As$ regrowth interface.

The detection limit of threading dislocations in a cross-sectional TEM micrographs is 5 x 10^7 / cm^2. Hence the absence of threading dislocations in a cross-sectional TEM micrograph does not imply that the epitaxial layer is dislocation free. Hence plan-view TEM analysis of epitaxial layers grown on $In_{0.3}Ga_{0.7}As$ lattice-engineered substrates was done. Sheila K. Mathis at UCSB did all the plan-view TEM analysis. Figure 4.19 shows the plan-view TEM micrograph of a $GaAs_{0.6}Sb_{0.4}$

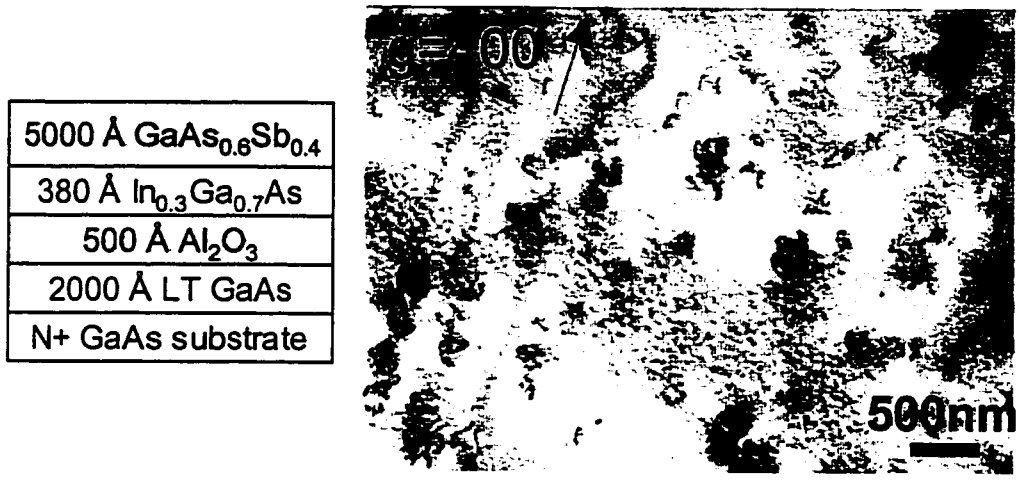


Figure 4.19: Layer structure and Plan-view TEM Micrograph of a $GaAs_{0.6}Sb_{0.4}$ epitaxial layer (f=1.7 %) grown on an $In_{0.3}Ga_{0.7}As$ Lattice-Engineered Substrate

epitaxial layer grown on an $In_{0.3}Ga_{0.7}As$ LES. The threading dislocation density as calculated from the plan view TEM micrograph is 1 x 10^8 / cm^2.

The reason behind the high dislocation density may be two-fold. The most obvious is the high effective lattice mismatch of 1.7 % between the $In_{0.3}Ga_{0.7}As$ LES and the regrown epitaxial layer. This is above the threshold lattice-mismatch (f=1.4 %) that results in high TD density during heteroepitaxial growth. The other reason is the incomplete removal of native oxides on the $In_{0.3}Ga_{0.7}As$ surface prior to regrowth because of the Ar sputter cleaning process. Cross sectional TEM analysis was done on a strain-free $In_{0.22}Ga_{0.78}As$ epitaxial layer grown on an $In_{0.3}Ga_{0.7}As$ LES. As seen from the TEM micrograph in Figure 4.20 threading dislocations are generated at the regrowth interface. In addition no strain contrast associated with misfit dislocations is seen in the regrown epitaxial layer. This confirms that the dislocations are generated either due to ion-damage or incomplete oxide removal.

From the above observations it is clear that to achieve a low dislocation density in epitaxial layers grown on lattice-engineered substrates, it is necessary to eliminate the low activation energy dislocation sources at the regrowth interface. As described before the use of a 20 Å thick GaAs cap layer above the InGaAs/GaAsSb LES permit surface cleaning by thermal desorption at high temperatures. It also eliminates the need for Ar ion sputtering to remove native oxides.

5000 Å $In_{0.22}Ga_{0.78}As$
380 Å $In_{0.3}Ga_{0.7}As$
500 Å Al_2O_3
2000 Å LT GaAs
S.I. GaAs substrate

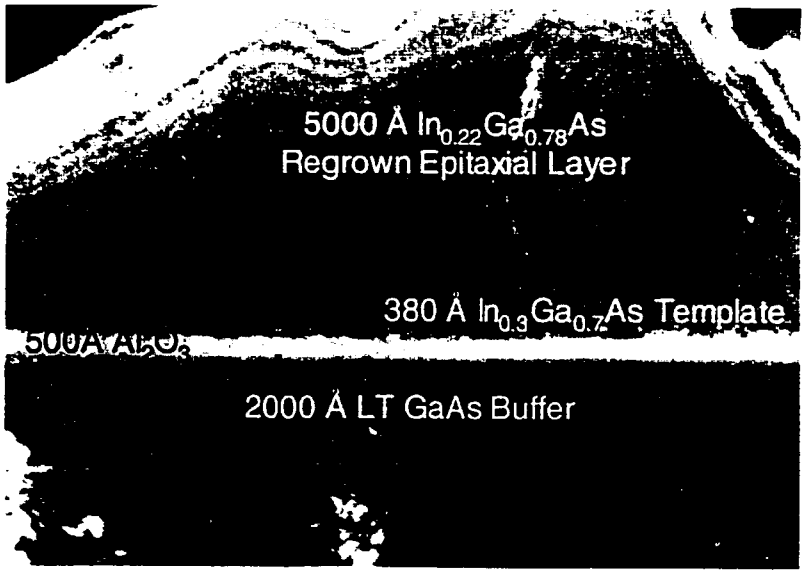


Figure 4.20: Layer structure and Cross-sectional TEM Micrograph of a strain –free $In_{0.22}Ga_{0.78}As$ epitaxial layer grown on an $In_{0.3}Ga_{0.7}As$ LES. It can be seen that dislocations originate at the regrowth interface.

4.6.3. Plan-View TEM Characterization of Epitaxial layers grown on $In_{0.3}Ga_{0.7}As$ Lattice-Engineered Substrates

While the cross section TEM is useful to determine the location of threading dislocations, measurement of dislocation densities requires the use of plan-view TEM. Figure 4.21 shows the layer structure and the plan-view TEM micrograph of a 5000 Å thick $In_{0.3}Ga_{0.7}As$ epitaxial layer grown at 500 °C on an $In_{0.3}Ga_{0.7}As$ Lattice-Engineered substrate. Prior to regrowth Ar ion sputtering and thermal desorption at 640 °C was used to remove the native oxides on the surface.

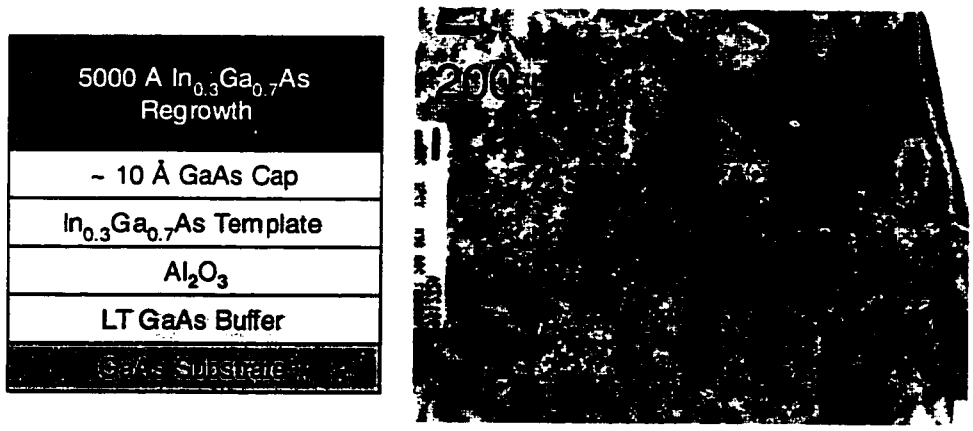


Figure 4.21: Layer Structure and PVTEM Micrograph of $In_{0.3}Ga_{0.7}As$ Epitaxial Layers grown on an $In_{0.3}Ga_{0.7}As$ LES. Argon ion sputtering and thermal desorption was used to remove the native oxides on the surface. The TD density as calculated from the above image is 5 x $10^9/cm^2$. (PVTEM Sample Preparation and Analysis done by Sheila Mathis)

The TD density in the regrown epitaxial layers is 5 x 10^9 /cm^2. The high TD density is attributed to dislocation nucleation at the ion-damaged surface. Figure 4.22 shows the layer structure and PVTEM micrograph of a 5000 Å thick $In_{0.3}Ga_{0.7}As$ epitaxial layer grown on an $In_{0.3}Ga_{0.7}As$ Lattice-

Engineered substrate under identical conditions. In this case only thermal desorption at 640 °C was used to remove the native oxides from the surface. As described before the GaAs cap on the surface prevents the decomposition of the underlying InGaAs template at high desorption temperatures.

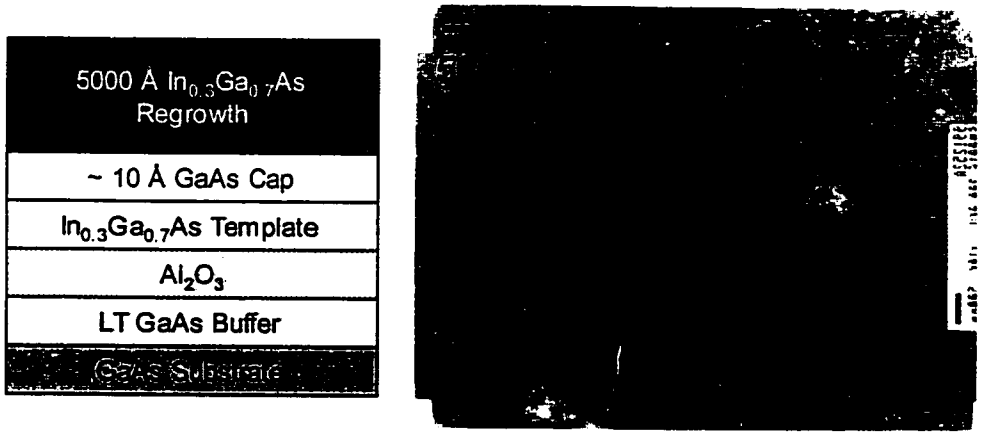


Figure 4.22: Layer Structure and PVTEM Micrograph of $In_{0.3}Ga_{0.7}As$ Epitaxial Layers grown on an $In_{0.3}Ga_{0.7}As$ LES. Only thermal desorption was used to remove the native oxides on the surface. The TD density as calculated from the above image is 8 x $10^7/cm^2$. (PVTEM Sample Preparation and Analysis done by Sheila Mathis)

The TD density these regrown epitaxial layers is 8 x 10^7 /cm^2. The significant reduction in TD highlights the detrimental effects of Ar ion sputtering. This number compares well the reported TD densities for heteroepitaxial layers grown on graded buffer layers. Bulsara et al. have reported a TD density of 2 x 10^8 /cm^2 for $In_{0.27}Ga_{0.73}As$ epitaxial layers grown on 4.5 μm thick graded buffer layers at 550 °C. Also a TD density of 8.5 x 10^6 was reported for a 2 μm thick $In_{0.33}Ga_{0.67}As$ epitaxial layer grown on a 5.5 μm thick graded InGaAs buffer layer [31]. A significantly higher dislocation

density of 5 x 10^8 /cm^2 was reported of 2 μm thick $In_{0.14}Ga_{0.86}As$ epitaxial layers grown by MOVPE [32].

The TD density in the epitaxial layers grown on lattice-engineered substrates can be further reduced by proper growth initiation techniques like low-temperature growth that reduces dislocation nucleation by maintaining a layer-by-layer or a 2D growth mode. It should also be noted that the InGaAs epitaxial layers as shown in the PVTEM images were grown under strain. (This is because the strain relaxation is not complete in the $In_{0.3}Ga_{0.7}As$ lattice-engineered substrate). Reduced TD density can also be achieved by choosing the appropriate composition of InGaAs so that epitaxial growth on the lattice-engineered substrate is strain free. Another way to realize TD density epitaxial layers is the use of GaAsSb buffers instead of InGaAs.

4.7. Conclusions

It is clear from the structural characterization of epitaxial layers grown on lattice-engineered substrates that substrate preparation prior to regrowth is crucial for achieving low dislocation density materials. Enhanced strain relaxation and better surface morphology is achieved in epitaxial layers grown on lattice-engineered substrates compared to those grown on GaAs substrates. The advantages of using a lattice-engineered substrate are most evident under conditions of proper surface treatment i.e. thermal desorption at high temperatures without the use of Ar ion sputtering. In this case suppression of processing related low activation energy dislocation sources results in a large difference in the structural quality between epitaxial layers grown on lattice-engineered substrates and GaAs substrates.

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Chapter 5.
Electrical and Optical Characterization of Epitaxial Layers Grown on Lattice Engineered Substrates

5.1. Introduction

The lattice-engineered substrate technology enables novel electronic and optoelectronic devices using semiconductors having lattice constants between those of commercially available III-V binary semiconductor substrates. For example long wavelength photodetectors and high efficiency solar cells can be implemented on GaAs based LES. Low power, low voltage heterojunction bipolar transistors can be fabricated using InP based LES. It is important to investigate the impact of dislocations on the performance of these devices. A pn junction diode is the most basic minority carrier based electronic device. Section 5.2 of this chapter discusses the performance of pn junction diodes grown on InGaAs lattice-engineered substrates.

The explosive growth of the Internet has lead to the increased demand for optical network access systems and long haul optical communication links. The wavelength of choice for these systems is 1.3 μm for the short-haul high-speed links and 1.55 μm for the long-haul low-loss links. These wavelengths correspond to the dispersion minima (1.3 μm) and the loss minima (1.55 μm) for optical fibers. Hence low cost, reliable sources at 1.33 and 1.55 μm wavelength are required. Conventional InGaAsP based long wavelength lasers grown on InP substrate have poor temperature characteristics and lower optical gain due to the low band-offsets in the InGaAsP material system. This is mainly due to the constraint of lattice matching to the InP substrate that limits the selection of active, separate confinement (SCH) and cladding materials. As a result, in most practical applications long wavelength lasers are mounted on thermoelectric (TE) coolers that maintain the operating temperature of the device.

In recent years, many approaches have been investigated to solve this problem. These include wafer fusion, growth at an intermediate lattice constant through the use of graded buffer, growth on ternary substrates and using long wavelength active regions on GaAs substrates. These approaches are summarized in section 5.3. Wafer fused long wavelength lasers will not be discussed here, as they do not use specialized epitaxial growth techniques. The common theme in all these approaches is to use material systems that have high band offsets to improve the temperature performance of long wavelength lasers. Section 5.4 will therefore discuss the effect of band-offsets on the performance of long wavelength lasers. Lattice-engineered substrates are also an attractive alternative approach for the growth of long wavelength lasers at intermediate lattice constants. In an edge-emitting laser the cladding layer typically constitutes a large fraction of the total epitaxial layer thickness. The

difficulties associated with growth on compositionally graded buffers, ternary substrates and lattice-engineered substrates make the choice of semiconductor materials for cladding layers an important factor as it also governs the material quality of active regions grown on top. This will be discussed in section 5.4. Finally, the optical characterization of 1.3 μm multiquantum well structures grown on lattice-engineered substrates is discussed in section 5.6.

5.2. Influence of Dislocations on Electronic Devices on Heteroepitaxial Layers

The effect of dislocations on electronic devices is commonly modeled as midgap traps. Structural dislocations in heteroepitaxial layers are mainly affect minority carrier based devices like bipolar transistors and photodetectors. Ito et al. modeled the effect of dislocations on AlGaAs/GaAs HBT. The presence of dislocation results in a reduction of current gain due to reduced electron lifetime in the base region and an increase in recombination current in the emitter-base junction depletion region [1].

On the other hand, high performance majority carrier based devices like field effect transistors have been demonstrated using graded buffers. The effect of dislocations on minority carrier based electronic devices can be analyzed with the help of a simple device like a pn junction diode. Mid-gap traps that are a result of dislocations act as generation centers in the depletion region of a reverse biased diode [2]. As a result, high reverse leakage currents are observed in devices fabricated from heteroepitaxial layers having a high dislocation density.

Figure 5.1 shows the layer structure and I-V characteristics of $In_{0.10}Ga_{0.90}As$ pn junctions grown on $In_{0.2}Ga_{0.8}As$ LES. The native oxide removal on the $In_{0.2}Ga_{0.8}As$ LES prior to regrowth was done by Ar ion sputtering and thermal desorption at 520 °C. The diode epitaxial layers were grown at a temperature of 510 °C. It can be seen the reverse bias leakage currents in diodes grown on LES are about 3 orders of magnitude lower than those grown on GaAs substrates. Thus it can be inferred that the threading dislocation density in diodes on LES is less than those on GaAs substrates. It is important to note that no threading dislocations were observed in $In_{0.10}Ga_{0.90}As$ epitaxial layers grown on both LES and GaAs substrates. That is the

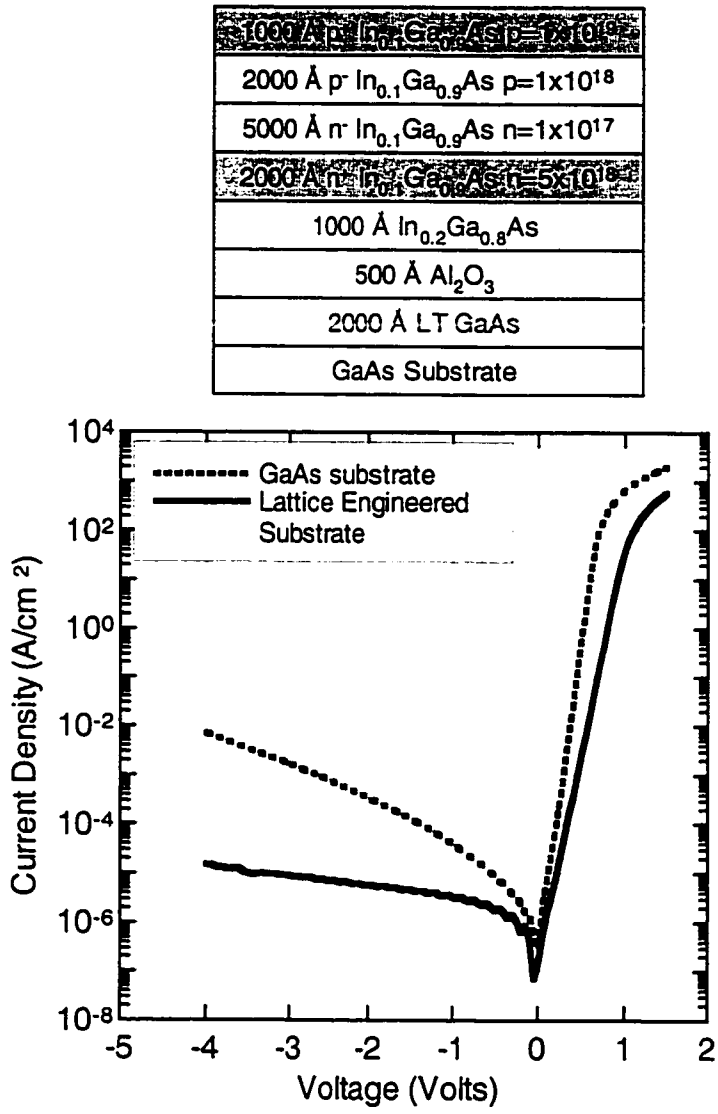

Figure 5.1: Layer Structure and I-V Characteristics of $In_{0.1}Ga_{0.9}As$ pn junction diodes grown on Lattice-Engineered substrates and GaAs substrates.

dislocation density was below the detection threshold in cross-sectional TEM. Thus the reverse bias leakage currents in pn junctions can be used to evaluate

structural quality when the dislocation densities are below the detection limits in TEM.

The forward bias ideality factor of diodes on LES was 2, where as diodes on GaAs substrate exhibited an ideality factor of 1.31. The ideality factor of diodes on LES may due to the fact that no defect diffusion barriers were used in the $In_{0.2}Ga_{0.8}As$ LES.

Figure 5.2 illustrates the layer structure and I-V characteristics of pn junction diodes grown on $In_{0.3}Ga_{0.7}As$ lattice engineered substrate and a GaAs substrate. The device structure and processing of these device structures is significantly different from the devices in Figure 5.1.

In this case a 50 Å AlAs barrier layer was inserted in the $In_{0.3}Ga_{0.7}As$ template layer to suppress defect diffusion during the lateral oxidation process. Also the $In_{0.3}Ga_{0.7}As$ template layer was protected with a 20 Å GaAs cap layer. This enabled thermal desorption at 640 °C prior to the growth of the device structure. However in this case Ar ion sputtering was used to assist in native oxide removal. Also the unstrained lattice constant of the regrown epitaxial layers was equal to the bulk lattice constant of the LES template. As a result, there exists a mismatch strain between the regrown layers and the LES substrate. However efficient strain relaxation is expected at the InGaAs/oxide interface.

The impact of using a AlAs defect diffusion barrier is evident in the forward bias ideality factor which is 1.3 for diodes grown on LES. In comparison diodes grown on GaAs substrate in this case had an ideality factor of 1.6. The reverse leakage in diodes grown on LES is lower than those grown on GaAs substrates only up to –4 V. Beyond that voltage, the reverse leakage is probably dominated by impact ionization in the low bandgap $In_{0.3}Ga_{0.7}As$ material.

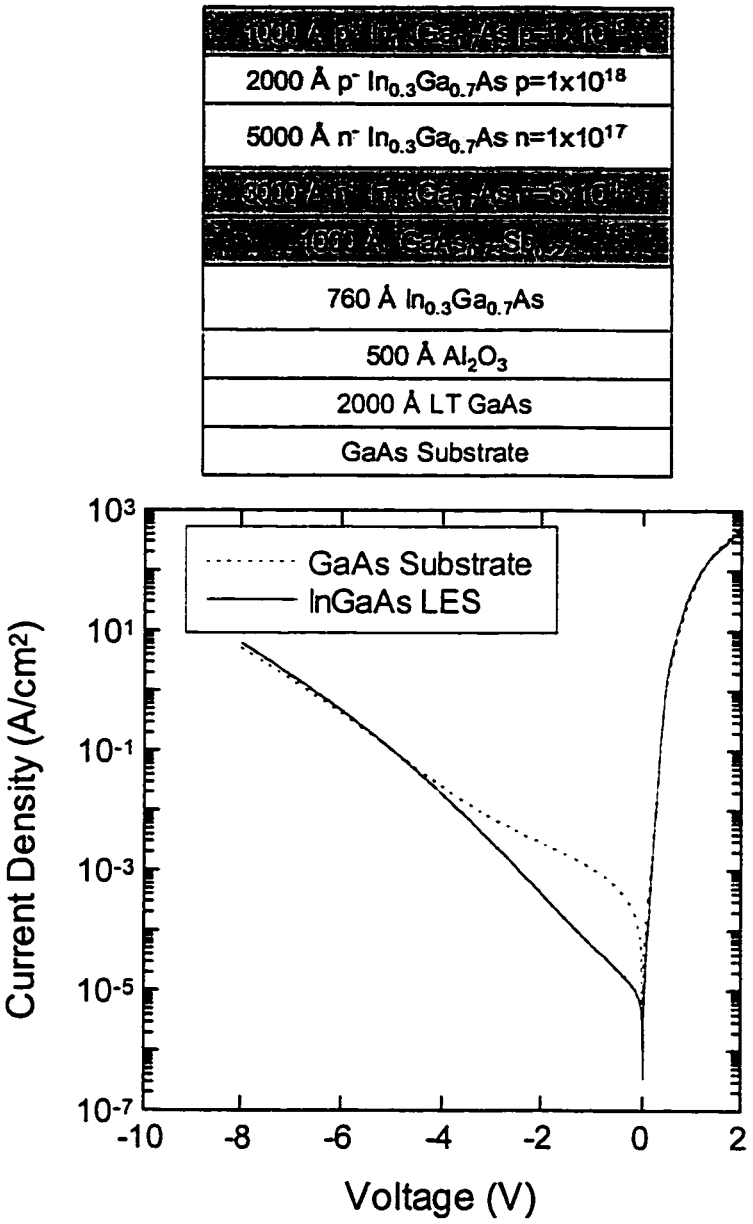

Figure 5.2: Layer Structure and I-V Characteristics of $In_{0.3}Ga_{0.7}As$ pn junction diodes grown on an $In_{0.3}Ga_{0.7}As$ Lattice-Engineered substrate (with a AlAs defect diffusion barrier) and GaAs substrates.

5.3. Material Systems for Long Wavelength Lasers

5.3.1. Active Regions for Long Wavelength Lasers

Long wavelength lasers (1.3 μm and 1.55 μm) are typically grown on InP substrates using InGaAsP/InP material system. This is because the bandgap of the quantum well has to be below 0.95 eV (0.8 eV) for an emission wavelength of 1.3 (1.55 μm). This can be achieved using InGaAs quantum wells with high Indium composition. High quality lattice-matched or psuedomorphic growth of these materials is possible on InP substrates. However there are many limitations of this approach. Lasers with InGaAsP/InP active regions have high threshold current density. This is mainly due low optical gain in the InGaAsP material system. Another disadvantage of high threshold currents is increased Auger recombination due to high carrier densities in the active region. The low band-offsets in the InGaAsP material system result in carrier leakage from the active region resulting in increased optical loss and increase in threshold current density with operating temperature. The $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ material system lattice matched to InP has higher band offsets compared to the InGaAsP/InP material system but suffers from poorer optical quality [3]. An additional disadvantage is the cost, mechanical strength and size of the InP substrate.

In recent years, there have been extensive efforts to implement long wavelength lasers on GaAs substrates. On the GaAs substrate, InGaAs/GaAs quantum wells can be used as the gain medium. Figure 5.3 shows the variation of the C1-HH1 transition wavelength of a strained 80 Å $In_xGa_{1-x}As/GaAs$ quantum well as function of Indium composition. The effect of compressive strain on the bandgap is included in the following calculation. The GaAs substrate is ideal for lasers operating

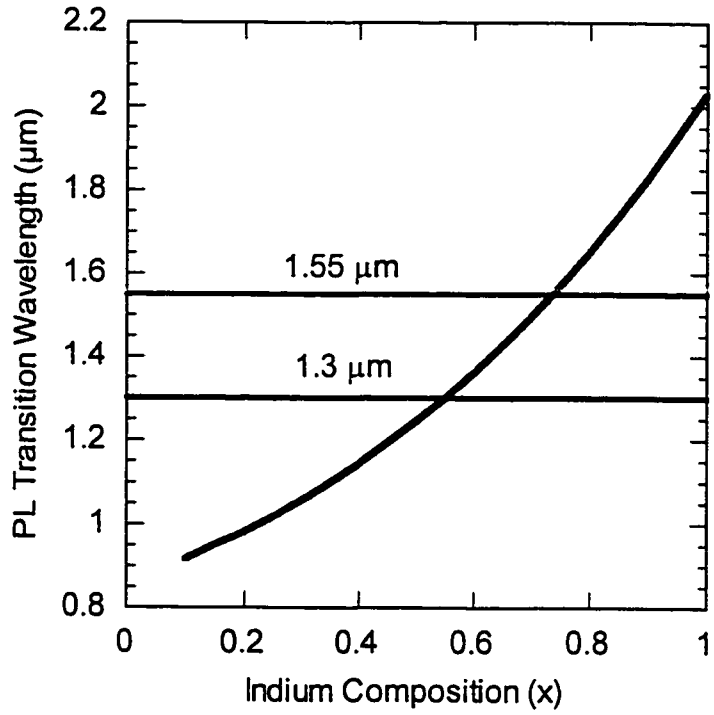

Figure 5.3: Variation of emission wavelength of an 80 Å $In_xGa_{1-x}As/GaAs$ quantum well as function of Indium composition

at 0.98 μm that are implemented using $In_{0.2}Ga_{0.8}As/GaAs$ active regions. Note that much higher (> 50%) indium composition is required to achieve 1.3 and 1.55 μm emission from an InGaAs/GaAs quantum well grown on a GaAs substrate. Figure 5.4 shows the variation of required $In_xGa_{1-x}As$ well thickness for a 1.3 μm $In_xGa_{1-x}As/GaAs$ quantum well on a GaAs substrate and compares it with the Matthews-Blakeslee critical thickness of the particular InGaAs composition on GaAs substrate. Though the required well thickness decreases with the increasing Indium composition, it still exceeds the

Matthews-Blakeslee critical thickness of the particular composition. The growth of highly strained (Misfit > 1.5 %) InGaAs on

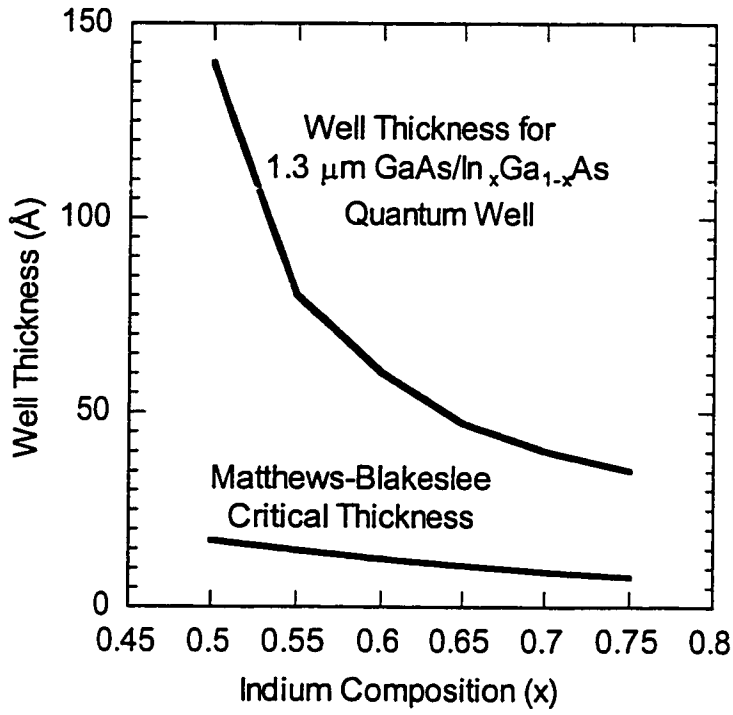

Figure 5.4: Variation of InGaAs well thickness as function of Indium composition for a 1.3 μm InGaAs/GaAs quantum well

GaAs results in poor material quality due to growth in three-dimensional mode, which results in high threading dislocation densities. As a consequence, the longest possible wavelength of an InGaAs/GaAs strained quantum well laser operating on a GaAs substrate is 1.21 μm [4]. Various other approaches have been investigated to solve this problem. These include InAs/GaAs short period superlattices, quantum dots and Sb-based quantum wells with staggered band lineups.

Replacing the InGaAs random alloy with an InAs/GaAs strained short-period superlattice (SPS) extends the PL transition to longer wavelength. Roan et al. reported room temperature photoluminescence at 1.35 μm with a FWHM of 54 meV from a 72 Å $(InAs)_1/(GaAs)_1$ strained SPS quantum well [5]. Kurakake et al. have reported a strained quantum laser with $(InAs)_1/(GaAs)_2$ SPS active region operating at 1.07 μm [6].

Long wavelength emission on a GaAs substrate can also be achieved by using InAs quantum dots [7]. However this approach is limited by non-uniformity in quantum dot distribution and size. Also at higher carrier densities transitions from higher energy levels that are closely spaced result in lasing at lower wavelength.

The other approach to bandgap reduction is incorporation of upto 1% of Nitrogen in GaInAs. This results in a reduction of the bandgap. However, to achieve 1.3 μm emission, high Indium content (upto 30 %) is required. In addition, significant damage is created by the use of a plasma source for activated Nitrogen. Kondow et al. demonstrated pulsed operation of 1.3 μm GaInNAs in-plane lasers at 1.3 μm [8].

Another way to increase the transition wavelength is to use quantum wells with staggered band line up. As seen from Figure 5.5 the transition energy between adjacent bilayers is lower than the bandgap of the either layers [9]. The electron and hole quantum wells exist in different materials. One disadvantage of this approach is that the spatial overlap of the electron and hole wavefunctions is less than a conventional quantum well. Mixed arsenide-antimonide compounds that exhibit a staggered band line up with the AlGaAs/GaAs material system are the materials of choice for this approach. Dowd et al. have reported an $In_{0.4}Ga_{0.6}As/GaP_{0.15}A_{0.4}Sb_{0.45}/ In_{0.4}Ga_{0.6}As$ quantum well with transition energy of 1.3 μm and a room temperature

linewidth of 110 meV [10]. Yamada et al. reported pulsed operation of an AlGaAs/$GaAs_{0.67}Sb_{0.34}$ in-plane laser with a threshold current density of 450 A/cm^2 [11]. Anan et al. reported pulsed room temperature operation of a VCSEL at 1.22 μm

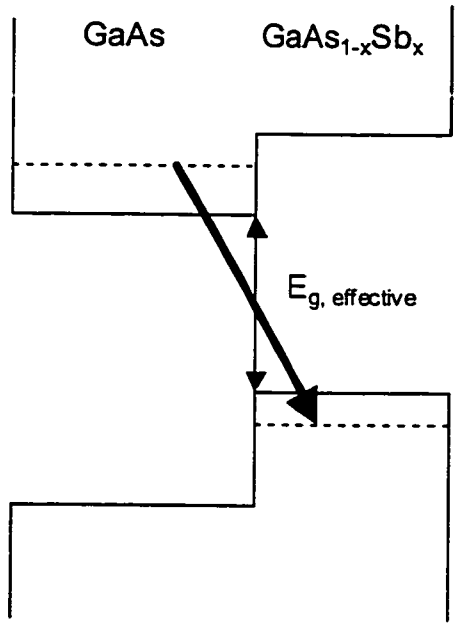

Figure 5.5: Band-Diagram of a Staggered Bilayer Quantum Well. The Spatially Indirect Transition occurs at a energy lower than the bandgap of both the materials

with a $GaAs_{0.69}Sb_{0.31}$/GaAs double quantum well [12]. The threshold current density was 3.2 kA/cm^2.

5.3.2. Long Wavelength Lasers on Heteroepitaxial Layers

Graded buffers have been conventionally used to achieve low dislocation density heteroepitaxial layers on GaAs substrate. It is possible to fabricate a laser on a GaAs substrate if the defect densities are kept low. Gourley et al. reported an optically pumped VCSEL grown on a 1.6 μm thick $In_{0.12}Ga_{0.88}As$ buffer on a GaAs substrate. The emission wavelength was 1.05

μm and the equivalent threshold current density was 1.8 kA/cm^2 [13]. The epitaxial structure had a linear MD density of 6 x 10^2/cm. Uchida et al. have demonstrated 1.3 μm InGaAs/GaAs strained quantum well lasers grown on top of a 3.4 μm graded InGaAs buffer layer on a GaAs substrate [14]. The threshold current density was 500 A/cm^2. Smooth surface morphology was achieved by using heavily doped Se cladding layers, but this increases the optical loss due to free carrier absorption [15]. Yamada et al. have reported a 1.3 μm laser on a Si substrate with a 2 μm GaAs buffer followed by a 13 μm InP buffer. The measured EPD on the InP buffer was 5 x 10^6 /cm^2 [16].

5.3.3. InGaAs Ternary Substrates

As an alternative to lattice-mismatched growth on GaAs substrates, development of an InGaAs ternary substrate with a lattice constant between that of GaAs and InP substrate is attractive as it enables lattice matched growth of suitable active and cladding semiconductor materials for 1.3 and 1.55 μm lasers. As in the case of conventional binary III-V substrates, ternary substrates can be grown by a variety of techniques like liquid encapsulated Czochralski (LEC), Bridgman growth method; multi-component zone and Vertical gradient freeze (VGF).

However there are many problems associated with the growth of ternary substrates. Constant temperature LEC growth of ternary InGaAs substrates has been demonstrated [17, 18]. With the LEC technique, the Indium composition is limited to less than 20% due to composition fluctuations at higher Indium compositions. In the case of the multi-component zone growth method, the lattice mismatch between the GaAs seed and the growing InGaAs crystal limits the Indium composition to less than 20 %. The conventional Bridgman growth

method is plagued by compositional variations in the growth direction. Recently InGaAs ternary substrates grown by VGF method were reported [19]. To maintain good crystal quality the composition difference between the GaAs seed and the InGaAs VGF crystal has to be less than 5 %. As a result, the Indium composition in the 15 mm long ternary substrate boule varies from 0 at the bottom to a maximum value of 34 % at the top. Hence unlike a GaAs boule that can be sliced to yield a number of substrate wafers, an InGaAs ternary substrate boule can yield only 1 or 2 high Indium composition InGaAs ternary substrates. Thus this process is not cost efficient. Other limitations of ternary substrates are composition control, small size and surface roughness (which results in high optical loss). Other than InGaAs, LEC growth of ternary InAsP and GaInSb substrates has also been demonstrated.

Table 5.1 compares the x-ray FWHMs of InGaAs ternary bulk substrates and epitaxial InGaAs lattice engineered substrates.

Substrate Type	X-Ray FWHM in (arcsec)
Bulk GaAs Substrate	20 arcsec
Bulk InGaAs Ternary Substrate	57 arcsec
1000 Å $In_{0.2}Ga_{0.8}As$ LES	312 arcsec
760 Å $In_{0.3}Ga_{0.7}As$ LES	455 arcsec
480 Å $In_{0.4}Ga_{0.6}As$ LES	604 arcsec

Table 5.1: Comparison of X-Ray FWHM of GaAs substrate, Bulk InGaAs Ternary Substrate and InGaAs Lattice-Engineered Substrates

The X-Ray FWHM of thin epitaxial InGaAs LES compares well with bulk ternary InGaAs substrates.

5.3.4. Long Wavelength Lasers Grown on InGaAs Ternary Substrates

Lasers on ternary substrates have also been recently demonstrated. Shoji et al. demonstrated a 1.03 μm InGaAs/InGaAsP Strained SQW laser with a threshold current density of 222 A/cm^2 on an $In_{0.05}Ga_{0.95}As$ Ternary substrate [20]. Otsubo et al. demonstrated the pulsed operation of 1.22 μm lasers upto 210 °C on an $In_{0.22}Ga_{0.78}As$ ternary substrate [21]. The highest possible Indium composition achieved in an InGaAs ternary substrate is 31%. Otsubo et al. have reported 1.3 μm lasers with InAlGaAs/InGaAs active regions on an $In_{0.31}Ga_{0.69}As$ ternary substrate [22]. Variation in substrate quality and surface morphology results in a large variation of threshold current density, J_{th} and characteristic temperature T_o over the substrate [23]. Table 5.2 summarizes the various reported results of long wavelength lasers on ternary substrates.

Substrate Composition	Active Region	λ	J_{th}	To	Reference
$In_{0.03}Ga_{0.97}As$	InGaP/ $In_{0.41}Ga_{0.59}As$	1.15		70 K	[24]
$In_{0.05}Ga_{0.95}As$	InGaAsP/ $In_{0.25}Ga_{0.75}As$	1.03	222 A/cm^2	221 K	[20]
$In_{0.22}Ga_{0.78}As$ (FWHM=490 s)	InAlGaAs/ $In_{0.41}Ga_{0.59}As$	1.22	245 A/cm^2	110 K	[21]
$In_{0.31}Ga_{0.69}As$ (FWHM=529 s)	InAlGaAs/ $In_{0.53}Ga_{0.47}As$	1.3	677 A/cm^2 (Pulsed)	76 K	[22]

Table 5.2: Summary of long wavelength lasers grown on InGaAs ternary substrates

5.4. Design of 1.3 μm Quantum wells on Intermediate Lattice Constants

As described before, one of the major problems in long wavelength lasers is the degradation of performance at high temperatures. The characteristic temperature T_0 of a laser can be considered as a measure of high temperature performance of the device. It can be defined by the following equation,

$$J_{th} = J_o\left(\frac{T}{T_o}\right) \tag{5.1}$$

where J_{th} is the threshold current density at an operating temperature of T and J_o is a constant. Strained quantum well lasers on GaAs substrates exhibit T_o values around 170 K, on the other hand InP based long wavelength lasers exhibit low T_o values around 50 K. One of the main reasons for this is the low band offset in the InGaAsP/InP material system. This results in leakage of carriers from the active region into the SCH region. Figure 5.6 shows the effect of temperature and carrier overflow on the optical gain in a 1.3 μm strained quantum well [25].

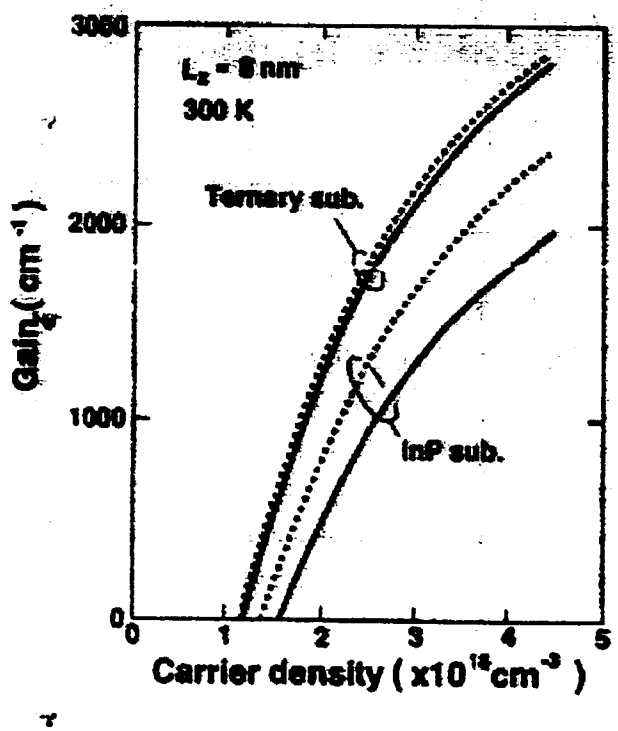

Figure 5.6: Variation of optical gain as a function of carrier density for a 1.3 μm quantum well on an InP Substrate and InGaAs Ternary Substrate [25]

If carrier overflow is considered, the reduction in optical gain with temperature is significant. In the case of quantum wells with high band offsets, the higher optical gain is achieved at low carrier density and the degradation in optical gain with the increase in temperature is reduced. This is mainly due to the reduction of carrier overflow from the active region to the SCH region. Higher optical gain at low carrier densities reduces the threshold current density. This is advantageous as operation at low current densities lowers Auger recombination. In addition, deeper quantum wells also result in higher modulation bandwidth of the laser [26]. This is particularly important for 1.3 μm lasers used in high-speed data links. A quantum well laser with high band

offset $In_{0.4}Ga_{0.6}As/In_{0.4}Ga_{0.6}As_{0.8}P_{0.2}$ quantum wells and $In_{0.3}Ga_{0.7}P$ cladding layers had a gain coefficient of 1530 /cm compared to InGaAs/InP quantum well lasers that had a gain coefficient of 823/cm [27].

Since the growth of high band offset active regions is not possible for long wavelength lasers on InP substrates, various other approaches have been investigated to reduce carrier overflow from the active region into the cladding layers. Compared to the InGaAsP based materials, high band offsets are achieved in the AlInAs/GaInAs material system that is lattice matched to InP. A long wavelength laser with AlGaInAs (λ=1.0 μm) /AlGaInAs active regions had a T_o of 125 K, and operation up to 125 °C was demonstrated [28]. A laser structure with an AlInAs electron stopper layers that reduced electron overflow from the active region into the p-type cladding layers was demonstrated by Munakata et al. [29].

Long-wavelength (1.3 μm) lasers with gain regions having deeper quantum wells can be implemented in material systems with a lattice constant of 5.75 Å, which lies between the available binary substrates GaAs (5.653 Å) and InP (5.8686 Å). As described the lattice constants are accessible with bulk InGaAs ternary substrates. The above lattice constant can also be achieved by a using a InGaAs lattice-engineered substrate on a GaAs substrate platform.

Figure 5.7 compares the band-offsets of various quantum wells that can be used for 1.3 μm emission. The barrier layers are lattice-matched to the corresponding substrate and the 80 Å thick well is compressively strained with a 1.4 % lattice mismatch. On a lattice-engineered substrate with a lattice constant of 5.75 Å the possible active regions are $Al_{0.2}Ga_{0.8}As_{0.78}Sb_{0.22}/GaAs_{0.58}Sb_{0.42}$, $In_{0.25}Ga_{0.75}As/In_{0.42}Ga_{0.58}As$ and $In_{0.7}Ga_{0.3}As_{0.08}P_{0.92}/In_{0.46}Ga_{0.54}As$. On an InP substrates the possible active

regions are $In_{0.87}Ga_{0.03}As_{0.29}P_{0.71}/In_{0.98}Ga_{0.02}As_{0.48}P_{0.52}$ and $Al_{0.32}Ga_{0.16}In_{0.52}As/Al_{0.16}Ga_{0.10}In_{0.74}As$.

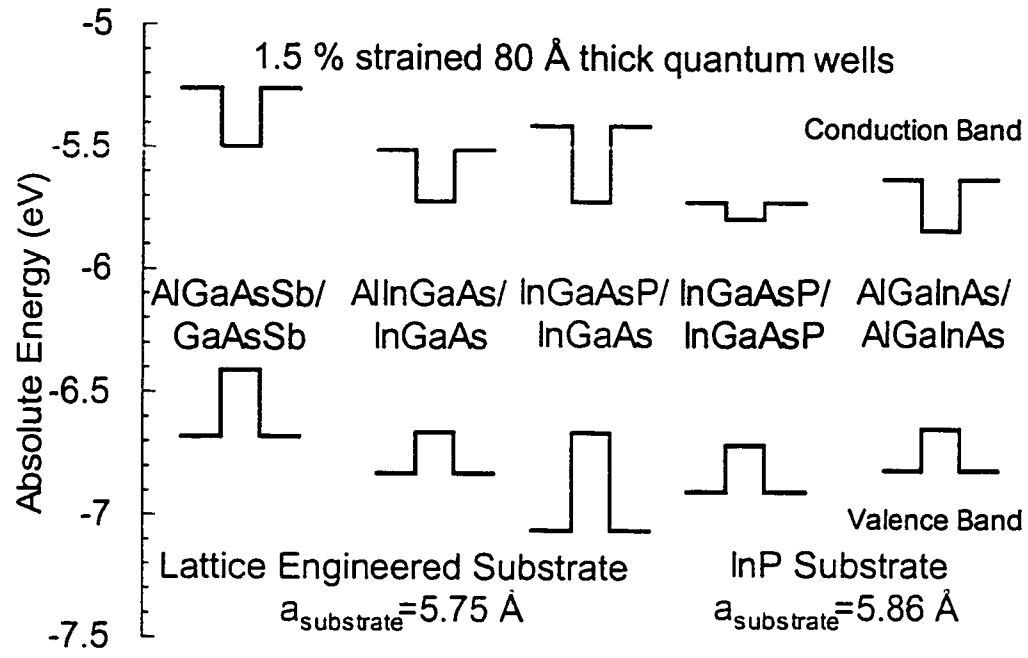

Figure 5.7: Band offsets of 1.3 μm quantum wells on Lattice Engineered Substrate and InP substrate

As seen from Figure 5.7 higher band-offsets can be achieved in quantum wells grown on lattice-engineered substrates when compared to those grown on InP substrates. Table 5.3 lists the conduction band and valence band offsets of the quantum wells depicted in Figure 5.7.

Barrier	Quantum Well	ΔE_c (meV)	ΔE_v (meV)
InGaAs Lattice Engineered Substrate			
$In_{0.22}Ga_{0.78}As$	$In_{0.42}Ga_{0.58}As$	100 meV	80 meV
$(Al_{0.2}Ga_{0.8})_{0.78}In_{0.22}As$	$In_{0.42}Ga_{0.58}As$	210 meV	170 meV
$Al_{0.2}Ga_{0.8}As_{0.78}Sb_{0.22}$	$GaAs_{0.58}Sb_{0.42}$	240 meV	270 meV
$In_{0.7}Ga_{0.3}As_{0.08}P_{0.92}$	$In_{0.46}Ga_{0.54}As$	310 meV	400 meV
InP Substrate			
$In_{0.87}Ga_{0.13}As_{0.28}P_{0.72}$	$In_{0.98}Ga_{0.02}As_{0.47}P_{0.53}$	70 meV	190 meV
$Al_{0.32}Ga_{0.18}In_{0.52}As$	$Al_{0.16}Ga_{0.10}In_{0.74}As$	210 meV	170 meV

Table 5.3: Conduction band and Valence Band offsets of 1.3 μm Quantum Wells Grown on InGaAs Lattice-Engineered Substrate and InP Substrate

Higher band-offset quantum wells will enable high temperature uncooled long wavelength lasers on InGaAs lattice-engineered substrates or bulk InGaAs ternary substrates. In addition to deep quantum wells, a lattice-engineered substrate enables the growth of a high bandgap cladding layer like $Al_{0.8}G_{0.2}As_{0.78}Sb_{0.22}$ or InGaP. On the other hand the highest possible bandgap achievable on an InP substrates is 1.4 eV for AlInAs. As seen in the following section, growth of high quality cladding layers (that is necessary for mode confinement) is an essential requirement for the growth of long wavelength laser structures.

5.5. Cladding Layer Design

In an edge-emitting laser the cladding layer confines both carriers and light in the active region of the device. As a result a high bandgap and low refractive index semiconductor is desired.

The growth of high quality cladding epitaxial layers with a smooth surface morphology is desirable for two reasons. Light is confined in the active region of a laser by total internal reflection at the cladding-active or cladding-SCH interface. The fraction of light incident to the normal to the surface that is scattered is given by the following expression [30],

$$\frac{I_s}{I_i} = \frac{16\pi^2\sigma^2 R}{\lambda^2} \qquad (5.2)$$

where I_s is the scattered light, I_i is the incident light, σ is the rms surface roughness and λ is the wavelength of the light. The fraction of scattered light is proportional to the square of the rms surface roughness. The scattered light at the cladding interface manifests itself as optical loss in the laser. Hence it is necessary to grow smooth cladding layers. The second reason for smooth cladding layers is to inhibit dislocation generation as detailed below.

In edge-emitting laser structures, the active region is grown on top a thick cladding layer. As a result, the most detrimental effect of a rough surface morphology is the lowering the dislocation nucleation barrier when a strained quantum well is grown on top. These issues are particularly important when growing on lattice engineered substrates and using other techniques of heteroepitaxial growth. The importance of maintaining a smooth surface morphology is demonstrated in the epitaxial growth of a 1.3 μm laser structure on a compositionally graded buffer layer on a GaAs substrate [31]. Compositional grading results in a low-dislocation density buffer and cladding layer. As in case of compositionally graded buffers, strain relaxation results in a crosshatched or undulating surface. Defects are generated in the quantum well active region near the undulation points of the Cladding layers. Maintaining a smooth surface morphology is essential to prevent defect generation in the quantum well. Se doping was used to improve the surface

morphology of InGaP cladding layer and prevent dislocation generation during growth of the strained quantum well.

On InGaAs lattice-engineered substrates, either high Al composition AlGaInAs or high Al composition AlGaAsSb epitaxial layers can be used as cladding layers. It is difficult to grow high quality AlGaInAs epitaxial layers by MBE due to the large difference in the mobility of Al and In atoms on the growing surface. On the other hand growth of AlGaAsSb is easier. This is due to comparable surface mobility of Al and Ga cations on the growing surface coupled with the surfactant effect of the Sb. The use of valved As and Sb cells enables accurate composition control of the AsSb based epitaxial layers.

Figure 5.8 illustrates the optical microscope images of a 5000 Å thick $Al_{0.78}In_{0.22}As$ and $Al_{0.8}Ga_{0.2}As_{0.78}Sb_{0.22}$ epitaxial layers grown on an $In_{0.3}Ga_{0.7}As$ LES. The rough surface morphology of $Al_{0.78}In_{0.22}As$ is mainly due to high Al content and the large difference in the mobility of Al and In atoms on the growing surface.

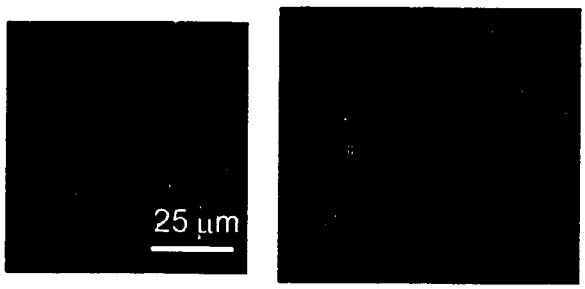

Figure 5.8: Optical Micrograph of a 5000 Å $Al_{0.78}In_{0.22}As$ and $Al_{0.8}Ga_{0.2}As_{0.78}Sb_{0.22}$ cladding layers grown on an $In_{0.3}Ga_{0.7}As$ LES.

In contrast, it is possible to grow thick AlGaAsSb epitaxial layers with a smooth surface morphology on $In_{0.3}Ga_{0.7}As$ LES. Figure 5.9 shows the AFM scans of $Al_{0.5}Ga_{0.5}As_{0.78}Sb_{0.22}$ and $Al_{0.8}Ga_{0.2}As_{0.78}Sb_{0.22}$ epitaxial layers grown

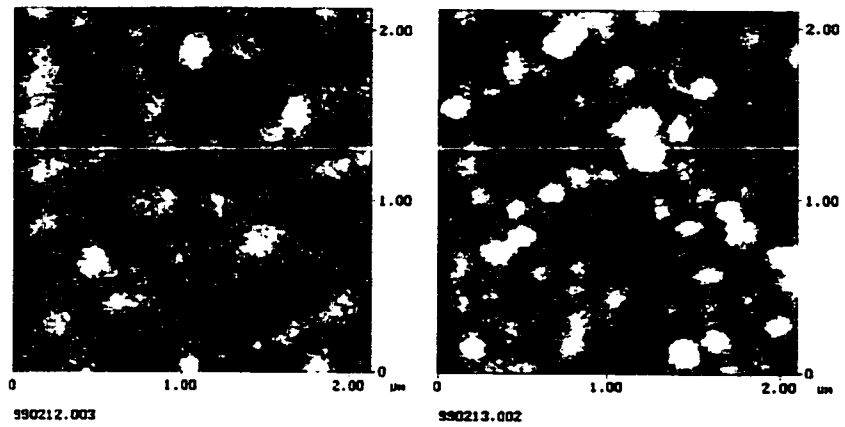

Figure 5.9: AFM Scans of high Al content AlGaAsSb Epitaxial Layers Grown $In_{0.3}Ga_{0.7}As$ Lattice-Engineered Substrates. 50 % Al epitaxial layer is on the left and 80% Al epitaxial layer is on the right.

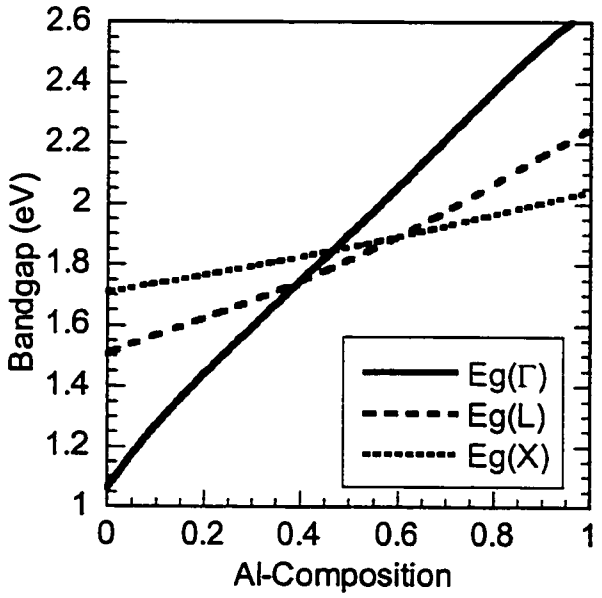

Figure 5.10: Variation of direct and indirect bandgap in $Al_xGa_{1-x}As_{0.78}Sb_{0.22}$ as a function of Al composition

on $In_{0.3}Ga_{0.7}As$ LES. The rms surface roughness increases from 6 Å to 8 Å when the Al composition is increased from 50 % to 80 %.

Figure 5.10 illustrates the variation of direct and indirect bandgap of $Al_{1-x}Ga_xAs_{0.78}Sb_{0.22}$ as a function of Al composition. $Al_{1-x}Ga_xAs_{0.78}Sb_{0.22}$ has a direct bandgap upto 40 % Al composition. The direct bandgap at this composition is 1.7 eV. Therefore SCH layers with bandgap as high as 1.7 eV are possible. This is 300 meV higher than the maximum possible bandgap achievable on an InP substrate, which is AlInAs. If $Al_{0.8}Ga_{0.2}As_{0.78}Sb_{0.22}$ is used as the cladding layer, the bandgap of the cladding layer increases to 1.9 eV. The low thermal conductivity of ternary and quaternary semiconductor cladding layers has to be taken into account when designing laser structures for uncooled operation.

Figure 5.11 compares the complete band-lineup of a 1.3 μm laser structure on a lattice-engineered substrate with a lattice constant of 5.75 Å and an InP substrate.

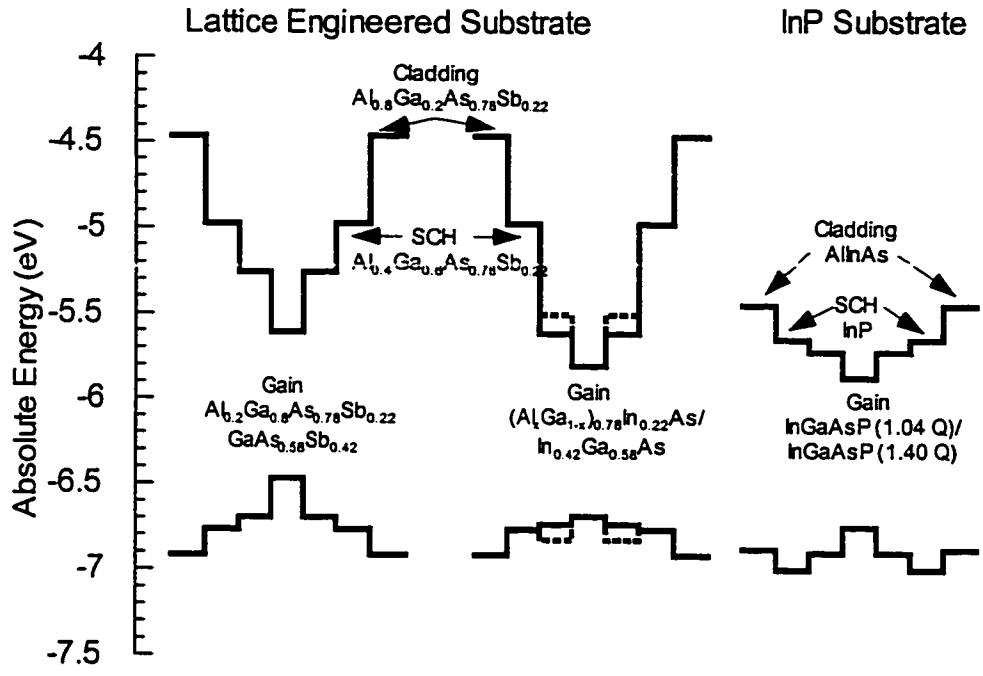

Figure 5.11: Comparison of Band lineups of Lasers on Lattice Engineered Substrates and InP Substrates

It is clear that significantly higher band-offsets can be achieved in both in the active region and between the active and cladding regions of the device. Hence 1.3 μm lasers on lattice-engineered substrates are expected to have better performance than those on InP substrates.

5.6. Optical Characterization of 1.3 μm Quantum wells grown on Lattice Engineered Substrates

As a first step towards the fabrication of 1.3μm lasers on GaAs based lattice engineered substrate arsenide and arsenide-antimonide based quantum wells were grown on lattice-engineered substrates. Optical Characterization of quantum wells grown on lattice-engineered substrates also offers valuable information on the impact of dislocation rated defects and lateral oxidation related defects and impurities on epitaxial layers grown on lattice engineered substrates.

5.6.1. 1.3 μm Single Quantum Wells Grown on $In_{0.2}Ga_{0.8}As$ Lattice Engineered Substrates

Initially, 1.3 μm quantum wells were grown on $In_{0.2}Ga_{0.8}As$ lattice-engineered substrates (LES). In case of an InGaAs quantum well a minimum composition of 43 % is required for 1.3 μm emission. As seen in the previous chapter low dislocation density InGaAs buffers with Indium compositions ranging from 10 to 15 % can be grown on $In_{0.2}Ga_{0.8}As$ LES. Thus the lattice-mismatch between the buffer layer and the quantum well is around 2 %. Since there is a possibility of dislocation generation during growth of multiple 80-100 Å thick quantum wells, test structures with only a single quantum well were grown. Prior to growth the native oxides from $In_{0.2}Ga_{0.8}As$ LES were removed by Ar ion sputtering and thermal desorption at 520 °C. As discussed before (in Chapter 4), stresses involved during the lateral oxidation process can enhance the defect diffusion in the InGaAs template layers of the LES. Subsequent regrowth on the LES results in the incorporation of these defects in the regrown epitaxial layers.

Figure 5.12 compares the low temperature (4K) PL spectra of an $In_{0.16}Ga_{0.84}As/In_{0.43}Ga_{0.57}As$ single quantum well grown on an $In_{0.2}Ga_{0.8}As$

LES with a 50 Å AlAs defect diffusion barrier. Due to the increased Indium composition in the quantum well the low temperature PL peak is now at 1.20 μm. This corresponds to 1.29 μm at room temperature. The intensity of emission from the quantum well grown on the LES is 7 times that of the quantum well grown on a GaAs substrate. This indicates improved quality of epitaxial layers grown on the LES compared to that on the GaAs substrate. The linewidth of the PL peak is 14 meV.

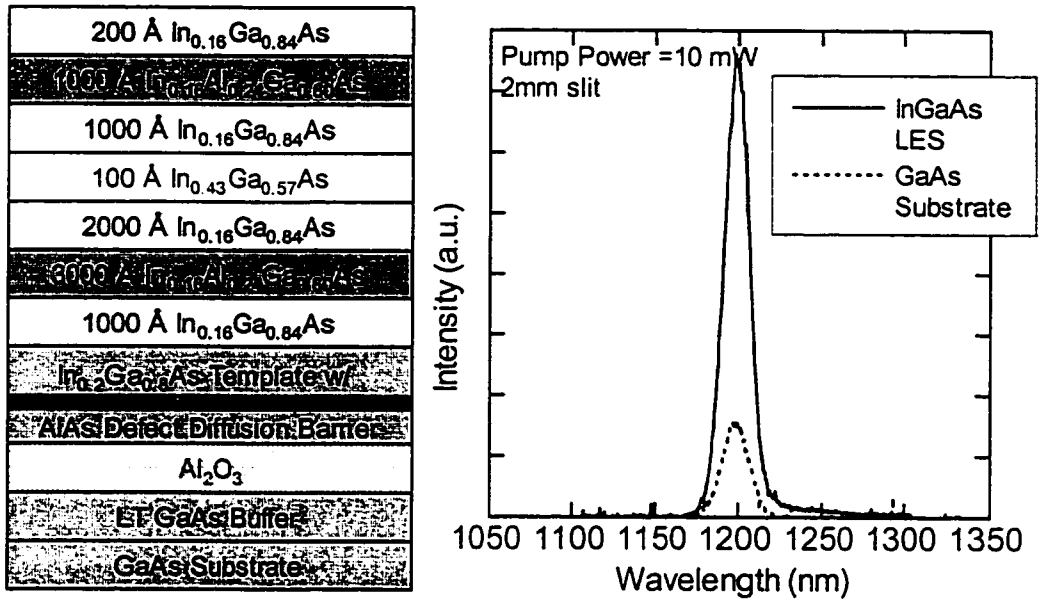

Figure 5.12: Comparison of Low temperature PL spectra of InGaAs/InGaAs SQW grown on an InGaAs LES (VGF Substrate) and GaAs Substrate

Figure 5.13 illustrates the room temperature PL spectra of the same an $In_{0.16}Ga_{0.84}As/In_{0.43}Ga_{0.57}As$ single quantum well. The PL emission peak is at 1.29 μm and the FWHM is 25 meV.

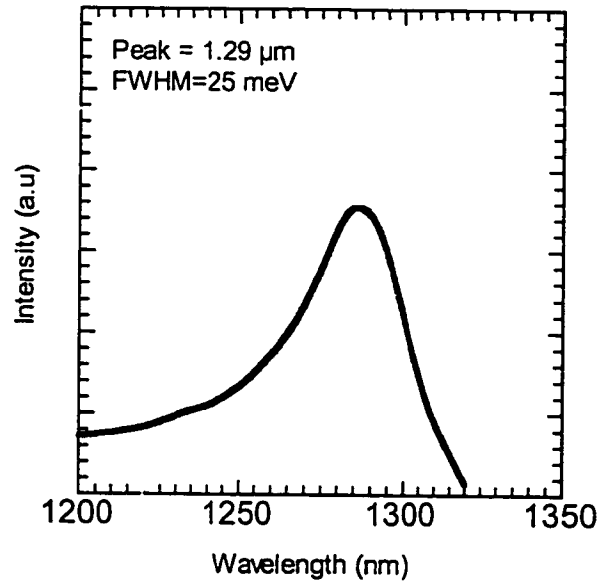

Figure 5.13: Room temperature PL spectrum of $In_{0.16}Ga_{0.84}As/In_{0.43}Ga_{0.57}As$ single quantum well grown on an $In_{0.2}Ga_{0.8}As$ Lattice-Engineered Substrate with an AlAs Defect Diffusion Barrier

Effect of oxidation induced defects on PL

Figure 5.14 illustrates the layer structures of $In_{0.2}Ga_{0.8}As$ LES with various defect diffusion barriers and the respective PL spectra of an $In_{0.16}Ga_{0.84}As/ In_{0.42}Ga_{0.58}As$ single quantum well grown on these substrates. In the case of an $In_{0.2}Ga_{0.8}As$ LES with an InAlAs/InGaAs epitaxial template on a LEC GaAs substrate, there is marginal improvement in PL intensity when compared to a quantum well grown on a GaAs substrate. In contrast significant improvement is observed in the case of an $In_{0.2}Ga_{0.8}As$ LES with a 50 Å AlAs

defect diffusion barrier. This highlights the importance of controlling diffusion of defects during the process of lateral oxidation.

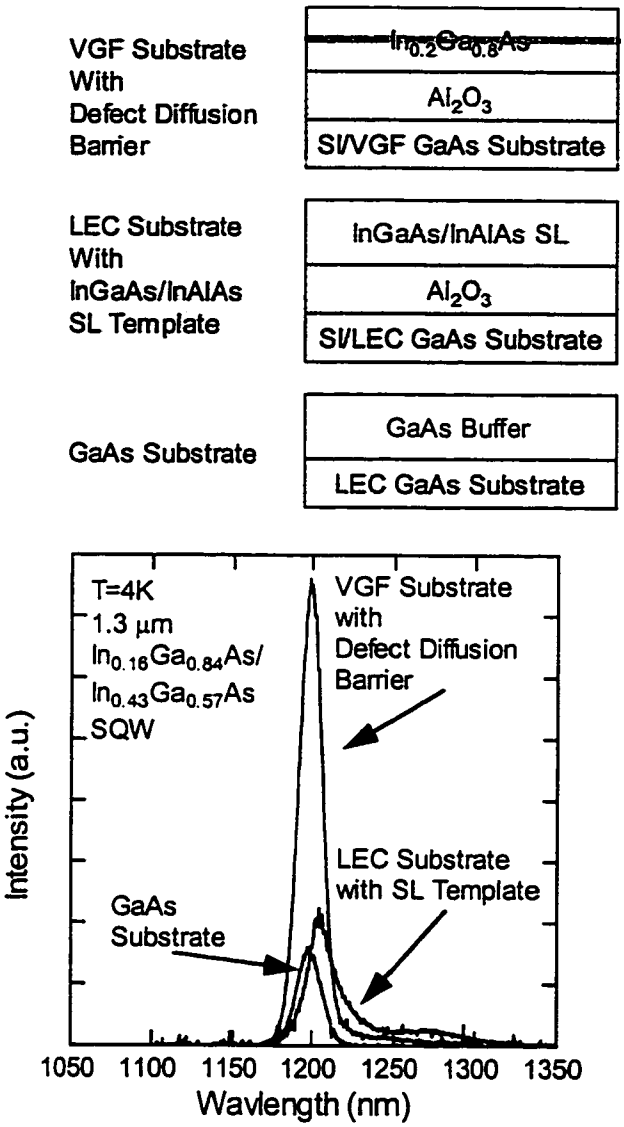

Figure 5.14: Comparison of low-temperature PL Spectra of InGaAs/InGaAs SQW grown on different Lattice-Engineered Substrates and GaAs Substrate

Comparison with Long Wavelength Quantum Wells Grown with Conventional Approaches

This low temperature FWHM value (14 meV) of the 80 Å $In_{0.43}Ga_{0.57}As$ quantum well grown on the $In_{0.2}Ga_{0.8}As$ LES is lower than 22 meV as observed (at 4 K) for a 73 Å lattice-matched $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ SQW with a emission peak of 1.3 μm that was grown on an InP substrate by MBE [32]. Even the room temperature PL linewidth (25 meV) is comparable to 18.4 meV as observed for 21 ML $In_{0.42}Ga_{0.58}As/GaAs$ single quantum well [33]. However the PL emission peak of that InGaAs/GaAs quantum well was at 1.23 μm. The PL emission linewidth of an $(InAs)_1(GaAs)_1$ strained short-period superlattice quantum well was 54 meV with the emission peak at 1.34 μm [5].

5.6.2. 1.3 μm Multiple Quantum Wells Grown on $In_{0.3}Ga_{0.7}As$ Lattice-Engineered Substrates (LES)

Using $In_{0.3}Ga_{0.7}As$ lattice-engineered substrates enables the growth of multiple quantum wells (MQW) with 1.3 μm emission wavelength. This is due to lower lattice mismatch (f ~ 1.4 %) between the substrate ($In_{0.25}Ga_{0.75}As/GaAs_{0.78}Sb_{0.22}$) and the quantum well layers ($In_{0.43}Ga_{0.57}As$).

1.3 μm $In_{0.25}Ga_{0.75}As/In_{0.43}Ga_{0.57}As$ MQW Structures on Ar Ion Sputtered $In_{0.3}Ga_{0.7}As$ LES

Initially, the MQW structures were grown on $In_{0.3}Ga_{0.7}As$ LES where the native oxide removal prior to regrowth was done by Ar ion sputtering and thermal desorption at 520 °C. This surface preparation process is effective for

$In_{0.2}Ga_{0.8}As$ LES. However, the higher Indium composition and lattice mismatch renders this process ineffective for $In_{0.3}Ga_{0.7}As$ LES.

Figure 5.15 illustrates the effect of inserting a thick epitaxial buffer layer on the optical properties of $In_{0.25}Ga_{0.75}As/In_{0.43}Ga_{0.57}As$ MQW. The PL intensity of quantum wells grown on 1.3 μm thick $Al_{0.7}Ga_{0.3}As_{0.78}Sb_{0.22}$ buffer layer is higher than those grown without the buffer layer. This is attributed to the dislocation density reduction after growth of the thick buffer layer. For MQW structures without the $Al_{0.7}Ga_{0.3}As_{0.78}Sb_{0.22}$ buffer, the emission intensity of the barrier layers (PL peak @ 1.12 μm) is higher than that from the quantum well (PL peak @ 1.3 μm). For MQW structures grown on $Al_{0.7}Ga_{0.3}As_{0.78}Sb_{0.22}$ buffer, the emission intensities of the $In_{0.25}Ga_{0.75}As$ barrier layers are comparable with emission intensity from the $In_{0.43}Ga_{0.57}As$ well. This indicates lower structural quality of epitaxial layers grown on Ar ion sputtered $In_{0.3}Ga_{0.7}As$ LES. Higher emission intensities from the barrier

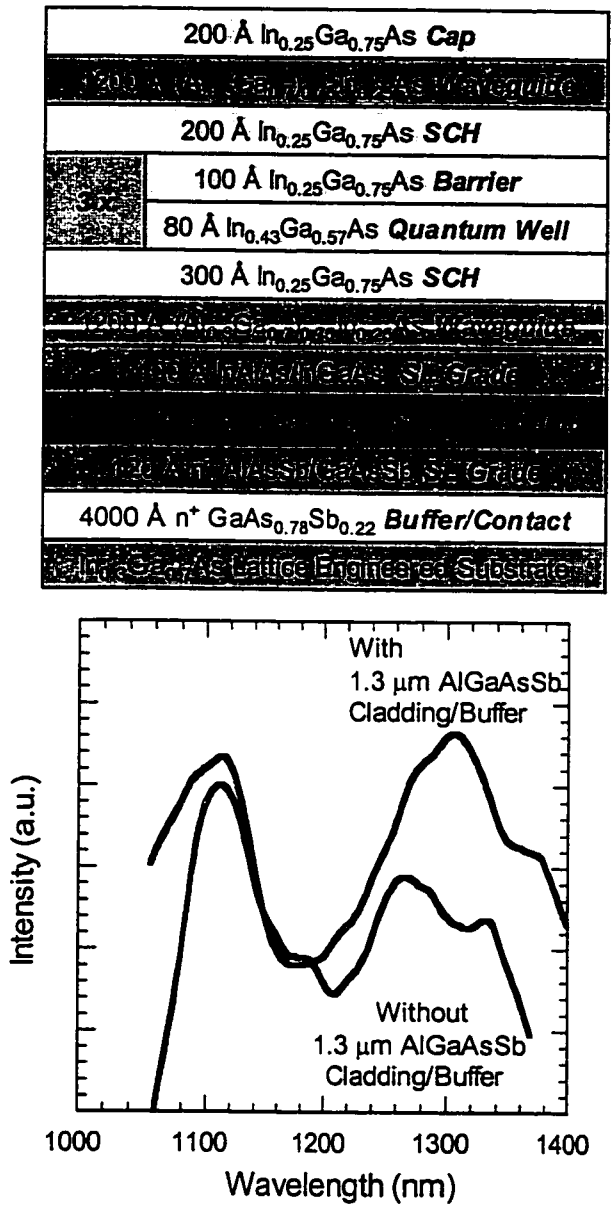

Figure 5.15: Effect of AlGaAsSb Buffer layers on room temperature PL spectra of $In_{0.25}Ga_{0.75}As/In_{0.43}Ga_{0.57}As$ MQW grown on $In_{0.3}Ga_{0.7}As$ Lattice Engineered Substrate

layers compared to the quantum well were observed in $In_{0.22}Ga_{0.78}As/In_{0.35}Ga_{0.65}As$ quantum wells grown on 1.0 μm thick $In_xGa_{1-x}As$ graded buffer layers [34]. The ratio of the emission intensities of the well and barrier layer improved when the structural quality of the buffer was improved.

1.3 μm AlGaInAs/GaInAs MQW Structures Grown on Thermally Desorbed $In_{0.3}Ga_{0.7}As$ Lattice-Engineered Substrates

In subsequent experiments, a 20 Å thick GaAs cap protected the InGaAs template layer in the LES structure. As a result, the native oxides on the surface could be removed by thermal desorption at 630 °C prior to regrowth. The elimination of Ar ion sputtering eliminates dislocation sources created by ion damage. This is corroborated by the fact that the degree of strain relaxation in MQW structures grown on thermally desorbed InGaAs LES was higher than those grown on Ar ion sputtered InGaAs LES.

In addition to changes in native oxide removal process prior to regrowth, the epitaxial structure of these MQW structures was also changed. The barrier layer was changed from $In_{0.25}Ga_{0.75}As$ to $In_{0.25}(Al_{0.2}Ga_{0.8})_{0.75}As$. Also instead of a random $In_{0.43}Ga_{0.57}As$ alloy, a $(In_{0.29}Ga_{0.71}As)_4/(InAs)_1$ short period superlattice was used as the quantum well. These changes are advantageous in three ways. First, the addition of Al increases both the conduction band and the valence band offsets between the quantum well and barrier layers, resulting in a better confinement of electrons and holes. Also the $(In_{0.29}Ga_{0.71}As)_4/(InAs)_1$ SPS has a lower effective bandgap than $In_{0.43}Ga_{0.57}As$ random alloy.

The advantage of using Al in the barrier layers is that the MQW structures can be grown without interruption. In a MBE machine, with a single

source of Al, Ga and In, growth of a InGaAs/InGaAs MQW quantum well requires significant growth pauses to allow the stabilization of the In or Ga cell temperatures. These prolonged growth pauses result in impurity incorporation at each of the barrier/well interfaces. In contrast, an AlGaInAs/GaInAs MQW structure can be grown without changing cell temperatures.

Figure 5.16 illustrates the layer structure and compares the room temperature PL spectra of an AlGaInAs/GaInAs MQW grown on $In_{0.2}Ga_{0.8}As$ LES. The PL peak is at 1.26 μm. Compared to the InGaAs LES, the FWHM of PL spectra is higher on the GaAs substrate. This is due to higher mismatch strain on the GaAs substrate that results in inhomogeneous strain relaxation in the epitaxial layers.

The room temperature FWHM of the quantum wells is 99 nm, which is higher than SQW structures. Peak broadening observed in MQW quantum wells is due to variation in well thickness and alloy composition, with the variation in well thickness being the dominant factor [35].

Figure 5.17 shows the layer structure and room temperature PL spectra of 1.3 μm MQW structures grown on thermally desorbed $In_{0.3}Ga_{0.7}As$ lattice engineered substrates. Table 5.4 compares the FWHM of the PL emission peak for various 1.3 mm MQW structures.

Substrate	PL Peak (nm)	PL FWHM (nm)
$In_{0.3}Ga_{0.7}As$ LES with 20 Å GaAs cap	1285 nm	49 nm
$In_{0.3}Ga_{0.7}As$ LES without 20 Å GaAs cap	1271 nm	41 nm
Unoxidized InGaAs LES Template	1280 nm	85 nm
GaAs substrate	1292 nm	104 nm

Table 5.4: Peak position and Peak FWHM of 1.3 μm AlGaInAs/GaInAs MQW structures grown on various substrates

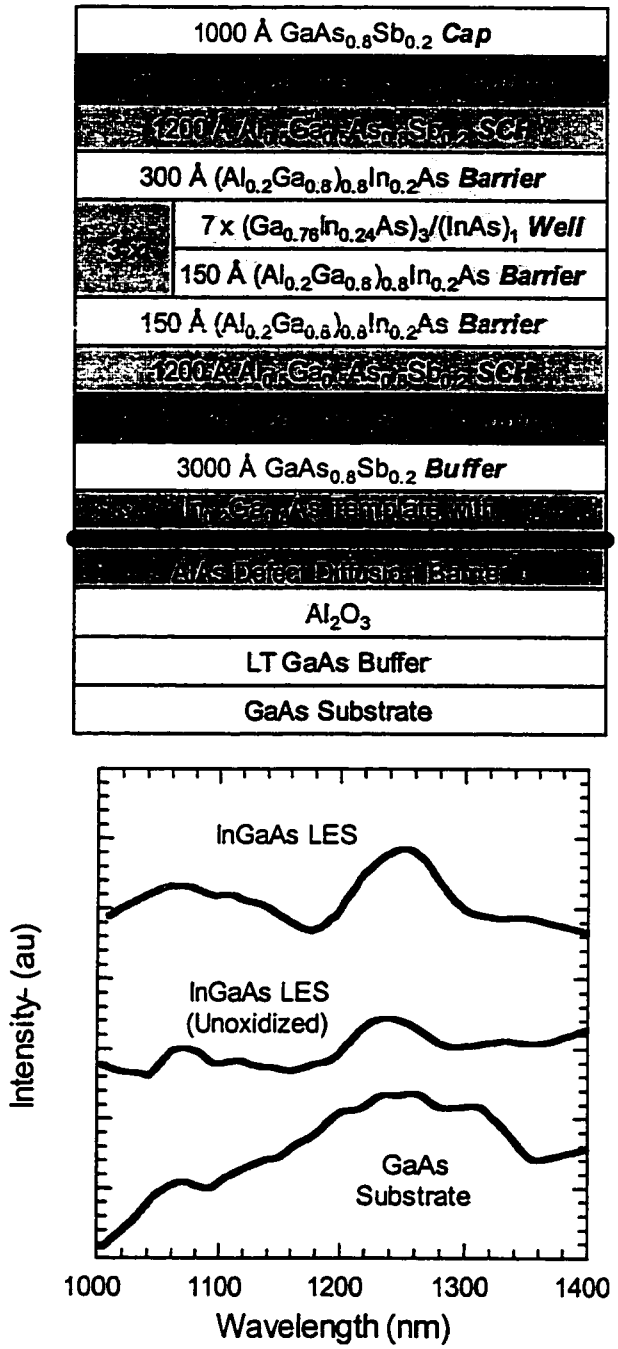

Figure 5.16: Room Temperature PL Spectra of AlGaInAs/InGaAs MQW grown on $In_{0.2}Ga_{0.8}As$ Lattice-Engineered Substrates

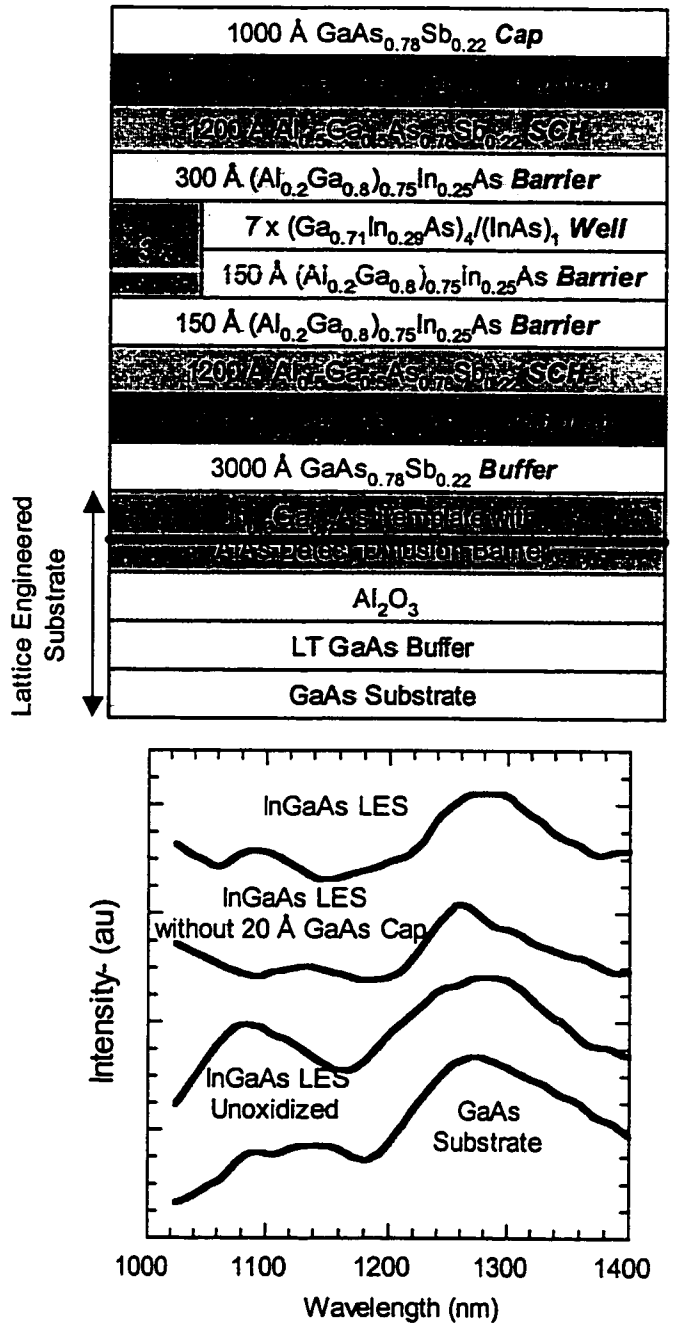

Figure 5.17: Layer structure and Room Temperature PL Spectra of 1.3 μm AlGaInAs/GaInAs MQW grown on $In_{0.3}Ga_{0.7}As$ Lattice-Engineered Substrates

It is clear that the FWHM of the MQW PL peak is narrower on InGaAs LES when compared to the GaAs and the unoxidized InGaAs LES Template. The lower intensity of MQW structures grown on a LES without the 20 Å GaAs protective cap is probably due to deterioration in surface morphology.

1.3 μm AlGaAsSb/GaAsSb MQW structures grown GaAsSb Lattice-Engineered Substrates

Other than InGaAs, the GaAsSb alloy system also offers the possibility of spanning lattice constants from GaAs to GaSb/InAs. As described before GaAsSb/GaAs quantum wells with staggered (Type II) band lineups were used for long wavelength emission on GaAs substrates. In contrast, AlGaAsSb/GaAsSb quantum wells with a straddling (Type I) band line up were used to grow 1.3 μm MQW structure on lattice-engineered substrates.

Again, the impact of native oxide removal processes on the optical quality of the MQW structures is again clearly evident. Figure 5.18 shows the layer structure and room temperature PL spectra of a 1.3 μm $Al_{0.2}Ga_{0.8}As_{0.78}Sb_{0.22}/GaAs_{0.58}Sb_{0.42}$ MQW PL structure grown on an $In_{0.3}Ga_{0.7}As$ LES. The LES structure in this case, did not have the protective 20 Å GaAs cap. As a result, prior to regrowth thermal desorption temperature was limited to 560 °C to prevent the decomposition of the $In_{0.3}Ga_{0.7}As$ surface. However, no Ar ion sputtering was used in this case. As the result complete native oxide removal from the surface was probably not achieved.

The broad PL spectrum of MQW structure grown on this substrate indicates inferior material quality.

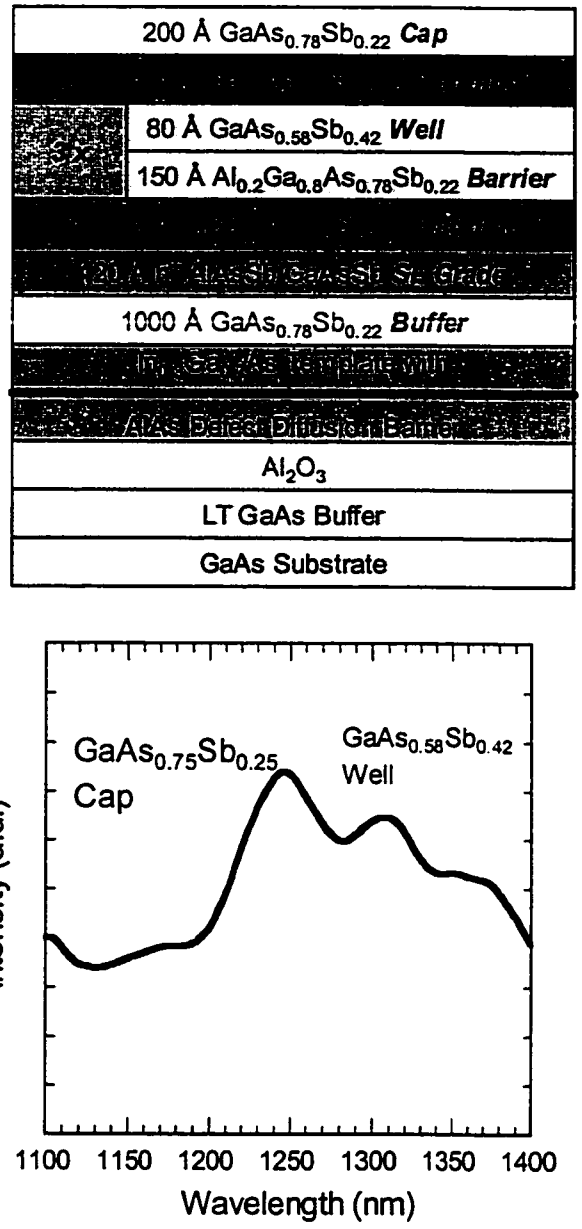

Figure 5.18: Layer structure and Room temperature PL Spectra of a1.3 μm AlGaAsSb/GaAsSb MQW structure grown on an $In_{0.3}Ga_{0.7}As$ LES

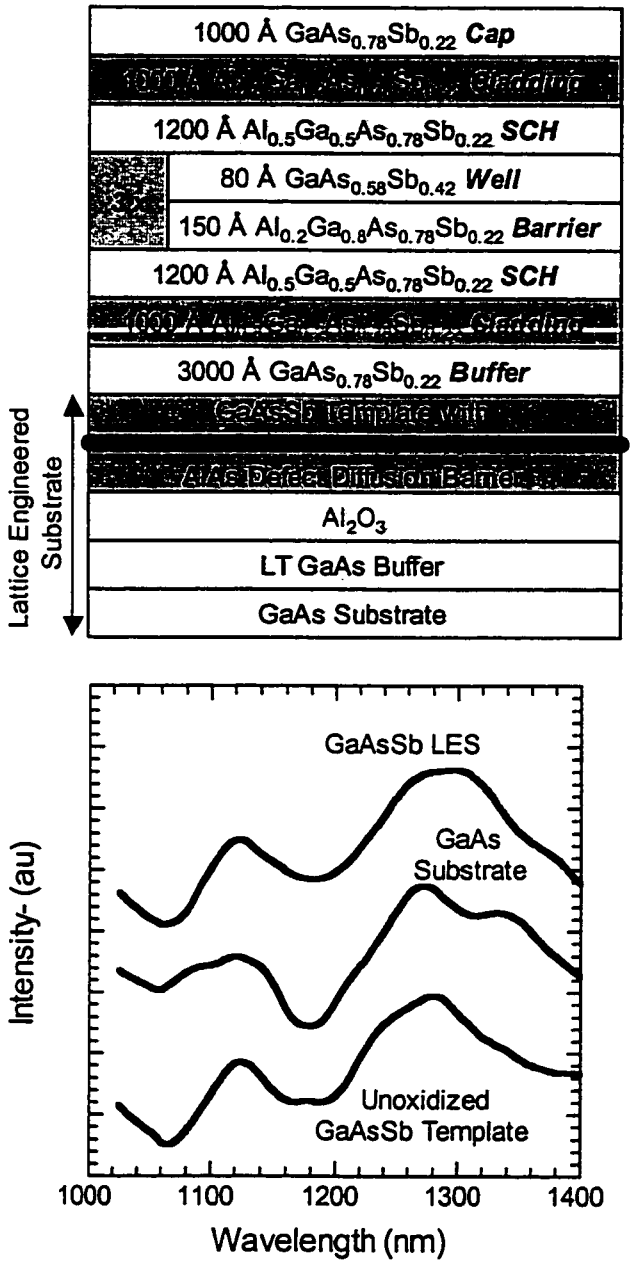

Figure 5.19: Layer structure and Room temperature PL spectra of AlGaAsSb/GaAsSb MQW structure grown on GaAsSb Lattice-Engineered Substrates

Figure 5.19 illustrates the layer structure and room temperature PL spectra of $Al_{0.2}Ga_{0.8}As_{0.78}Sb_{0.22}/GaAs_{0.78}Sb_{0.22}$ MQW structures grown on a $GaAs_{0.73}Sb_{0.27}$ lattice engineered substrate and GaAs substrate. The PL peak in this case is also at 1300 nm. The poor structural quality of MQW structures grown on GaAs substrates is evident in the double peaks observed near 1.3 μm. X-ray diffraction on these structures also indicated higher strain relaxation in the MQW structures on the GaAsSb LES compared to those on GaAs.

5.7. Conclusions

As seen in this chapter, the improved material quality of epitaxial layers and device structures on lattice-engineered substrates compared to those on GaAs substrate is due to lower defect density. InGaAs pn junction grown on lattice engineered substrates have lower reverse bias leakage currents and better forward bias ideality factors compared to the pn junctions grown directly on GaAs substrates.

In the case of long wavelength lasers, the InGaAs and GaAsSb based lattice engineered substrate technology enable the growth of laser structures with higher conduction and valence band barriers. This not results in higher optical gain and lower threshold current densities. Also suppression of carrier leakage from the active region into the cladding layers enables better high temperature performance of these devices. Optical characterization of 1.3 μm MQW structures demonstrated improved material quality on lattice-engineered substrates compared to GaAs substrates. However, it is clear that suppression of defect diffusion during the lateral oxidation process and development of a damage free native oxide removal process is necessary in order to achieve high

structural and optical quality in materials and device structures grown on lattice-engineered substrates.

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Chapter 6.
Conclusion and Future Directions

6.1. Introduction

The approach to achieve low dislocation density heteroepitaxial materials has two requirements. The first is suppression of dislocation nucleation and the second is the optimum use of existing dislocations by enhancing dislocation glide. The enhanced dislocation glide is achieved by either increasing the available driving force for dislocation glide, or by eliminating the barriers to dislocation movement.

In the lattice-engineered substrate approach to heteroepitaxy, a low growth temperature coupled with the Frank-van der Merwe growth mode suppresses dislocation nucleation during the growth of the InGaAs/GaAsSb epitaxial structure. Threading dislocation glide is a perquisite for the creation of strain relieving misfit dislocation segments. Structural changes occurring during the lateral oxidation process result in stresses that enhance threading dislocation glide in the highly strained InGaAs/GaAsSb epitaxial layer. In addition, reactive removal of existing misfit dislocation segments removes the barriers to the glide of other threading dislocations. Another important aspect is the effect of dislocations and lattice mismatch on surface morphology. The reactive removal misfit dislocation segments coupled with the enhanced threading dislocation glide in the relaxed InGaAs/GaAsSb epitaxial template

eliminates the dislocation related strain fields on the epitaxial surface. As a result, regrowth of epitaxial layers with good surface morphology is possible on lattice engineered substrates.

6.2. Achievements

6.2.1. MBE growth of highly strained InGaAs and GaAsSb

The LES approach requires the growth of highly strained low dislocation density epitaxial layers with thicknesses well in the excess of the Matthews-Blakeslee critical thickness. Strain relaxation in highly mismatched epitaxial layers was suppressed by a combination factor which included low growth temperature, maintaining a 2D growth mode and reduction of other dislocation sources like substrate threading dislocation through the use of low dislocation density VGF substrates. The suppression of dislocation generation and strain relaxation also ensures a smooth surface morphology, which is a principle requirement for regrowth of high quality epitaxial layers on the lattice-engineered substrates.

InGaAs epitaxial layers with Indium compositions ranging from 20% to 40% were grown on AlAs oxidation layers at growth temperatures ranging from 300 °C to 430 °C. The InGaAs layer thickness was 20 times the equilibrium Matthews-Blakeslee critical thickness. It was observed that the degree of strain relaxation and rms surface roughness in the as grown layers increased with the lattice mismatch. In contrast GaAsSb epitaxial layers with similar lattice mismatches exhibited lesser degree of strain relaxation and smoother surface morphology. The smoother surface morphology may be attributed to the surfactant effect of Sb on the growth surface.

6.2.2. Lateral oxidation of AlAsSb

Lateral oxidation of the AlAs(Sb) oxidation layers under the strained InGaAs (GaAsSb) overlayers results in structural changes in the epitaxial structure and the nature of the InGaAs (GaAsSb)/oxide interface. The lateral oxidation process of AlAs(Sb) oxidation layers was studied extensively. Apart from achieving high oxidation rates, it is also important to suppress the stress enhanced diffusion of vacancies and defects generated during the lateral oxidation process.

Incorporation of Sb in the AlAs oxidation rates, result in an oxide with increased porosity. As a result the diffusion rates of reactants from the oxidation mesa edge to the reaction interface are enhanced. This not only increases the oxidation rate but also changes the oxidation process from a diffusion-limited mechanism to a reaction-limited mechanism. However, an undesirable effect of Sb addition to AlAs is the non-uniform segregation of Sb at the upper oxide interface. This can be prevented by increasing the oxidation temperature, which ensures the conversion of all the Sb to Sb_2O_3 that diffuses out from the oxide.

The diffusion of defects generated during the lateral oxidation process was suppressed in two ways. The AlAs(Sb) oxidation layers were grown on top of annealed LT GaAs layers. The As precipitate clusters in the annealed LT GaAs layers are expected to act as defect gettering centers. In addition, the diffusion of defects in the strain overlayers was suppressed by insertion of a 50 Å thick AlAs defect diffusion barrier.

6.2.3. Strain relaxation during lateral oxidation

Strain relaxation in InGaAs and GaAsSb strained overlayers was studied extensively as function of lattice mismatch in the overlayer and the

oxidation temperature. No strain relaxation was observed in strained overlayers annealed under similar conditions (with the exception of $In_{0.4}Ga_{0.6}As$ epitaxial layers annealed at higher temperatures). This confirms that enhanced strain relaxation in the overlayers is due to structural changes occurring in the epitaxial structure and not due to high temperature annealing. This was verified by plan-view TEM analysis that indicated a reduction of misfit dislocation density at a $In_{0.2}Ga_{0.8}As$/AlAs interface by 2 orders of magnitude upon oxidation.

It was observed that the degree of strain relaxation increased with the oxidation temperature and the efficiency of strain relaxation reduced with the increasing lattice mismatch. The efficiency of strain relaxation was increased by suppressing strain relaxation during the growth of the highly strained InGaAs (GaAsSb) overlayers. It was observed that the residual elastic strain in the resultant InGaAs (GaAsSb) lattice-engineered substrates was significantly lower than heteroepitaxial layers of the same thickness grown on GaAs substrates. This is mainly due to the efficient strain relaxation (higher driving forces coupled with lesser barriers) occurring during the lateral oxidation process.

6.2.4. Regrowth on Lattice Engineered Substrates

Removal of Native Oxides

The structural quality of epitaxial layers grown on lattice-engineered substrate process is very sensitive to surface preparation and native oxide removal techniques used prior to initiating growth. The surface of the InGaAs (GaAsSb) template during processing and lateral oxidation was protected by a sacrificial AlAs/GaAs cap. Prior to loading these sacrificial layers were removed by selective wet chemical etching.

Removal of native oxides from ternary semiconductor surfaces is difficult as the required high temperatures result in a change in the alloy composition at the surface. In the case of InGaAs surfaces this is due to the low volatility of the Indium atoms. In the case of GaAsSb surfaces, As/Sb exchange at the surface results in a change in the composition. As a result, initially the native oxides on the surface were removed by Ar ion sputtering. This however results in a damaged surface that can act as source of dislocations. In addition, the Ar ion sputtering is successful is only removing the loosely bound Ga_2O_3 native oxide and is unsuccessful in complete removal of the tightly bound In_2O_3 oxide. Also after Ar ion sputtering thermal desorption temperatures were limited to 520 °C.

This surface preparation technique was found to be adequate for $In_{0.2}Ga_{0.8}As$ lattice-engineered substrates due to the lower Indium composition and lattice mismatches. However, this approach results in significantly higher dislocation densities in $In_{0.3}Ga_{0.7}As$ lattice-engineered substrates.

The best approach to native oxide removal prior to regrowth is to protect the InGaAs (GaAsSb) epitaxial layers with a 20 Å GaAs cap. As the result, the ternary surfaces are never exposed to the atmosphere. This also eliminates the need for Ar ion sputtering as the native oxide on the 20 Å GaAs cap can be removed by thermal desorption at 630 °C while still protecting the underlying ternary epitaxial layers. The thickness of the remaining GaAs epitaxial layer after thermal desorption is expected to be less than 10 Å.

Structural Properties of Epitaxial Layers grown on Lattice-Engineered Substrates

The structural characterization of epitaxial layers on LES was done by transmission electron microscopy (TEM), x-ray diffraction and atomic force microscopy (AFM).

Cross-sectional TEM micrographs of InGaAs epitaxial layers grown on $In_{0.2}Ga_{0.8}As$ epitaxial layers showed no threading dislocations indicating that the dislocation density is below 5 x $10^7/cm^2$. However in the case of $In_{0.3}Ga_{0.7}As$ LES some dislocations were observed originating at the regrowth interface. This is attributed mainly due to the damage created by Ar ion sputtering and incomplete removal of native oxides due to lower desorption temperatures. Structural characterization of epitaxial layers grown on thermal desorbed LES is in progress.

X-Ray diffraction analysis showed that the residual elastic strain in epitaxial layers grown on lattice-engineered substrates is significantly lower than those grown GaAs substrate. In the case of epitaxial layers grown on Ar ion sputtered LES, this difference was not significant. When Ar ion sputtering was eliminated a large difference was observed between the residual elastic strain on LES and GaAs substrates. This confirms the fact that the ion damaged surface acts as a source of strain relieving dislocations and also results in a higher dislocation density.

Surface morphology analysis by AFM shows that the rms surface roughness of epitaxial layers grown on LES is lower than those grown on the GaAs surface. This is direct consequence of the removal of misfit dislocations at the InGaAs/oxide interface during lateral oxidation. The elimination/reduction of mismatch strain between the epitaxial layer and the LES and the dissipation dislocation strain fields in the relaxed LES template, suppresses the tendency for 3 dimensional growth mode.

In general it was observed that the structural quality and surface morphology of GaAsSb epitaxial layers was much better compared to InGaAs epitaxial layers grown on lattice-engineered substrates. This is attributed to the relative "softness" of the antimonide based semiconductors and the surfactant effect of Sb on the growth surface.

6.2.5. Electrical and Optical Characterization of Device Structures Grown on Lattice-Engineered Substrates

InGaAs pn junction grown on lattice engineered substrates have lower reverse bias leakage currents and better forward bias ideality factors compared to the pn junctions grown directly on GaAs substrates.

In the case of long wavelength lasers, the InGaAs and GaAsSb based lattice engineered substrate technology enables the growth of laser structures with higher conduction and valence band barriers. This not results in higher optical gain and lower threshold current densities. Also suppression of carrier leakage from the active region into the cladding layers enables better high temperature performance of these devices. Optical characterization of 1.3 μm MQW structures demonstrated improved material quality on lattice-engineered substrates compared to GaAs substrates. However, it is clear that suppression of defect diffusion during the lateral oxidation process and development of a damage free native oxide removal process is necessary in order to achieve high structural and optical quality in materials and device structures grown on lattice-engineered substrates.

6.3. Future Directions

6.3.1. Lattice Engineered Substrates on Other III-V Binary Substrates

In addition to GaAs based substrates, the LES approach can also be used to achieve low dislocation density heteroepitaxial materials and devices on other binary substrate platforms. An InP based LES, will enable the implementation of low voltage HBTs at a lattice constant between that of InP and InAs. Implementation of this approach on GaSb will enable the growth of Arsenide-Antimonide semiconductors having lattice constants > 6.1 Å. Figure 6.1 illustrates the typical layer structure of templates with a 2.1 % lattice mismatch for lattice-engineered substrates on InP and GaSb substrates.

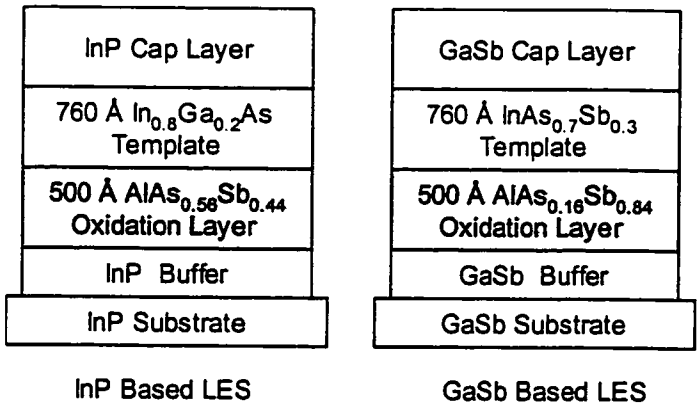

Figure 6.1: Layer structure of InP and GaSb based Lattice Engineered Substrate with a20 x $h_{critical}$ thick template with a 2.1% lattice mismatch

Since the oxidation layers in InP and GaSb based LES have significantly high amount of Sb, Sb segregation during lateral oxidation has to be addressed.

In addition to compressively strained overlayers, strain relaxation in tensile strained overlayers can also be investigated. For example on GaAs based lattice-engineered substrates, strain relaxation in tensile GaAsP layers

can be investigated. Also on InP substrates strain relaxation in tensile GaAsSb and InGaAs layers can be investigated.

6.3.2. Improving strain relaxation efficiency

In the case of InGaAs lattice-engineered substrates, it was observed that 90% strain relaxation is achieved in $In_{0.2}Ga_{0.8}As$ LES, however for higher lattice mismatches the maximum achievable strain relaxation was around 70 %. The strain relaxation efficiency in the highly mismatched overlayers could be improved by addition of Sb to the AlAs oxidation layer. Also mixed Arsenide-phosphide ($AlAs_{1-y}P_y$) and mixed phosphide-antimonide ($AlSb_{1-y}P_y$) oxidation layers could be investigated for use in lattice-engineered substrates. Further strain relaxation as a function of oxidation layer thickness can also be investigated.

High temperature thermal annealing prior to regrowth may result in further strain relaxation. An alternative approach is use of "softer" materials like GaAsSb as the strained overlayer. Figure 6.2 illustrates the approaches that can be used to improve the strain relaxation efficiency.

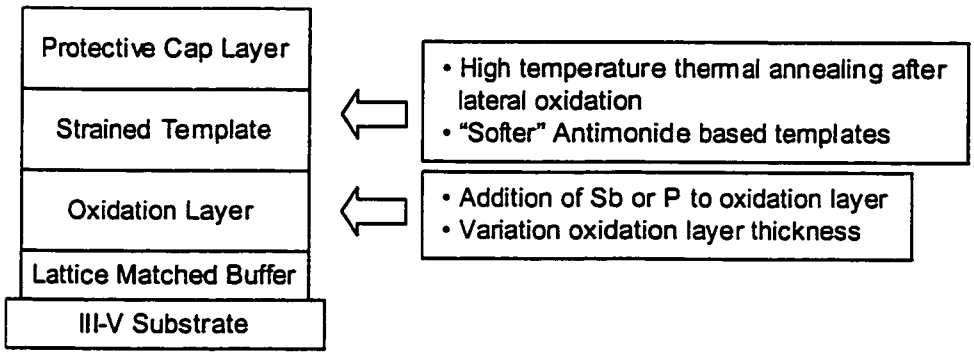

Figure 6.2: Approaches that can be used to improve strain relaxation efficiency in lattice-engineered substrates

6.3.3. Improved Regrowth Initiation Techniques

It has been shown in thesis that use of ion beam sources for surface preparation is highly undesirable in the case of lattice-engineered substrates. The resultant ion–damaged material can act as a low activation energy source of dislocations. Pure thermal desorption was found to be the best method for removal of native oxides from surfaces of lattice-engineered substrates. However high temperature thermal desorption may result in a faceted surface with a low dislocation nucleation barrier. This barrier can be overcome by initiation of regrowth a low growth temperature to maintain a 2D surface morphology. After the growth of the Low-temperature buffer layer, subsequent epitaxial layers could be grown at high temperatures. Figure 6.3 illustrates the improved regrowth initiation techniques.

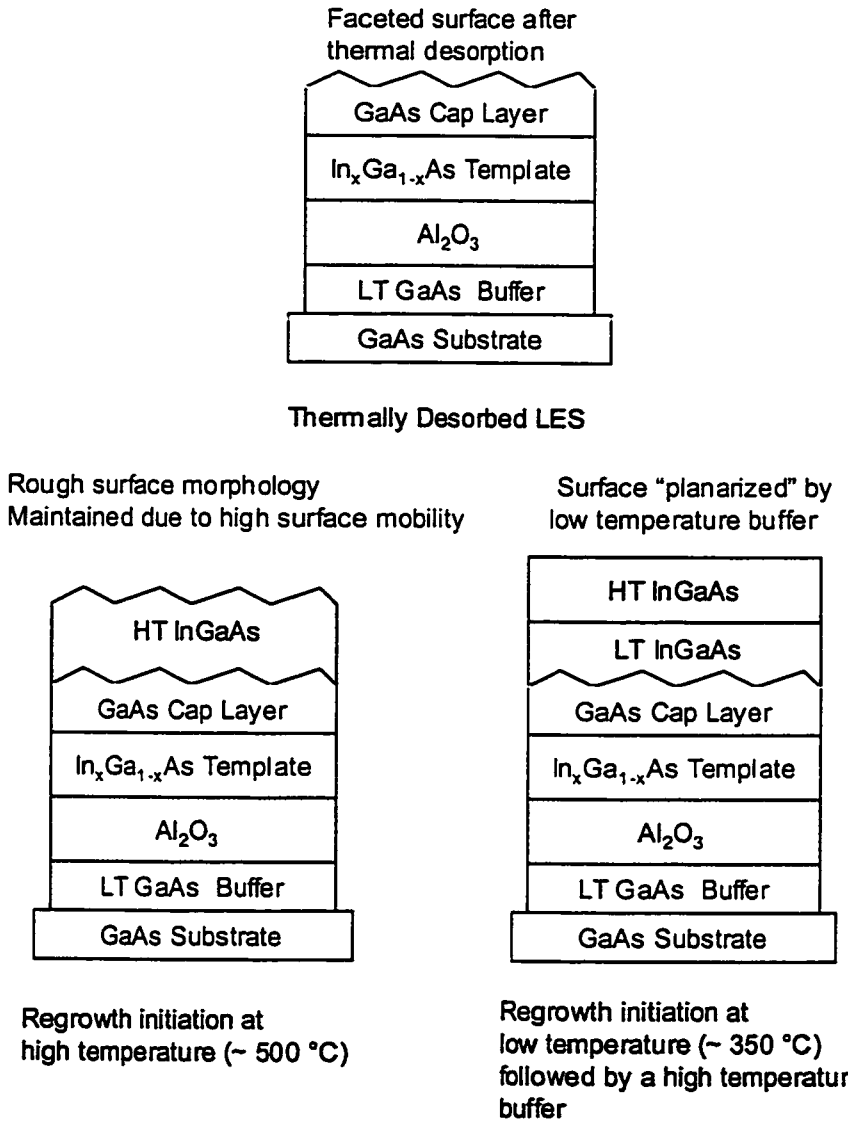

Figure 6.3: Effect of regrowth initiation techniques on surface morphology of epitaxial layers grown on lattice-engineered substrates

6.3.4. Device Structures on Lattice-Engineered Substrates

In addition to improvements in the processing and growth techniques for lattice-engineered substrates, many different devices structures like

photodetectors, solar cells and field effect transistors can be grown on lattice-engineered substrates.

On GaAs based LES, high efficiency pHEMTs with Indium composition channels approaching 50% can be fabricated. Current high Indium composition channel HEMTs are either grown on InP substrates (which are fragile and costly) or on graded buffer layers on GaAs substrates (where leakage due to dislocations in the buffer is problem and rough surface morphology is a problem). The problems can be potentially solved by growth on GaAs based lattice-engineered substrates.

Another device structure that can be grown on GaAs based lattice-engineered substrates is a 1.3 μm edge-emitting laser. As shown in this thesis, growth of AlGaAsSb based cladding layers and 1.3 μm active region using both InGaAs and GaAsSb quantum wells is possible on GaAs based LES. However to achieve laser operation strict control and further reduction of dislocation densities in the epitaxial layers grown on lattice-engineered substrates is necessary.

It is also possible to grow 1.3 μm photodetectors on GaAs based lattice-engineered substrates. It is possible to monolithically integrate GaAs based electronics and a long wavelength photodetector on a LES platform to make a high-speed optoelectronic receiver.

On an InP based lattice-engineered substrate, low voltage heterostructure bipolar transistors with $In_{0.7}Ga_{0.3}As$ base and collector layers can be implemented. The turn-on voltages in these transistors could be as low as 0.5 V compared to 0.75 V that is possible with a lattice-matched AlInAs/GaInAs HBT on an InP substrate. This could significantly lower the power dissipated in high-speed dense HBT-based digital circuits.

Since the lattice-engineered substrate approach enables epitaxial growth at an arbitrary lattice-constant that is between commercially available

substrates, any device structure that is grown on conventional substrates can be implemented on a lattice-engineered substrate by choosing the appropriate semiconductor alloys that offer a significant improvement in the device performance.