UNIVERSITY OF CALIFORNIA

Santa Barbara

Oxide Based Electronics in Gallium Arsenide

A dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy
In
Electrical and Computer Engineering

by

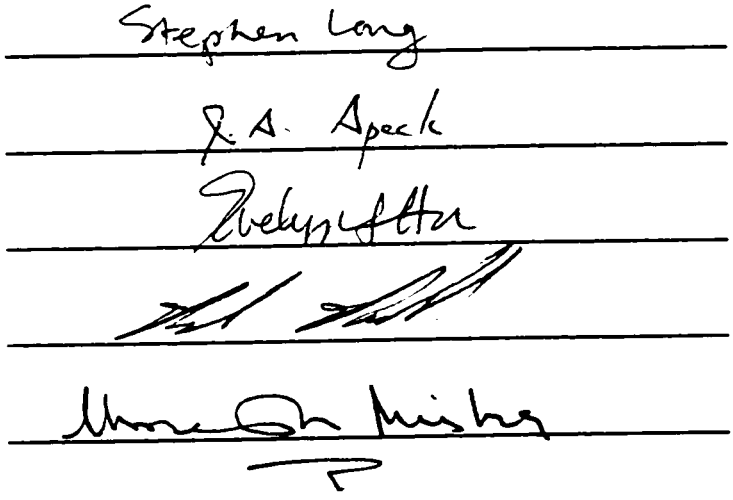
Primit. A. Parikh

Committee Members

Professor Umesh Mishra, Chairperson
Professor Evelyn Hu
Professor Stephen Long
Professor Mark Rodwell
Professor James Speck

June 1998

The dissertation of Primit Parikh is approved



Committee Chairperson

June 1998

Chance favors the prepared mind .....

Anonymous

Dedicated to my parents,
Arun and Ranjana Parikh

Acknowledgements

The last four years in Santa Barbara, without an iota of doubt, rank as the best in my life, thus far. Be it the gorgeous sunny skies and the beaches, a great academic program, an excellent research environment, vociferous discussions with my labmates or just the tons of fun I had with my friends, there never was a dull moment.

I have learnt a lot from my advisor Professor Umesh Mishra. Most important are the intangible skills including marketing an idea, interacting positively with people, convincing others, managing work, and always focusing on and achieving aggressive goals. Ofcourse if one hangs around with Umesh for four and a half years, it is but natural to get acquainted a little with transistors and semiconductor technologies. His constant support, guidance and encouragement has been invaluable.

I received a lot of positive input from Professors Evelyn Hu and James Speck in the area of wet oxidation and its mechanisms, which was an important ingredient of my dissertation. Over the last four years I have had the pleasure of interacting with and learning from Professor Mark Rodwell, about electronic devices and circuits and smart ideas in general. Professor Steve Long was always available for guidance and valuable insights for my project. Next to Umesh though, the most fun I had in interacting with faculty was with Professor Bob York. On and off, through mainly informal discussions, I have picked up some cool tips from Bob. More importantly, Bob was the first (other than myself ofcourse) to trust

me with investing money. Special thanks to James Ibbetson and Professor Steve Denbaars for following suit. I hope the list grows.

I can never thank enough all my past and present colleagues at UCSB. Weinan and Kursad for teaching me processing amongst other things, Prashant for being an ever ready source of MBE material, Jeff , Nguyen, Bernd for MOCVD regrowths, James for MBE samples and insightful technical discussions, Dan Docter for active collaboration on my project, Lijie Zhu for TEMs, Ernie Caine for E-beam lithography, Jack Whaley , Bob Hill for cleanroom support, Yifeng for the most interesting discussions and help on diverse technical and non technical subjects, Angelos for help in a variety of matters, Rob for keeping the lab in shape, Nick for being a cool investment buddy, Jon & Laura for being wonderful party hosts, Gia, Peter, Amit, Jane, Vicki, Lee, James, Dave, Brian and lots of other fellow solid state students at UCSB. Things would have been much harder without the administrative help from Janie, Cathy and Lee.

I will always cherish the times spent with my friends Harpreet, Raja, Chandu, Madhukar, Bipul, Ajit, Doli, Ashok, Satish, Ayan, Uddalak, Bhavna, Meghna, Ambi, Dr. Atul Rai to name a few. Special thanks to everyone else who helped me organize events for India Association (often I enjoyed this more than my Ph.D !) ; Ashish, Shobha, Minu, Sunil & Hema, Anurag amongst innumerable others.

I wish to thank my uncle & aunty Akshay & Rita Marfatia for always being there for me, ever since I have been in the US. Above all I place my parents, Arun & Ranjana Parikh and my sister Priyanka for their constant support and encouragement throughout my entire career. I could never have done it without them.

Vita

August 24, 1971	Born, Baroda, INDIA
June 1993	Bachelor of Technology, Electrical Engineering, Indian Institute of Technology, Bombay, India
December 1994	Master of Science, Electrical & Computer Engineering, University of California, Santa Barbara
May 1998	Doctor of Philosophy, Electrical & Computer Engineering (Major : Solid State, Minor : Analog & Digital Circuits), University of California, Santa Barbara

Invited Publications / Presentations

1. Oxide Based Compound-Semiconductor Electronics : Umesh K. Mishra, Primit Parikh, Prashant Chavarkar, Jeff Yen, James Champlain, Brian Thiebeault, Helen Reese, Song Stone Shi, Evelyn Hu, Lijie Zhou and James Speck, International Electron Devices Meeting, Washington, Dec. 1997.

2. GaAs On Insulator (GOI) for Low Power Applications, U.K. Mishra, P.A. Parikh, P. Chavarkar and J. Champlain, Workshop On Frontiers of Electronics, Tenerife, Spain, 1997.

3. InP based devices and their Applications for Merged FET-HBT Technologies (Invited Paper) : P. A. Parikh, K. Kiziloglu, M. Mondry, P. Chavarkar, B. Keller, S.P. Denbaars, U.K. Mishra, Microwave and Optical Technology Letters, February 1996, vol. 11, no. 3, pp. 121-25.

Journal Publications

4. Record Power Added Efficiency, Low Voltage GOI (GaAs On Insulator) MESFET Technology for Wireless Applications : P. Parikh, J. Ibbetson, U. K. Mishra, D. Docter, M. Le, K. Kiziloglu, D. Grider, J. Pusl, Submitted to Journal of Microwave Theory and Techniques, 1998.

5. GaAs MESFETs on a truly insulating buffer layer : Demonstration of the GaAs On Insulator technology : P. Parikh, P. Chavarkar, U.K. Mishra, IEEE Electron Device Letters, March 97 Vol. 18. no 3, pp. 111-14.

6. Hydrogenation of GaAs MISFETs with Al_2O_3 as the gate insulator : P.A. Parikh, J. Ibbetson, S. Shi, E.L. Hu, U.K. Mishra, Electronics letters, 1996, vol. 32 , no. 18 pp. 1724-6.

7. A new FET-Based Integrated Circuit Technology : The SASSFET, P.A. Parikh, W.N. Jiang, P.M. Chavarkar, K. Kiziloglu, B. Keller, S.P. DenBaars, U.K. Mishra, IEEE Electron Device Letters, July 96, vol. 17, no. 3, pp. 375-77

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10. Record Power Added Efficiency, Low Voltage GOI (GaAs On Insulator) MESFET Technology for Wireless Applications : P. Parikh, J. Ibbetson, U. Mishra, D. Docter, M. Lee, K. Kiziloglu, D. Grider, J. Pusl; 1998 IEEE MTT-S International Microwave Symposium and Exhibition, June 1998.

11. Depletion mode Al_2O_3 / GaAs MOSFETs with high current level : P.A. Parikh, P. Chavarkar, J. Ibbetson, B. Keller, U.K. Mishra, IEEE CORNELL Conference on High Speed Devices and Circuits, Aug. 1997.

12. Effect of oxidation of $Al_xGa_{1-x}As$ on adjacent semiconductor layers : HALL (Electrical) and TEM (Structural) Characterization, P.A. Parikh, P. Chavarkar, L. Zhu, J. Ibbetson, J. Speck and U.K. Mishra, 39'th Electronic Materials Conference, Fort Collins, Colorado, June 1997.

13. PHEMTs in the newly developed GOI technology, P.A. Parikh, P. Chavarkar, Y. F. Wu, P. Pinsukanjana, U.K. Mishra : 1996 International Electron Device Meeting, San Francisco, Dec. 1996.

14. First demonstration of GaAs On Insulator Technology, P.A. Parikh, P. Chavarkar, U.K. Mishra : 54'th Device Research Conference, Santa Barbara, June 1996

15. DLTS measurements of MIS capacitors with Al_2O_3 as the gate insulator : P.A. Parikh, S. Jain, P. Chavarkar, J. Ibbetson, J. Champlain, L. Macarthy, S. Shi, E.L. Hu, U.K. Mishra, 38'th EMC conference Santa Barbara, June 1996

16. n-HJFET-Pnp HBT technology for complementary circuit applications : P.A. Parikh, K. Kiziloglu, M. Mondry, P. Chavarkar, B. Keller, S.P. Denbaars, U.K. Mishra, 21'st International Symposium on Compound Semiconductors, SanDiego, September 1994.

17. The effect of a Non-Stoichiometric Buffer on the Oxidation and Electrical Properties of GaAs On Insulator (GOI) Field Effect

Transistors : J. G. Champlain, P. A. Parikh, U. K. Mishra, 40'th Electronics Materials Conference, Virginia, 1998.

18. CV and DLTS Characterization of MIS Capacitors on $In_{0.53}GaAs$ with Oxidized $Al_{0.44}AsSb$ as the Insulating Dielectric : J.G. Champlain, P.M. Chavarkar, P.A. Parikh, U.K. Mishra, 39'th Electronic Materials Conference, Fort Collins, Colorado, June 1997.

Magazine Articles / Referrals

19. Electronic Engineering Times, April 7, 1997 : GaAs research looks to oxide layer

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ABSTRACT

The rapid growth of wireless communications has spawned several emerging markets in electronics whose needs cannot be satisfied by the conventional Silicon technology. High efficiency electronics including power transmitters and signal processing is crucial for satellite and hand held devices; as this results in smaller, lighter, cheaper and more reliable modules. Thus far, not many device technologies have addressed this issue.

We propose that judicious introduction of oxides within a device structure to eliminate leakage currents will be a major step towards achieving this goal. The main objective of this thesis is to investigate the technique of wet lateral oxidation of high Al composition $Al_xGa_{1-x}As$ layers to obtain Al_2O_3 and FETs incorporating this oxide for ultra high efficiency applications, to meet the needs of the above markets.

We present the newly developed GaAs On Insulator (GOI) technology and discuss the impact of the buffer oxide insulator on dc, small signal rf and large signal power performance. GOI MESFETs with record Power Added Efficiency (PAE) of 72 % at C-Band (4 Ghz) for very low drain voltage operation (3 Volts) are demonstrated. We also discuss the feasibility of the oxide for gate insulator applications, that would potentially lead to CMOS type architectures in GaAs.

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CHAPTER 1. Introduction

1.1 Overview

The rapid growth of mobile communications has spawned several emerging markets in electronics whose needs cannot be satisfied by the conventional Silicon (Si) technology. This has led to the revitalization of III-V compound semiconductor industry, particularly in the last decade. Figure 1.1 illustrates the most important markets fueled by non Si technologies.

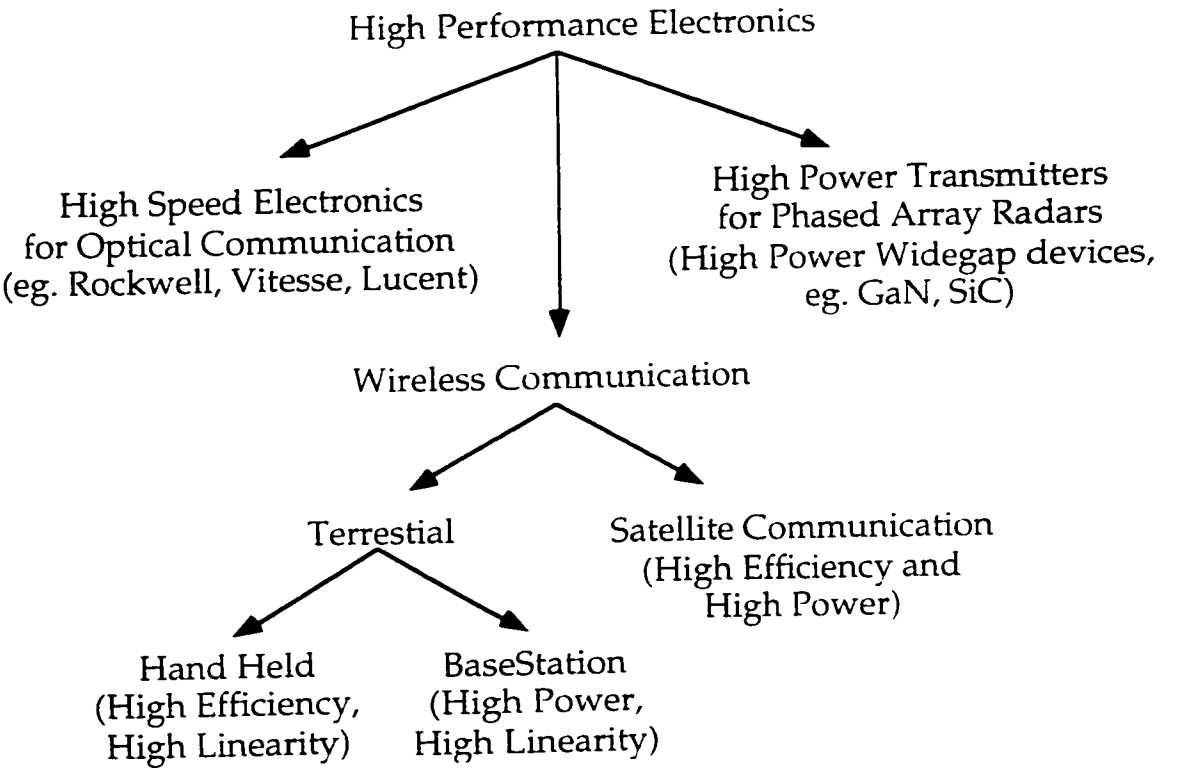

Figure 1.1 Market Segments for High Performance Electronics

The high speed optical communication networks rely heavily on the electronics backbone consisting of devices like switches,

multiplexers, drivers. The general trend here has been to go towards higher speeds, and these needs are being currently satisfied with GaAs (Gallium Arsenide) and InP (Indium Phosphide) based MESFET (Metal Semiconductor FET), HEMT (High Electron Mobility Transistor) and HBT (Heterostructure Bipolar Transistor) technologies. The high power phased array radar markets, conventionally supplied by vacuum tube technology, are looking more and more towards widegap device technologies like Silicon Carbide and Gallium Nitride. These have the immense potential of reducing system cost and increasing reliability by replacing tubes with solid state devices, while maintaining superior performance. The wireless market can be viewed as comprising of two distinct segments namely satellite and terrestrial. The widegap devices are making inroads into high power applications such as base stations and power devices in satellites. The need for high efficiency electronics on satellites cannot be overstated, as this would contribute to power savings, implying smaller and lighter power sources which directly translates to reduced launch cost. Ultra high efficiency power transmitters and signal processing are crucial for hand held devices where maximizing battery life is one of the most important requirements. Thus far, not many device technologies have addressed this issue. We propose that judicious introduction of oxides within a device structure to eliminate leakage currents will be a major step towards achieving this goal. The main goal of this thesis is to investigate the technique of wet lateral oxidation and FETs incorporating oxides for ultra high efficiency applications, to meet the needs of emerging markets discussed above.

1.2 Oxides in compound semiconductor technologies

The biggest drawback of the III-V compound semiconductor technology in comparison with Silicon has been the lack of a stable insulator like SiO_2. Leakage resulting from the absence thereof is a bottleneck in achieving high levels of integration, reliability and performance. Consider a simple FET structure shown in Figure 1.2. The gate and substrate leakage current constitute a part of the total current that is not modulated by the gate. Any such unmodulated currents contribute to lost power and must be eliminated to facilitate high efficiency electronics.

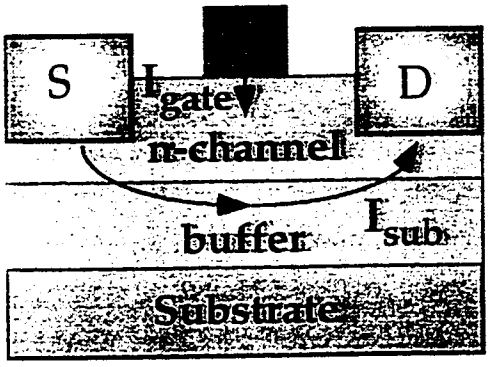

Figure 1.2 MESFET Schematic illustrating leakage current paths

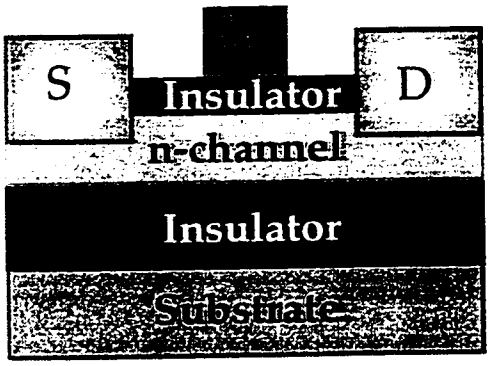

Figure 1.3 MESFET with gate and buffer insulators

A natural solution would be the use of insulating layers to block these undesirable currents, as shown in Figure 1.3. Several insulators have been tried in GaAs like native oxides [i,ii] and deposited insulators[iii,iv], and the insitu deposition of Ga_2O_3/Gd_2O_3 to achieve MOSFETs [v]. Of these, the latter seems to be most promising as a stable insulator with low interface state density.

Recently, the discovery of an oxide created by the lateral wet thermal oxidation[vi,vii] of $Al_xGa_{1-x}As$ compounds has renewed excitement in the potential of an oxide for compound semiconductors.

A typical structure is shown in Figure 1.4. Since the oxidation is lateral in nature, controlling oxidation depth, as shown in Figure 1.4 allows one to readily achieve current confinement. Furthermore it makes it possible to fabricate buried oxides. The versatility of this lateral oxidation approach enables several new attractive devices which would not be possible with traditional approaches.

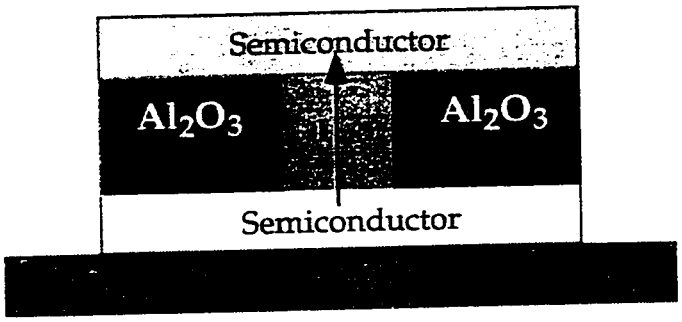

Figure 1.4 Typical oxide based device schematic

Oxides in Optoelectronics

Due to the ability to form buried oxides, lateral wet oxidation technology is finding widespread success in optoelectronics. Here, the oxide is used for optical and electrical carrier confinement resulting in record performance LASERs [viii,ix]. The oxide aperture can be used to form a dielectric lens, which can give modal control with low optical loss as shown in Figure 1.5 a. Another application is in fabricating efficient Bragg reflectors (Figure 1.5 b).

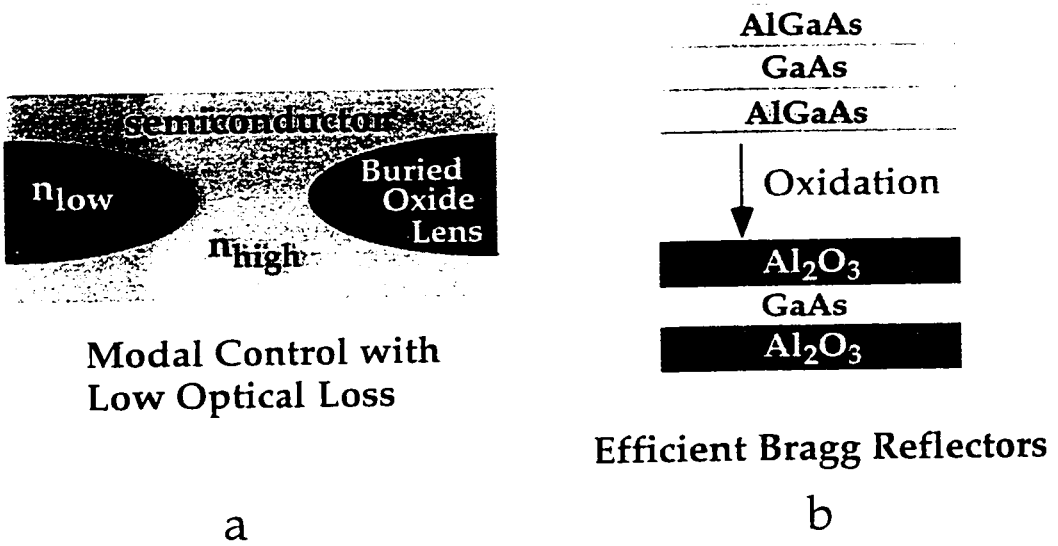

Figure 1.5 Typical applications of buried oxides in optoelectronics

Due to the high dielectric contrast of the oxide with GaAs, mirror stacks can be easily implemented, with fewer number of layers than with the traditional AlGaAs/GaAs approach (since the reflectivity per period will be greater in the Al_2O_3/GaAs than the AlGaAs/GaAs case, less periods are required to achieve the same total reflectivity).

Oxide based electronics

With the demonstrated success of the Al_2O_3 insulator in the optoelectronics arena, the natural question to ask would be whether or not these oxides could be used for electronic applications in III-V technology. Initial investigations demonstrate devices that utilize the current aperturing property of the oxide. HBTs[x] with buried Al_2O_3 have been used to reduce the extrinsic base-collector capacitance. This is achieved by converting the high dielectric constant semiconductor (ε_r=13) to the low dielectric constant oxide (ε_r=5), reducing undesirable parallel plate capacitances that are inherent in any vertical device structure. A simple schematic is shown in Figure 1.6. Resonant tunnel diodes that use the oxide aperture to tune the peak to valley ratio have recently been reported[xi]. This would be a useful feature in RTD based circuit technology where exact control of RTD peak to valley ratio and the current is difficult. Another use of the buried oxide would be for device isolation[xii]. This could be of particular use in optoelectronic circuits in GaAs and even for integration of GaAs based circuits with Si based circuits.

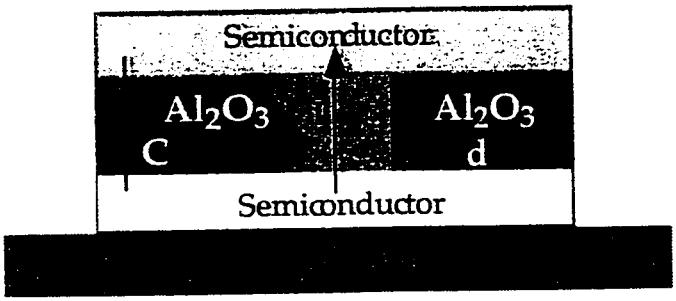

Figure 1.6. Schematic of a generic vertical device

1.3 Oxide based FET electronics

Thus far, Al_2O_3 obtained by the wet oxidation of $Al_xGa_{1-x}As$ promises to be a suitable insulator in GaAs based technology. Until now, the use of oxides has been limited to current aperturing applications. The next step is to try to complete the oxidation of the aperture shown in Figure 1.4 to have a continuous buried insulator as shown in Figure 1.3 which would eliminate undesirable leakage currents. A GaAs based MISFET with Al_2O_3 as the gate insulator has recently been reported[xiii].

As described above, wet oxidation technique makes it possible to have an oxide insulator layer buried anywhere in a FET structure. This versatility makes it possible to fabricate lateral devices with buried insulators. The main role of the oxide is to block current in the vertical direction, with the lateral current flow being the useful device current.

A variety of oxide based FET technologies are then possible with Al_2O_3 as the insulating layer. These are summarized in Figure 1.8. The oxide improves the efficiency of the FET by reducing ungated electron currents in unipolar devices by eliminating the gate and substrate leakage current.

The work in this thesis represents the first concentrated effort focused on utilizing the oxide for electronic applications. We have demonstrated GaAs On Insulator (GOI) FETs[xiv] and oxide based MISFETs[xv] for high efficiency electronics which are technologies described in detail in this thesis. The GOI technology can draw an analogy from the well established Silicon On Insulator (SOI)

technology[xvi] which is shown in Figure 1.7. The source and drain regions extend to the buried insulator and only their sides serve as junctions, yielding a considerable reduction in parasitic capacitances and leakage currents. This makes it possible to integrate denser and faster circuits in SOI than bulk Si. SOI devices lead to the reduction of short channel effects[xvii]. The leakage currents in SOI are much lower and the subthreshold slope sharper, leading to a reduction in threshold voltages, and enabling low power operation.

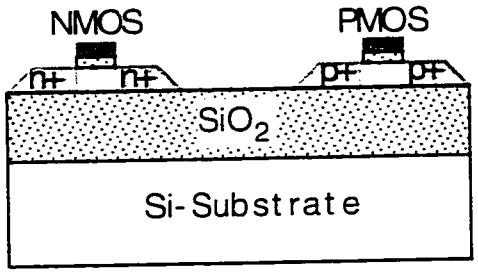

Figure 1.7 Basic Schematic of CMOS in SOI technology

As shown in Figure 1.8 though, future possibilities are very exciting. A GaAs CMOS architecture would be very attractive for high speed VLSI. Since AlAs is lattice matched to Germanium, CMOS in Ge is a possibility. This is particularly interesting due to the high hole mobility in Ge which can overcome some of the traditional problems resulting from lack of the same in today's Si CMOS. Moving to InAs, ultra low operating voltage (<0.5V) FETs can be fabricated with low gate leakage and this would be an ideal device for high speed, high efficiency, reduced battery size wireless communication needs.

Some of the above technologies are high risk requiring a stable Al_2O_3 with a clean oxide semiconductor interface. Though a detailed characterization of the oxide would be required before

successful realization of these structures, the potential rewards can be very significant.

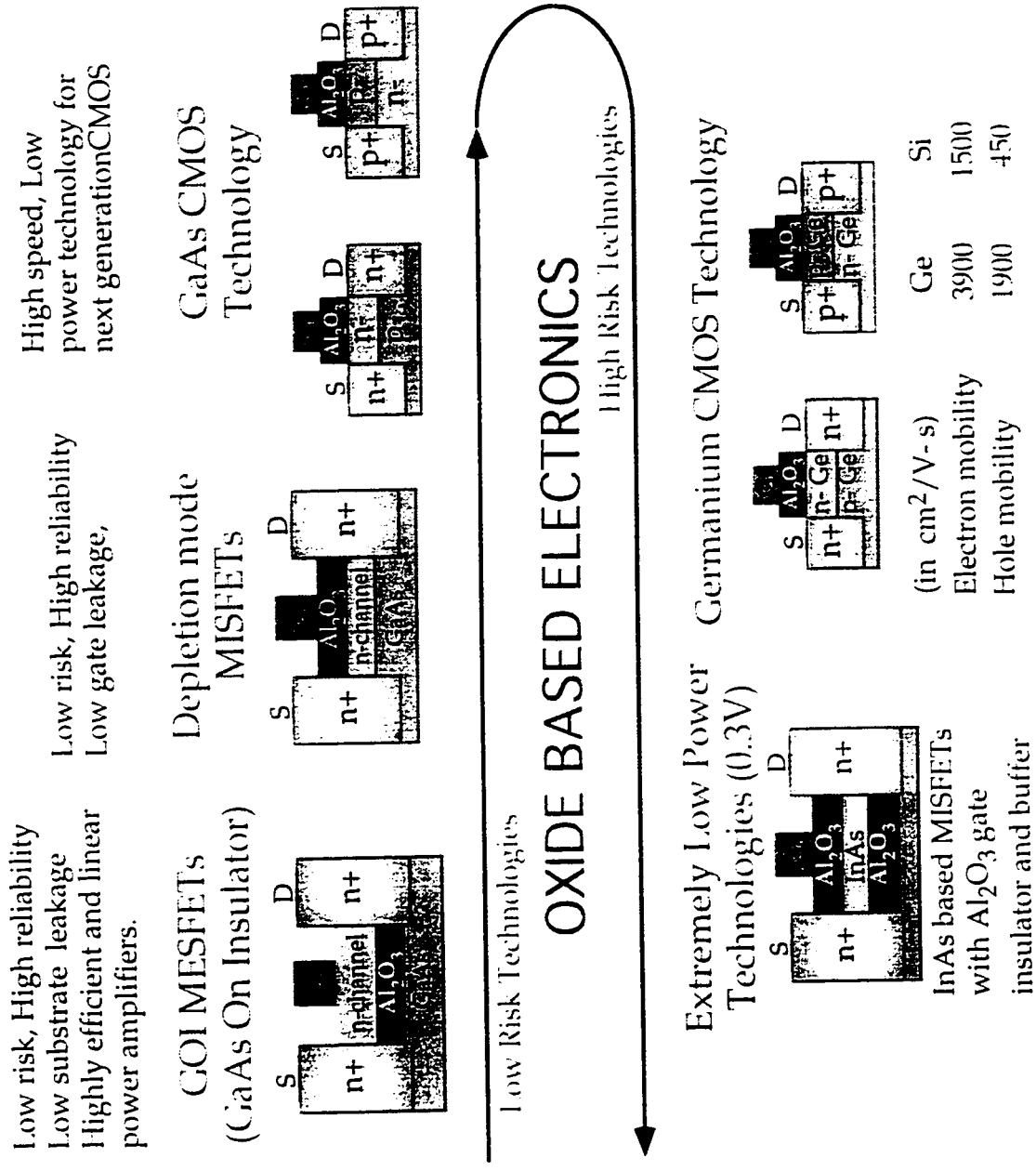

Figure 1.8 Oxide based FET electronics in III-V Technology

1.4 Synopsis

The previous few sections provided a brief overview of the application of Al_2O_3, obtained by wet oxidation of AlGaAs compounds, to electronics, mainly FETs. The major focus of this work was the GOI technology and investigating the applicability of the wet oxidation technique to gate oxides. Chapter 2 contains a detailed overview of the oxidation process : the setup, parameters effecting oxidation and the issues involved in obtaining a stable oxide with a clean interface.

The work done on gate oxides is summarized in chapter 3. First, C-V and DLTS results are presented that show that modulation of charge through the oxide barrier is possible and identifies the nature of interface states. Next, the initial oxide MISFET is demonstrated and the effect of hydrogenation in reducing state density is evaluated. Finally, MISFETs with improved I-V characteristics and the first rf results of oxide based MISFETs (obtained by wet oxidation technique) are presented.

Chapter 4 starts with the need for GOI technology, and potential applications. The impact of GOI FETs on dc and small signal rf characteristics is discussed. Initial GOI devices are shown, and the problem of charge depletion is addressed. The fabrication of the GOI MESFET is discussed in detail. The novel use of Low Temperature Grown (LTG) GaAs and AlGaAs layers in minimizing the charge depletion is presented. Finally a short section addresses the issue of GOI pHEMTs.

The fabrication and characterization of submicron GOI MESFETs is the focus of chapter 5. The impact of GOI FETs on large

signal rf performance is discussed. Complete RF characterization and load pull power, efficiency and linearity measurements are presented. Record high efficiency GOI MESFETs are reported.

Finally we summarize in chapter 6 with possibilities for the future. The requirements for further improving the GOI MESFET and developing a GOI pHEMT technology are brought out. The possibility of a CMOS technology in GaAs are also discussed.

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CHAPTER 2. Wet Oxidation : Process, Parameters, Issues.

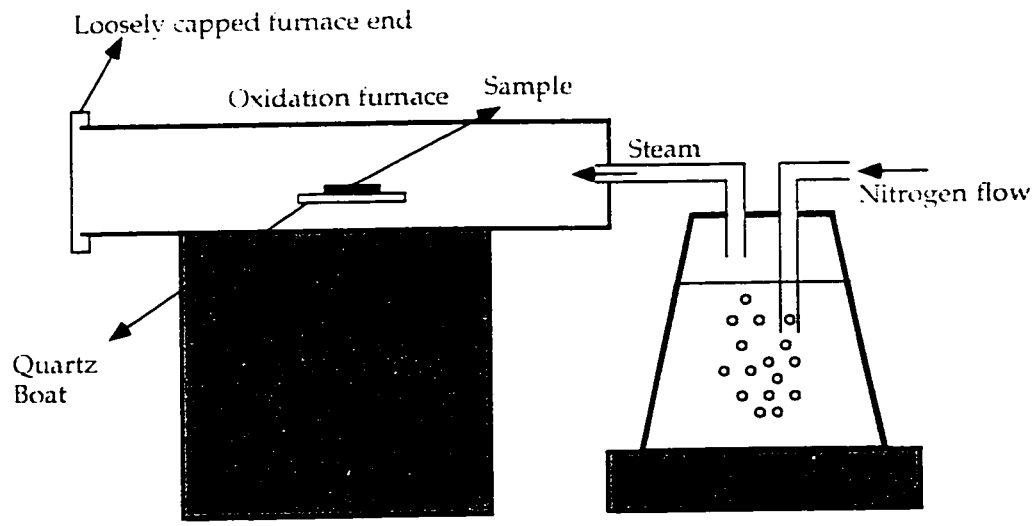
2.1 Introduction

The recently developed technique of water vapor oxidation of high Al content AlGaAs based layers to obtain a stable oxide holds great promise in obtaining device quality insulators for use in GaAs technology. Although the resulting Al-based native oxide is far from being completely characterized, it has already been used extensively because of its ability to electrically insulate, isolate and passivate AlGaAs-GaAs heterostructure devices. In the optoelectronics area, it has also been used for current/optical confinement in light emitting devices and vertical cavity surface emitting lasers. An important feature of the oxidation process is the high selective oxidation rate, which allows it to be accomplished laterally, thus preventing any undesirable exposure of the oxidation layer to atmospheric contamination. Moreover, the possibility of obtaining buried oxides opens up the way for new device structures, that utilize the insulating/current aperturing property of the oxide in various configurations within the existing device structures.

2.2 Experimental Setup for Wet Oxidation

Essentially, the experimental setup is similar to "standard" quartz-tube based furnace oxidation systems which, in this case, consists of a three zone temperature controlled oxidation furnace manufactured by Lindberg Associates. The typical range of

temperatures used for oxidation is between 400° C and 450° C. The sample is introduced into the furnace from the loosely capped end and sits on a quartz boat. The steam enters the furnace from the opposite end by means of a nitrogen carrier gas, bubbled through water maintained at 75° C to 85° C. The flow of nitrogen is controlled by a valve which allows the gas to be switched either directly to the furnace or through the water bubbler. Prior to inserting the oxidation samples into the quartz tube, the furnace is flushed with nitrogen for five minutes. The water in the bubbler is allowed to stabilize at 80° C with the nitrogen carrier gas flowing for about 30 minutes. It is after this that the samples are inserted into the quartz oxidation tube.



$$2AlAs + 3H_2O \longrightarrow Al_2O_3 + 2AsH_3$$

Figure 2.1 Oxidation Setup Schematic

The purpose of the above procedure is to ensure that the initial conditions are the same every time that a sample is introduced into

the furnace for oxidation. To begin an oxidation, the samples are introduced into the mouth of the quartz tube on a quartz boat, which is pushed gradually to the center of the furnace with a quartz rod. The temperature profile of the furnace is constant over the central 10 inches, which avoids any oxidation nonuniformities due to small errors in positioning of the boat. To terminate an oxidation, the nitrogen flow is shut off and the quartz boat is slowly pulled out of the furnace. The samples are allowed to cool down for five minutes before taking them off the boat and placing them in a sample box.

2.3 Oxidation Mechanism

The basic mechanism of the wet oxidation process is the chemical reaction between aluminum in AlAs with oxygen in steam (H_2O), to form Al_2O_3, with the liberation of AsH_3. Other volatile products such as As_2O_3 could also be involved[i]. This is a rather simplified picture of what, in reality, is a complicated process. Extensive work has been carried out to analyze the microstructure of the oxide and the reaction mechanism[ii]. The net reaction occurring can be summarized as :

$$2\ AlAs + 3\ H_2O \longrightarrow Al_2O_3 + 2\ AsH_3$$ **Equation 2.1**

Other intermediate reactions that could occur during the oxidation of AlAs are [iii] :

$$AlAs + 3H_2O \longrightarrow Al(OH)_3 + AsH_3$$ **Equation 2.2**

$$AlAs + 2H_2O \longrightarrow AlO(OH) + AsH_3$$ **Equation 2.3**

Previous studies have found that oxides resulting from steam oxidations at temperatures > 400° C were more stable than those grown under atmospheric conditions at room temperature. The

latter process is thought to be predominantly hydrolysis, forming hydroxyl groups that are unstable, whereas steam oxidation at higher temperatures behaves more like the reaction represented in Eq. 2.1. This was confirmed by the greater extent of As depletion in these samples[iii]. Furthermore, it is in agreement with the information from the Al_2O_3-H_2O phase diagrams[iv] which indicates that at high temperature (> 1100° C) a stable corundum (α) phase is formed whereas low temperature wet processes tend to favor the hydroxide phases, most commonly gibbsite. The gibbsite is also known to dehydrate to the gamma phase upon annealing from 270-500° C. Another issue that needs to be noted is that As can play a significant role in the formation of native oxides, and, as will be discussed in chapter 3, also have an important influence on the electrical characteristics of the oxides.

The microstructure of the steam grown oxides has been identified as the γ Alumina (Al_2O_3) phase[v]. There has been no intermediate hydroxyl groups observed, which would indicate that these have been converted to γ Alumina, if formed. A single molecule of AlAs, crystallizing in the zinc blende structure (lattice constant 5.66 Å) corresponds to a volume of 45.4 $Å^3$, while γ Al_2O_3 crystallizes in a spinel like structure with a cube edge of 7.9 Å, corresponding to a volume of 46.2 $Å^3$ per molecule of Al_2O_3. Therefore Eq. 2.1 would imply a shrinkage of about 50 % by volume, which corresponds to a linear shrinkage of about 20 %. This would translate to hydrostatic stresses which can be relieved by mechanisms such as formation of voids at grain boundaries or shrinkage of the layer in the growth direction. In practice, smaller

contractions have also been observed [vi,ii] which would require the layer to be porous. There has been evidence of an amorphous Al_2O_3 film near the transition region between the oxidized and unoxidized AlGaAs layer[vii], which is speculated to provide stability to the structure. The porosity argument is also supported by the observed oxidation kinetics which are found to be of the linear reaction rate limited type rather than the parabolic diffusion limited type, as is presented in the next section.

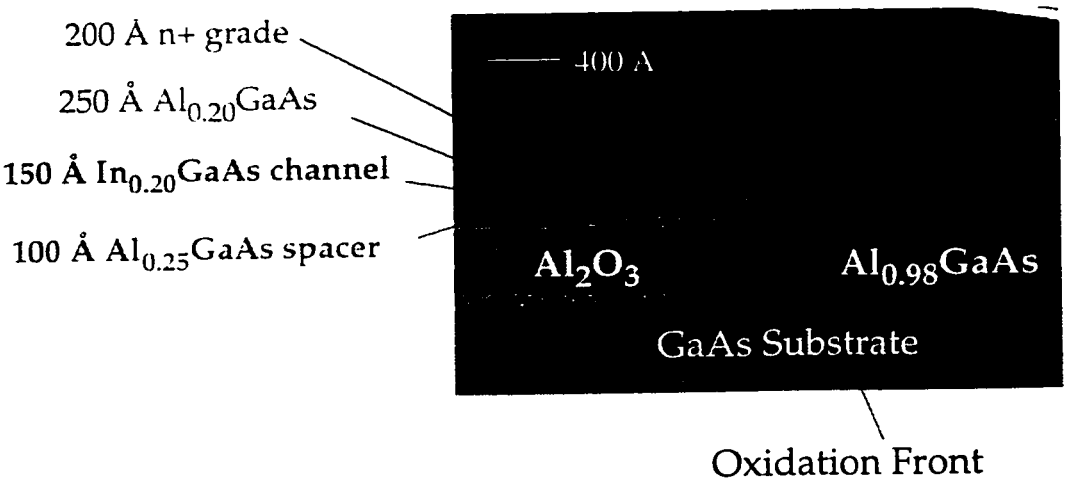


Figure 2.2. TEM micrograph of Oxidation sample

A TEM micrograph of one of our oxidation samples (AlGaAs-InGaAs-AlGaAs-$Al_{0.98}GaAs$ structure, oxidized at 450° C) done by Lijie Zhu at UCSB is shown in Figure 2.2. The oxidation front is clearly visible and the linear shrinkage from unoxidized to the oxidized region (about 15 %) is also evident. The dark regions on either side of the Al_2O_3 layer may be interfacial voids, Arsenic pile-up or simply a manifestation of the TEM imaging.

2.4 Oxidation Kinetics

For any device application, control of the extent of lateral oxidation is essential. Thus it is essential to understand and model the kinetics of the oxidation process. The dominant oxidation mechanism is the replacement of As in AlAs by O_2 from the steam. This involves, in the case of lateral oxidation, transport of O_2/H_2O in one direction from the exposed edge of the mesa to the oxidation front and the transport of As/AsH_3 in the opposite direction. To the first order, such an oxidation process can be either diffusion rate limited ($x_{ox}^2 \sim t$, parabolic thickness-time dependence) or reaction rate limited ($x_{ox} \sim t$, linear thickness-time dependence). The well known Deal and Grove's model for oxidation kinetics in Si predicts a linear oxidation law for short oxidation times and a parabolic oxidation law for longer times[viii]. Most evidence from previous studies for the wet oxidation of AlGaAs compounds suggests a linear growth rate[ix] and this is confirmed by our experiments. A diffusion limited parabolic growth rate could be observed when the oxidation extent becomes larger, but this was not observed in the regimes of oxidation depths we investigated (which were around 50 microns).

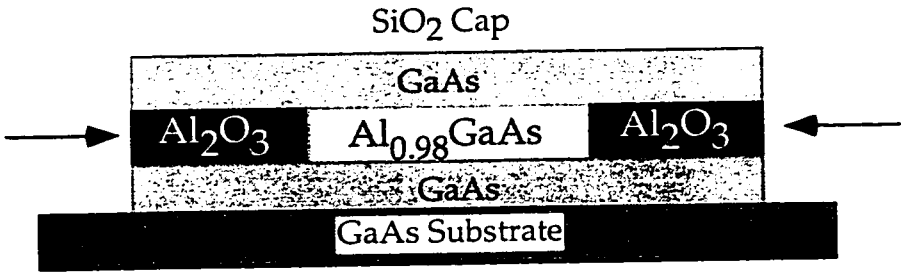


Figure 2.3 Oxidation Schematic

The layer structure used in the present study was grown by MBE and consists of 500 Å of $Al_{0.98}GaAs$ grown on a 2000 Å GaAs buffer on a S.I. GaAs substrate (see Figure 2.3). Next a 100 Å $Al_{0.3}GaAs$ spacer layer is grown, followed by a 1000 Å n-doped GaAs channel. The channel layer is capped with an $Al_{0.7}GaAs$ etch stop layer, and finally an n+ InAs/GaAs contact layer.

This is the layer structure used in one of our early GaAs On Insulator (GOI) MESFET designs, more of which will be discussed in chapter 4 and 5. The basic schematic of the structure is shown in Figure 2.3, which shows the cap, channel and the oxidation layer along with the buffer.

The fabrication procedure is relatively straightforward. 1000 Å PECVD (Plasma Enhanced Chemical Vapor Deposition) SiO_2 is deposited as a mask to prevent any undesirable oxidation occurring from top of the device. Next, the SiO_2 is patterned and Cl_2 based RIE (Reactive Ion Etching) is used to etch the mesa structure in the sample down to the substrate. The sample is then cleaned in acetone and isopropyl alcohol and given a 30 second dip in 1:10 solution of NH_4OH and H_2O. Finally, the sample is cleaved into 3 mm x 3 mm small pieces, each for a different oxidation time and temperature. For an oxidation experiment, they are loaded in the oxidation furnace following the procedure described in section 1. The oxidation times are varied from 5 minutes to 60 minutes and this is repeated at each temperature in the range from 405° C to 465° C.

The extent of lateral oxidation is easily determined under an optical microscope, since a distinct color change is observed in the layer after oxidation which is visible through the overlying semiconductor layers and the SiO_2 masking layer. This color change

is due to the change in dielectric constant upon oxidation of the $Al_{0.98}GaAs$ layer.

Figure 2.4 Top view showing the oxidized (outer, light) region and unoxidized (inner, dark) region

The top view of an oxidized sample is shown in Figure 2.4. Thus, the extent of lateral oxidation can be directly measured under an optical microscope and this procedure is repeated for different oxidation times. Note that a new sample is used for each oxidation time. The reason for this is that it is difficult to initiate oxidation in a sample once it has been subjected to oxidation and removed from the furnace. This is probably due to the formation of a denser form of oxide at the mesa edge when the sample is exposed to the non-steam furnace ambient and/or laboratory ambient upon completion of the oxidation process. Such a layer would hinder inward transport of reactants and outward transport of reaction byproducts.

Clearly, it is important to obtain a thorough understanding of the oxidation rates since they are essential in order to determine the correct oxidation depth the first time while doing an actual device (though this requirement can be relaxed by using test oxidation

samples prior to the real wafer). Figure 2.5 shows the results of this experiment.

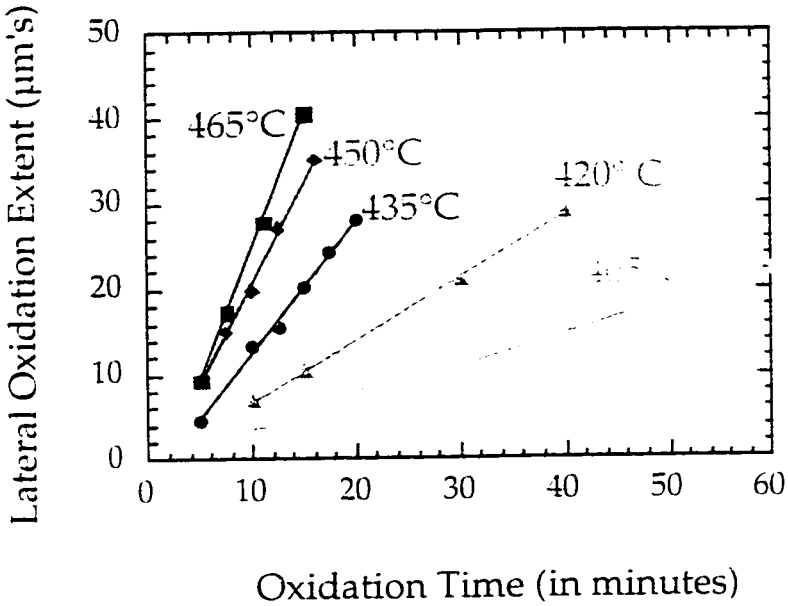


Figure 2.5 Oxidation rate characterization

Three observations are evident from this plot are :

1. At a given temperature, the oxidation is linear in time.
2. The oxidation rate is higher for higher temperature.
3. The extrapolated lines do not pass through the origin.

Whereas the second observation is to be expected, the first one clearly indicates that the oxidation proceeds via a reaction rate limited mechanism and not a diffusion limited mechanism. The latter would result in a parabolic growth law. A logical explanation, which is consistent with the reaction rate mechanism is the existence of a porous oxide, or possibly a porous interface[v]. The supply of reactants is not a limiting factor since the flow rate of the

carrier gas quite high. This has also been reported in a previous study[ix] where a study of oxidation rate vs. N_2 flow rate (i.e. water vapor supply) showed that these are independent as long as the flow rate is above 50-60 lit/hr. Observation 3 is that zero oxidation depth is not at zero time. While this may seem counter intuitive at first glance, it is reasonable for there to be an 'initiation' time. For example, the quartz boat represents a relatively large thermal mass and time is required for it to heat up with the sample and reach the internal furnace temperatures. This in itself could explain the 2-3 minutes of initiation time. Another plausible explaination for this could be a hyper linear intial oxidation process. This type of oxidation has also been observed in Si, particularly for thin oxides.

Since oxidation is a temperature activated process, one can expect that an Arrhenius plot will yield an activation energy. This can be represented by the oxidation rate R, in μm/min.,

$$R = C_o \exp(-E_a/kT) \qquad \textbf{Equation 2.4}$$

where Co is a constant, Ea is the activation energy, T is the temperature in Kelvin and k is the Boltzmann constant. Taking the natural logarithm of both sides of 2.4, gives

$$\ln R = C_o - E_a/kT \qquad \textbf{Equation 2.5}$$

From a plot of ln R vs. 1000/T, the slope will give the activation energy. Figure 2.6 shows the result of this plot, from which the activation energy is calculated to be 1.6 eV. The activation energy will in general be a function of the Al content in the $Al_xGa_{1-x}As$ oxidation layer and can be also dependent on the particular layer structure of the oxidation sample. Activation energies of 1.1 eV to 1.8 eV have been reported in literature[ix].

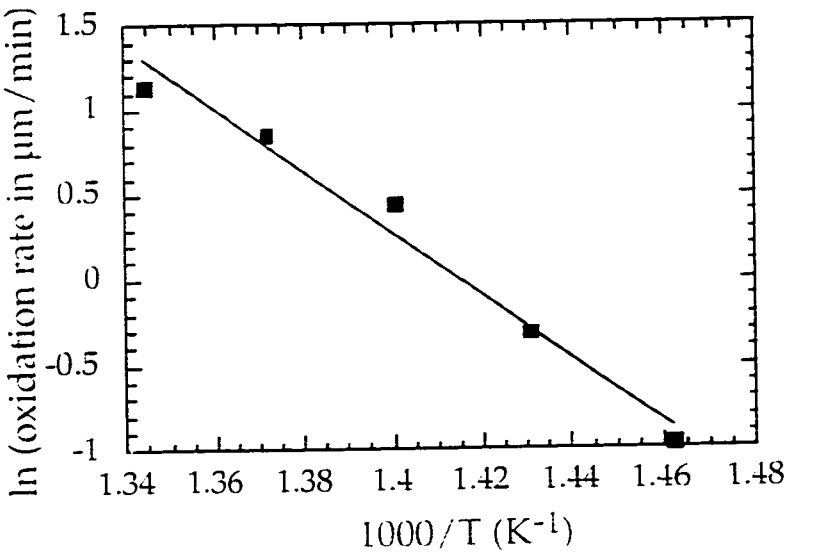


Figure 2.6 Activation energy extraction

Activation energies can be usually correlated with the chemical reactions occurring in the process. For example, they could be related to the energy required for breaking a particular bond or sustaining diffusion of a particular reactant/byproduct. For the dry thermal oxidation of AlGaAs, XPS data show a chemical shift of 1.7 eV for the Al-2p level in AlGaAs and the corresponding level in Al_2O_3 after oxidation[x]. Though no direct inference can be drawn, this can be correlated with the 1.6 eV activation energy observed in our case.

2.5 Parameters effecting oxidation

The steam oxidation is dependent on several parameters, and the most important ones are reviewed here. Understanding the effect of these parameters on the oxidation process is critical to obtaining stable oxides, and repeatable results.

Aluminum Content

The higher the Al content in $Al_xGa_{1-x}As$, the faster is the oxidation rate. The oxidation rate decreases by more than two orders of magnitude from going to $Al_{0.84}GaAs$ from AlAs[xi]. The significance of this fact is that it enables selective oxidation of high Al content layers with minimal oxidation of low Al content layers, easily. Such a process has been used to form lens shaped tapered oxide apertures in VCSELs[xii] by using compositionally graded Al_xGa_{1-x} layers. A lower oxidation, with a lower Al composition would be desirable for applications where precise control of oxidation depth is required. On the other hand, oxidation of larger lateral structures needs a faster oxidation rate, which would be easier with high Al composition layers. Most of our work has been centered around the oxidation of $Al_{0.98}GaAs$. The reason for this is that our previous work has shown that the presence of slight amounts of Ga in the $Al_xGa_{1-x}As$ results in the oxide film being much more stable to post oxidation high temperature steps such as annealing, which are frequently encountered during device processing. This has been confirmed by other researchers as well[xiii]. Sometimes even with the 2 % Ga, the oxide is affected by heat steps.

Figure 2.7 shows a MESFET which has an Al_2O_3 buffer (details about Buffer oxide MESFETs will be presented in chapters 4,5), and has been subjected to alloying at 410° C for 30 seconds. In some cases, the oxidation front is the weak spot, and subject to delamination as shown in Figure 2.8. However the samples with 2% Ga are still superior to the samples with pure AlAs.

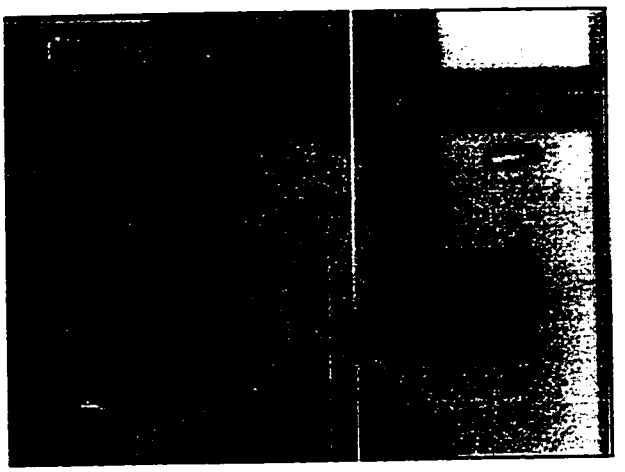


Figure 2.7. A FET structure with oxidized buffer subjected to heat treatment

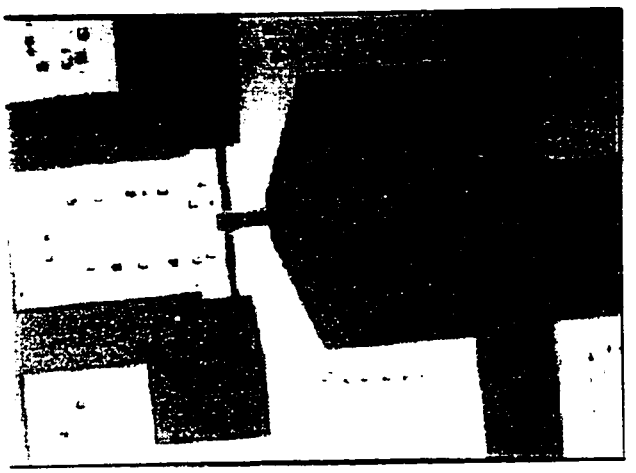


Figure 2.8 Oxide subjected to heat treatment showing a weak oxidation front

The resulting oxide is γ phase of $(Al_xGa_{1-x})_2O_3$. It is reported[xiii] that for x <= 0.98 (i.e oxidation of $Al_xGa_{1-x}As$), no evidence of strain or other extended defects is apparent, even at the oxidation front, whereas evidence of strain field is observed in the case of oxidation of AlAs. This could be related to the fact that thickness of the oxide is reduced compared to the original semiconductor layer, more so for

higher Ga compositions[i]. The reduced thickness can result in strain fields at the oxide terminus. The exact role of the addition of trace amounts of Ga is unclear, but the net result is that the stability of the oxide film is improved vastly.

Temperature

As presented in the section on oxidation kinetics, higher oxidation temperatures result in faster oxidations. The typical oxidation range for wet lateral oxidation has been restricted to approximately between 400° C and 475° C. This has been mainly dictated by the need to obtain reasonable oxidation rates based upon the dimensions of the actual devices being oxidized in typical applications which range from a few μm to about 200 μm. A very low temperature however may be restrictive inasmuch as the formation of the stable γ phase of the oxide is concerned (eg. the Al_2O_3 may not oxidize to completion), whereas a very high temperature may result in oxidation and/or damage of the adjacent semiconductor layers. Both of these issues can significantly degrade device temperature. We have found that in some cases, oxidation at lower temperatures results in slightly higher quality oxide-semiconductor interfaces, as discussed in chapter 4. Reducing the oxidation temperature by novel techniques such as the use of oxidation enhancing layers such as LTG (Low Temperature Grown) GaAs[xiv] is useful in trying to improve the interface quality.

Time

Oxidation time is in general determined by the required extent of lateral oxidation and a knowledge of oxidation rates for the given oxidation conditions. For current aperturing applications, the control of oxidation time is absolutely crucial, since over-oxidation may result in closing of the aperture. In other applications, such as GaAs On Insulator or MISFETs, where the complete layer needs to be oxidized, it might appear that overoxidation can help in densifying the oxide or removing the residual As from the oxide. However our studies have shown that overoxidation results in more damage to the adjacent semiconductor layers. This has been confirmed both by structural (TEM) and Electrical (FET) characterizations. The TEMs for the same oxidation structure presented in Figure 2.2, are shown in Figure 2.9 and Figure 2.10, but in this case after being subjected to overoxidation for 15 and 30 minutes, respectively. In this context overoxidation is defined as the extra oxidation time after the mesa is fully oxidized. As it is evident from the diagrams, the oxidation has attacked the layers above and below the original oxidation layer in the 15 minute overoxidation and further degraded these layers when overoxidized for an additional 30 minutes.

Another study reports that with continued oxidation, the oxide films crystallize from an initial amorphous state[vii]. This is often the cause for delamination between the oxide and the semiconductor. The overoxidation issue can be critical if there are devices of various sizes on the same wafer, which all need to be completely oxidized. If care is not take to properly layout these devices on the mask, the smaller devices will invariably be overoxidized when the larger ones are just oxidized. Novel use of

materials such as LTG-AlGaAs relax this requirement to a large extent, as will be discussed in chapter 4.

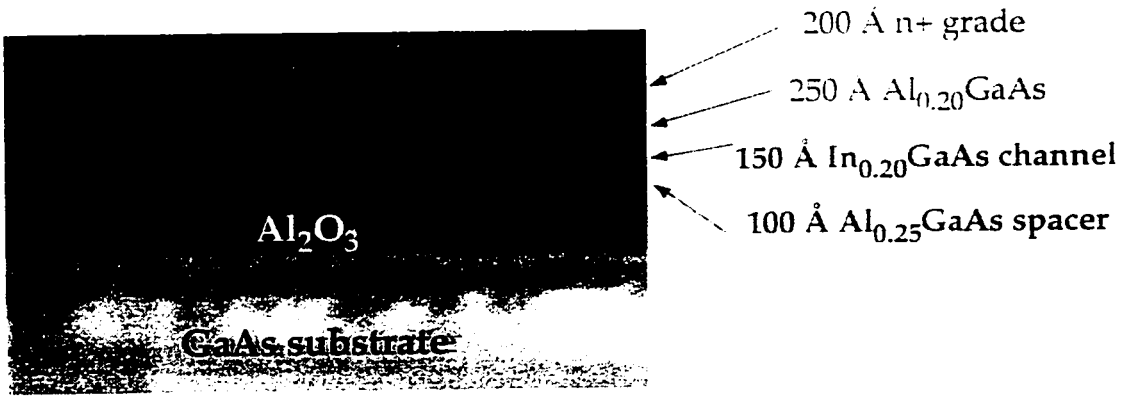


Figure 2.9 Sample overoxidized for 15 minutes

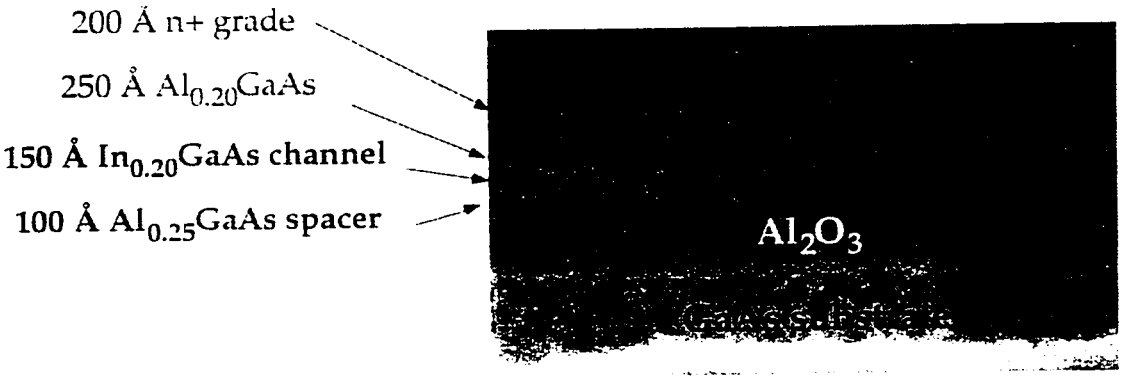


Figure 2.10. Sample overoxidized for 30 minutes

Stress

Stress could be one of the most important factors that determines the quality of the oxide and the nature of the surrounding interfaces. Since volumetric considerations discussed

earlier require a shrinkage which cannot occur completely because the oxide is constrained by the epilayers surrounding it, stresses are present in the structure. Such stresses may create defects (which will degrade the interface and affect device performance) or in extreme cases can also lead to delamination at the interface. We have found that the use of LTG-AlGaAs below the oxidation layer, helps in preserving the quality of the semiconductor layer adjacent to the oxidation layer, as manifested by the charge density in the doped semiconductor layer, which is a FET channel. Our results show that oxidizing an AlAs layer below a FET channel resulted in a charge loss of about 2-3 x $10^{12}/cm^2$ whereas the presence of a LTG layer reduced it to 5-7 x $10^{11}/cm^2$. One plausible explanation for this behavior can be related to the roughness of the LTG layer, which may result in accommodating more stress and thereby in some fashion shielding the channel layer from the effects of stress. However more experiments such as direct stress measurement will need to be carried out to confirm this.

Thickness of the AlAs layer

In general, thicker layers of AlAs oxidize faster than thinner layers. However, the effect on oxidation rate is much more pronounced at lower thicknesses. This can be understood by the fact that it would be in general easier for the reactant (H_2O) to be transported in and the byproduct (AsH_3) to be transported, out for a thicker layer. Our results show that very thin layers (around 50 Å or less) cannot be oxidized at all, which may be due to the inability to set up a transport path for the reactants and the byproducts. The implication of this fact is that device applications requiring thin

oxides, such as oxide barrier RTDs or even more simply FETs with ultrathin gate oxides, may need more novel processing techniques to facilitate the oxidation. A systematic study of these issues has been done by Naone et. al.[xv] from which Figure 2.11 is reproduced.

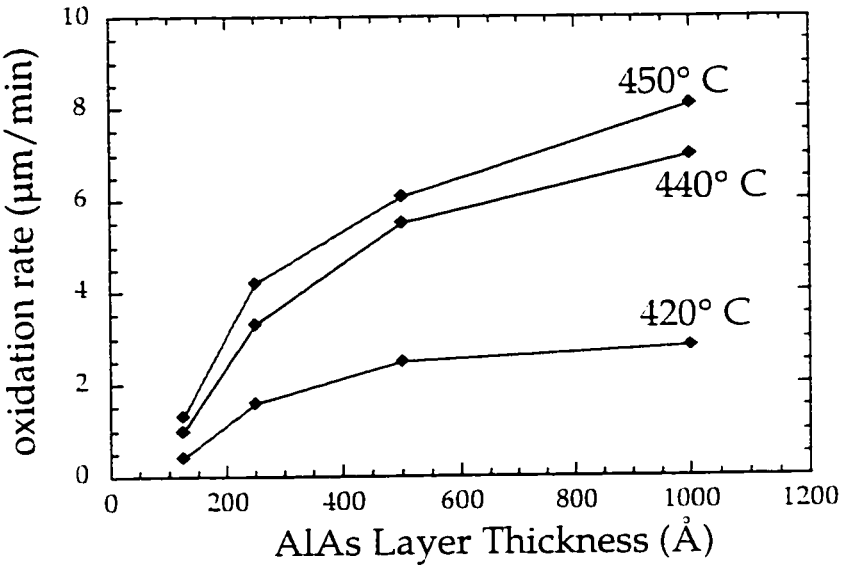


Figure 2.11 Oxidation rate as a function of AlAs layer thickness at different temperatures. (replotted from ref).

Other factors

Other factors that influence the oxidation process are the nitrogen flow rate, doping of the oxidation layer, use of different capping layers, water temperature, and oxidation from the top as opposed to laterally. The nitrogen flow needs to be sufficient so that the furnace is saturated with water vapor and thus providing a supply of water vapor which will not be one of the limiting factors in oxidation. Flow rates of greater than 1 lit/min. result in oxidation rates being independent of flow rate[ix]. P-type samples tend to oxidize more rapidly than n-type , which has been explained using the

position of fermi levels in these samples[xvi]. We have found that at water temperatures around 75-95° C, the oxidation rate remains fairly constant but drops somewhat at lower temperatures. This is due to the reduction in saturated water vapor present in the oxidizing ambient. Different capping layers such as SiO_2, Si_3N_4 or GaAs itself, can affect the oxidation process due to differences in stresses within these structures. Top oxidation can turn out to be quite a different process, although the inherent mechanism is similar to wet lateral oxidation. The limitation in this case is that it would be difficult to achieve buried oxide layers and oxide apertures. Also, there is the issue of exposing the oxidation layer to atmosphere. Some novel techniques such as insitu oxidation under ultra high vacuum conditions[xvii] appear very promising.

2.6 Oxides in other systems

Most of the work in wet oxidation has been performed on GaAs with high Al composition AlGaAs as the oxidation layer. The incomplete removal of As is a problem, and is generally viewed as being responsible for causing oxide charges and interface states. Alternative layers such as AlP, AlSb would also be viable candidates for oxidation. AlAsSb can be lattice matched to InP, opening up the way for oxide based devices in InP technology. There have been a few reports of oxidation of AlAsSb[xviii] but the problem has been the formation of metallic antimony (Sb) at the interfaces. AlSbP system would be a very interesting candidate for the oxidation layer because phosphorous (P) is in the conduction band and Sb is in the valence band in GaAs, unlike As which is at midgap. Thus, incomplete

removal of these elements may not introduce any states close to midgap and hence not have such a detrimental effect on device performance. Moreover, AlSbP can also be lattice matched to InP. Another point to note is that AlAs is also lattice matched to Germanium (Ge), and the oxidation technique can be fruitful in realizing a stable oxide on Ge. The room temperature hole mobility in Ge is 1500 cm^2/Vs, which can overcome some of the traditional problems of low performance p-channel FETs in Si CMOS and be the basis of a Ge CMOS technology. This was briefly alluded to in the preceding chapter. Finally, epitaxial oxides on Si itself are an active area of research with the constant thrust towards thinner and thinner oxides for use in sub 0.1 μm CMOS. Oxidation of AlP on Si is a viable candidate here. The wet oxidation technology is still in its nascent stage and a greater research effort is required before the possible applications mentioned above can be realized.

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CHAPTER 3. Gate Oxide Applications.

3.1 Introduction

Low gate leakage current in FETs is desirable for several applications, most notably in low-power, high-speed ICs and high reliability power amplifiers. This is because gate leakage is one of the main contributors to standby power dissipation, and also because it is a significant component of total device current that is not modulated by the gate. Any such unmodulated currents directly contribute to DC power drain and degrade device performance in high efficiency applications. Furthermore, enhancement-mode FETs with low gate leakage as required for dense low power ICs or power amplifiers operating off a single pwer supply, is extremely difficult to achieve.

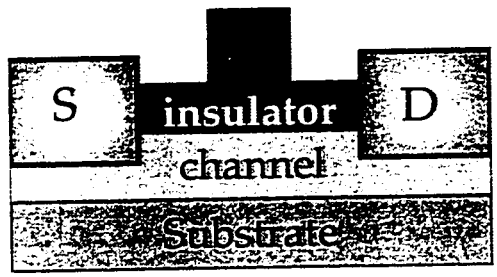


Figure 3.1 Gate Insulator in a MESFET

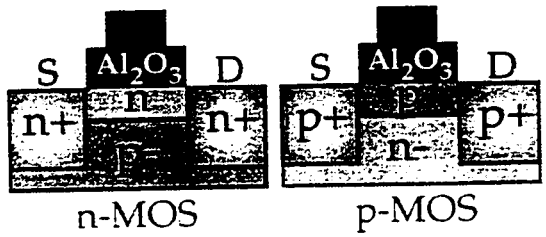


Figure 3.2 CMOS architectures in GaAs technology

An insulating gate analogous to that used in the ubiquitous silicon MOSFET could provide an ideal solution for the fabrication of high speed GaAs FETs with minimal gate leakage. However the insulator under the gate is required to have sufficiently low interface state density at the insulator/semiconductor interface. In depletion type FETs shown in Figure 3.1, the presence of interface states and oxide charges would lead to dispersion and compression in the I-V characteristics. On the other hand, enhancement type devices shown in Figure 3.2 (which are the building blocks of a CMOS technology) require the formation of an inversion channel. This would not be possible unless the interface state density is minimized and the FETs would not function at all. The requirement of a clean insulator-semiconductor interface is necessary for both types of devices, but is much more stringent for MOSFETs requiring inversion.

In the past, the development of GaAs based electronic devices has been hampered by the lack of a suitable insulating layer. It is precisely for this reason that Al_2O_3 obtained by wet oxidation of AlGaAs based compounds has been investigated as a potential candidate for forming stable insulating layers in GaAs FET based technology.

The most sensitive device structures commonly used to electrically characterize an insulator for applications in semiconductor technology are MIS capacitors and MIS FETs. This chapter presents the fabrication and characterization of both MIS capacitors and MISFETs that incorporate Al_2O_3 as the gate insulator. The C-V characterization was used to assess the quality of the oxide for enhancement mode MOSFETs. The depletion mode MISFET described later in this chapter is essentially a traditional GaAs

MESFET with an insulating oxide. This is not to be confused with the inversion channel MISFETs and MOSFETs common in Silicon technology. The issue of the origin of interface states in this system and possible techniques to minimize them are also addressed.

The work on Al_2O_3 gate oxides presented in this thesis is only an exploratory study, both for demonstrating feasibility and as a tool for characterizing the electrical parameters of the Al_2O_3 layer and the Al_2O_3/GaAs interface. To develop a gate oxide technology that would be suitable for MOS enhancement and depletion type devices, far more extensive characterization and experimentation would be required, which is beyond the scope of this thesis.

3.2 MIS Capacitors : C-V characterization

A preliminary study of the electrical properties of the oxides such as interface states, leakage current and dielectric constant was carried out using MIS capacitors. The layer structure used for fabricating the MIS capacitors is shown in Figure 3.3

200 Å n+GaAs Cap
500 Å AlAs
1000 Å p-GaAs, $2.5 \times 10^{17}/cm^3$
2000 Å p+ GaAs Buffer
p+ GaAs substrate

Figure 3.3 Epitaxial layer structure for the MIS capacitor

The GaAs cap protects the underlying AlAs layer from any undesirable oxidation from the top. The AlAs layer is converted to Al_2O_3 by lateral oxidation from the edges of the mesa. The p- GaAs layer thickness and doping are chosen so that the thickness is greater

than the maximum depletion width, W, that could be supported before inversion occurs at the Al_2O_3/p-GaAs interface (assuming that it does), which is calculated to be 780 Å from equations 3.1 and 3.2 [1]

$$W = \sqrt{2\varepsilon(2\emptyset_f - kT/q)/qN_a} \qquad \textbf{Equation 3.1}$$

where W is the depletion width at strong inversion, N_a the acceptor doping and $2\emptyset_f$ is the surface band bending at strong inversion given by, $2\emptyset_f = 2(kT/q) \ln (N_a/n_i)$, **Equation 3.2**

where n_i is the intrinsic carrier concentration.

The bottom ohmic contact is formed on the p^- GaAs layer. The substrate was chosen to be p^- type in order to simplify the fabrication process in cases where it was deemed necessary to use the backside of the wafer for ohmic contacts to the p^- GaAs. The MIS capacitor fabrication sequence is relatively straight forward. The first step is mesa definition by Cl_2 based Reactive Ion Etching (RIE) with Plasma Enhanced Chemical Vapor Deposition (PECVD) SiO_2 as a mask. Next the oxidation of the AlAs layer is carried out at 450° C in the quartz tube oxidation furnace with steam introduced into the chamber from a bubbler maintained at 85°C. The oxidation rate is about 2.5 µm/min for the 500 Å thick AlAs layer. Next, the ohmic contact to the p^- GaAs layer is formed using Ti/Au metallization to the p^- GaAs layer. The last step is the fabrication of the top contact which forms the gate of the MIS capacitor. After the lithography, first the SiO_2 cap is removed using buffered HF. Then the GaAs cap is removed prior to depositing the top contact and so the metal after the lift off process, is directly on the oxide to form the MOS capacitor. The

etch time is controlled to avoid etching beyond the cap region. The final schematic is shown in Figure 3.4.

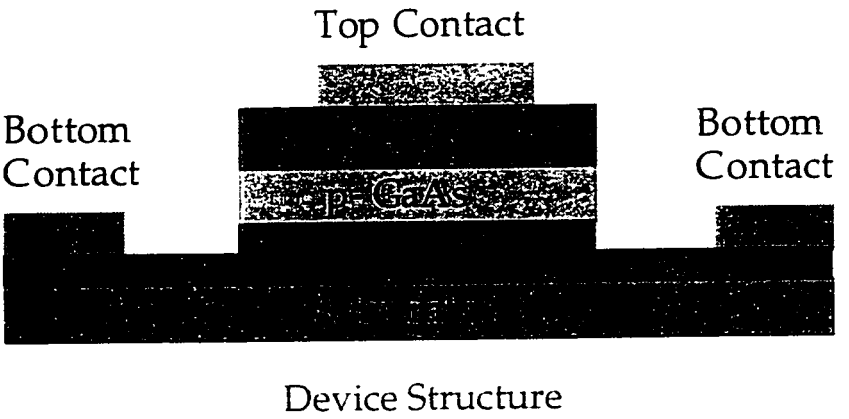


Figure 3.4 Schematic of the fabricated MIS capacitor

The high frequency C-V (HFCV) characteristic of the MOS capacitors is shown in Figure 3.5. The HFCV measurement was carried out using a Keithley 595 CV meter, at a test frequency of 1 Mhz. The tested capacitor was 6000 μm^2 in area.

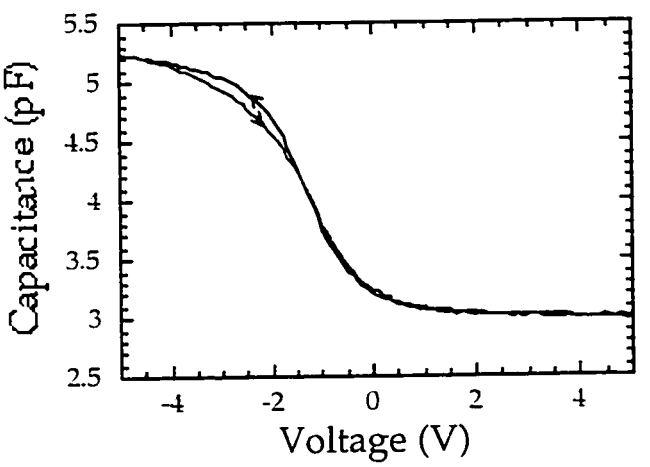


Figure 3.5 High Frequency C-V characteristics

The measured leakage current through the oxide was less than 10 pA at 5V which is in the $fA/\mu m^2$ range for the given area. The C-V curve indicates the characteristics typical of a p-type MIS structure, with accumulation at negative biases, depletion and finally what appears to be inversion at positive biases. It is difficult to ascertain precisely whether or not inversion has occurred from HFCV measurements, and so Quasi-Static measurements were attempted using the Keithley 595 Quasi Static CV meter. For this set-up, problems were encountered due to excessive leakage current, which is quite low, but still not low enough to perform quasi-static CV measurements. This is because the leakage current is comparable in magnitude to the capacitive displacement current that is measured in the quasi-static mode. The electrical permittivity of the oxide was extracted to be around 5, from the measured valued of the capacitance under accumulation conditions, which compares well with that reported by others[ii]. For a sanity check, the doping was calculated from the C-V curve to be $2x10^{17}/cm^3$ from the C_{min}/C_{max} value which is close to the expected value of $2.5x10^{17}$ $/cm^3$ from MBE growth. The voltage was swept from inversion to accumulation and accumulation to inversion and no significant hysterisis was observed.

3.3 MIS Capacitors : DLTS characterization

Deep Level Transient Spectroscopy (DLTS) is an accurate method for determining the density, capture cross section and energy level of interface and bulk states[iii]. The essence of this technique is monitoring of the charge emission/capture as

evidenced by the capacitive transient that occurs after the application of a bias pulse which fills the traps.

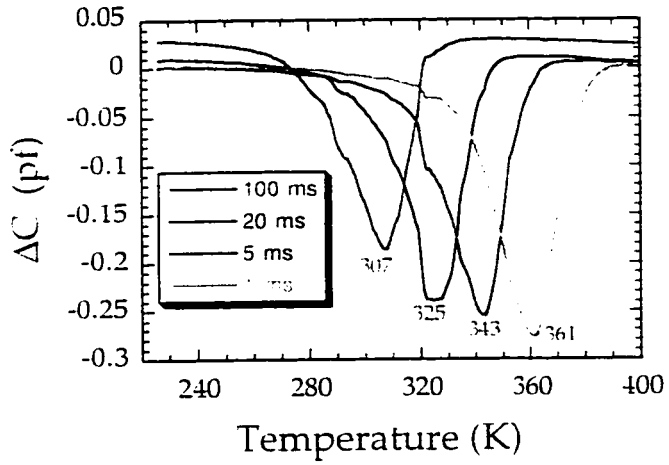


Figure 3.6 Boxcar DLTS signal for different t1 (initial delay) with t2/t1 constant

The DLTS measurements were carried out to quantitatively extract the characteristics of traps at the Al_2O_3/p-GaAs interface. The method used was Boxcar DLTS[iv] which involves the measurement of a difference signal from a capacitive transient following the application of a voltage pulse. The basic C-t transient is assumed to follow an exponential time dependence of the form

$$C = C_0\left[1 - \frac{n_T(0)}{2N_A}\exp\left(-\frac{t}{\tau_h}\right)\right] \qquad \textbf{Equation 3.3}$$

where $n_T(0)$ is the concentration of filled traps at t=0 (when the bias pulse is applied), N_A is the doping level, C_0 is the steady state capacitance (at t->∞), τ_h is the time constant of the transient which depends on temperature as

$$\tau_n = \frac{\exp[(E_t - E_v)/kT]}{\gamma_p \sigma_p T^2}$$ **Equation 3.4**

where E_t and E_v are the trap and valence band edge energies, γ_p is a constant that depends on the material, σ_p is the capture cross section, and T is the temperature. Details of the technique can be found in reference iv. A typical set of Boxcar DLTS signal is shown in Figure 3.6. The time delay t_1 is the time after the application of the bias pulse that first capacitance measurement (C_1) is done and t_2 is for the second measurement (C_2). The DLTS signal is C_1-C_2 = ΔC, which is a difference signal.

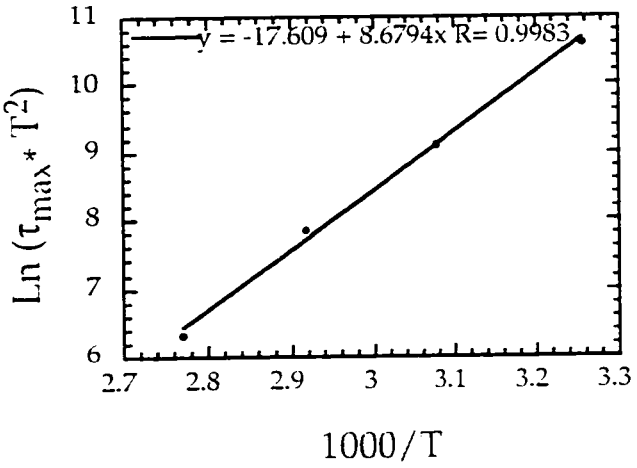


Figure 3.7 Activation energy plot for the DLTS signal

The observed DLTS signal has the characteristic signature of a single, dominant trap level and an activation energy plot (based on equation 3.4) is generated to give the energy location of the trap (Figure 3.7). The slope of the activation energy plot gives the location of the trap at 0.74 eV above the valence band, i.e. a midgap trap. From the intercept, the capture cross section is calculated to be $2x10^{-14}$ /cm^2.

From the magnitude of the DLTS difference signal (Figure 3.6) the density of interface states is calculated to be 5.5 x $10^{11}/cm^2$. The trap energy is close to the EL2 defect in bulk GaAs[v], suggesting that the origin of interface traps in this system may be related to excess Arsenic in the MIS structure. This would suggest that efficient removal of As, either by suitable oxidation conditions or subsequent treatments such as hydrogenation and/or annealing could contribute to a reduction in trap density, and result in a more ideal oxide-semiconductor interface.

3.4 GaAs MISFETs with Al_2O_3 as the gate insulator.

A MISFET is an ideal test structure for certifying the quality of a gate insulator, since the pinch-off of the FET requires that the Fermi level be able to move freely through the bandgap. Furthermore, the presence of interface states can be readily observed via g_m compression at particular gate bias voltages.

In the present study, we have fabricated GaAs MISFETs with Al_2O_3 formed by the wet oxidation of AlAs as the gate oxide, and have looked into the effect of hydrogenation in improving the device characteristics. The current level in the first GaAs MISFETs was quite low. In the second run, depletion mode GaAs MISFETs with high current level were realized, by a more controlled oxidation process.

Device Fabrication

The layer structure used to fabricate the depletion-mode MISFET is shown in Figure 3.8a. The GaAs cap is to prevent the

oxidation of AlAs in atmosphere. First, SiO_2 is deposited and patterned to open the source/drain regions (i.e. the gate mesa is defined). Then we etch down to the channel using Cl_2 based RIE (wet etch is avoided to prevent any undesirable undercutting), thereby exposing the AlAs from the side). The nominal gate mesa size is 4 μm. This is followed by the wet oxidation of AlAs (Figure 3.8 b)The steam oxidation is carried out in a single zone quartz furnace at 450°C, fed by a water bubbler maintained at 85°C. The oxidation time is around 5 minutes which is sufficient to completely convert the AlAs layer under the gate to Al_2O_3 via lateral oxidation from the edges of the mesa. The next step is Cl_2 based RIE etch down to the buffer layer (Figure 3.8 c). After this, n+ GaAs is selectively regrown by MOCVD to form the source and drain contacts (Figure 3.8 c). The SiO_2 deposited initially, serves as the mask for the selective regrowth. Next, device isolation is accomplished by mesa etching, again with Cl_2 based RIE. The SiO_2 is removed and tungsten (by sputtering) is used to define the source, drain and gate electrodes (Figure 3.8 d). The 200 Å GaAs cap is etched off just prior to depositing the gate metal, which then sits directly on the Al_2O_3 forming the MISFET. The use of a refractory metal (W) in conjunction with the MOCVD regrowth was intended to provide high temperature stable contacts.

Finally some of the devices were also subjected to a room temperature hydrogenation treatment with hydrogen ions at 400 eV for 30 minutes, with the sample was tilted to facilitate penetration of hydrogen into the gate oxide. The details of the hydrogenation system are described elsewhere[vi].

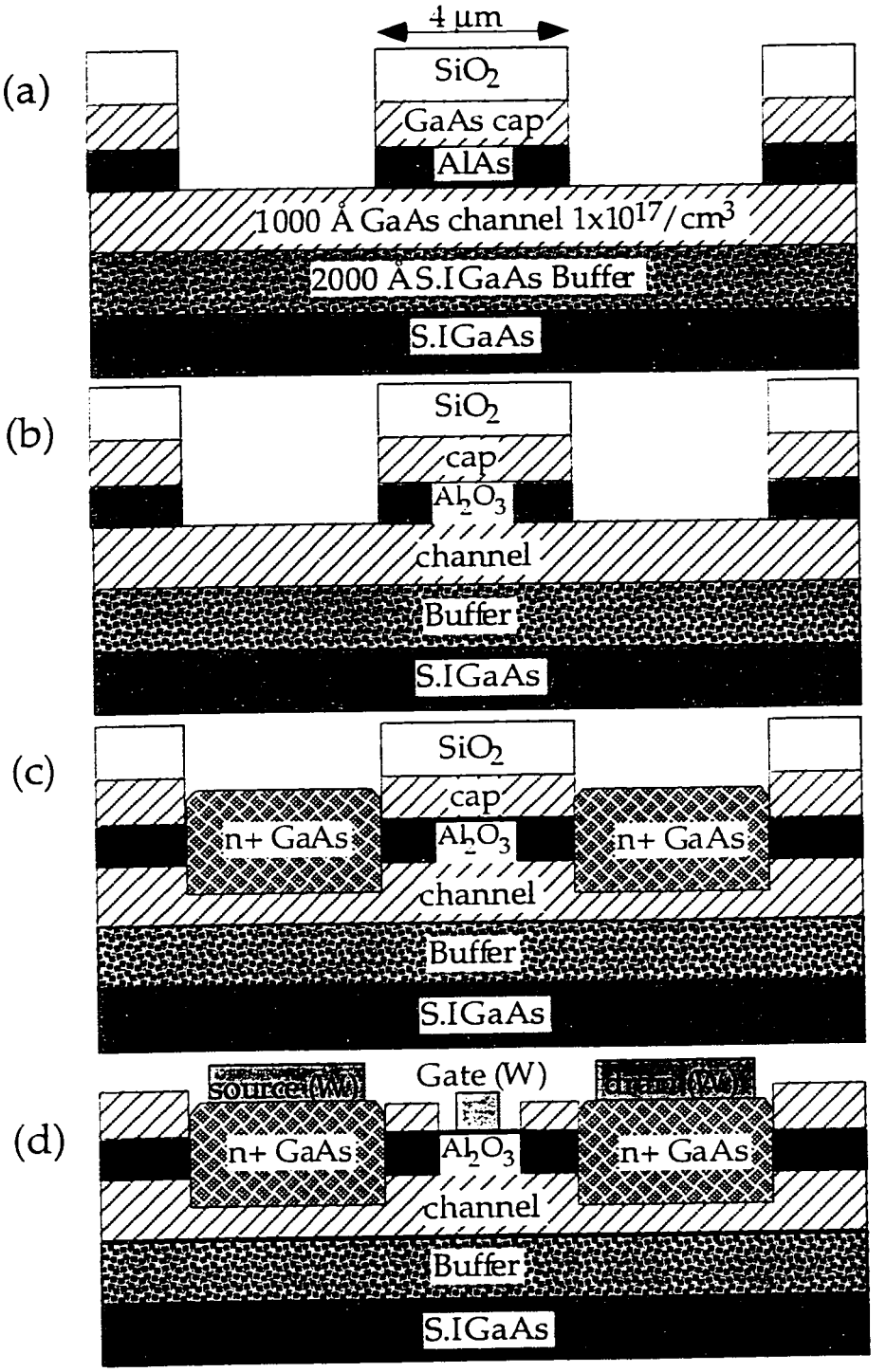
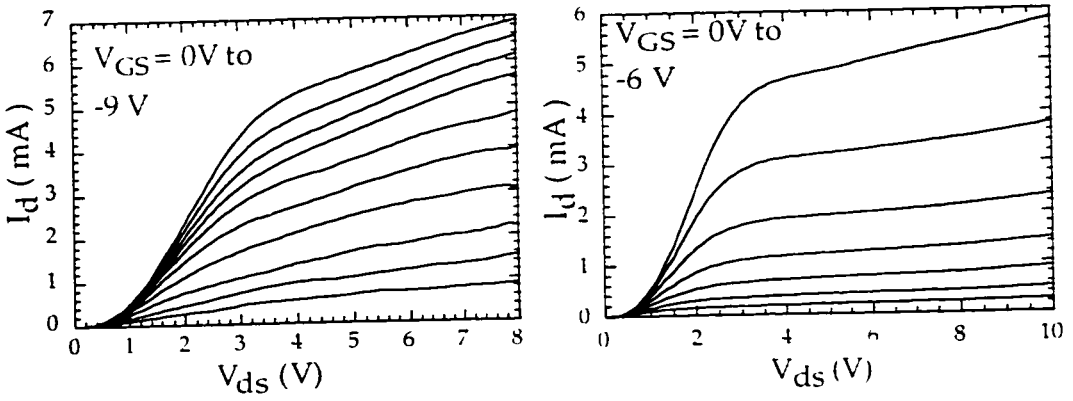


Figure 3.8 Process Flow for the Oxide MISFET

Results and discussion

The measured I-V characteristics of the MISFET are shown in Figure 3.9a. The FETs have a maximum gate current of about 50 mA/mm, and maximum transconductance g_m of about 7 mS/mm. The knee voltage is high because the source and drain contacts were not perfectly ohmic. This was due to the fact that tungsten was deposited directly on n^- GaAs, which results in a Schottky type contact. Grading the MOCVD regrowth to n^- InAs would solve this problem.

The drain current level is reduced possibly due to the damage of the active channel layers due to oxidation, or charge depletion that would occur due to interface trap charge at the oxide-semiconductor interface.



a. Before Hydrogenation b. After Hydrogenation

Figure 3.9 a,b. I-V characteristics of the Al_2O_3 MISFET before and after hydrogenation (75 μm wide device)

The modulation of charge in the FET requires that the Fermi level be able to move freely through the band gap with changes in gate bias. The presence of interface states can be readily observed via g_m compression at particular bias voltages and is evident in Figure 3.9 a, especially at higher gate biases. Figure 3.9 b shows the I-V characteristics of the FET after hydrogenation. It is clear that the g_m compression has been considerably reduced and the pinchoff characteristics have also improved. The g_m of the device after hydrogenation is enhanced and is around 15 mS/mm. This suggests that the interface state density at the oxide/GaAs interface has been reduced by hydrogenation, perhaps due the passivation of dangling bonds or due to removal of excess As. We hypothesize that the interface states in this system arise mainly due to the excess Arsenic remaining after the oxidation of AlAs. This is supported by our DLTS study of the oxide formed by wet oxidation which yielded a single dominant trap level at 0.74 eV, very close to the commonly observed As_{Ga} antisite. It has previously been shown that hydrogenation is helpful in removing any excess As as AsH_3[m]

3.5 Improved MISFETs

The main reason for reduced drain current level observed in the first batch of MISFETs could be charge depletion, and/or due to damage to the semiconductor resulting from overoxidation of the AlAs (that is oxidizing a region beyond the point when the two oxide fronts meet from the edges of the mesa). In the next batch of devices, we achieved depletion mode Al_2O_3/GaAs MISFETs with high current level of 330 mA/mm (I_{dss}), and simultaneously a high

gate-drain breakdown voltage of 30 volts. In this run, we also fabricated regular MESFETs from the same wafer which exhibited an I_{dss} of 360 mA/mm. This indicates that the charge loss after oxidation has been reduced.

This improvement has been made feasible, in part, by oxidizing at a lower temperature of 420° C (previously done at 450° C) and preventing any significant overoxidation of the device. The layer structure and fabrication process were very similar to the previous run. One main difference was the use of $Al_{0.98}GaAs$ instead of the previously used AlAs as the oxidation layer. This modification was based upon recent research findings that the oxidation of the former results in oxides that are more stable to subsequent heat treatments and do not 'peel' off upon being subjected to high temperature steps such as alloying[VIII]. The completed structure is shown in Figure 3.10

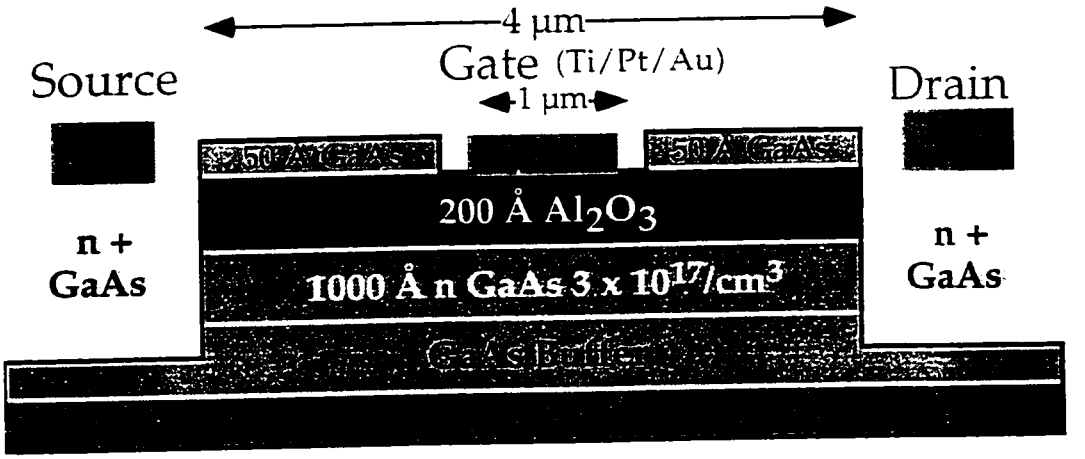


Figure 3.10 Device Schematic of the MISFET

The three-terminal DC I-V characteristics indicate that the full channel current level in the MISFET is around 330 mA/mm(Figure 3.11). The peak g_m is around 30 mS/mm which results in a relatively

high pinchoff voltage of around 28 Volts. The g_m compression observed in the I-V characteristics is due to the defect level created by excess Arsenic that is left behind in the oxide and at the interface after oxidation[ix]. The high gate-drain breakdown voltage of over 30 Volts enables the device to be pinched off.

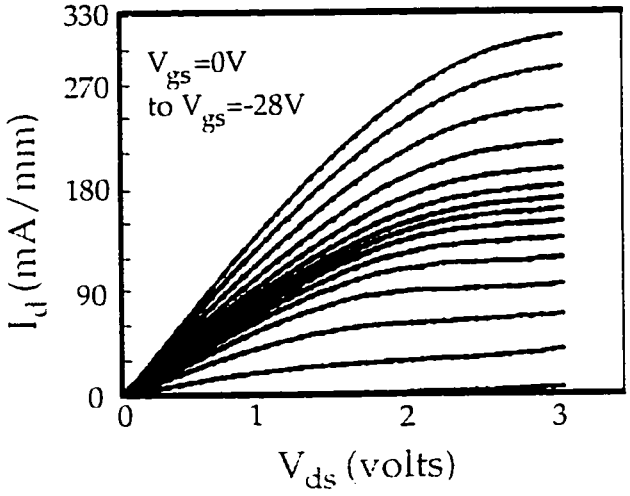


Figure 3.11 I-V characteristics of the MISFET

Figure 3.12 shows the gate diode characteristics of the device (the two curves show the same current plotted on the log scale on the right side and linear scale on the left side). As observed, the reverse leakage current at about -22 V is 50 μA/mm. The breakdown

voltage estimated from the three terminal I-V characteristics is around 30 V. In the forward direction though there is significant conduction indicating that the Al_2O_3 is not an ideal insulator. Further detailed studies on the oxidation of AlAs to form Al_2O_3 are presently underway as part of a separate research project.

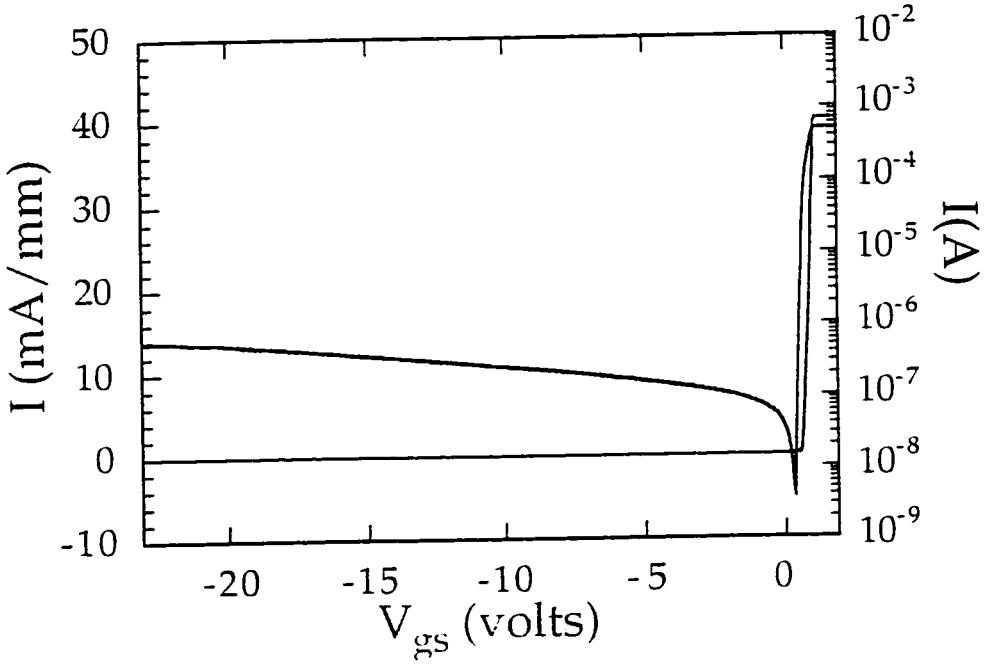


Figure 3.12 Gate Diode I-V characteristics of the MISFET

An estimation of the threshold voltage can be done from the top portion of the I-V characteristics where g_m compression is absent (hence the traps are absent). The I-V characteristics are linear rather than the square law type. This would be expected if the velocity is saturated, which is a reasonable assumption. Hence the V_t estimation is done by plotting I_{dsat} vs. V_{gs}, (intrinsic V_{gs} obtained by subtracting $I_d * r_s$ voltage drop, where the source resistance r_s is estimated from the linear part of the I-V characteristics) as shown in

Figure 3.13. The V_t is obtained to be -20 Volts. However the actual V_t is -28 Volts. To first order the 8 Volt shift can be assumed to be arising from interface trapped charge, n_t. This can be written as,

$$\Delta V = \Delta Q / C_{ox} \qquad \textbf{Equation 3.5}$$

where ΔQ is the charge density and C_{ox} is the oxide capacitance per unit area, given by,

$$C_{ox} = \varepsilon_{ox} / d_{ox} \qquad \textbf{Equation 3.6}$$

For the given sample, d_{ox} = 200 Å and n_t ($\Delta Q/q$) = 1.1 x $10^{13}/cm^2$ is charge density per unit area. This would include charges in the oxide as well those at the interface. Unfortunately hydrogenation could not be done on this sample to reduce the interface state density, as the system was not functional.

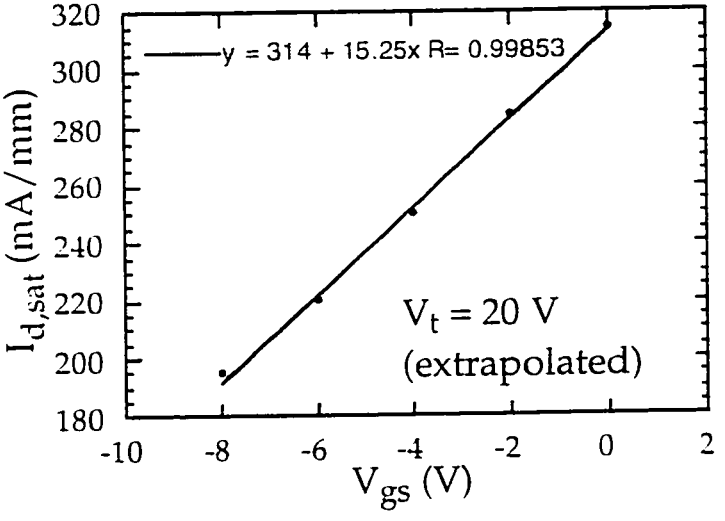


Figure 3.13 Threshold voltage estimation

The I-V characteristics of Figure 3.11 have two distinct regions, one which shows g_m compression and one which does not. To first order, we assume that all the traps are active in the region which

exhibits g_m compression and none in the other. First we calculate the intrinsic $g_{m,int}$ from the extrinsic (measured) value $g_{m,ext}$ using the source resistance r_s estimated from the I-V characteristics.

$$g_{m,int} = \frac{g_{m,ext}}{1 - g_{m,ext} r_s}$$ **Equation 3.7**

This is done for both the trap free region (g_m^{notrap}) and the for the compressed region (g_m^{trap}), giving
g_m^{notrap} = 20 mS/mm and g_m^{trap} = 5.5 mS/mm. Both are intrinsic values. Next consider the operation in the region where the traps are active, and an incremental voltage ΔV is applied to the gate. This voltage drops across the oxide (ΔV_{ox}) and the semiconductor (ΔV_s). Relating the voltage change to the field, we can write,

$$\Delta E_{ox} = \Delta V_{ox}/t_{ox} = q(\Delta n_t + \Delta n_s)/\varepsilon_{ox}$$ **Equation 3.8**

where t_{ox} is the oxide thickness and Δn_t and Δn_s are the change in the trap and channel charge respectively. For a change in current ΔI_d, the voltage drop across the channel (semiconductor), ΔV_s is simply $\Delta I_d / g_m^{notrap}$ and is calculated to be 0.5 Volts for ΔI_d = 10 mA/mm (from the region of the I-V where traps are active). Since $\Delta V = \Delta V_{ox} + \Delta V_s$, for the given ΔV of 2 Volts, ΔV_{ox} = 1.5 Volts. Also assuming a saturated velocity of 1 x 10^7 cm/s, $\Delta n_s = \Delta I_d / q v_{sat}$ = 6.5 x 10^{10}/cm^2. Using these values, from equation 3.8 we get,

Δn_t = 2 x 10^{12}/cm^2

which is a first order estimate of the interface trap density.

RF measurements

S-parameter measurements were carried out using an HP 8510 Network analyzer and the f_t and f_{max} of the depletion mode MISFET are 9 GHz and 21 GHz, respectively (Figure 3.14).

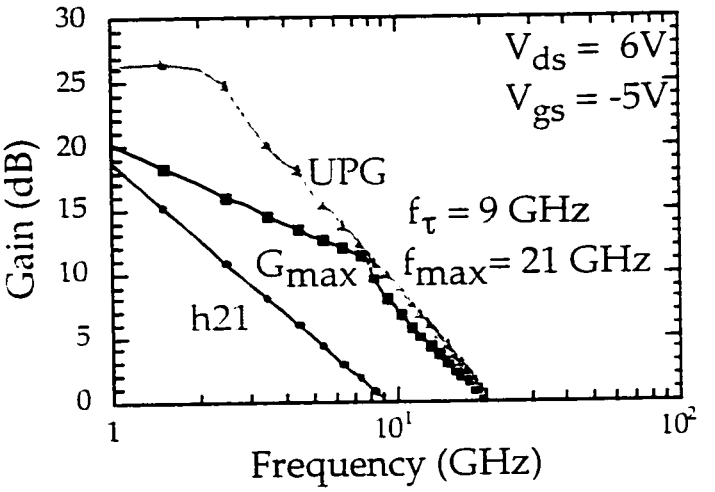


Figure 3.14 RF Characteristics of 1.1 μm x 300 μm GaAs MOSFET

These are the first reported f_t and f_{max} results on GaAs MISFETs formed by the wet oxidation of $Al_xGa_{1-x}As$ based compounds. The intrinsic f_t for a 1.2 μm GaAs FET should be around 13 GHz assuming a saturated velocity of 1 x 10^7 cm/s. Thus, these results show that the velocity in the channel is not impacted negatively by the oxidation process and proves that it is possible to have high speed devices with Al_2O_3 as the gate insulator.

3.6 Summary

In this chapter, we presented the possibilities of application of the wet oxidation technique in fabrication of gate oxide insulators. The results of the MIS capacitors from C-V and DLTS techniques are

promising, and give information about the position and density of interface states in this system. The initial MISFET experiment and the hydrogenation results gives an indication as to how to go about improving the interface properties and reducing the interface state density. The rf measurements on the improved MISFETs demonstrate the feasibility of high performance channel layers below an oxide. Most of the experiments are a clear pointer to the fact that excess As is very closely related to the quality of the oxide semiconductor interface and the insulator charge density. Efficient removal of As during or after oxidation will thus be crucial in obtaining good quality oxides, which could be used in a GaAs based Al_2O_3-CMOS technology.

The demands on insulator quality imposed by MISFET technology are far more stringent than those required for an insulating layer for GOI applications. From this point of view, this study would indicate that Al_2O_3 layer of adequate quality can be grown to satisfy the main aims of this thesis which are related to the demonstration of a high performance GaAs On Insulator (GOI) technology. The GOI technology can be compared to the well established Silicon On Insulator (SOI) technology in Si. The quality of the interface at the buried oxide could be an order of magnitude worse than the top interface[x]. Despite this the SOI devices benefit from the reduced parasitic capacitances, supression of short channel effects, low power-low threshold voltage operation and improved dielectric isolation as compared to their bulk Si counterparts[xi] and are not directly affected by the high density of states at the back interface. In the next chapter, we discuss the development of the GOI

technology and the impact of the oxide on dc and small signal rf performance.

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CHAPTER 4. GaAs On Insulator (GOI) Technology : Impact on DC/small signal RF characteristics

4.1 Introduction

With the proliferation of wireless communications, a growing market exists for efficient, linear, high-speed electronics. The fundamental requirements for transistors for communications markets are efficiency and linearity. Though these parameters are a function of material choice, device technology, circuit topology and system needs, it is highly desirable for a device to exhibit transfer or amplification characteristics that lead to maximum linearity and efficiency. Improved linear performance and efficiency at the device level, reduces the cost of amplifier design for all applications.

GaAs MESFETs and pHEMTs are extensively used in microwave analog and high-speed digital applications, albeit lacking a stable insulator.

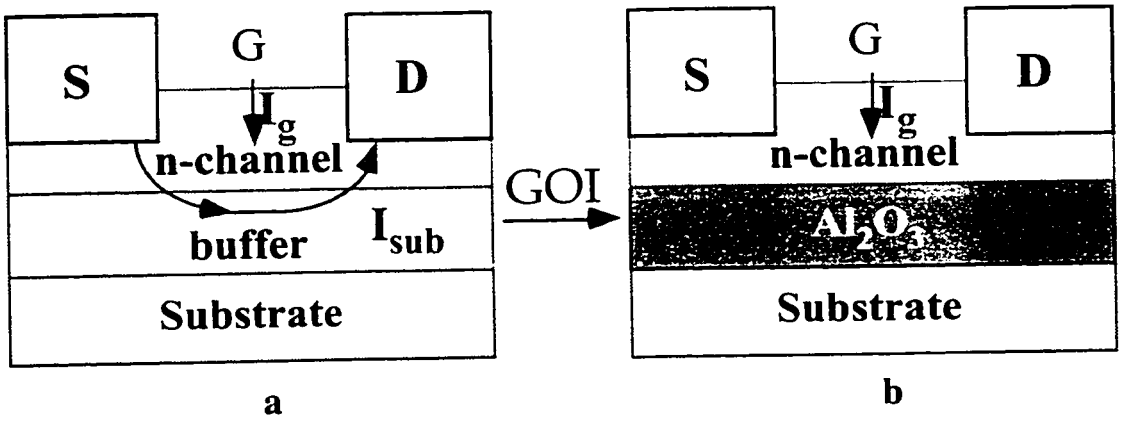


Figure 4.1 Schematic of a MESFET illustrating substrate leakage

The gate and the substrate leakage currents in a traditional device (Figure 4.1a) constitute a component of the total current that does not get modulated by the gate. Any such current leads to inefficiency and nonlinearity in the device.

Recently, advances have been made in the field of wet oxidation of $Al_xGa_{1-x}As$ to obtain Al_2O_3, which is used as an electrical insulator in both electronic and optoelectronic structures, as reviewed in the previous chapters. The GOI technology incorporates an insulating buffer layer, below the channel of the FET (Figure 4.1b). An insulating buffer in a FET results in the elimination of substrate leakage current and gives excellent charge control, making devices with high efficiency and linearity possible. The elimination of substrate leakage current also improves the output resistance of the FET. These benefits of an insulating buffer would contribute towards the development of a high performance compound-semiconductor FET technology for wireless markets.

Previous attempts to achieve an insulating buffer layer have focused on Low-Temperature-Grown (LTG) GaAs which has very high resistivity[10,11]. Since LTG-GaAs growth requires controlled Molecular Beam Epitaxy (MBE), it may not be acceptable in certain manufacturing environments. Moreover due to the large number of traps in LTG-GaAs, the 1/f noise and the corresponding phase noise performance of the devices is often compromised. We have demonstrated the use of Al_2O_3 as the buffer layer insulator in the newly developed GOI (GaAs On Insulator Technology) technology, which is suitable for both MBE and MOCVD environments.

For any new technology to be accepted by mainstream industry, it has to:

1. **Leverage existing fabrication technology,**
2. **Have minimum impact in cost, and**
3. **Provide superior performance.**

The GOI technology offers all of the above advantages:

1. The only difference between the GOI FET technology and current state of the art MESFET technology is the presence of an oxide insulator. The baseline FET can be completely identical to current industry devices.
2. There are no additional mask steps and the oxide itself is also compatible with existing processing technology, thus adding very little cost to the process.
3. The GOI devices provide increased efficiency and linearity over current structures.

4.2 GOI Fabrication and Initial Results

The first devices that were fabricated with the GOI technology were GOI MESFETs. The epi-structure is shown in Figure 4.2.

n+ grade to InAs
30 Å $Al_{0.7}$GaAs etch stop
1000 Å GaAs channel $3x10^{17}/cm^3$
100 Å $Al_{0.3}$GaAs spacer
500 Å AlAs
2000 Å Buffer
S.I GaAs

Figure 4.2 GOI MESFET layer structure

First a conventional GaAs buffer is grown. Next the 500 Å AlAs layer (which after oxidation will become the insulating buffer) is grown, followed by 100 Å $Al_{0.3}Ga_{0.7}As$ spacer. This is intended to prevent the GaAs channel from being affected by the relatively harsh oxidation environment. This is followed by a 1000 Å GaAs channel and a 30 Å $Al_{0.7}Ga_{0.3}As$ etch stop. The AlGaAs is graded to n^+ InAs to enable ohmic contacts[111]. The oxidation layer in this structure is AlAs. It was found later that using $Al_{0.98}Ga_{0.02}As$ instead of AlAs as the oxidation layer renders the final oxide more stable to high temperature processing steps such as alloying, as presented in chapter 2. Hence all our subsequent structures incorporated the $Al_{0.98}Ga_{0.02}As$ as the oxidation layer.

The GOI process flow is shown in Figure 4.3. First, a 2000 Å SiO_2 mask is deposited by PECVD and patterned using $SF_6/Ar/O_2$ based RIE. Next the device mesa isolation is performed using Cl_2 RIE (fig 4.2a). This exposes the AlAs layer from the side. The next step is the lateral wet oxidation of the AlAs in steam (fig 4.2b). The temperature of the furnace is 450° C. The steam is introduced into the furnace by bubbling nitrogen through DI water maintained at 85° C. The SiO_2 cap deposited initially, protects the surface of the active areas of the device from being affected by the oxidation process. At this step the AlAs is converted to Al_2O_3. It has been shown that the resulting oxide is Al_2O_3 in the γ phase, as discussed in chapter 2. Figure 4.4 shows the top view of the device after oxidation, in which

the oxidized and unoxidized areas are clearly visible. This is because the difference in refractive index of the oxide and the semiconductor layers results in distinct colors.

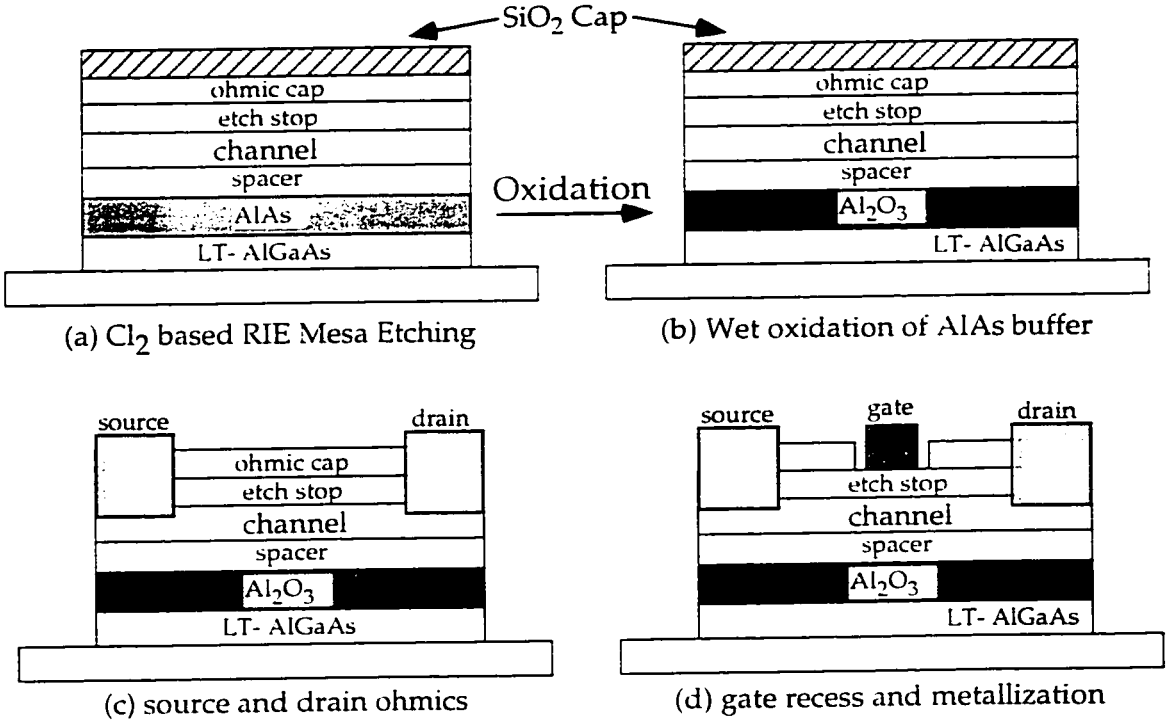


Figure 4.3. GOI Process Schematic

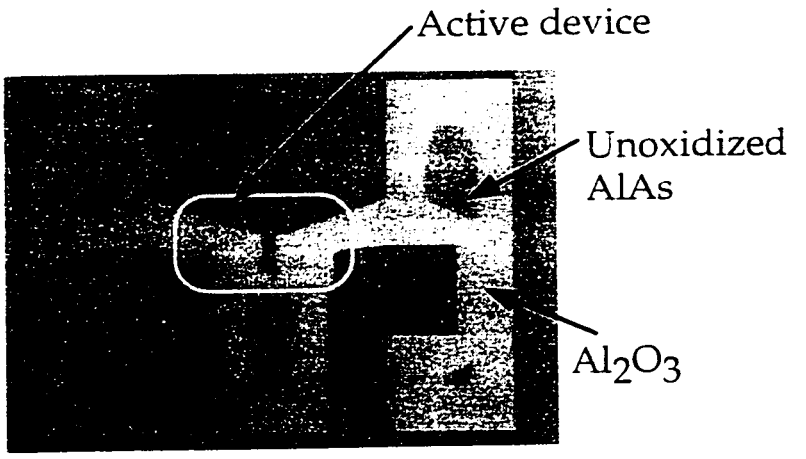


Figure 4.4. GOI MESFET top view after mesa isolation and oxidation

The processing thereafter, is similar to that of a conventional FET. Next the SiO_2 is removed in $SF_6/Ar/O_2$ based RIE and standard AuGe/Ni/Au metallization scheme is used to define the source and drain ohmic contacts (Figure 4.3c). The contacts are sintered at 370° C for 30 seconds. The oxide is stable during this step. After this, gate lithography is done and the n^+ ohmic cap is selectively etched away in a citric acid based etchant. Ti/Pt/Au, defined by lift-off, is used for the gate Schottky contact to complete the GOI MESFET (Figure 4.3d).

The DC three terminal I-V characteristics are shown in Figure 4.5. The channel current I_{dss} at V_{gs}=0 volts is 60 mA/mm and the peak g_m is 100 mS/mm.

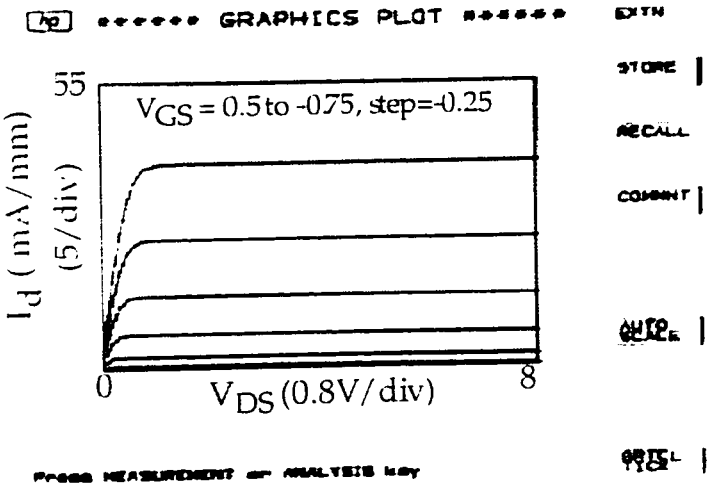


Figure 4.5 DC I-V Characteristics of the first GOI MESFET

The current level in the control device where the AlAs buffer was not oxidized was higher by about 250 mA/mm. This reduction of the current level by about 250 mA/mm in the oxidized device is due to the back depletion of charge caused by defects at the insulator/channel interface. Despite the lower current levels, the almost textbook like I-V characteristics with negligible output conductance illustrate the benefit of the insulating buffer layer.

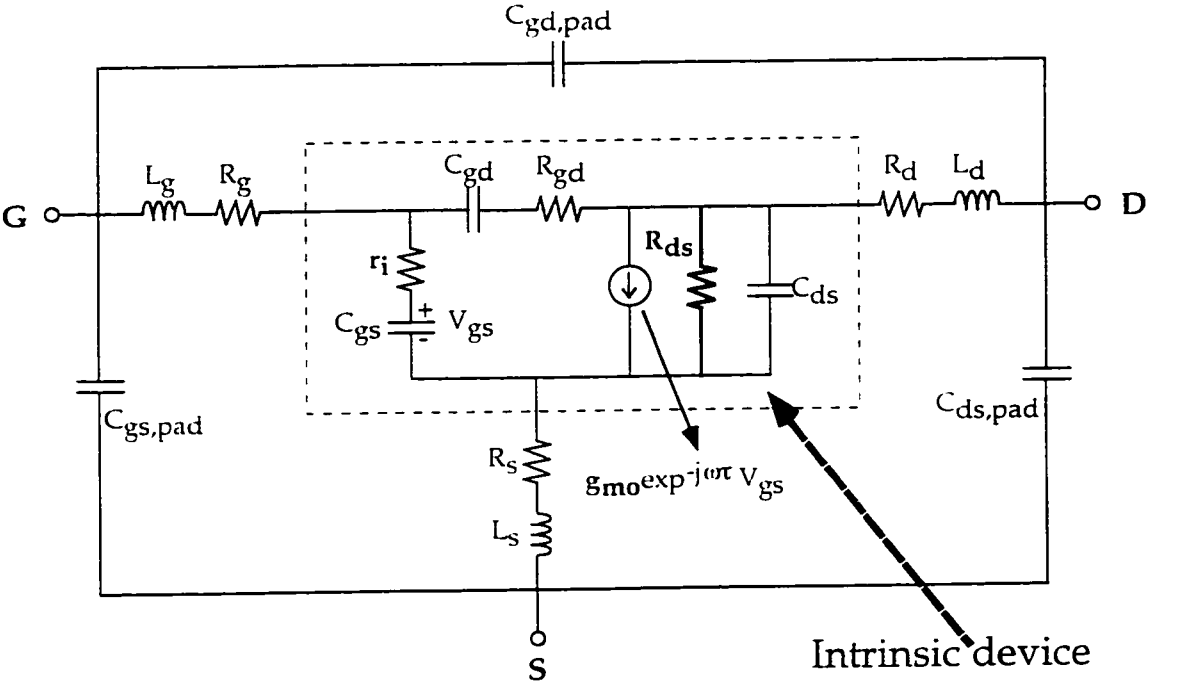


Figure 4.6 Generic FET equivalent circuit model with the intrinsic and extrinsic model elements.

S-parameter measurements (done with a HP-8510 B Network Analyzer) yielded short circuit current gain cutoff frequency f_t and the maximum frequency of oscillation f_{max} of 2 GHz and 9 GHz

respectively. An equivalent circuit model (Figure 4.6) using an accepted topology for the intrinsic and extrinsic elements of a FET was extracted from the S-parameter measurements[iv]. The f_t value is low because of the reduced current level translating to increased effects of parasitics in the structure. The channel resistance r_i is 4.5 Ω-mm. The rf output resistance R_{ds} was determined to be 330 Ω-mm from the circuit extraction.

To increase the current level of the MESFET, either the back depletion has to be reduced by lowering the state density at the oxide/semiconductor interface or the channel charge has to be increased to compensate for the depleted charge. The former is the desired long term solution and is being currently developed (J. Champlain) using innovative gettering effects of LTG grown materials as briefly discussed in section 4.4.

The latter approach is more expedient and was employed to demonstrate the feasibility of the technology. The channel thickness was increased to 2000 Å to double the channel charge. The DC characteristics of this second GOI MESFET are shown in Figure 4.7. Now the current level is 300 mA/mm at a maximum g_m of 185 mS/mm. The g_m is high over a large range of gate bias voltages, implying good charge control for the GOI MESFET, as shown in Figure 4.8. The reason for the two peaks in the g_m curve is presently unclear.

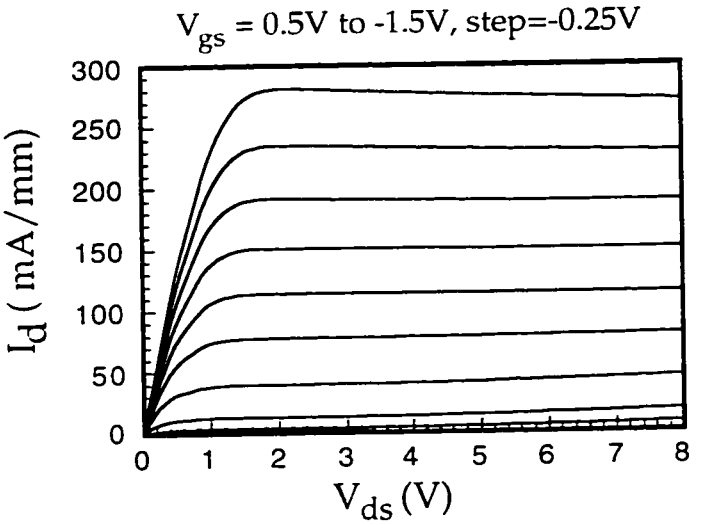


Figure 4.7 DC I-V Characteristic of the improved GOI MESFET

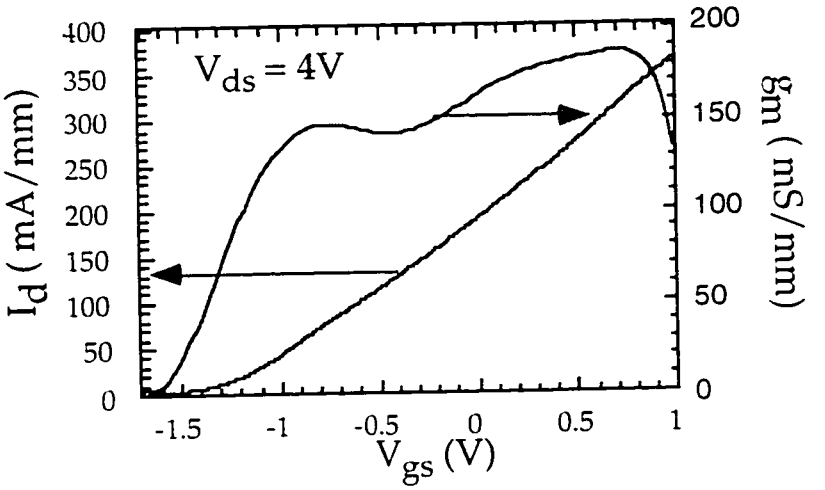


Figure 4.8 Transconductance of the improved GOI MESFET

Again, the equivalent circuit model is extracted from the S-parameter data. The f_t of the second GOI MESFET is increased to 9 GHz and the f_{max} is 45 GHz (Figure 4.9, V_{ds}=3V, V_{gs}=0V). This is attributed to minimizing the effect of parasitics due to the increased

current level over the previous device. The bump in the calculated UPG curve is due to uncertainty in measuring S_{12}, arising from possible calibration problems. This is close to the intrinsic value for a 1.5 μm gatelength GaAs MESFET (10.5 GHz assuming a velocity of 10^7 cm/s). This proves that there is no adverse impact on the electron velocity in transport layers above the oxide, an important feature for the success of the GOI technology. The channel resistance r is now 1.3 -mm and the output resistance of the GOI MESFET remains high at 320 -mm, giving the high f_{max}/f_τ ratio. Note that this is the rf output conductance, the dc I-V characteristics exhibit negligible output conductance, if any.

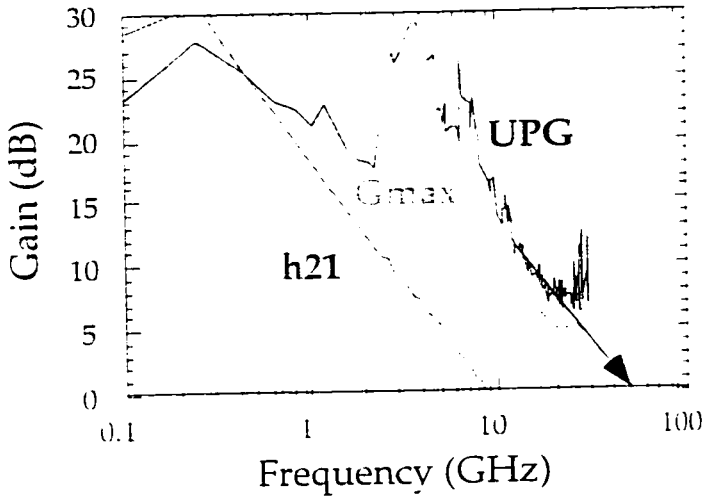


Figure 4.9 rf characteristics of the improved GOI MESFET

The rf performance of the device as a function of bias is shown in Figure 4.10 and Figure 4.11. Below the knee voltage of the FET, which is around 1.5 V, both f_τ and f_{max} drop rapidly due to the

decrease in gain. The f_τ peaks at around 2V and decreases gradually after that with increasing drain bias.

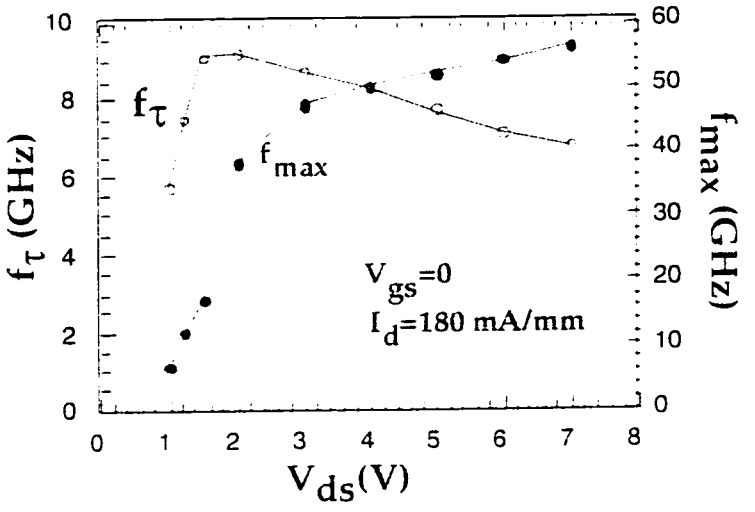


Figure 4.10 f_τ, f_{max} of the improved GOI MESFET as a function of V_{ds}

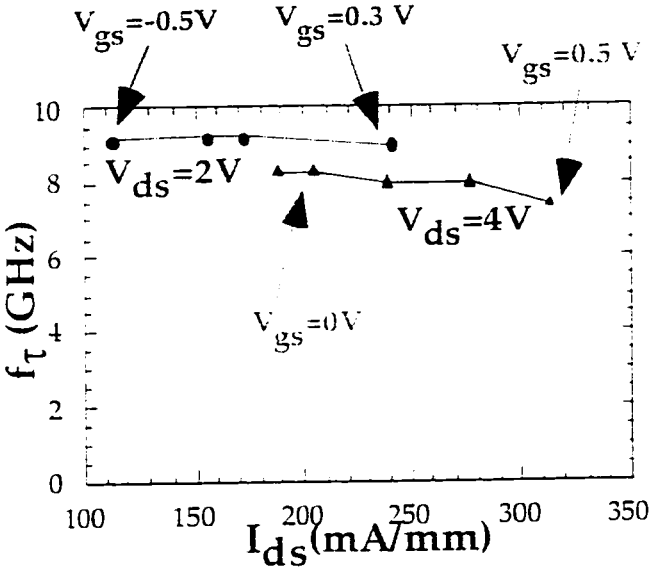


Figure 4.11 f_t of the improved GOI MESFET as a function of I_{ds}

These are general trends that are observed in most traditional FETs. The high f_{max}/f_τ ratio indicates a high output resistance in these devices. This can be attributed to two factors. The first is the increase

in the gate to drain depletion region which introduces an additional delay for the transport of the carriers from the drain edge of the gate to the drain contact. The second is the decrease in electron velocity due to heating (thermal) as a higher dc power is applied. The f_{max} continues to rise gradually as the feedback capacitance, C_{gd} decreases with increasing reverse bias on the gate to drain diode, as the drain voltage is increased.

4.3 Charge depletion issues in the GOI MESFET

The initial experiments helped prove the viability of the GOI technology. To take this technology one step ahead and make state of the art, high performance devices would require to take a closer look at the problem of loss of charge after oxidation. The major reason for charge depletion in the GOI FETs is thought to be back depletion of charge from the oxide-semiconductor interface as shown in Figure 4.12.

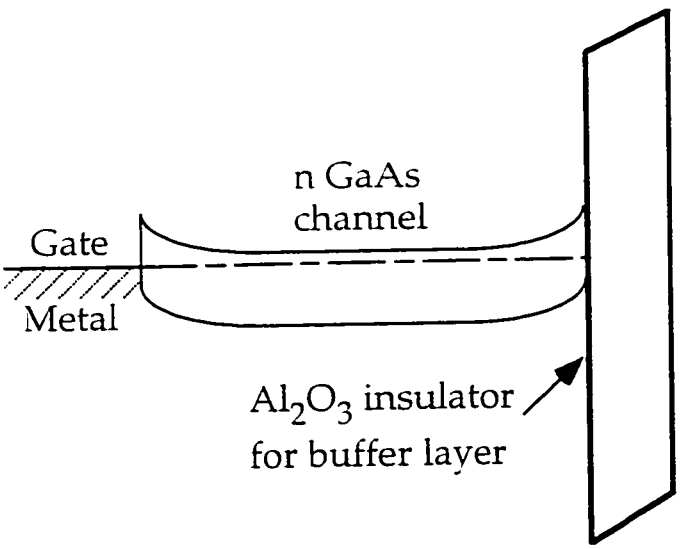


Figure 4.12 Band diagram of the GOI MESFET illustrating back depletion

We need to ascertain how the electronic properties of the FET channel overlying the oxidation layer are affected as shown in Figure 4.13, inasmuch as the mobility and the sheet charge density are concerned.

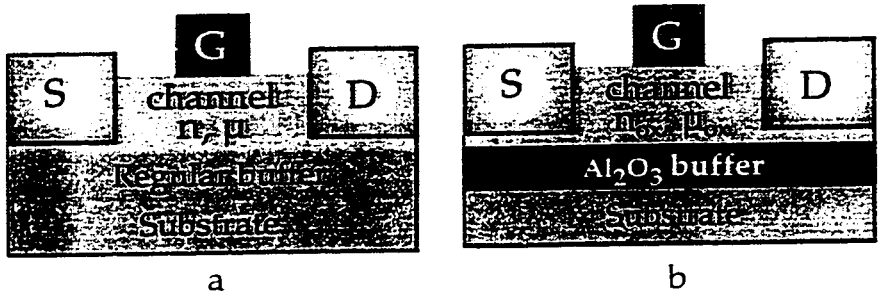


Figure 4.13 Schematic of a MESFET before and after oxidation

Hall measurements of the sample pre and post oxidation would be an ideal experiment. The conventional Hall pattern is a Van der pauw type structure with the center active area about 1-2 mm in diameter as shown in Figure 4.14 a.

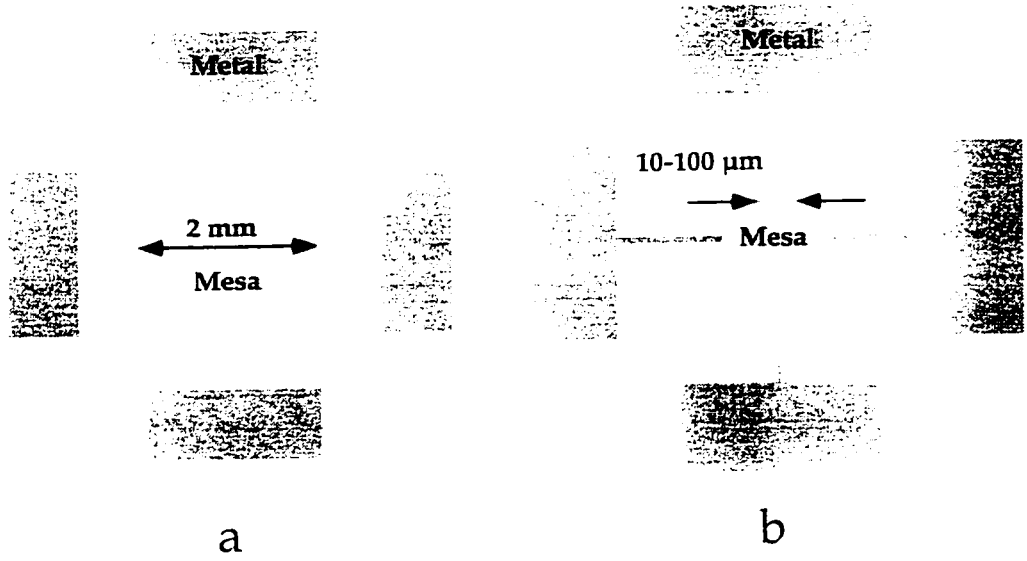


Figure 4.14. Schematic of the top view of a: conventional Hall mask and b: the designed hall mask with small active areas.

We have observed that though the oxidation rate is initially linear, it tends to saturate after a lateral oxidation depth of about 60-70 microns. Furthermore it is very difficult to oxidize laterally more than about 100 microns. This necessitated us to design a new hall mask with smaller active areas ranging from 10 μm^2 to 100 μm^2 as shown in Figure 4.14 b. One concern was the accuracy of the hall signal from such a small active area. However, when we compared the hall data from the same wafer using both the masks, it was found to be very close. Hence the new hall mask can be used to compare data from oxidized and unoxidized samples.

For the GOI devices described so far, we found the charge loss after oxidation to be around 300-400 mA/mm in various samples. As said earlier, this is due to back depletion of charge from the oxide-semiconductor interface. Our studies on gate oxides suggest that excess As is partly responsible for the creation of interface states, hence efficient removal of As could be very important in minimizing the charge depletion.

The experiment we tried was to investigate the effect of various buffer layers below the oxidation layer. Initial experiments at UCSB demonstrated that a Low Temperature Grown (LTG) GaAs layer below the oxidation layer results in increased oxidation rates[v]. This led us to believe that the LTG layer could be playing a significant role in the oxidation mechanism itself. The basic structure of the samples investigated is shown in Figure 4.15. We had four samples, each with a different buffer layer[1]. The variations were in the buffer layer being LTG GaAs or LTG AlGaAs (with 30 %

[1] The samples were grown by James Ibettson on MBE system # 2 at UCSB and this experiment was done jointly with James

Al) and the annealing temperature (after growth at 240° C) of this low temperature layer, which were as follows.

Sample 1 : LTG GaAs, annealed @ 700° C

Sample 2 : LTG GaAs, annealed @ 500° C

Sample 3 : LTG AlGaAs, annealed @ 700° C

Sample 4 : LTG AlGaAs, annealed @ 500° C

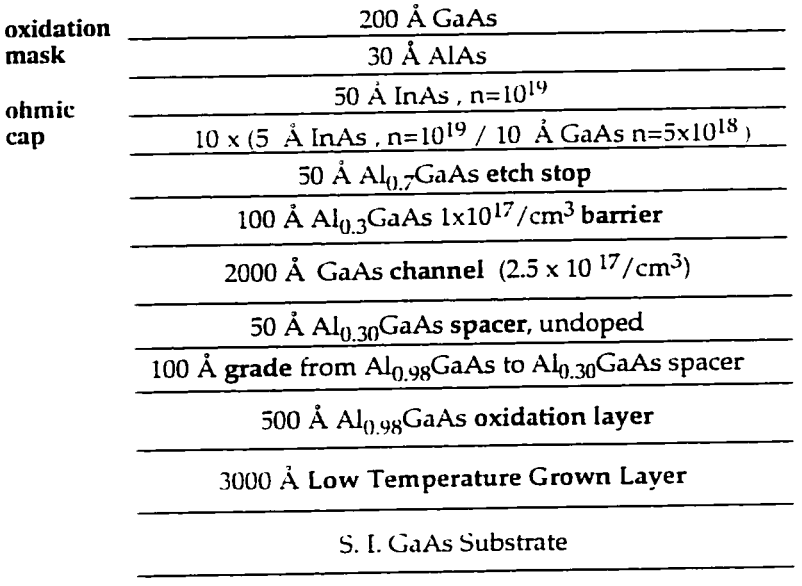


Figure 4.15 Layer structure of GOI samples with LTG buffer layers

The fabrication of the Hall sample is similar to GOI MESFET fabrication, beginning with the mesa etching step, followed by oxidation (@ 420° C), removal of the GaAs cap layer, and finally the lithography and evaporation of contact metal (Ni/Ge/Au/Ni/Au). The mobility and sheet charge density of the samples before and after oxidation, as obtained from Hall measurements are summarized in Table 4.1 (the n^+ cap is removed). As observed, the buffer layer influences to quite an extent the sheet charge after oxidation. The mobility does not seem to be effected much. Samples 1 and 2 exhibit

a charge depletion around 1.6-1.7 x $10^{12}/cm^2$ upon oxidation. Sample 2 had a high sheet charge to begin with but our main interest here is comparing the sheet charge before and after oxidation so this discrepancy is irrelevant. On the other hand samples 3 and 4 which incorporated the LTG AlGaAs buffer, had a much reduced charge depletion of around 0.6-0.9 x $10^{12}/cm^2$. The mobility in sample 3 was unusually low, which is due to the fact that the LTG AlGaAs buffer could have been so rough that the channel of the FET was degraded. The conclusion from this experiment is that LTG AlGaAs buffer results in greatly reduced charge depletion following oxidation. A more detailed study of the effect of LTG AlGaAs buffers with varying Al composition is currently underway (J. Champlain).

Sample	Control n_s (cm^{-2})	Oxidized n_s (cm^{-2})	Control μ (cm^2/Vs)	Oxidized μ (cm^2/Vs)
1	3.7 x 10^{12}	2.1 x 10^{12}	3200	2700
2	4.6 x 10^{12}	2.9 x 10^{12}	3000	
3	3 x 10^{12}	2.1 x 10^{12}	1400	1300
4	3.4 x 10^{12}	2.8 x 10^{12}	3000	3000

Table 4.1 Hall Results for GOI sample with different buffer layers

We also compared the current levels in actual FET structures for each of these samples before and after oxidation. These required mesa, oxidation and source/drain metallization steps. The FET mask had various device sizes ranging from 50 μm wide gates to 150 μm

wide gates. The oxidation time was chosen such that the 150 μm device was just oxidized. The actual oxidation time was different for the different samples (because the oxidation rates are dependent on the layer structure) but the oxidation extent was kept constant. Hence the smaller devices would be 'over-oxidized' and the effect of overoxidation on the channel charge could be evaluated. This issue of overoxidation was briefly described in chapter 2. The results for different device sizes and samples are presented in Figure 4.16. The general trend is that overoxidation results in more charge depletion. This makes it necessary to know and control the oxidation rates accurately and adjust the time so that the oxidation is just complete.

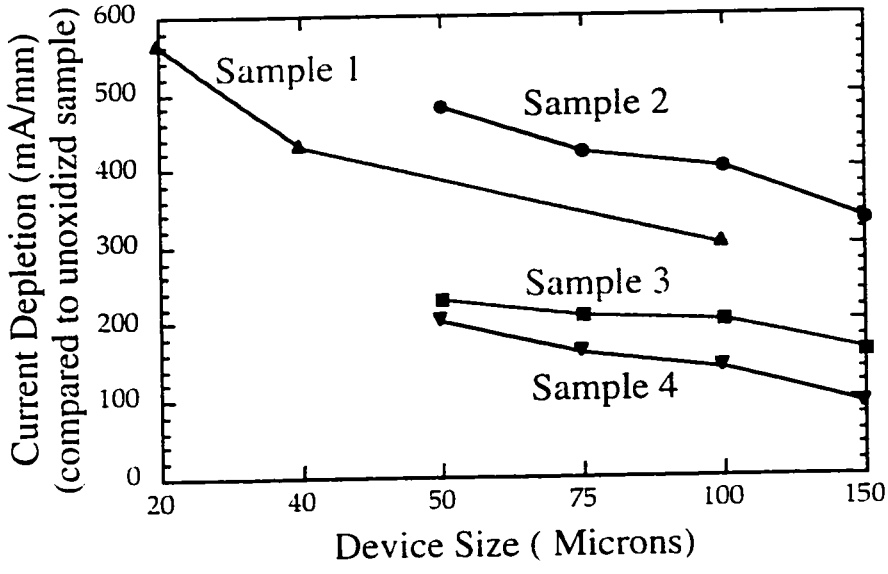


Figure 4.16 FET current (source/drain, no gate) depletion as a function of device size for the various GOI samples.

The FET data reconfirms the results of the Hall experiments that LTG AlGaAs, annealed at 500° C results in greatly reduced charge depletion. We also speculate that the Al composition in the

LTG AlGaAs layer could further effect the charge depletion in the GOI FET samples after oxidation.

It is worthwhile to point out that one of the GOI samples which incorporated a LTG-GaAs layer (sample # 5), exhibited no charge depletion. One of the reasons could be that the channel thickness in this sample was 2000 Å. The properties of the channel could be a strong function of the stress conditions existing in the sample during and after oxidation. A thicker channel, coupled with a LTG-GaAs buffer could be resulting in reduced stress. Though more studies are needed to confirm this hypothesis, it is a clear pointer to the fact that with further optimization, GOI samples that do not result in any charge depletion are possible. The epilayer structure of sample # 5 was similar to one shown in Figure 4.15, except that the channel thickness was 2000 Å. The reason for the channel being thicker than the previous samples was that these samples were designed for fabricating 1 μm gatelength devices. The previous samples were designed with a view to fabricating 0.25 μm gate length devices and hence the channel depth had to be reduced to maintain the aspect ratio[vi].

The Hall results for this sample (sample # 5) are compared to the control sample (sample # 6, with a regular GaAs buffer). The oxidations were done at 450° C and the 10 minute oxidation time resulted in just completely oxidizing the active Hall area. Oxidation rate for both the samples was around 1.85 μm/min.

It is clear that sample 5 results in no depletion of charge even when subjected to overoxidation, while sample 6 exhibits loss of charge around $1.4 \times 10^{12}/cm^2$ upon oxidation, which becomes worse upon overoxidation. Furthermore the mobility on sample 5 is also

similar to its pre-oxidation value. Since sample 5 retained both its sheet charge density and mobility upon oxidation, it would make an excellent vehicle to compare the properties of GOI and control MESFETs on this sample. This is the subject of the next section.

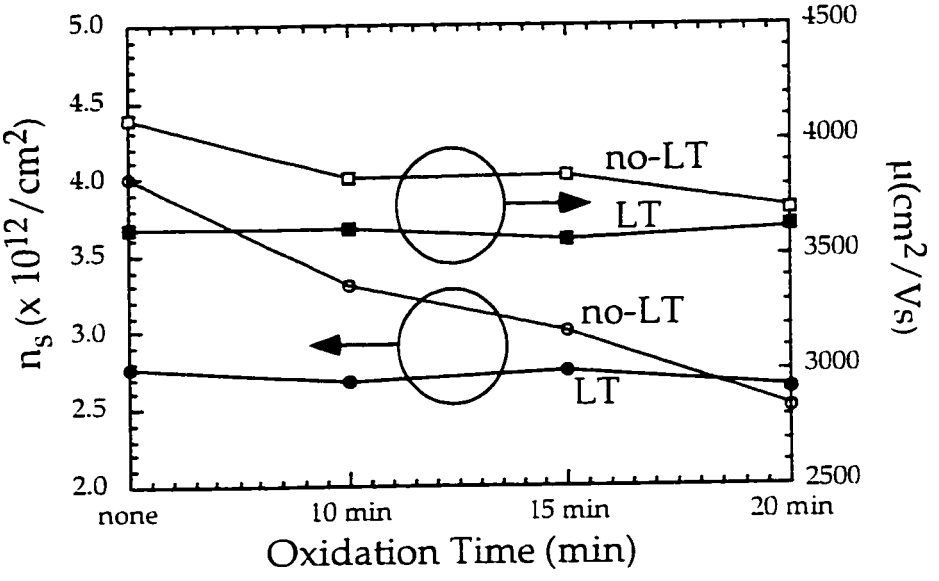


Figure 4.17 Hall results for the GOI sample with LTG-GaAs and Regular Buffer layers.

The reason for the improvements observed with LTG layers may be due to a number of possible processes. Figure 4.18 shows a schematic of what we believe is happening during the oxidation of AlGaAs on an LTG-buffer. During the oxidation, the AlGaAs is converted into oxide. Most of the arsenic is removed through the formation of AsH_3. However, as suggested by our work on gate oxides (chapter 3), some elemental Arsenic might be remaining at the interfaces between the oxide and the semiconductor, or in the oxide itself. We believe that this affects both charge and mobility in

the structure. The LTG layers might be enhancing the movement of Arsenic towards the bottom interface, via a gettering mechanism. This would, in the worst case lead to the Fermi-level getting pinned at this back interface. The reason why the Arsenic movement is preferentially directed towards the bottom interface is not clear. However, one of two very simple mechanisms may be responsible.

One mechanism that may be responsible for improvements with LTG - layers is precipitate enhanced diffusion. It is well known that LTG layers have excess As that upon suitable annealing, forms precipitates[9,11]. These could be serving as sinks for the As from the oxide hence gettering the As into the LTG layer as depicted in Figure 4.18a.

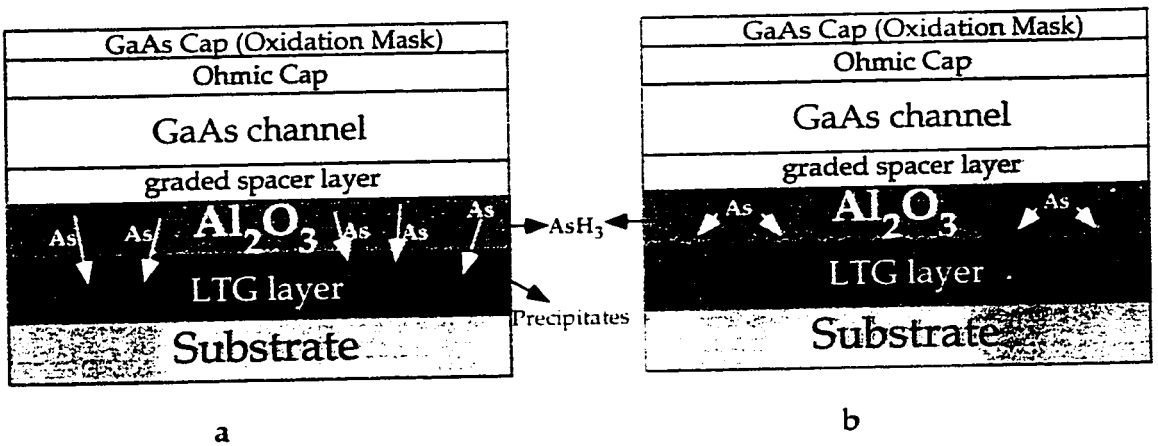


Figure 4.18 Arsenic leaves the oxide layer via AsH3 and moves toward the interfaces between the oxide and semiconductor. The LTG-layer enhances the As removal via the bottom interface, thus reducing the charge loss and effects of oxidation on mobility.

The other mechanism may be simply one of roughness of the interface between the oxide and LTG layer (Figure 4.18b). MBE RHEED signal confirms that the LTG grown layers are rough.

Roughening of near surfaces has been used in silicon structures to remove impurities from active device areas and the oxide semiconductor interface[viii]. The same mechanism may be responsible for the preferential movement of arsenic. A rough surface could also lower the free energy required for oxidation[ix] which would explain the faster oxidation rates with LTG layers. By using a higher composition of aluminum in the LTG buffer layer, the roughness (and hence gettering efficiency) of the bottom interface may be enhanced. Whether the rough surface in itself or the rough surface coupled with the microstructure of the LTG layers is causing the above effects is difficult to ascertain at this point. An interesting experiment (suggested by Prof. Hu) would be to grow a regular GaAs buffer and roughen it by etching a grating. This would increase the net interfacial area between the layer to be oxidized and the underlying area. This may or may not have the same effects in the oxidation rate and improvements in the channel properties as the LTG layers depending on the exact mechanism of the process. However such a study would be a useful pointer to further our understanding of this process.

4.4 Optical Gate Lithography GOI and control MESFETs

The first two GOI MESFETs (without the LTG buffer layers) helped demonstrate the concept of the GOI technology, and elimination of substrate leakage resulted in MESFETs with near ideal dc I-V characteristics. The problem of charge depletion was addressed merely by compensating for the lost charge. The next step was to obtain GOI MESFETs with minimal charge depletion, which

would enable comparison with a control MESFET (without the oxidized buffer) and highlight the salient benefits of the GOI technology. Sample #5 with the LTG-GaAs buffer that resulted in no loss of charge after oxidation was used to fabricate optical gate GOI MESFETs. The layer structure is shown in Figure 4.19.

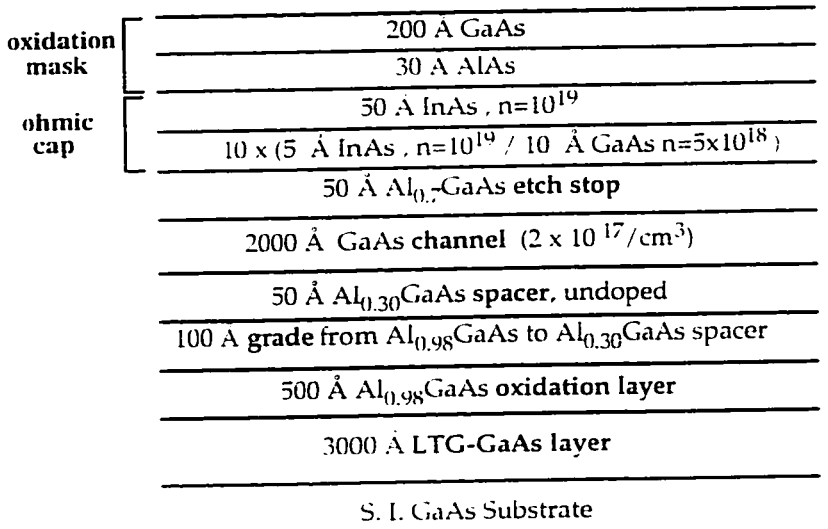


Figure 4.19 Layer structure of the optical gate lithography GOI MESFET with minimal charge depletion

The processing is similar to that described in section 4.2 with one notable change. A 30 Å AlAs etch stop layer and a 200 Å dummy GaAs cap have been added above the n^+ InAs ohmic layer. The purpose of this is to eliminate the steps of depositing PECVD SiO_2 as a protective cap layer and then the subsequent removal of this layer after oxidation by RIE. Instead the GaAs itself is used as the protective layer to prevent the active device areas from any undesirable oxidation from the top. After oxidation is accomplished, the dummy GaAs layer is removed in a wet citric acid based blanket etch which stops on the AlAs layer. Next the AlAs layer is removed

by a 2 second dip in phosphoric acid based wet etchant. HF could have been used to selectively remove this AlAs layer but this sometimes leads to severe undercutting of the Al_2O_3 layer and hence was avoided. After the removal of these 2 cap layers, the ohmics and the gate metal processes are done as described before. The drain I-V characteristics of the GOI MESFET and the control device are shown in Figure 4.20 a,b. The GOI exhibits near ideal I-V characteristics. The unoxidized device has a clear evidence of substrate leakage.

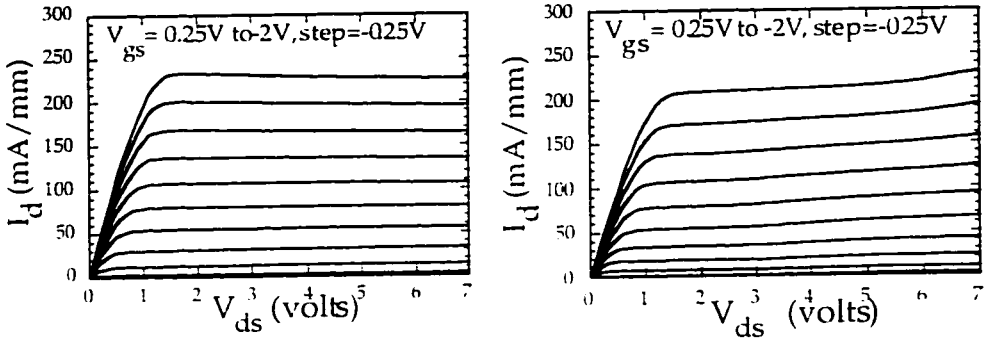


Figure 4.20 a,b. Drain I-V characteristics of the GOI (a) and control MESFET (b) with minimal charge depletion

The current levels in both the devices are very similar and so are the pinchoff voltages, hence a fair comparison of the various dc and rf properties of the devices can be done. The transconductance characteristics of the two devices are superimposed in Figure 4.21. It is seen that the oxidized device has a broader g_m curve with enhanced g_m near pinchoff. This results from the elimination of substrate leakage. This effect is more prominent near pinch off,

where the channel charge being modulated is adjacent to the non-ideal buffer layer.

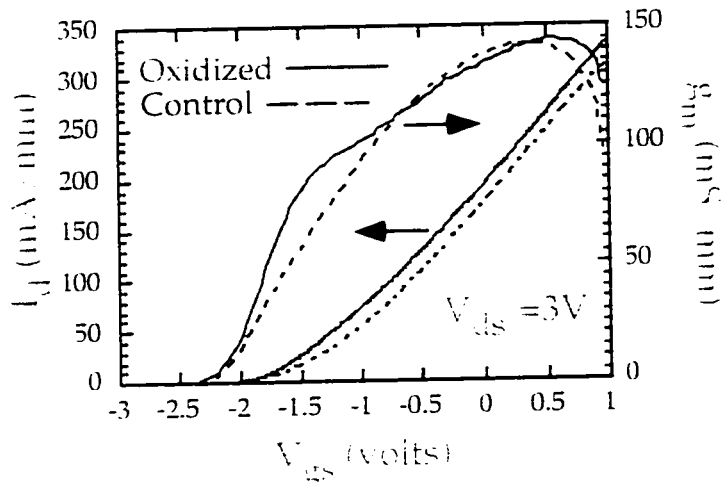


Figure 4.21 Transconductance of the GOI and control devices

An insulating oxide buffer confines the charge to the channel of the FET, thereby minimizing this leakage current. The higher g_m near pinchoff is particularly useful for high efficiency application as the typical bias points for a high efficiency amplifier configuration are near pinchoff, as is discussed more in the next chapter.

Next, we compared the RF performance of the two devices. The f_τ and f_{max} data was extracted from S-parameter measurements. This was done as a function of bias for various gate and drain bias voltages. The results are summarized in Figure 4.22. These f_τ values are normal for a 1.3 μm gatelength device. The GOI device exhibits a higher f_{max}/f_τ ratio over most of the bias range. This is due to the superior output resistance of the GOI device, which was achieved by the elimination of substrate leakage. Furthermore, the f_τ and f_{max}

values for the GOI device retain higher values over a broader bias range which suggests enhanced charge control.

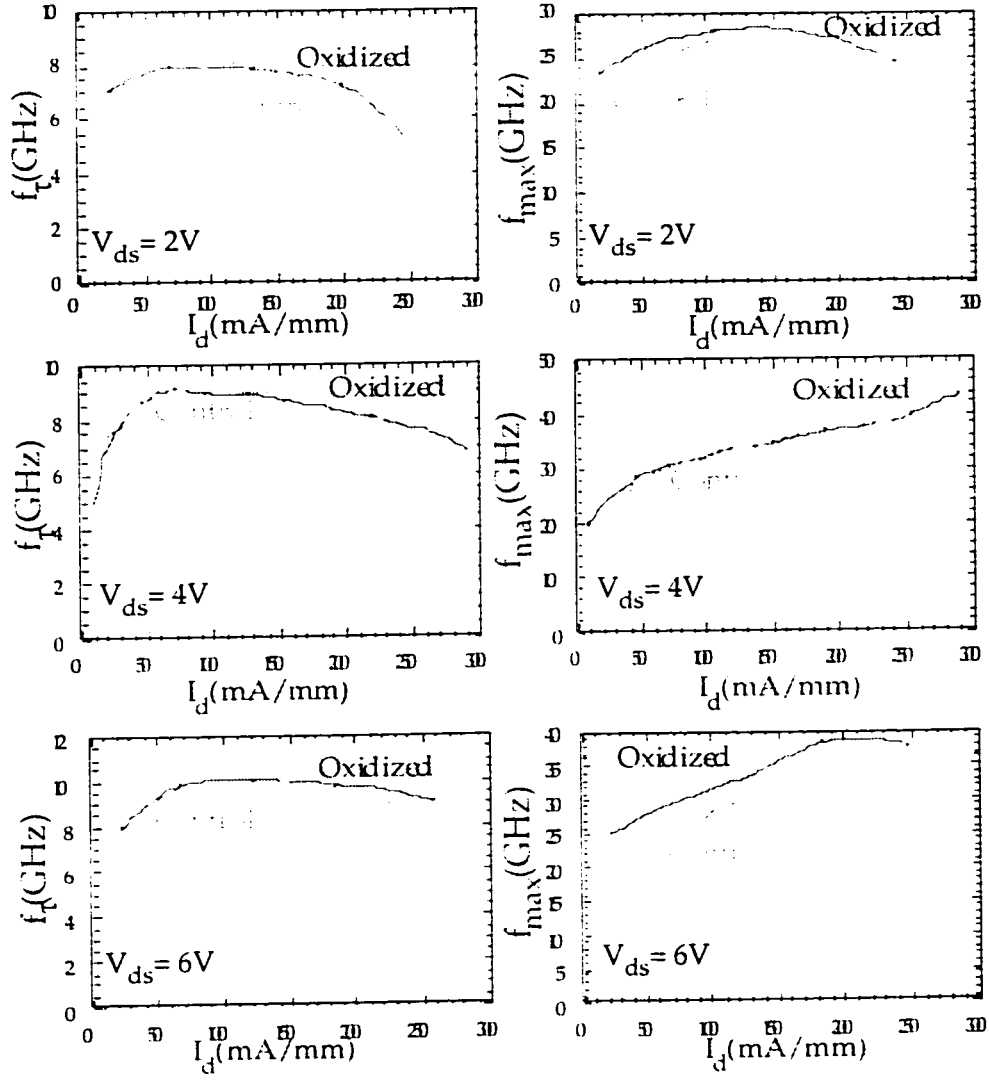


Figure 4.22 f_τ and f_{max} as a function of drain currents and voltages

This experiment illustrates the benefits of the buffer insulator at both dc and rf. In the next chapter, we will describe the performance of submicron GOI MESFETs which show how the

superior characteristics of the GOI device translate to higher efficiencies when used as power amplifiers.

4.5 GaAs On Insulator pHEMTs

The pHEMT (AlGaAs-InGaAs on GaAs) is widely used in the GaAs microwave power industry due to the superior power, efficiency and linearity performance available from the device, in comparison with a MESFET. The high power performance is a result of the increased charge density in the channel of the pHEMT due to the confining potential at the AlGaAs barrier-InGaAs channel interface as shown in Figure 4.23.

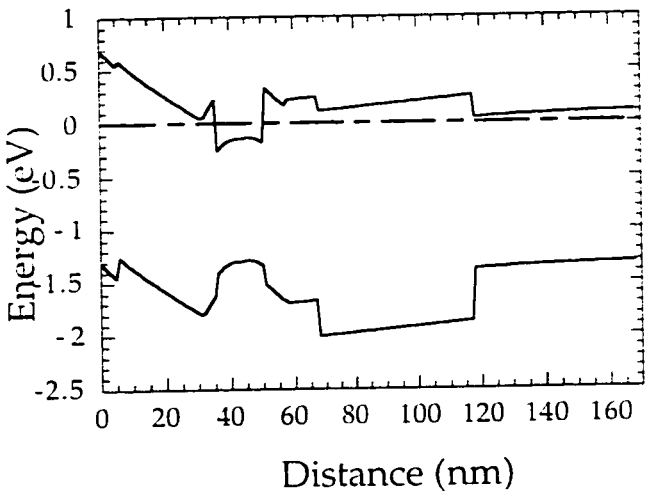


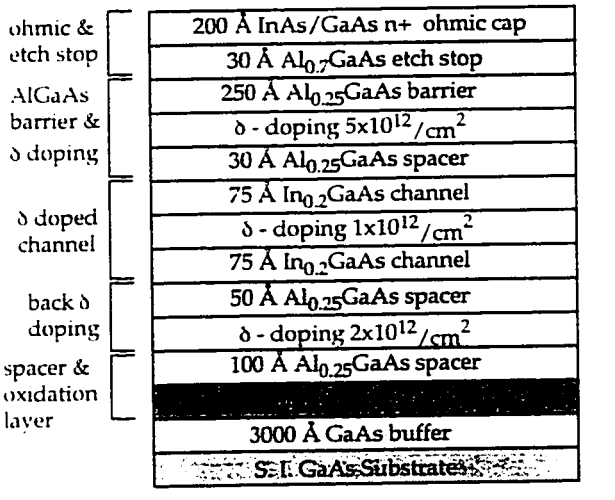
Figure 4.23 Energy Band diagram for the pHEMT of Figure 4.24

The higher mobility of the InGaAs channel (compared to a GaAs channel of a MESFET) result in lower knee voltage which translates to increased efficiencies as explained in section 5.2. Furthermore pHEMTs exhibit improved linearity over MESFETs.

These issues are explained in more detail in the next chapter. Having successfully demonstrated the GOI technology in MESFETs, a logical extension would be the application of GOI technology to pHEMTs. This would then be expected to improve the performance of pHEMTs even further. This section describes the results of the first pHEMTs fabricated in the GOI technology.

Growth and Fabrication

The epistructure, grown by MBE on a S.I. GaAs substrate is shown in Figure 4.24.



Layer structure for the GOI pHEMT

Figure 4.24 Layer structure of the GOI pHEMT

First a conventional GaAs buffer is grown. Next the 500 Å $Al_{0.98}Ga_{0.02}As$ layer (which after oxidation will become the insulating buffer) is grown, followed by 100 Å $Al_{0.25}Ga_{0.75}As$ spacer layer (this layer helps in preventing the GaAs channel from being degraded by

oxidation). The channel comprises of 150Å $In_{0.2}Ga_{0.8}As$ and is δ doped at the center, with additional δ dopings at the top and the bottom, separated by spacer layers. The barrier is 250 Å $Al_{0.25}Ga_{0.75}As$, followed by an etch stop and finally grade to n^+ InAs to enable ohmic contacts.The GOI pHEMT process and the oxidation scheme is very similar to the GOI MESFET fabrication described in the earlier sections, since the GOI technology is transparent to any generic FET device. The schematic of the fabricated device is shown in Figure 4.25. The only difference in fabrication from the MESFET case is that a slightly higher alloying temperature of 430° C is used due to the presence of the wider bandgap $Al_{0.25}Ga_{0.75}As$ barrier layer.

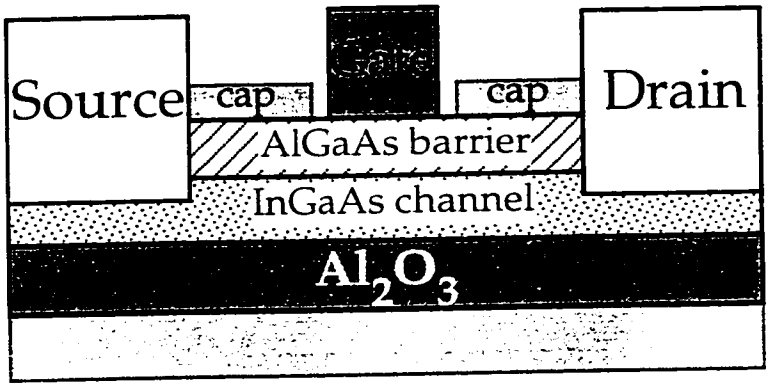


Figure 4.25 GOI pHEMT schematic

Results and discussion :

The three-terminal DC I-V characteristics of the GOI pHEMT in Figure 4.26, indicate that the device has negligible output conductance. The peak g_m (Figure 4.27) is 140 mS/mm at a drain current of 85 mA/mm. The full channel current is around 140 mA/mm.

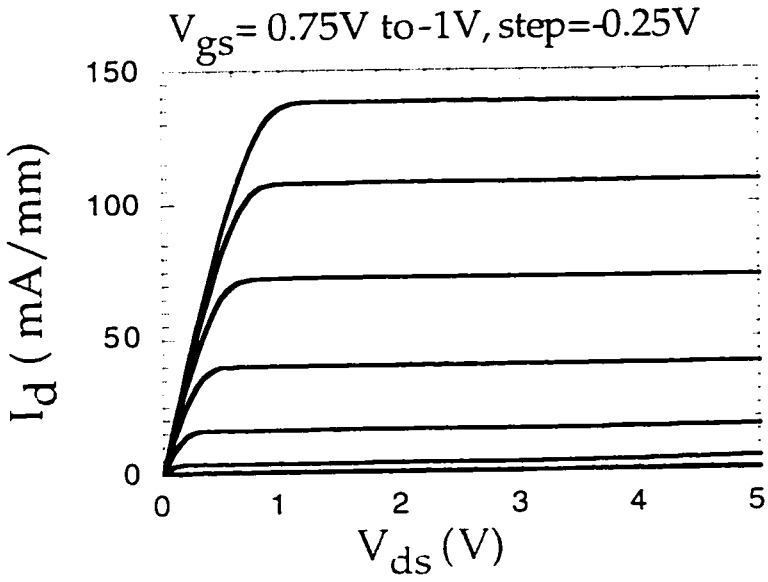


Figure 4.26 GOI pHEMT drain I-V characteristics

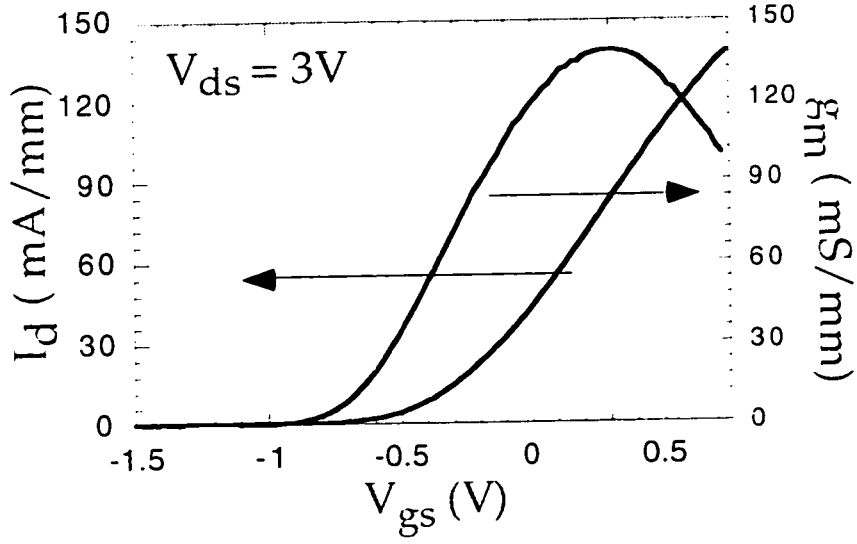


Figure 4.27 GOI pHEMT transconductance characteristics

The pinch-off characteristics are excellent, implying good charge control in the GOI pHEMT. The current level is lower than expected due to the charge depletion as a result of the oxidation process.

RF characterization was done on an HP-8510B S-parameter system. The f_t and f_{max} of this device are 6.4 GHz and 16 GHz respectively. The output resistance R_{ds} as extracted from the S-parameter measurements is around 570 -mm corresponding to a very low output conductance of 1.8 mS/mm and a high voltage gain ratio g_m/g_{ds} of 70.

The use of LTG grown layers to minimize the charge loss after oxidation, is being investigated for application to GOI pHEMTs as a part of a separate research effort at UCSB.

These results demonstrate the feasibility of pHEMTs in our newly developed GOI technology and that Al_2O_3. This can form an enabling technology for low substrate leakage, high output resistance GOI pHEMTs, attractive for linear, high efficiency power amplifiers.

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CHAPTER 5. Submicron GaAs On Insulator (GOI) Technology : Impact on large signal rf performance.

5.1 Introduction

Microwave power amplifiers are fundamental components for wireless mobile communication, satellite and space technology and phased array radar applications. Output power, efficiency, linearity and large signal gain are the most important characteristics of a microwave power amplifier. Higher efficiency would allow for lighter and smaller power sources, reduced cooling requirements and increased operating time. For wireless applications, the choice of system and the corresponding modulation method defines the rf waveform and has direct implications on the rf transmitter, particularly the power amplifier. The power amplifier is the most significant source of non-linearities, which can lead to interference with other channels of the system or even other services. A linear power amplifier minimizes such undesirable effects. Furthermore, low drain bias, while meeting other system specifications, is desirable for amplifiers in transmitters of handheld telephones to reduce the battery size. To meet the above requirements is a challenge at the device, circuit and system level and often the optimal performance is achieved by a suitable trade-off of one or more of the above parameters. This chapter reviews the basic requirements of efficiency and linearity and looks at the impact of the GOI technology on these issues.

5.2 Efficiency of a power amplifier

The two most common measures of efficiency are the drain efficiency (DE) and the power added efficiency (PAE) as shown in Equation 5.1 and 5.2 respectively.

$$DE = \frac{P_{out}}{P_{dc}}$$ **Equation 5.1**

where P_{out} is the rf output power and P_{dc} is the average dc power dissipated in the device. While drain efficiency reflects the intrinsic device performance quite well, often it can be misleading for devices with low gain. For example it can be possible to have high DE even when the input rf power exceeds the output power, in which case the amplifier is obviously useless. An alternate definition which overcomes this shortcoming is PAE.

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}}$$ **Equation 5.2**

where P_{in} is the rf input power. The gain of the amplifier G is defined as P_{out}/P_{in}. Hence in terms of the gain, the PAE can be related to DE as shown below.

$$PAE = DE\,(1 - 1/G)$$ **Equation 5.3**

In the limit of infinite gain the PAE approaches DE. It is clear from equation 5.3 that high gain is fundamental to high efficiency amplifier operation. In general the gain of a device drops as f, the operating frequency gets closer to f_{max}, the maximum frequency of

oscillation. This necessitates a high value of f_{max} and correspondingly high f_τ, the short circuit gain cutoff frequency as seen from the relation below.

$$f_{max} = \frac{f_\tau}{2\sqrt{\frac{r_i + r_g + r_s}{r_{ds}} + 2\pi f_\tau r_g c_{gd}}} \qquad \textbf{Equation 5.4}$$

Hence submicron devices (gate length ~ 0.25 μm) were used to investigate the impact of the GOI technology on efficiency. The fabrication and results of the submicron GOI technology are discussed in the later part of this chapter.

Based on the quiescent bias point and the input and output rf signals, amplifier can be divided in various classes.

1. Class A : Device conducts for full input cycle (360°)
2. Class B : Device conducts for 1/2 the input cycle (180°)
3. Class C : Device conducts for <1/2 the input cycle (<180°)
4. Higher Classes D, E, F etc. : Device acts as a switch.

The basic analysis of Class A and tuned class B is presented here. Other results and more details can be found elsewhere[1].

Class A operation

The FET I-V characteristics, biasing point, and the drain current and voltage waveforms of Class A operation are shown in Figure 5.1. The output power is maximized when the voltage and current swings are maximized. The upper voltage limit is set by the breakdown voltage (V_{bd}) and the lower limit by the knee voltage (V_k). Operation below the knee voltage is avoided as the FET is out of saturation and the gain decreases rapidly. The maximum current limit I_{max}, is set by the maximum current before the gate diode turns

on I_{max}, which is typically greater than the full channel current I_{dss}) and the minimum by 0 when the device pinches off.

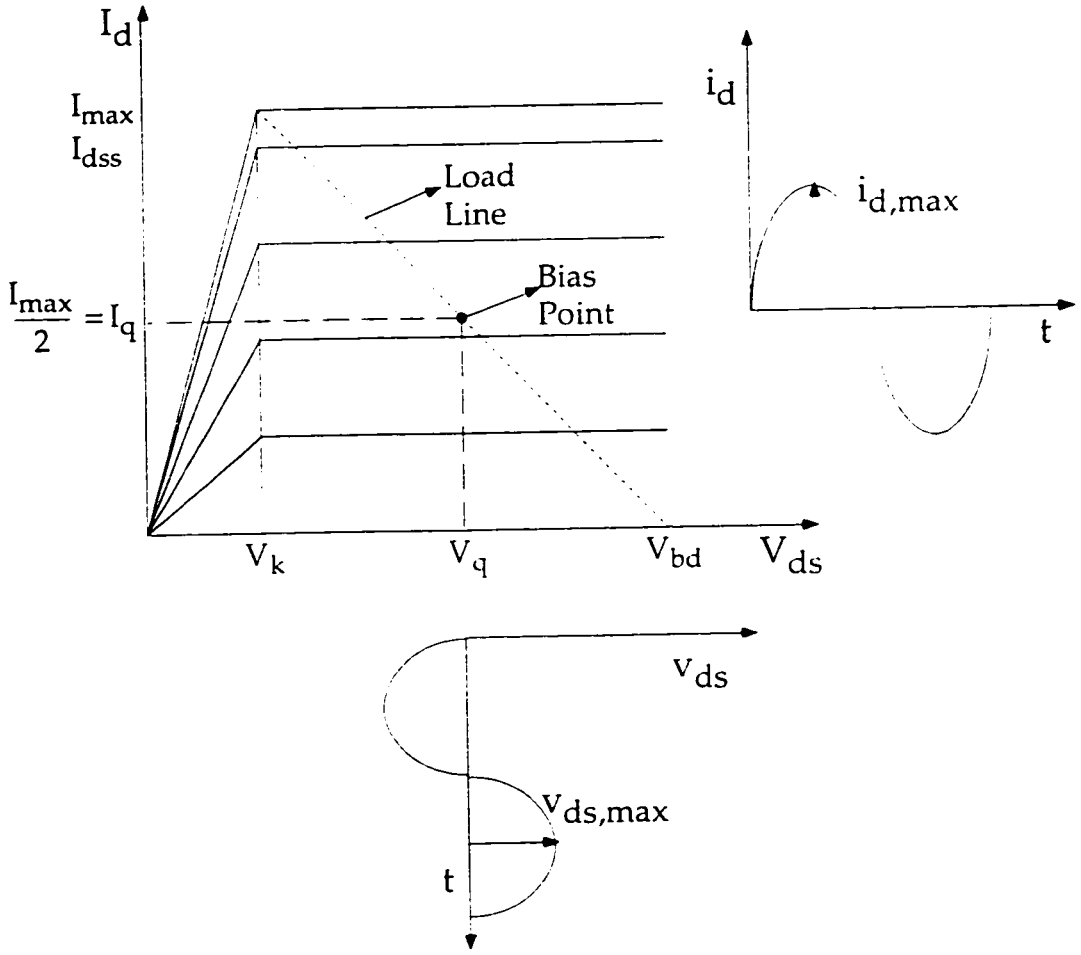


Figure 5.1 Class A operation

The rf power output is given by

$$P_{out} = \frac{v_{ds.peak} * i_{ds.peak}}{2} \qquad \textbf{Equation 5.5}$$

and the maximum rf output power is delivered when the voltage and current swings assume their maximum value.

$$P_{out.max} = \frac{I_{max}}{2} * \frac{V_{bd} - V_k}{2} * \frac{1}{2}$$ **Equation 5.6**

This is also the maximum linear RF output power that can be achieved from the FET since the voltage and current waveforms are purely sinusoidal. The dc power dissipation is given from the bias point as

$$P_{dc} = \frac{I_{max}}{2} * \frac{V_{bd} + V_k}{2}$$ **Equation 5.7**

Using Equation 5.3,

$$PAE = \frac{1}{2} * \left[1 - \frac{1}{G}\right] * \frac{V_{bd} - V_k}{V_{bd} + V_k}$$ **Equation 5.8**

Therefore the maximum ideal value of PAE under Class A conditions is seen to be 50 % when the gain is infinite and the knee voltage is zero. The major disadvantage of Class A operation is the fact that dc power is independent of rf power as the FET is always on, even when there is no input signal, resulting in wastage of power. However the main advantage is that output power is linear with input power (assuming gain is constant, which as seen in the next section is the major determinant of linearity).

Tuned Class B operation

Class B operation of a FET is shown in Figure 5.2. The main difference from Class A operation is that the FET is biased at pinchoff with no current flowing in the absence of input signal. This is also one of the fundamental advantages of Class B, that no power is wasted in the absence of rf input drive. However as a consequence of this, the output current flows only during the positive half cycle of input voltage. Since tuned conditions are assumed at the load, only the fundamental component of the current flows through the load.

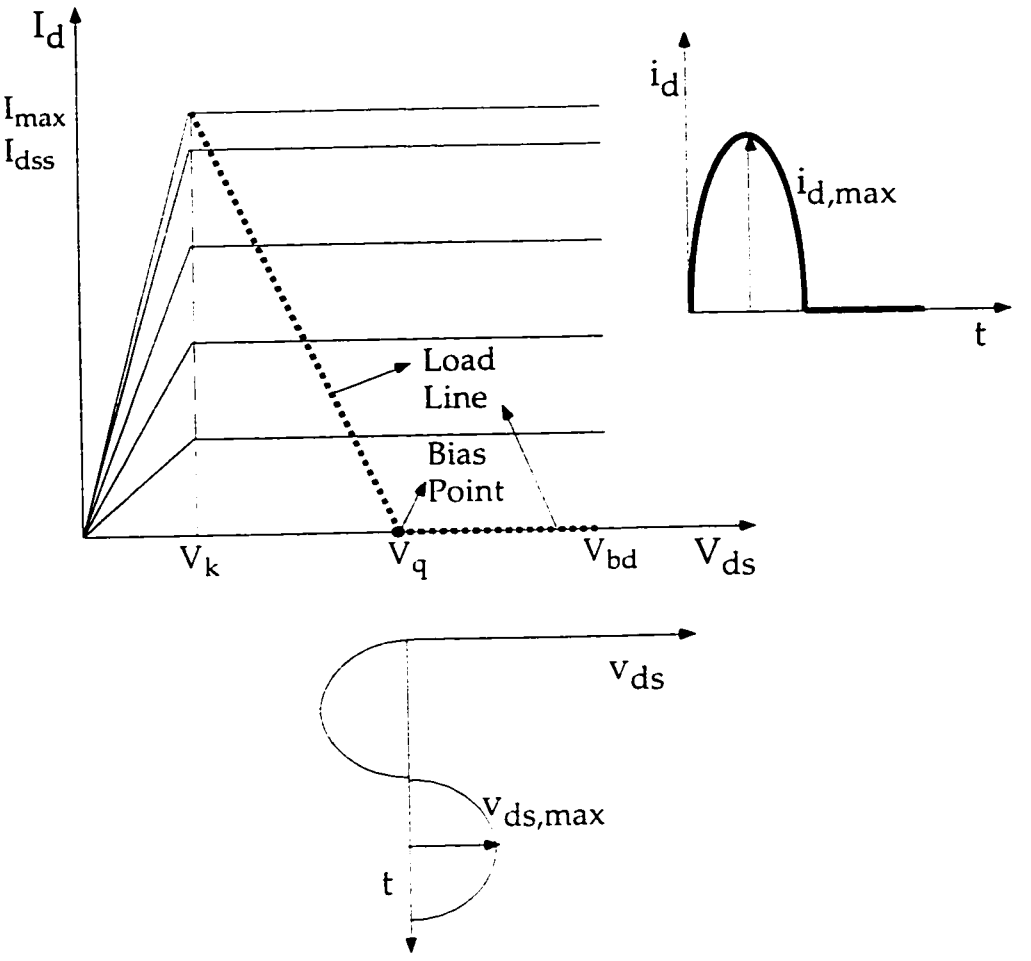


Figure 5.2 Class B operation

The rf drain current is a half sine wave as shown and can be expressed as a fourier series.

$$i_d = \frac{i_{dpeak}}{\pi} + \frac{i_{dpeak}}{2}\sin\omega_0 t + \text{even harmonics} \qquad \textbf{Equation 5.9}$$

The dc component of the current is now a function of rf output unlike the class A case. The dc power can be calculated as

$$P_{dc} = \frac{i_{dpeak}}{\pi} * \left(\frac{V_{bd} + V_k}{2}\right) \qquad \textbf{Equation 5.10}$$

Note that the breakdown voltage here is the three terminal breakdown voltage. Usually the gate-drain breakdown voltage, $V_{dg,max}$ of a FET is specified. When the drain source voltage is at its maximum value, V_{bd}, the gate source voltage is at its most negative value, which in the case of a class B amplifier is $-(2V_p+V_{on})$ where V_p is the magnitude of the pinchoff voltage as before and V_{on} is the gate voltage for maximum drain current, I_{max} (before the gate diode turns on). This is so as the gate is biased at pinchoff and the maximum input rf swing on the positive side is limited by V_{on}, making the rf input voltage swing on the positive side, V_p+V_{on}. Since the input is sinusoidal, the same swing occurs on the negative side also. Hence the maximum drain source voltage is,

$V_{bd} = V_{dgmax} - (2V_p+V_{on})$ **Equation 5.11**

(On similar lines V_{bd} for class A case would be $V_{dgmax} - V_p$)

The maximum value of i_{dpeak} in this case is I_{max} which makes the maximum value of the fundamental component of current flowing through the load $I_{max}/2$ as evident from equation 5.7. The maximum voltage swing is $(V_{bd} - V_k)/2$ as before. Hence the maximum linear rf output power (here linear is with reference to the fundamental, harmonics are always generated in class B since the FET is on only for half the cycle) is given by

$$P_{out,max} = \frac{I_{max}}{2} * \frac{V_{bd} - V_k}{2} * \frac{1}{2}$$ **Equation 5.12**

From the above, the maximum PAE is calculated as,

$$PAE = \frac{\pi}{4}\left(1 - \frac{1}{G}\right)\left(\frac{V_{bd} - V_k}{V_{bd} + V}\right)$$ **Equation 5.13**

which gives the maximum PAE for the class B case to be 78.5 %. The increased efficiency comes at the cost of reduced linearity since harmonic generation is inherent in class B operation. In a lot of practical applications a compromise between efficiency and linearity is achieved by operating the amplifier in Class AB mode, in which the quiescent bias level for the current is between class A and B, typically from $I_{dss}/4$ to $I_{dss}/20$.

A drawback of the Class B amplifier is that twice the RF input voltage is required to get the same rf output power (since the FET is biased at pinchoff rather than in the middle of the I-V characteristics). Assuming similar input impedances, a FET operating in Class B would exhibit 6 dB less gain than the corresponding Class A case. Moreover the g_m reduces near pinchoff which makes this issue more crucial. Substrate leakage near pinchoff is one of the reasons for g_m reduction. By eliminating the substrate leakage, and providing a higher g_m near pinchoff, the GOI technology achieves superior efficiencies. The measurement results and the comparison of GOI and control FETs is the topic of section 5.5.

Harmonic matching and Class F amplifiers

Ideal high efficiency operation occurs when the harmonics of the output voltage have the right magnitudes and phases to form a square wave[11]. This requirement can be met by having short circuits at the even harmonics and open circuits at the odd harmonics[1]. This mode of operation is referred as Class F. The transistor is operated close to the Class B mode with the drain current waveform of a half rectified sine wave as shown in Figure 5.2. The output circuit is tuned at the fundamental to pass only the fundamental frequency. The second harmonic is shorted to suppress these components in

the voltage waveform, while the third harmonic is open circuited to provide the appropriate third harmonic component to the output voltage. This causes the flattening of transistor output voltage waveforms approximating a square wave. When the magnitude of this component is properly adjusted, a maximum drain efficiency of 100 % can be realized[iii].

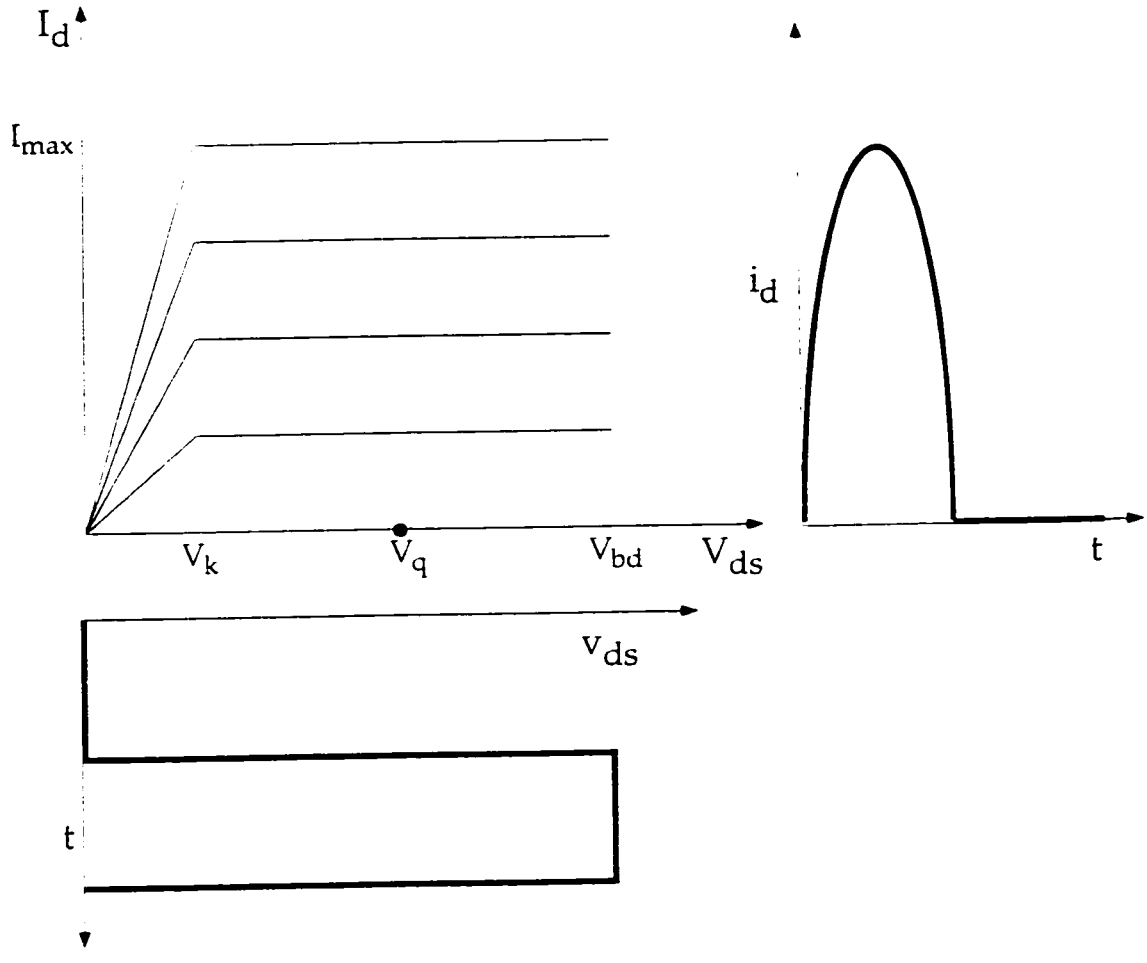


Figure 5.3 Ideal Voltage and Current Waveforms for Class F operation

5.3 Linearity of a power amplifier

Transmitters and receivers for wireless communication systems require high linearity devices that can minimize intermodulation distortion. Intermodulation products would cause spectral regrowth that would interfere with signals from other channels in the same system of a different service. The issue of linearity can be addressed by device, circuit and system solutions. In this section we will try to address the effect of the device characteristics on linearity, using FETs. In most FET type devices, the transconductance (g_m) variation with input gate voltage has been found to play the first order effect on intermodulation distortion.

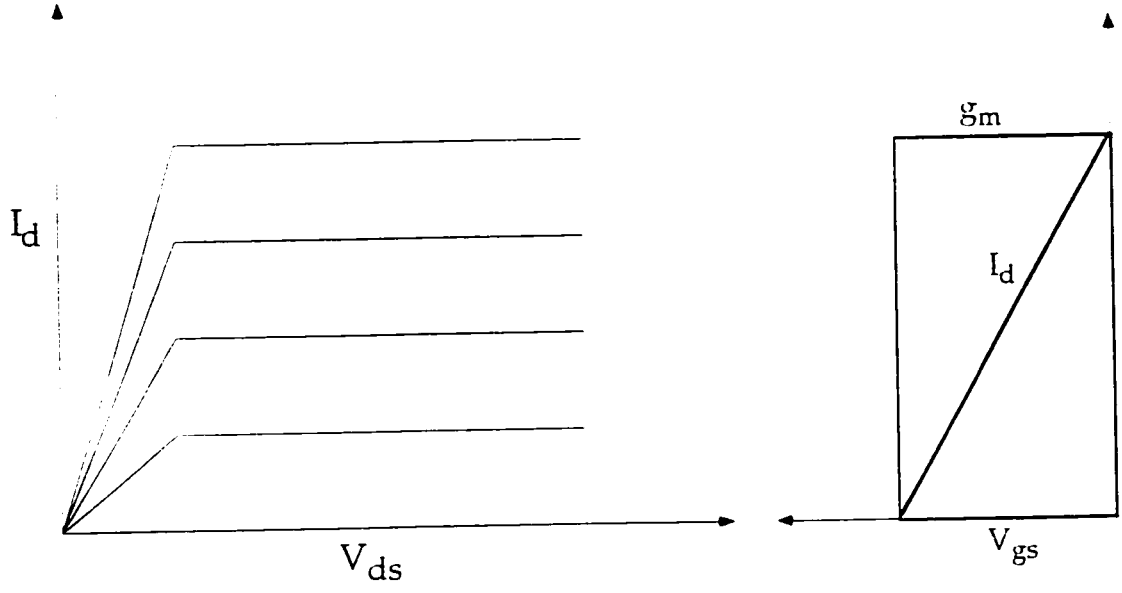


Figure 5.4 Ideal I_d and g_m characteristics for a linear device

Ideally, a constant transconductance characteristic as shown in Figure 5.4 is desirable since this results in constant gain, independent of the input power level. This translates into the

output power being linear with input power. Consider a MESFET schematic shown in Figure 5.5. In general the g_m of the device is proportional to C_g (gate capacitance) and v(velocity).

$g_m \sim C_g v$ **Equation 5.14**

$dg_m/dV_g \sim vdC_g/dV_g + C_g dv/dV_g$ **Equation 5.15**

Hence the variation in g_m comes from the variation in the gate capacitance (which results from the variation in depletion width with gate voltage in a MESFET) or due to a variation from velocity.

For larger gate length devices, velocity will be a function of electric field in the channel, which will in turn depend on the charge density and hence the gate voltage. Assuming constant doping, mobility, abrupt depletion region and the gradual channel mode of operation, and no velocity saturation, the saturated drain current is derived to be[iv]

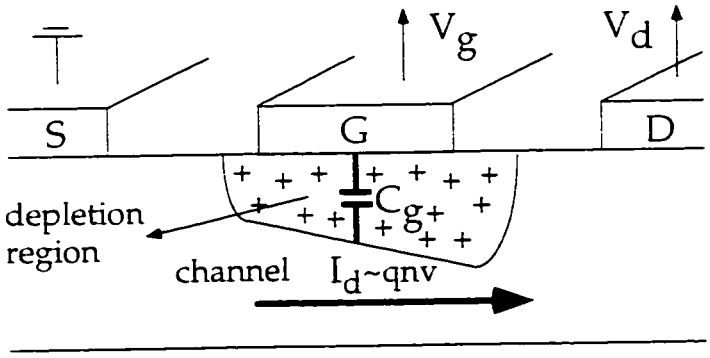


Figure 5.5 Schematic of a MESFET

$$I_{dsat} = I_{dss}\left[1 - 3\left(\frac{V_g + V_{bi}}{V_p}\right) + 2\left(\frac{V_g + V_{bi}}{V_p}\right)^{\frac{3}{2}}\right] \qquad \textbf{Equation 5.16}$$

and the g_m which is dI_{dsat}/dV_g can be written as

$$g_m = g_{m0}\left[1 - \sqrt{\frac{V_g + V_{bi}}{V_p}}\right]$$ **Equation 5.17**

where V_p is the voltage required for the channel to be fully depleted, V_{bi} is the built in voltage and V_g is the magnitude of the gate voltage. On the other hand for a completely velocity saturated device (true for submicron gate length GaAs devices), the only contribution in g_m variation will be from the capacitance change.

$$dg_m / dV_g = v_s \, dC_g / dV_g$$ **Equation 5.18**

To minimize the g_m variation, it is necessary to have a velocity saturated device in which the capacitance does not change with gate voltage. In a small gate length MESFET, such a scenario can be achieved by modifying the doping profile so that the depletion layer thickness does not change rapidly.

Another solution would be to use a HEMT instead of a MESFET where the channel charge is confined in a quantum well, as shown in Figure 5.6.

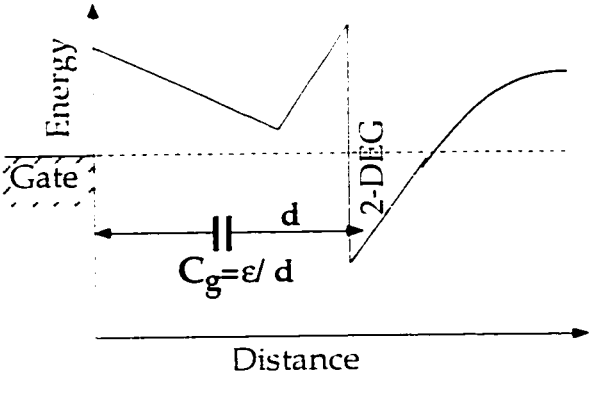


Figure 5.6 Conduction band energy of a generic HEMT

The capacitance is then determined by the distance of the gate from centroid of the charge distribution in the quantum well which is fairly constant with changing input gate voltage. This makes a HEMT more linear device than a MESFET and is one of the main reason for HEMTs and pHEMTs in GaAs being used widely for power amplifier applications. As is discussed in the next sections, the GOI technology achieved MESFETs with record high efficiency, with decent linearity performance. With GOI pHEMTs, we expect to achieve both high efficiency and high linearity at the same time.

5.4 First Submicron GOI MESFETs

The fabrication of the submicron GOI MESFETs is similar to the optical gate lithography devices other than the gate lithography is done by the means of electron-beam lithography. The source and drain spacing is reduced (to minimize access resistances to the device) and the source-drain mask level incorporates e-beam alignment marks. Another important difference is in the layer structure design. The channel thickness is reduced to 1000 Å from 2000 Å for the optical gate devices. The doping is increased to maintain the current level. This is to maintain the aspect ratio of the device in order to minimize short channel effects. The GOI technology in submicron devices is expected to have a greater impact on eliminating the substrate leakage current. This is so as the substrate leakage current varies inversely as the square of the gate length[v], and is expected to be much higher in submicron devices. The first submicron MESFET layer structure is shown in Figure 5.7.

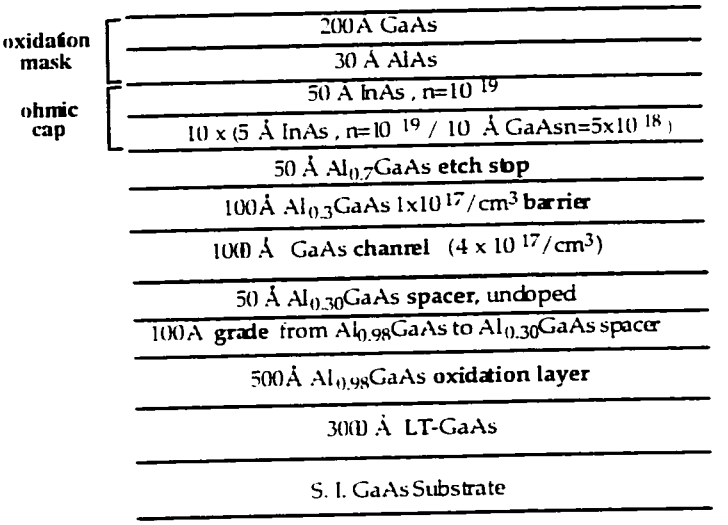


Figure 5.7 Submicron GOI MESFET layer structure

The LTG-GaAs layer was incorporated to minimize the problem of charge depletion and was based upon the effectiveness of LTG-GaAs used in sample #5 described in the previous chapter. The detailed process flow is described in the appendix. The E-beam lithography was done at HRL, Malibu, with their 0.25 μm E-beam process.

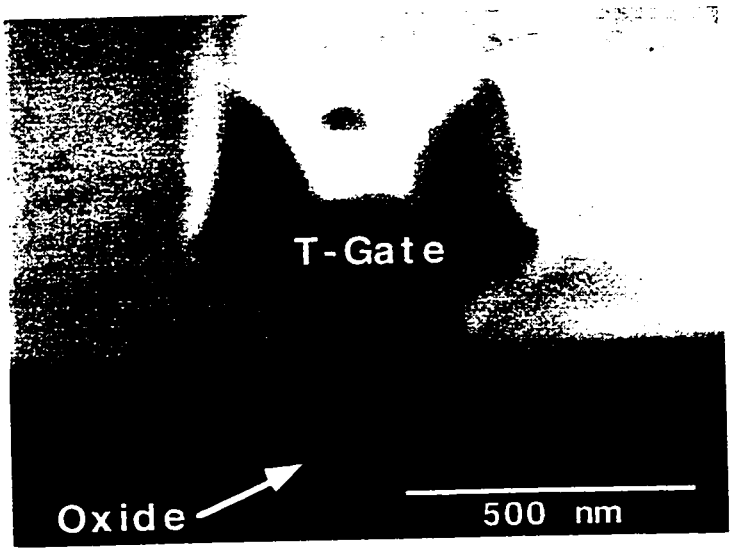


Figure 5.8 SEM of the T-gate written at HRL

The cross sectional SEM of the T-gate is shown in Figure 5.8. Figure 5.9 shows the completed device. The actual gate footprint was measured to be 0.3 μm with a 0.5 μm top. The metal thickness was 4000 Å (Ti/Pt/Au).

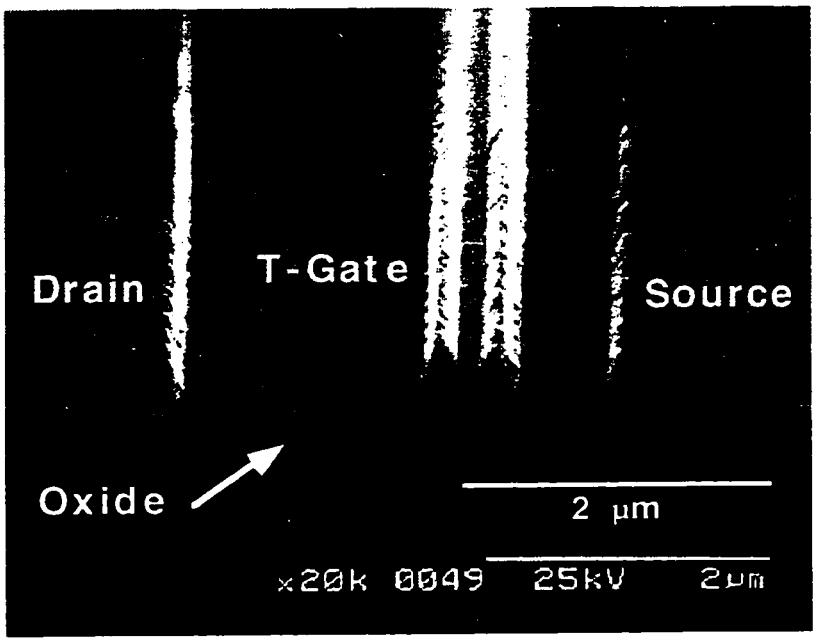


Figure 5.9 SEM of the completed submicron GOI MESFET

The drain I-V characteristics of this device are shown in Figure 5.10. The maximum current level is around 225 mA/mm. The submicron device also exhibits very low output conductance and reduced substrate leakage. However the current level in the oxidized sample was much lower than expected. The I-V characteristics of the control sample are shown in Figure 5.11. The current level is about 550 mA/mm which corresponds to a loss in current of over 300 mA/mm after oxidation.

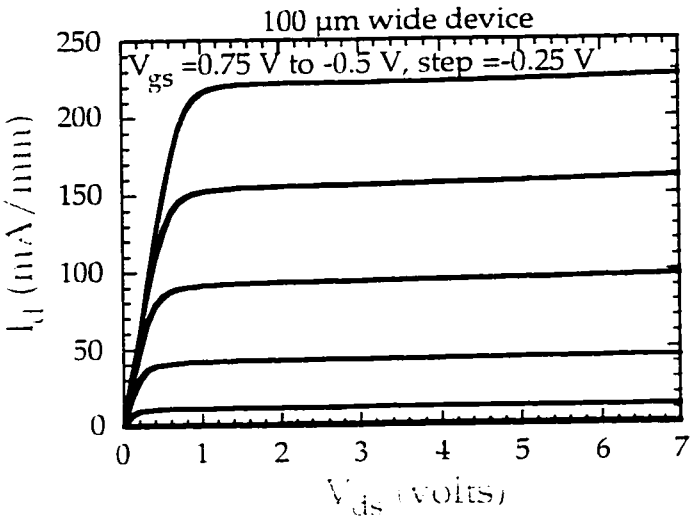


Figure 5.10 DC I-V characteristics of the first submicron GOI MESFET

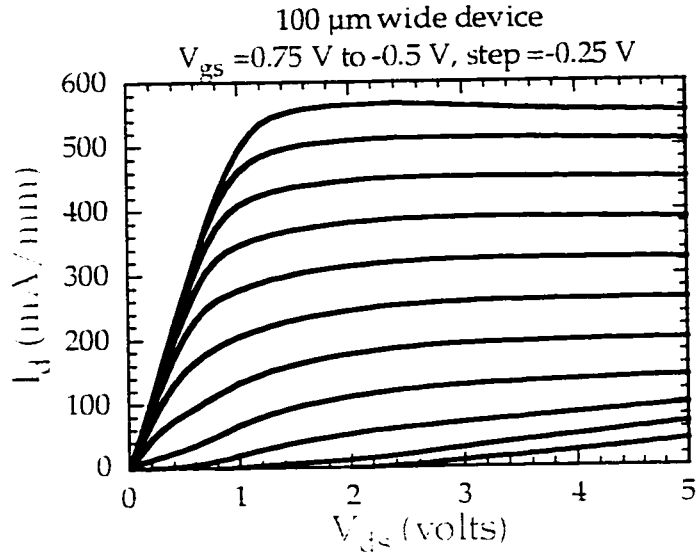


Figure 5.11 DC I-V characteristics of the submicron control MESFET

However the unoxidized sample shows clear evidence of leakage, especially near pinchoff and relatively soft saturation characteristics. Both devices had a high peak g_m of around 260

mS/mm.In this case the LTG-GaAs buffer was not helpful in minimizing the charge loss after oxidation. Two plausible theories for the role of LTG grown layers in eliminating charge depletion were presented in chapter 4.

Both relied upon the gettering of Arsenic by the LTG layer, which could be precipitate enhanced or roughness enhanced. The study with the LTG-GaAs and LTG-AlGaAs buffers (Samples 1,2,3,4) as presented in chapter 4, revealed that LTG-AlGaAs was much more effective in reducing charge depletion. This is consistent with the roughness hypothesis as LTG-AlGaAs layers grow rougher than LTG-GaAs layers[vi]. Though reduced, the current level was still adequate for the submicron GOI MESFET to deliver state of the art dc and rf performance. Next we compare the rf results obtained from the first submicron GOI MESFETs (GOI-1) and control MESFETs.

RF Performance Comparison : GOI-1 and control MESFETs.

F_t, f_{max} and other small signal parameters of the two devices were extracted from S-parameter measurements. The f_{max} and f_t versus drain bias for the GOI and control MESFET are shown in Figure 5.12. At lower current levels in the control device, I_{ds} increased with drain bias hence the data is compared for a higher current level in the control MESFET. The f_t of both devices exhibits a similar shape, dropping at first and then leveling out. As the drain voltage is increased, the gate-drain depletion region extends (which is commonly referred to as drain extension) and introduces an additional delay. If the drain extension reaches the edge of the n^+ drain region, it can change only slowly (due to the higher doping)

and the transit times levels out. The f_τ values in the GOI devices are slightly lower than those in the control. This could be due to the effective gate footprint (after recessing) to be slightly larger in the GOI device.

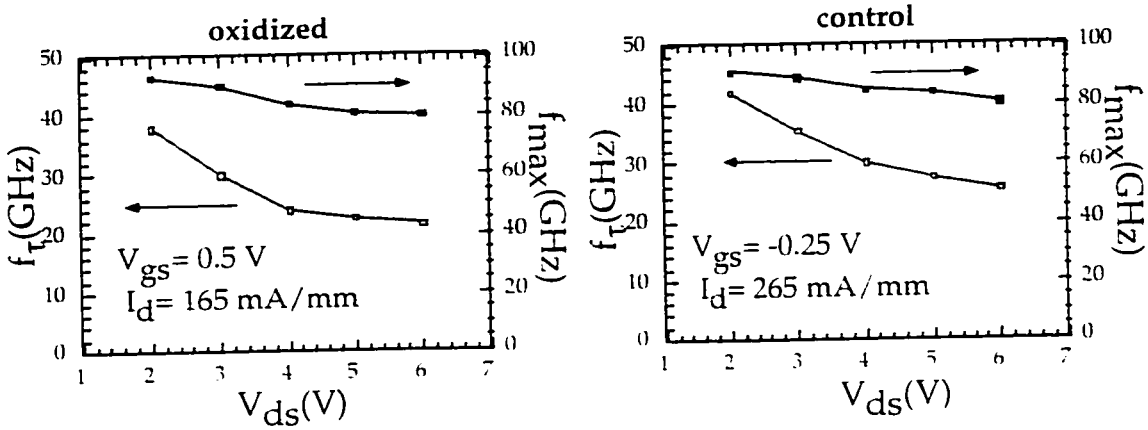


Figure 5.12 f_t and f_{max} for the GOI and Control MESFETs

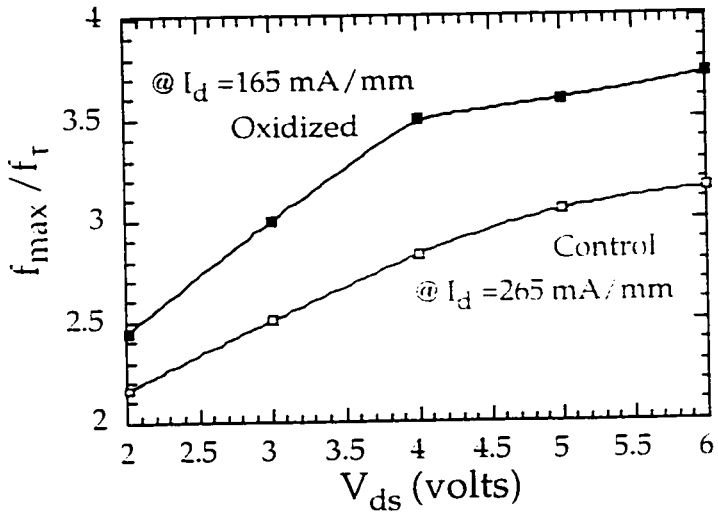


Figure 5.13 f_{max}/f_t ratio for GOI and control devices

As reported in chapter 4, the oxidation itself does not impact the electron velocity. But as can be seen from Figure 5.12, the f_{max}

values are very similar for both devices, giving a higher f_{max}/f_τ ratio for the GOI device (Figure 5.13). The improvement in the f_{max} of the GOI device comes from the increased output resistance resulting from the elimination of substrate leakage. The effect of output resistance on f_{max} is given in Equation 5.19[vii].

$$f_{max} = \frac{f_\tau}{2\sqrt{\frac{r_i + r_g + r_s}{r_{ds}} + 2\pi f_\tau r_g c_{gd}}} \qquad \textbf{Equation 5.19}$$

where r_{ds} is the output resistance, c_{gd} is the gate-drain capacitance and r_i, r_g and r_s are the channel, gate and source resistances respectively. The rf output resistance of both devices was also extracted from s-parameter measurements and is shown in Figure 5.14. It is clear that the improvement in output resistance in the GOI device is not merely a dc phenomena but is obtained at higher frequencies also.

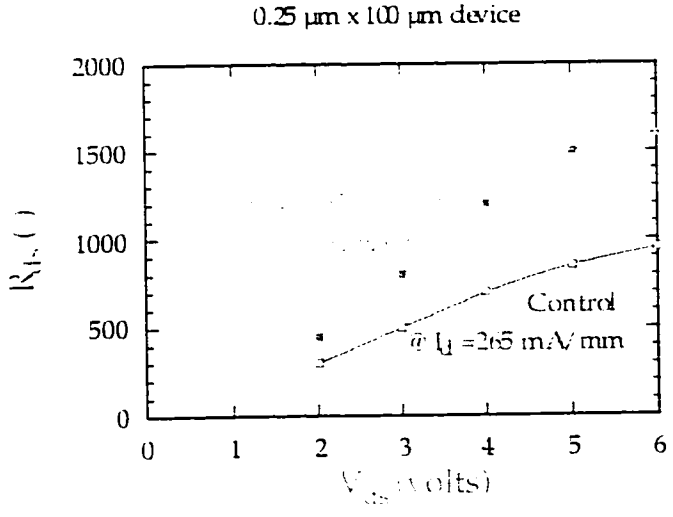


Figure 5.14 Extracted rf output resistance of the GOI and control device

Finally the voltage gain (g_m*r_{ds}) of the two devices is compared in Figure 5.15. The GOI device exhibits a higher voltage gain, mainly because of the higher R_{ds}. Voltage gain over 30 is an excellent number for a quarter micron gate length device.

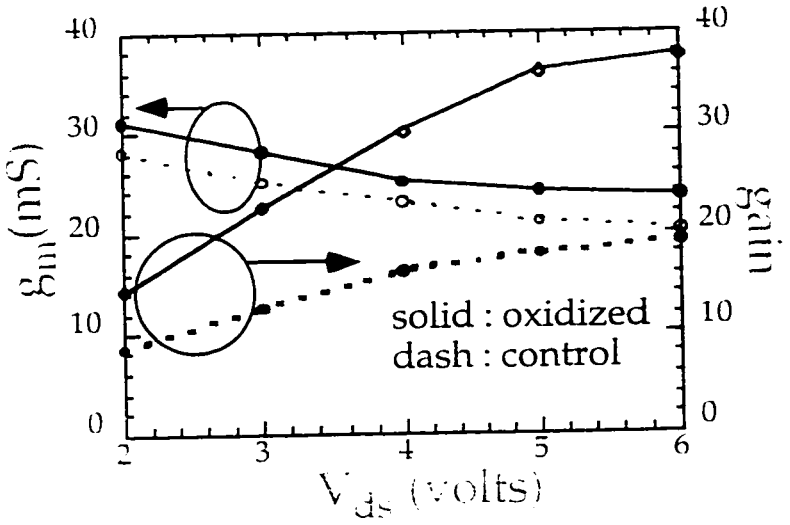


Figure 5.15 Extracted gain of the GOI and control device

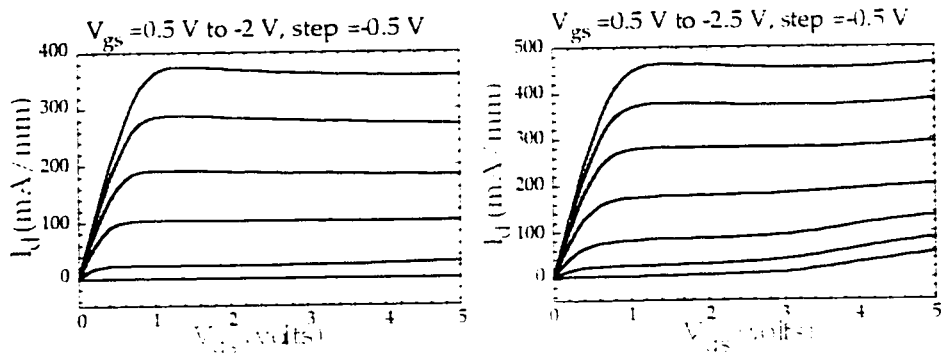
The first submicron GOI MESFET illustrated that the potential benefits of the GOI technology can be realized in a submicron technology. Improvements in dc and rf characteristics were observed despite the fact that the current level in the oxidized sample was reduced. The next step was to investigate the large signal performance of these devices to examine whether the GOI technology results in an improvement in efficiency. The power measurements are carried out using the ATN LP1 Load Pull measurement system. Unfortunately the measurement was limited by the available load states from the output tuner of the system. This was due to two reasons. First, the current level in the devices was

small requiring large values of output loads (refer to load line in Figure 5.1). Secondly, in this run the largest oxidized device had a width of 100 μm as the larger devices (150 μm) were not fully oxidized. Since a smaller device has lower absolute current, this further compounded the problem.

5.5 Improved Submicron GOI Technology

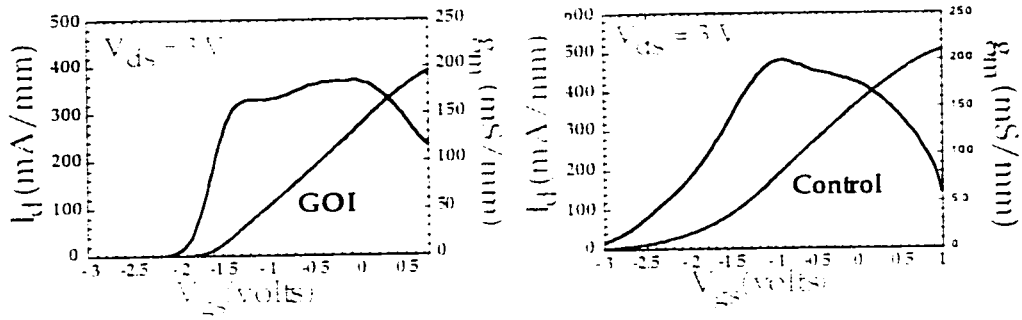
In the second set of submicron devices, we sought to fix the above problem. The fundamental problem of charge depletion was considered first. As described in chapter 4, different LTG grown buffers were studied. The best one (which resulted in minimum charge depletion after oxidation) was the LTG-AlGaAs buffer from sample # 4. This sample was used for fabricating the submicron GOI devices. Also the oxidation time was increased slightly so that the 150 μm devices are just fully oxidized.

The drain I-V characteristics of the oxidized and control devices are shown in Figure 5.16a and b. The charge depletion in these devices is about 100 mA/mm which is much lower than the over 300 mA/mm observed in the previous devices. This is also in agreement with the results of the charge loss experiment described in chapter 4. As before the superior I-V characteristics of the GOI device are clear. The ohmic contact resistance in these devices was around 0.2 -mm, as determined from TLM measurements. From the transconductance characteristics of Figure 5.17, it is clear that the insulating buffer results in much sharper g_m characteristics near pinchoff, approaching the ideal curve shown in Figure 5.4.



a b

Figure 5.16 Drain I-V characteristics of the improved submicron GOI (a) and control (b) MESFETs



a b

Figure 5.17 Transconductance characteristics of the improved submicron GOI (a) and control (b) MESFETs

The nominal two terminal gate-drain diode breakdown voltage was around 10.5 volts, defined at 1 mA/mm of reverse bias current (Figure 5.18, current plotted on linear and log scales). The control devices exhibited similar behavior.

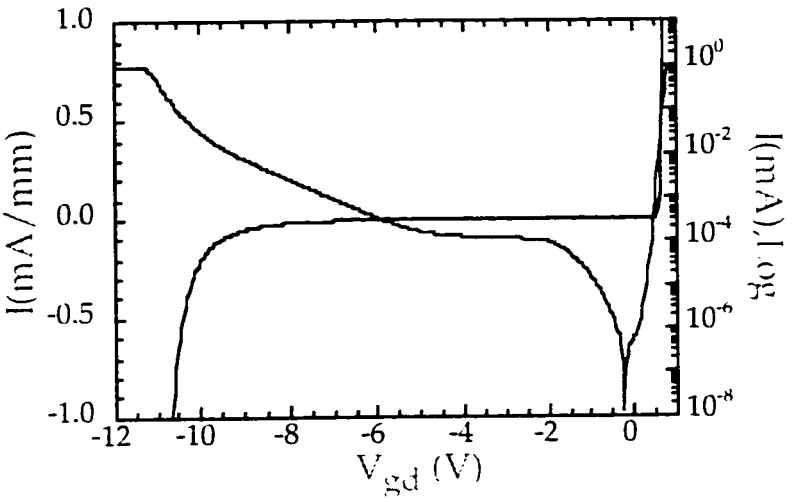


Figure 5.18 Gate-drain diode characteristics for the GOI MESFET

Subthreshold Characteristics

The influence of Al_2O_3 on the subthreshold characteristics is an important issue, as is for any buffer layer. For a uniformly doped device, the natural logarithm of I_d vs. V_g is almost a straight line, the reciprocal slope of which determines the gate swing (S) needed to reduce subthreshold current to any desired level[viii]. The drain current in the subthreshold regime can be approximately expressed as,

$$I_d \sim \exp\left[-\frac{V_{gs}}{n\,kT/q}\right] \qquad \textbf{Equation 5.20}$$

where, n is the ideality factor. The subthreshold swing S can be expressed as,

$$S = n\,\frac{kT}{q}\ln 10 \qquad \textbf{Equation 5.21}$$

or, S ~ 60 n mV/decade at room temperature. Clearly, smaller the subthreshold slope, the easier it is to turn off the device to a desired

off state current. In the ideal case, for n=1, at room temperature, S = 60 mV/decade. The ideality factors in typical commercial GaAs MESFETs are usually over 2 (resulting in subthreshold slopes of over 120 mV/decade). The subthreshold characteristics of the GOI MESFET are shown in Figure 5.19, showing a subthreshold slope of 100 mV/decade for the GOI devices. The improvement in the GOI devices over the control and regular commercial GaAs MESFETs is due to the presence of the insulating buffer which eliminates substrate leakage leading to better charge control. A low subthreshold slope is also of great importance in digital circuit applications where fast turn-on and turn-off for a FET are desirable.

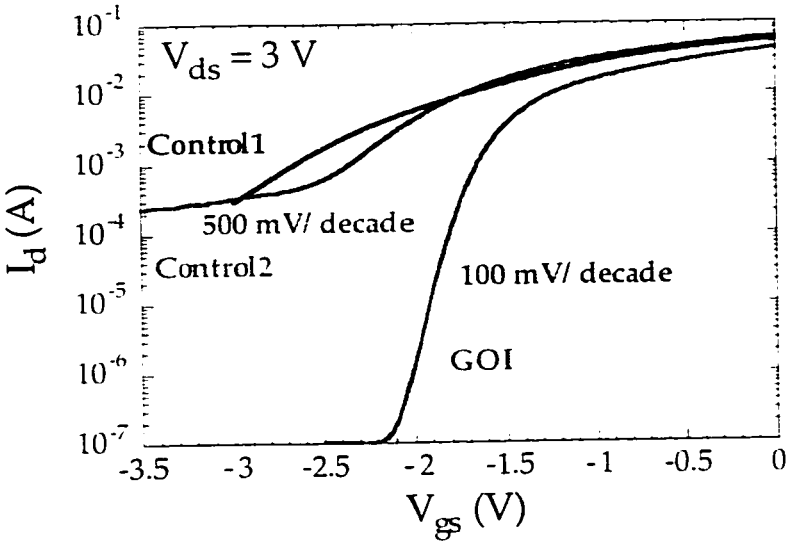


Figure 5.19 GOI/Control MESFETs subthreshold characteristics

Small Signal rf performance

The f_t and f_{max} of these devices were lower than the first submicron GOI and control devices. The reason for this was that the

gatelength turned out to be larger than the intended value of 0.25 μm. In this run the actual gatelength was about 0.4 μm. The nominal f_τ / fmax values were 22 GHz/75GHz (GOI, I_d=168 mA/mm) and 23 GHz/67GHz (control, I_d=178 mA/mm) at V_{ds} = 3V. These became 17.5 GHz / 76 GHz (GOI, I_d=170 mA/mm) and 18 GHz / 71 GHz (Control, I_d=280 mA/mm) at V_{ds}=6V.

However our main goal in this sample was to get GOI devices with higher current level and minimal charge depletion, which was satisfied. Though the f_τ and f_{max} values were lower, they were sufficient for most of our power measurements which were done at 4 GHz. While higher values would definitely help, this is something that would be addressed by E-beam lithography. The GOI device still exhibits performance advantages as expected such as higher r_{ds}, higher gain and higher f_{max}/f_τ ratio. This are similar to those reported for devices in section 5.4 and are not repeated again.

5.6 Load Pull Power Measurements for the improved submicron GOI and control MESFETs.

The simple schematic of the Load Pull set up for power measurement is shown in Figure 5.20. The setup is controlled using ATN LP1 software. Details of the measurement process are found in the ATN LP1 users manual[ix]. The range of the ATN system is from 2-18 GHz, determined by the tuner bandwidth. Currently the system is setup for 2-9 GHz measurements.

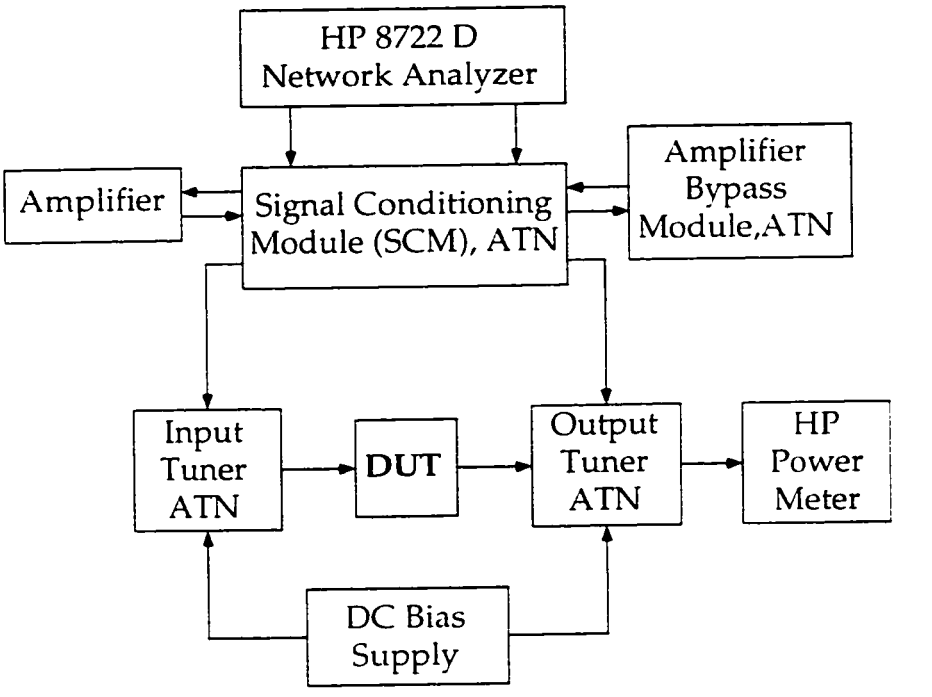


Figure 5.20 Schematic of the ATN Load Pull System

Power and efficiency measurements were performed at 4 GHz using the ATN LP1 load pull system. The GOI device had an efficiency of 67.7 % at a low drain bias of 3V with an associated output power of 75 mW/mm (P_{1dB} = 10.5 dBm, out); under class B (I_d = 2 mA) biasing conditions, as shown in Figure 5.21. P_{1dB} is the output power level at which the gain is 1 dBm compressed from its value in the linear region) The highest efficiency obtainable from the control device was 58 % under similar conditions (V_{ds}=3V, I_d=3mA, P_{1dB} = 10 dBm, out), which was considerably lower than the GOI sample. Low drain bias operation, as said earlier is crucial for wireless handset applications.

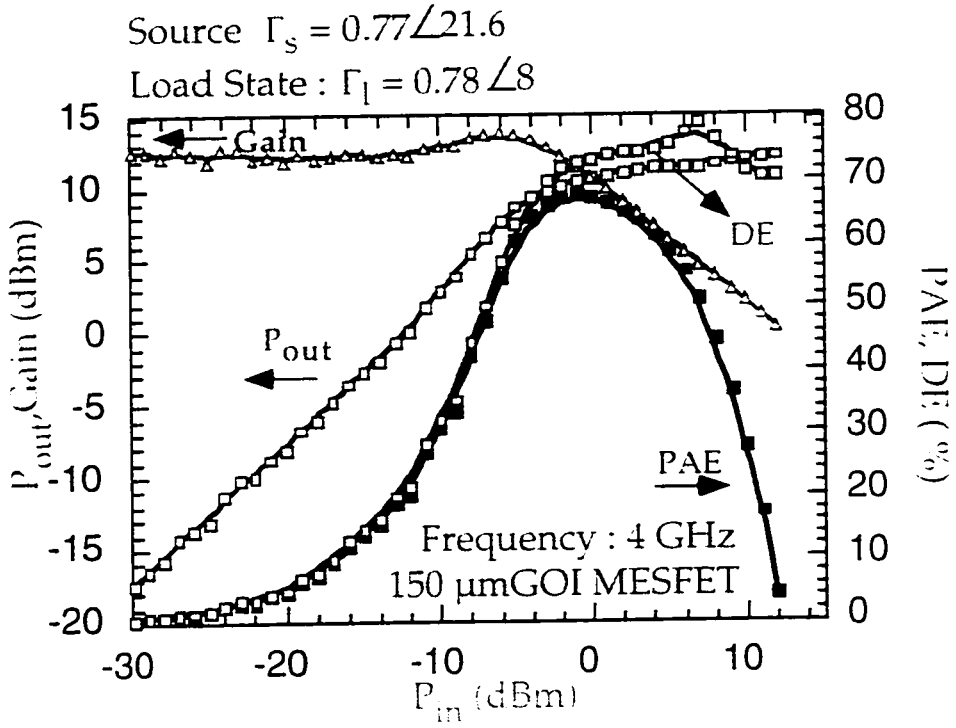


Figure 5.21 Power Measurements for the submicron GOI MESFET

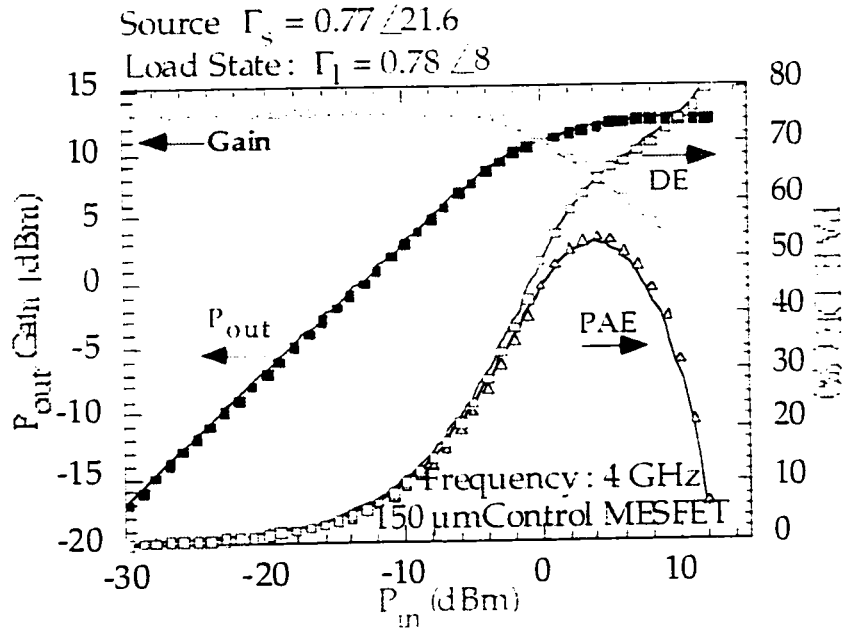


Figure 5.22 Power Measurements for the submicron control MESFET

This illustrates that the benefit of the insulating buffer in having reduced substrate leakage, superior charge control, and sharper pinchoff characteristics extends to large signal operation also. The GOI device performed very well even with an ultra low drain bias of 1.5 V, with a PAE of 57 % and P_{out} of 30 mW/mm. With such performance, the GOI MESFETs could be suitable for under 2.2 V operation with ultra small NiMH batteries, which is very important in reducing the size and the weight of a wireless handset.

All the measurements were optimized for maximum efficiency. When optimized for maximum power, the output power increased by 1 dB but the corresponding drop in efficiency was around 5-10 %. Near Class A operation for the GOI MESFET (V_{ds} = 5V, I_d = 200 mA/mm) resulted in a P_{out} of 335 mW/mm (P_{1dB} = 16 dBm, out) with a peak PAE of 48 %. The maximum saturated power was 420 mW/mm (18 dBm) These results are shown in Figure 5.23.

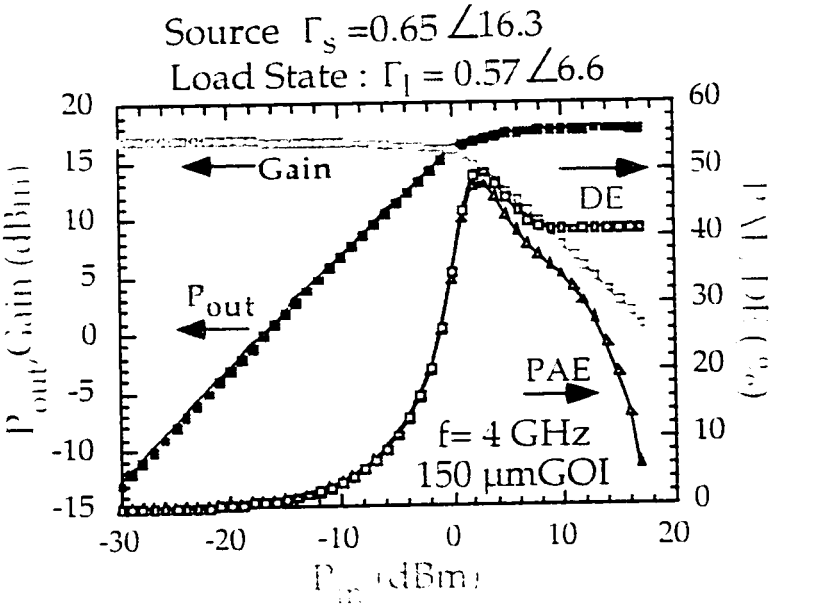


Figure 5.23 Near Class A measurements for the GOI MESFET

For the given load match, with Γ_L = 0.57, the resistance R can be calculated to be 183 ohms.

$$\frac{Z_L}{Z_0} = \frac{1+\Gamma_L}{1-\Gamma_L} \qquad \textbf{Equation 5.22}$$

where Z_0 is 50 ohms. Since R is also the slope of the load line,

$\Delta V/\Delta I$ = R= 183 ohms **Equation 5.23**

Since the biasing is near Class A, the output power is given as

$$P_{out} = \frac{1}{8}\Delta V \Delta I = 50 \text{ mW}. \qquad \textbf{Equation 5.24}$$

where ΔV and ΔI are the large signal voltage and current swings. From equations 5.18 and 5.19,

ΔV=8.5 Volts, and ΔI = 46 mA (or 306 mA/mm).

The theoretical expected voltage and current swings (for perfect Class A operation) can be estimated from the dc I-V characteristics of Figure 5.16 a as :

$\Delta V = V_{bd}-V_k = 9-1 = 8$ Volts

$\Delta I = I_{max}$ (at V_{gs}=0.5 V) = 350 mA/mm

The close agreement of these numbers; calculated from the measured power performance and expected from the dc characteristics demonstrate that there there is a close match between the dc and large signal rf performance with the GOI technology.

Power measurements were also done for 100 μm wide devices. The I_{dss} of the GOI and control devices was 27 mA and 39 mA respectively. The maximum power added efficiency for both the device is compared as a function of the bias condition.

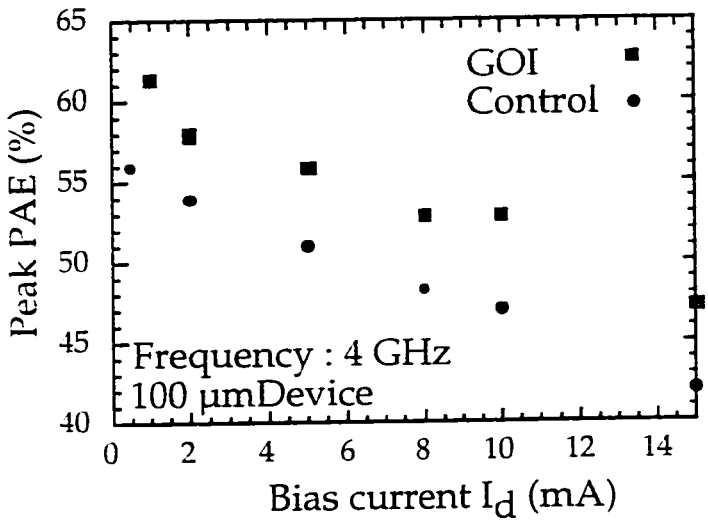


Figure 5.24 Peak PAE as a function of Bias Condition

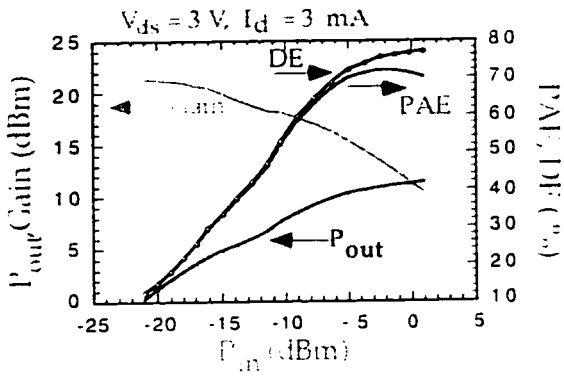
The bias is varied from Class B, through Class AB towards Class A. Clearly the GOI device is superior to the control device over the entire bias range as evident from the higher values of PAE.

Active Load Pull measurements with Harmonic Matching

Providing the optimum loads at the harmonics can lead to an improved performance as was discussed in section 5.2. Active load pull measurements were done at Hughes Space and Communication (J. Pusl). The advantage of an active load pull system is that all gammas on the Smith chart can be realized[x], hence optimal matching loads can always be found.

Active Load Pull measurements with 2'nd and 3'rd harmonic matching, resulted in a PAE of 72 % [Figure 5.25] at an output power level of 85 mW/mm at 4 GHz with V_{ds} of 3 V. The third harmonic termination was near open circuit while the second harmonic termination was near short circuit. *To the best of our knowledge,*

these results represent the highest reported PAE for a C-band GaAs based MESFET with low voltage operation.



Load State : $\Gamma_L = 0.79 \angle 9$
Fundamental : 4GHz
150 μmGOI MESFET

Figure 5.25 Active Load Pull measurements with Harmonic Matching for the GOI MESFET

5.7 Preliminary Linearity measurements

A power amplifier for wireless condition has to satisfy stringent linearity specifications, depending on the system it is used in. This makes it very important to have an estimate on the linearity performance of our GOI MESFETs. The ATN load-pull system at UCSB is not equipped with the linearity measurement option currently. Hence the linearity measurements are done in collaboration with Wright Patterson Air Force Base Laboratories (L. Kehias and T. Jenkins).

The basic system load pull system used is from Maury Microwave which is similar to the ATN system with some exceptions. An important one is that the tuners in the Maury system are mechanical, while those in the ATN system are solid state. The mechanical tuners made the system slower but the advantage was

the realization of higher load gammas (upto 0.85 at 4 GHz). The configuration of the two tone IMD and power measurement system is shown in Figure 5.26.

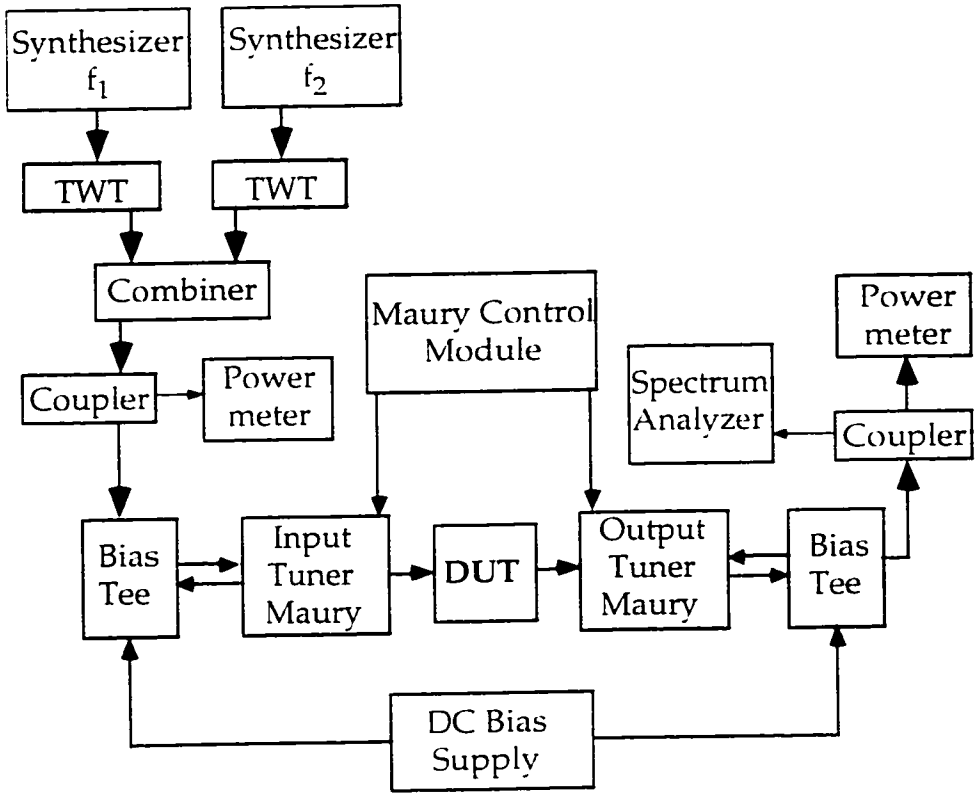


Figure 5.26 2 Tone Intermodulation Distortion and Load Pull System Schematic, WPAFB.

The two tones, f_1 and f_2 are separated by 100 KHz. These measurements were done at 8 GHz, as determined by the availability of the TWT amplifiers at X-band. The basic principle of two tone IMD measurement is shown in Figure 5.27. The third order non-linearities result in the unwanted products near the signal output frequency as shown. The IMD is a measure of how much below the carrier output power are these 3'rd order terms.

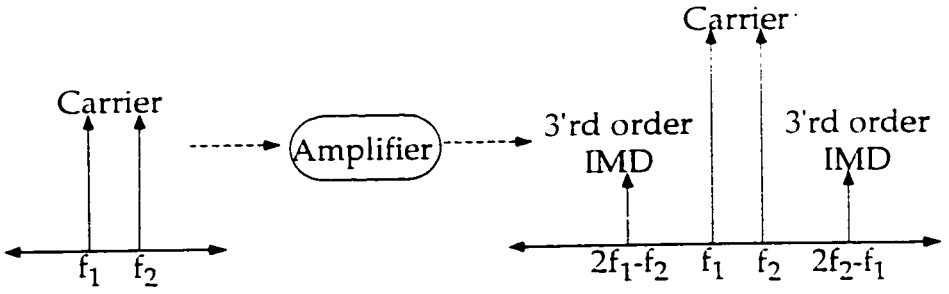


Figure 5.27 Principle of Two Tone 3rd Order IMD distortion

An intermodulation product termed as IP_3 can be defined as the power level when the extrapolated carrier power becomes equal to the extrapolated 3'rd order IMD power as shown in Figure 5.28, which plots the results of IMD measurements for both the samples under Class A biasing. The IP_3 product is similar in both samples, around 20 dBm. The P_{1db} compression levels at the output are 8.5 dBm and 8 dBm for the GOI and control samples respectively. In general, if the IP3 is 10 dBm above the 1 dB saturated power, the amplifier is considered to be fairly linear. The GOI technology satisfies this criterion, simultaneously obtaining high efficiency. The Carrier to Intermodulation separation is slightly higher in the GOI sample.

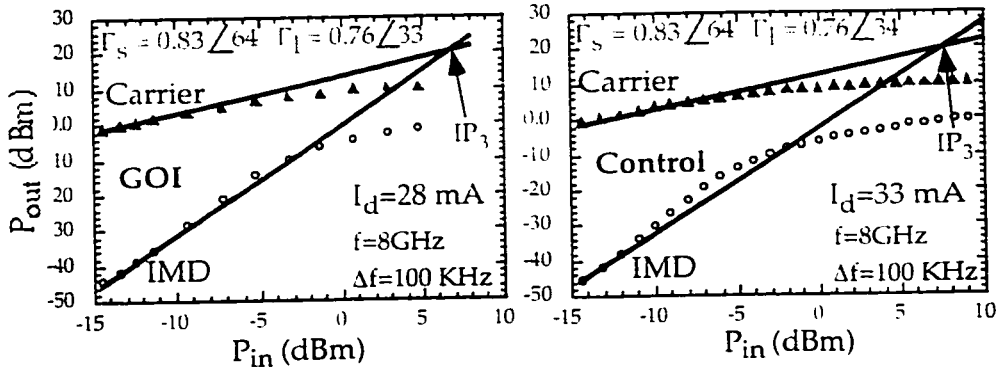


Figure 5.28 IP_3 measurements

5.8 Summary

In this chapter, we presented the dc, rf and large signal performance data for the submicron GOI technology. It is demonstrated the advantage gained by the insulating buffer by eliminating substrate leakage current is reflected in the dc, rf and power performance of the GOI MESFETs with respect to the control MESFETs. Submicron GOI MESFETs with world record efficiencies were fabricated. The highest PAE obtained was 72 % (with harmonic matching) at 4 GHz, at a low drain bias of 3 volts, the highest reported under these conditions to the best of our knowledge.

While more detailed measurements on linearity of the devices are required, initial IMD measurements show that the GOI MESFETs have a fairly decent linearity performance with IP_3 about 20 dBm, 10 dBm higher than the saturated 1dB output power.

A technology that can obtain high efficiency with high linearity at low supply voltages would be an ideal choice for wireless applications, and the GOI technology satisfies this requirements. Finally, the high efficiency performance of the GOI MESFETs is compared to the state of the art results, reported in literature, in Table 5.1.

Device Type	Freq. GHz	V_{ds} V	PAE %	P_{out} mW/mm
GaAs/InGaAs HEMT[xi]	1.9	3.0	53.5	30.5
Ion-Implanted GaAsMESFET[xii]	1.9	2.2	62	77
GaAs MESFET[xiii]	0.9	3.5	74	116
PHEMT[xiv]	4.5	5	79	290
E-mode Power pHEMT[xv]	1.8	3.0	65.4	167
This Work, GaAs MESFET	*4*	*3.0*	*72*	*85*
This Work, GaAs MESFET	*4*	*1.5*	*57*	*30*

Table 5.1: State-of-the-art performance for FETs geared for wireless communication applications.

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CHAPTER 6. Summary and Future Work

6.1 Summary

The main goal of this thesis was to investigate :

1. *The technique of wet lateral oxidation and*
2. *FETs incorporating oxides for high efficiency applications.*

in order to meet the needs of emerging markets in the area of wireless handheld and satellite communications. *The work reported here represents the first concentrated effort to determine the applicability of the Al_2O_3 obtained by the wet lateral oxidation in steam of high Al content AlGaAs layers, in electronics.* The important highlights of this study are summarized below.

The lateral wet oxidation technique :

The wet oxidation process has been successfully implemented to obtain an insulating oxide for GaAs based FETs. We investigated the mechanism of oxidation and determined that the oxidation rate is linear in time, suggesting a reaction rate limited process. TEM characterization showed that overoxidation can be detrimental, inasmuch as the quality of the active semiconductor layers and the interface surrounding the oxide are concerned. For post oxidation stability of the oxide (when exposed to high temperature processing steps), $Al_{0.98}Ga_{0.02}As$ was found to be superior to pure AlAs. This was then used as the oxidation layer in most of the device work.

Al_2O_3 for gate oxide applications :

The quality of the oxide-semiconductor interface is crucial for the wet oxide to be established as a viable gate insulator. CV and DLTS characterization was performed on MIS capacitors with Al_2O_3 as the gate oxide. The interfacial trap energy level was found to be around midgap and was associated with the excess As remaining in the system after oxidation. Al_2O_3 based depletion mode MOSFETs were fabricated and characterized. Due to the presence of interface states, g_m compression was observed in the FET I-V characteristics, but was eliminated using the technique of hydrogenation. Hydrogen helps in removing the excess As from the system as AsH_3. RF measurements on 1.1 μm gatelength depletion mode MOSFETs yielded f_τ and f_{max} of 9 GHz and 21 GHz respectively. However, extensive characterization of the oxide-GaAs interface is still required to reduce the interface state and charge densities to values commonly encountered in Si based technology. It was clear that at the present time, the most impact Al_2O_3 can have in GaAs based FETs was as a buffer layer insulator, which formed the basis of our GOI (GaAs On Insulator) technology.

Al_2O_3 for buffer oxide applications (GOI Technology):

The impact of an insulating oxide buffer on dc, small signal rf and large signal power performance of traditional GaAs based MESFETs was evaluated. Though the quality of the oxide-semiconductor interface is not as crucial as that for gate oxide applications, interface charge leads to a current reduction in the MESFETs. This occurs via backdepletion of the channel.

Hall measurements on doped active layers above an oxide were done to understand the issue of charge depletion. Following this, the novel use of LTG-grown GaAs and AlGaAs layers was demonstrated in minimizing the current depletion. The mechanism responsible for this improvement was hypothesized to be gettering of the excess As by the LTG layers.

Initial GOI MESFETs demonstrated the feasibility of this technology. The elimination of substrate leakage led to I-V characteristics with negligible output conductance. However these GOI MESFETs exhibited charge depletion of over 250 mA/mm.

Using the As gettering approach of LTG layers, GOI MESFETs with negligible current depletion were fabricated. The devices had high full channel current of around 300 mA/mm and a peak g_m of about 145 mS/mm. *The optical gate 1.3 μm gatelength GOI MESFET exhibited reduced substrate leakage and broader gm characteristics with higher gain near pinchoff; when compared to a non oxidized control MESFET.* For the 1.5 μm gatelength GOI MESFET, the optimum f_τ and f_{max} values are around 9 GHz and 33 GHz respectively. The GOI device had a higher f_{max} than the control due to increased output resistance. Initial results of the GOI technology in pHEMTs were presented.

Submicron GOI MESFETs incorporating LTG-AlGaAs layer for As gettering were demonstrated. The improvements in dc characteristics due to the oxide buffer were retained in the submicron devices. The current level in the GOI MESFET was 280 mA/mm and that in the control MESFET was 380 mA/mm. *With the LTG-AlGaAs layer, the charge depletion was repeatably*

minimized to less than 100 mA/mm. The extracted output resistance was consistently higher for the GOI MESFET and led to a higher f_{max}/f_t ratio.

Finally, record power added efficiency was obtained from the GOI MESFET. *With harmonic tuning, a PAE of 72 % with an output power of 85 mW/mm at a low drain bias of 3 Volts was achieved. This represents the highest reported value of PAE for a C-band GaAs based MESFET operating at low bias voltage, to the best of our knowledge.* Ultra low voltage 1.5 volt operation was also demonstrated with a PAE of 57 % and an output power of 30 mW/mm. Near Class A operation resulted in a PAE of 48 % with output power of 410 mW/mm. The GOI MESFETs had vastly improved efficiencies over control (non oxidized) MESFETs for all bias conditions (Class B, AB, A). A comparison with state of the art technologies was presented in Chapter 5.

6.2 Future Work

As stated before, this thesis attempted an exploratory study of the electronic device applications of Al_2O_3 obtained by the wet oxidation of AlGaAs. Extensive material and device characterization is needed in order to obtain a reproducible, stable oxide technology with reduced interface state density. An attempt is made in this section to identify possible future thrusts.

1. The charge depletion issue in the GOI technology needs to be further addressed. LTG-AlGaAs layers were more effective in minimizing the charge depletion, than LTG-GaAs layers. The LTG-

AlGaAs layers used in this work had an Al composition of 25 %. Recent work by J. Champlain has demonstrated that LTG-AlGaAs buffers with higher Al composition result in increased oxidation rate. These may then be even more effective for As gettering. If successful, the gate oxides can also employ this solution.

2. Due to their superior power performance and higher linearity, pHEMTs are becoming the devices of choice for high performance microwave electronics. The GOI technology in pHEMTs can be expected to improve their performance even further. The pHEMT channel is typically a thin (~100-150 Å) $In_xGa_{1-x}As$ (x=0.1-0.3) strained layer. The effect of oxidation on thin and strained conducting layers has to be evaluated. Further, the LTG layer As gettering approach could be applied to pHEMTs to eliminate current loss.

3. The biggest impact of the wet oxidation technique could be in the field of GaAs CMOS, as a high speed low power digital IC technology. Gate oxides that have interface charge densities low enough to support an inversion channel have to be developed. Some approaches that can be looked at include various annealing techniques, hydrogenation and LTG layers for As gettering. All the oxidations described in this work were lateral. Wet oxidation of AlGaAs in steam from the top could possibly result in improved interfaces. A practical realization of an enhancement mode MOSFET would require a self-aligned device technology possibly employing ion implantation. Then the impact of high activation temperatures on the stability of the oxide and the underlying channel needs to be investigated.

4. As in optoelectronic applications, buried oxides can also help to improve vertical devices. Here, the demands on the oxide-semiconductor interface will not be crucial. Some of the potential applications include oxide apertured RTDs for controlling the peak to valley ratio, oxide apertured HBTs to reduce the active area and parasitic capacitances, and vertical FET structures using current aperturing.

5. The oxidation technique can be extended to other material systems like InP. AlAsSb, which can be lattice matched to InP is a viable oxidation candidate. Presently the oxidation of AlAsSb is complicated by the fact that Sb does not leave the layer after oxidation but segregates at one of the interfaces. We have correlated the interface state formation to excess As in the structure resulting in midgap states. Use of other innovative materials such as AlSbP (which could be lattice matched to both InP and GaAs) is encouraging as neither Sb nor P introduce a state in the bandgap.

To summarize it all, Figure 1.8 is reproduced with some modifications in Figure 6.1, outlining a roadmap for the future.

Figure 6.1 Roadmap for Oxide Based Electronic Technologies

APPENDIX

Process flow for GOI MESFET

1. Wafer Clean

1. Soak in Acetone for 3 minutes
2. Soak in Isopropyl Alcohol for 3 minutes
3. DI water rinse for 3 minutes
4. Blow dry in Nitrogen
5. Dehydration bake at 120 °C for 30 minutes in the oven

2. Mesa Isolation

Lithography

1. Spin PR 4110 at 6000 rpm for 30 seconds
2. Soft bake at 95 °C for 1 minute on the hot plate
3. Edge removal
    a. Expose the edges of the wafer for 1 minute at 7.5 mW/cm^2 of intensity on the Karl Suss Aligner.
    b. Develop for 1 minute in 1 : 4 AZ400K Developer : Water.
    c. Blow dry in Nitrogen
4. Use the mesa level mask and expose for 8 seconds at 7.5 mW/cm^2 of intensity on the Karl Suss Aligner.
5. Develop for 50-55 seconds in 1 : 4 AZ Developer : Water.
6. Examine the pattern in the optical microscope.
7. Oxygen plasma descum at 100 W, 300 mT O_2 for 30 seconds.

Etching (RIE # 5, UCSB Clean Room)

8. Make sure that the laser monitor is aligned.
9. Etch conditions : $Cl_2/SiCl_4/BCl_3$ 2.5/5/25, 60 W dc power, 5 mT pressure. Approximate etch rate : 1500 Å / min, but varies with system conditions. Always use laser monitor to check etch depth. The desired etch depth is about 500 Å below the oxidation layer, into the GaAs buffer layer.
10. Unload sample, make sure that the etch has proceeded beyond the oxidation layer.
11. Strip photoresist in acetone (3 minutes), with ultrasonic dip for 5-10 seconds, and finish with a wafer clean step.

3. Oxidation

1. Set the oxidation furnace and the water beaker at the desired temperature. Make sure the oxidation rate is calibrated.
2. Introduce the sample gradually from the mouth of the furnace and push the quartz boat in till the sample sits in the middle of the furnace.
3. Monitor time and stop the oxidation by pulling the sample out of the furnace gradually.

4. Cap Removal

1. Give an ammonium hydroxide dip for 15 seconds (NH_4OH : H_2O, 1 : 15).
2. Etch the GaAs dummy cap in citric acid based selective etchant (10 parts of 1:1 Citric Acid Anhydrous and water mix with 1 part of H_2O_2) for 10 seconds.

3. Remove the AlAs etch stop layer by a short 2 second Phosphoric acid based etchant (H_3PO_4:H_2O_2:H_2O 3:1:50).

4. Dehydration bake at 120 °C for 30 minutes in the oven.

5. Source and drain contacts

Lithography

1. Spin HMDS at 6000 rpm for 30 seconds.
2. Spin PR 5214 (Image reversal) at 6000 rpm for 30 seconds.
3. Soft bake at 100 °C for 1 minute on the hot plate.
4. Edge removal
    a. Expose the edges of the wafer for 1 minute at 7.5 mW/cm^2 of intensity on the Karl Suss Aligner.
    b. Develop for 1 minute in 1 : 5.5 AZ400K Developer : Water.
    c. Blow dry in Nitrogen
5. Use the source-drain mask and expose for 17 seconds at 7.5 mW/cm^2 of intensity on the Karl Suss Aligner. Use the I-line filter. The filter is not critical and the process can be done without one, although the exposure time can be slightly different.
6. Bake at 107 °C for 1 minute on the hot plate (Image reversal bake).
7. Flood expose for 1 minute.
8. Develop for 30-35 seconds in 1 : 5.5 AZ400K Developer : Water.
9. Examine the pattern in the optical microscope.
10. Oxygen plasma descum at 100 W, 300 mT O_2 for 30 seconds.

Metallization

11. 1:15 BHF dip for 10 seconds.

12. Evaporate Ni (30 Å), Ge (260 Å), Au (540 Å), Ni (200 Å), Au (2000 Å)

13. Liftoff in Acetone for 10-20 minutes.

14. Isopropyl alcohol dip for 3 minutes.

15. DI water clean for 3 minutes.

16. Blow dry in Nitrogen.

17. Anneal in the RTA (Forming gas ambient) for 40 seconds, 410° C.

5. Gate Contact

Optical Gate

1. Same resist process as for source and drain contact lithography.

2. A good contact is critical for gate lengths of 1 micron.

3. Develop time is slightly longer, around 40 seconds. Examine under optical microscope and develop until the gate finger is completely open.

4. Oxygen plasma descum at 100 W, 300 mT O_2 for 30 seconds.

5. 1:15 BHF dip for 10 seconds.

Gate recess etch

6. Monitor the source-drain current before beginning the etch. Use new probe tips to ensure probing through the photoresist.

7. Etch the n^+ ohmic cap in citric acid based selective etchant (10 parts of 1:1 Citric Acid Anhydrous and water mix with 1

part of H_2O_2) for 12 seconds. The etch stops on the $Al_{0.7}GaAs$ layer.

8. Remove the $Al_{0.7}GaAs$ etch stop layer with a 2 second phosphoric acid based etchant (H_3PO_4:H_2O_2:H_2O 3:1:50).

9. Monitor the source-drain current again. The current reduces by about 150 mA/mm after the ohmic cap is etched.

10. Gate Schottky metallization is Ti (100 Å), Pt (100 Å), Au (3500 Å). Make sure that the gate metal thickness is greater than the total mesa height since the gate climbs over the mesa.

11. Liftoff in acetone (30 minutes) and clean in Isopropyl Alcohol (3 minutes).

Gate by Electron beam lithography

1. Use the source drain mask which has E-beam alignment marks for the gate level.

2. HRL (Malibu) 0.25 μm E-beam process.

3. Oxygen plasma descum at 100 W, 300 mT O_2 for 1 minute.

4. 1:15 BHF dip for 10 seconds.

5. Gate recess etch as above.

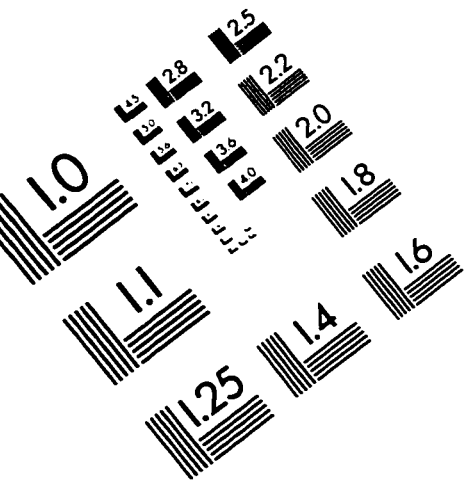
6. Gate metallization as above. Metal thicknesses of over 4000 Å are difficult to liftoff with the E-beam resist process.

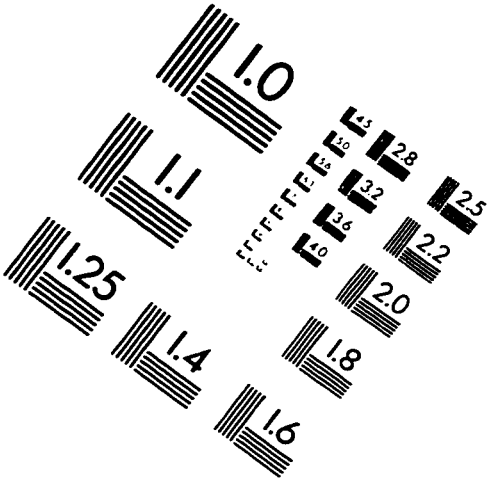
7. Liftoff in Methylene Chloride (heat to ~ 60 °C with stirring) for 5 minutes, and clean in acetone, isopropyl alcohol.

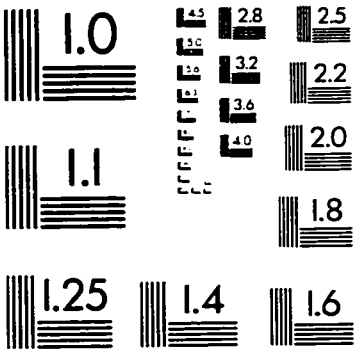
8. Gate pad lithography (with the E-beam gate, the pad is done separately), with the PR 5214 process.

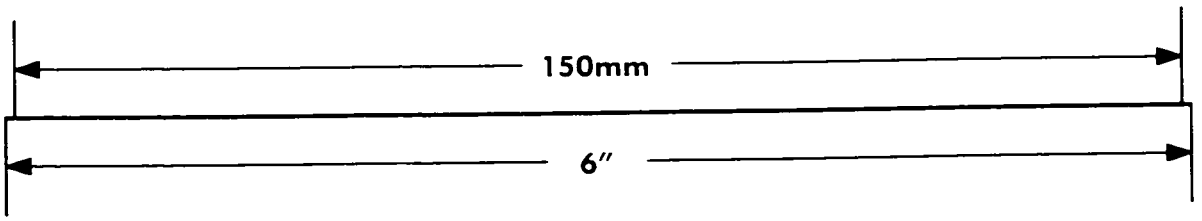
9. Gate pad metallization, Ti (100 Å), Au (5000 Å)

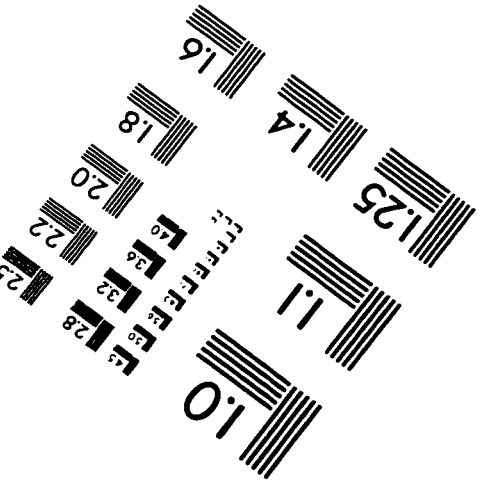
IMAGE EVALUATION
TEST TARGET (QA-3)

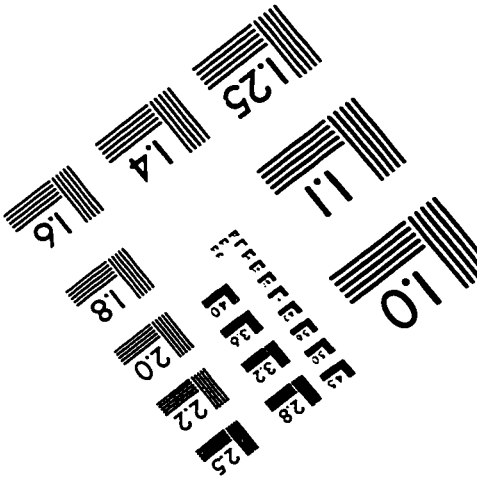












APPLIED IMAGE, Inc
1653 East Main Street
Rochester, NY 14609 USA
Phone: 716/482-0300
Fax: 716/288-5989